256K × 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM416C256B/BL/BLL-5	50ns	15ns	90ns
KM416C256B/BL/BLL-6	60ns	15ns	110ns
KM416C256B/BL/BLL-7	70ns	20ns	130ns
KM416C256B/BL/BLL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Self Refresh operation (LL-version)**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +5.0V±10% power supply**
- **Refresh Cycle**
  - **-512 cycle/8ms (Normal)**
  - **-512 cycle/64ms (L-version)**
  - **-512 cycle/128ms (LL-version)**
- **Power Dissipation**
  - **-Standby: 5.5mW (Normal)**
    1.1mW (L-version)
    0.83mW (LL-version)
  - **-Active (50/60/70/80): 605/495/440/415mW**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP II**

GENERAL DESCRIPTION

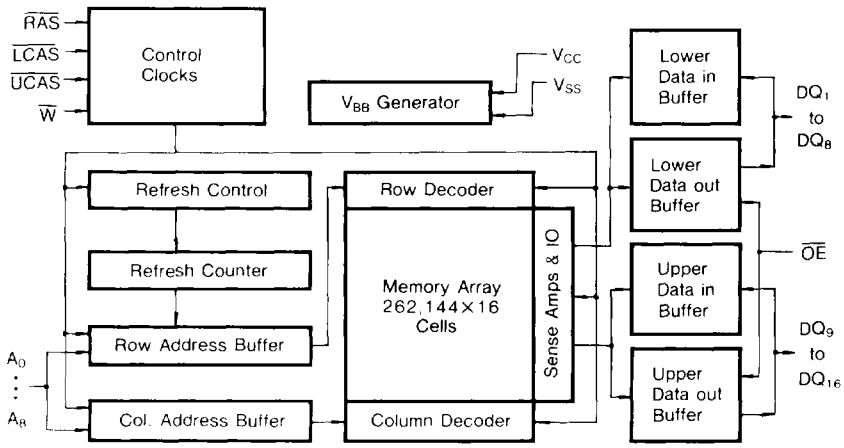
The Samsung KM416C256B/BL/BLL is a CMOS high speed 262,144 bit × 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM416C256B/BL/BLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM416C256B/BL/BLL is fabricated using Samsung's advanced CMOS process.

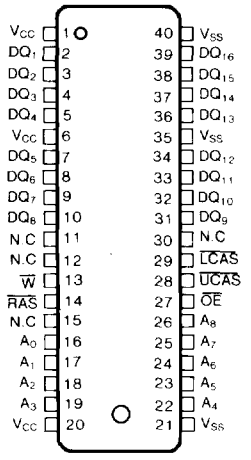
4

FUNCTIONAL BLOCK DIAGRAM



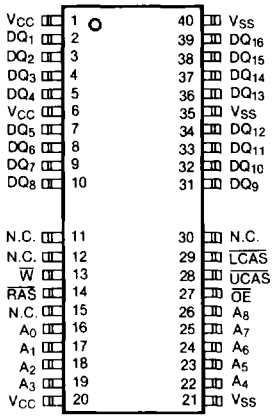
PIN CONFIGURATION (Top Views)

• KM416C256BJ/BLJ/BLLJ



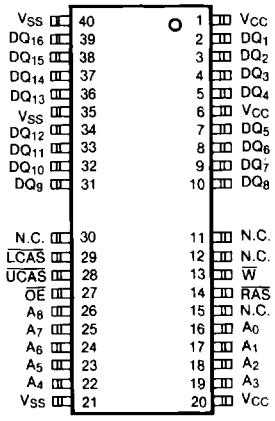
(SOJ)

• KM416C256BT/BLT/BLLT



(TSOP(II)-Forward Type)

• KM416C256BTR/BLTR/BLLTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A_0-A_8	Address Inputs
$DQ_{1\text{-}16}$	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power (+5V)
N.C.	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

4

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @ t_{RC}=min.)	KM416C256B/BL/BLL-5	I_{CC1}	-	110	mA
	KM416C256B/BL/BLL-6			90	mA
	KM416C256B/BL/BLL-7			80	mA
	KM416C256B/BL/BLL-8			75	mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @ t_{RC}=min.)	KM416C256B/BL/BLL-5	I_{CC3}	-	110	mA
	KM416C256B/BL/BLL-6			90	mA
	KM416C256B/BL/BLL-7			80	mA
	KM416C256B/BL/BLL-8			75	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @ t_{PC}=min.)	KM416C256B/BL/BLL-5	I_{CC4}	-	70	mA
	KM416C256B/BL/BLL-6			60	mA
	KM416C256B/BL/BLL-7			55	mA
	KM416C256B/BL/BLL-8			50	mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)	KM416C256B	I_{CC5}	-	1	mA
	KM416C256BL			200	μA
	KM416C256BLL			150	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @ t_{RC}=min.)	KM416C256B/BL/BLL-5	I_{CC6}	-	110	mA
	KM416C256B/BL/BLL-6			90	mA
	KM416C256B/BL/BLL-7			80	mA
	KM416C256B/BL/BLL-8			75	mA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter		Symbol	Min	Max	Units
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{UCAS}$=$\overline{LCAS}$=0.2V D_{IN}=Don't Care, T_{RC}=125μS T_{RAS}=T_{RAS} min.~300ns	KM416C256BL	I_{CC7}	-	300	μA
Self Refresh Current $\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_8=V_{CC}-0.2V or 0.2V DQ_1-DQ_{16}=V_{CC}-0.2V, 0.2V or Open	KM416C256BLL	I_{CCS}	-	200	μA
Input Leakage Current (Any input 0V $\leq V_{IN} <$ V_{CC}+0.5V, all other pins not under test=0 volts)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V $\leq V_{OUT} <$ V_{CC})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_8)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_{16})	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C$\leq$Ta$\leq$70°C, V_{CC}=5.0V$\pm$10%, See notes 1,2)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	135		155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	15	10,000	20	10,000	20	10,000	ns	

(*) 50ns Product:VCC=5V $\pm$ 5%, Cout=50pF

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	35	20	45	20	50	20	60	ns	
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	4
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	11
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	6
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		10		10		ns	8
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		50		55		ns	
Write command pulse width	tWP	10		10		10		10		ns	6
Write command to $\overline{RAS}$ lead time	tRWL	15		15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		15		20		ns	
Data-in set-up time	tDS	0		0		0		0		ns	
Data-in hold time	tDH	10		10		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	10
Refresh period (Normal)	tREF		8		8		8		8	ms	6
Refresh period (L-version)	tREF		64		64		64		64	ms	
Refresh period (LL-version)	tREF		128		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		40		50		50		ns	
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	75		85		95		105		ns	8
Column address to $\overline{W}$ delay time	tAWD	50		55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	55		60		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast page mode cycle time	tPC	35		40		45		50		ns	
Fast page mode read-modify-write cycle time	tPRWC	80		80		95		100		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	

(*) 50ns Product:VCC=5V ± 5%, Cout=50pF

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{CAS}$ precharge time (Fast Page Mode)	tCP	10		10		10		10		ns	
access time from $\overline{OE}$	tOEA		15		15		20		20	ns	
$\overline{OE}$ to data-in delay time	tOED	15		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	15		15		20		20		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	12

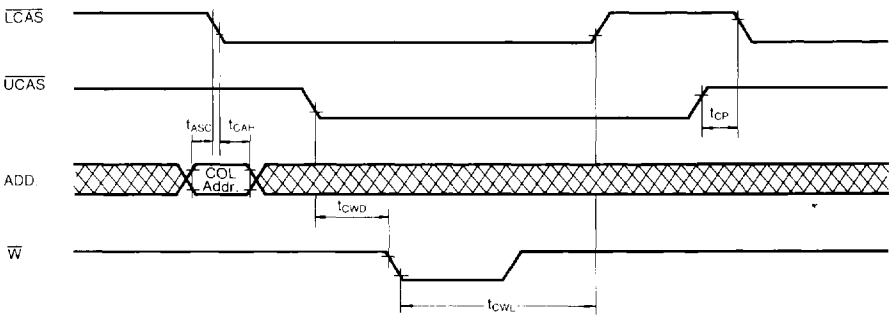
(*) 50ns Product:VCC=5V ± 5%, Cout=50pF

KM416C256B Truth Table

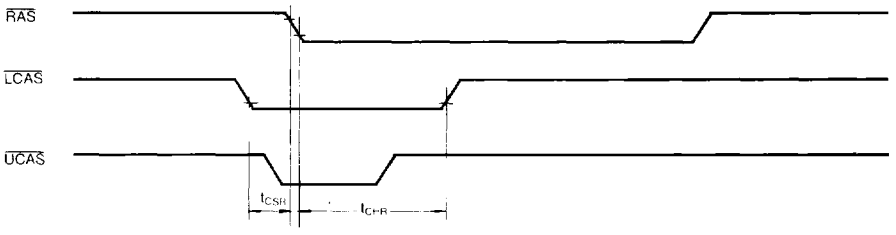
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16	STATE
H	H	H	H	H	HI-Z	HI-Z	Standby
L	H	H	H	H	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

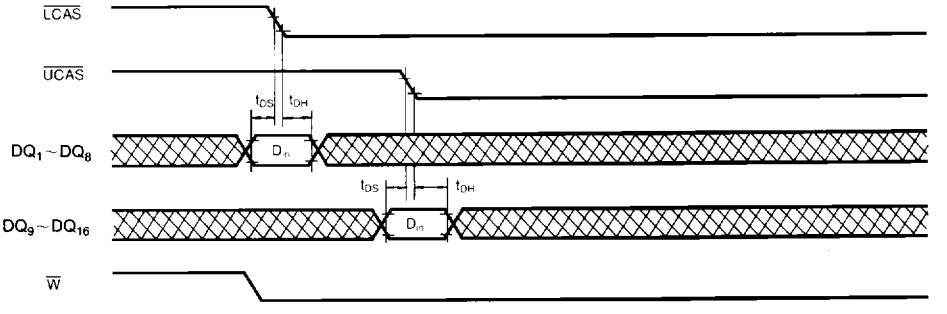
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. 512 cycles of burst refresh must be executed within 8ms before and after self refresh, In order to meet refresh specification.
13. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
14. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
15. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
16. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



17. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
18. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.

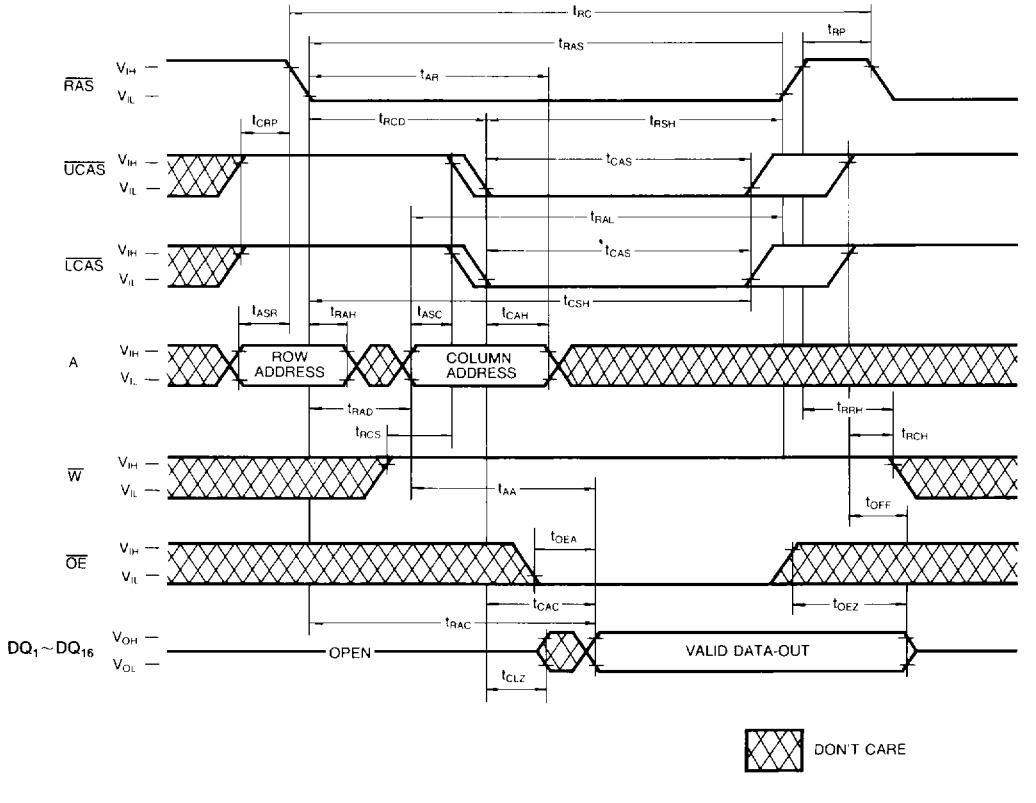


19. t_{DS}, t_{DH} is independetly specified for lower byte $D_{in(1\sim8)}$, upper byte $D_{in(9\sim16)}$.



TIMING DIAGRAMS

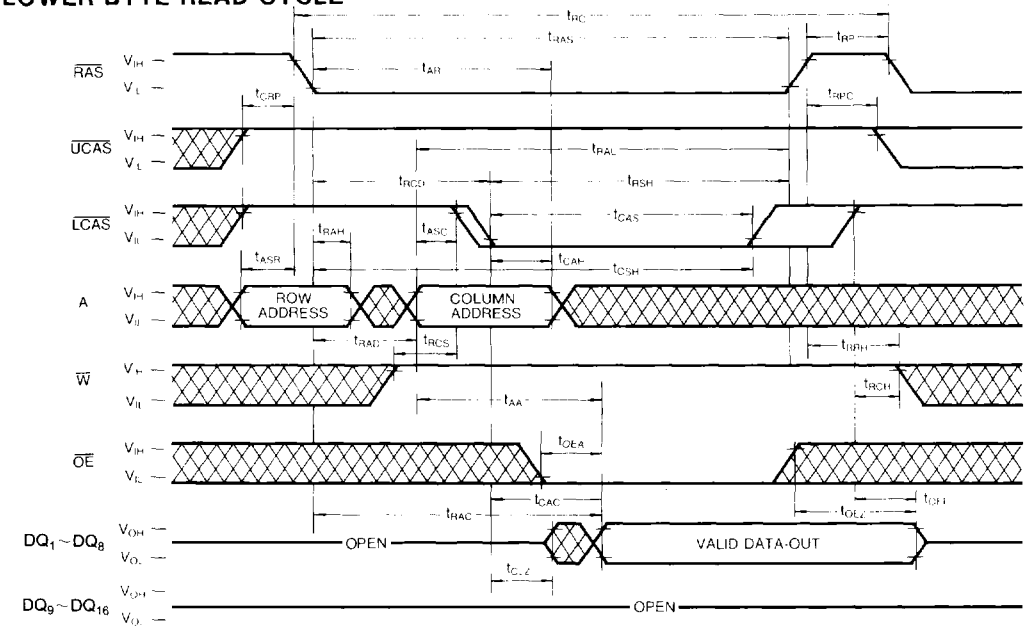
WORD READ CYCLE



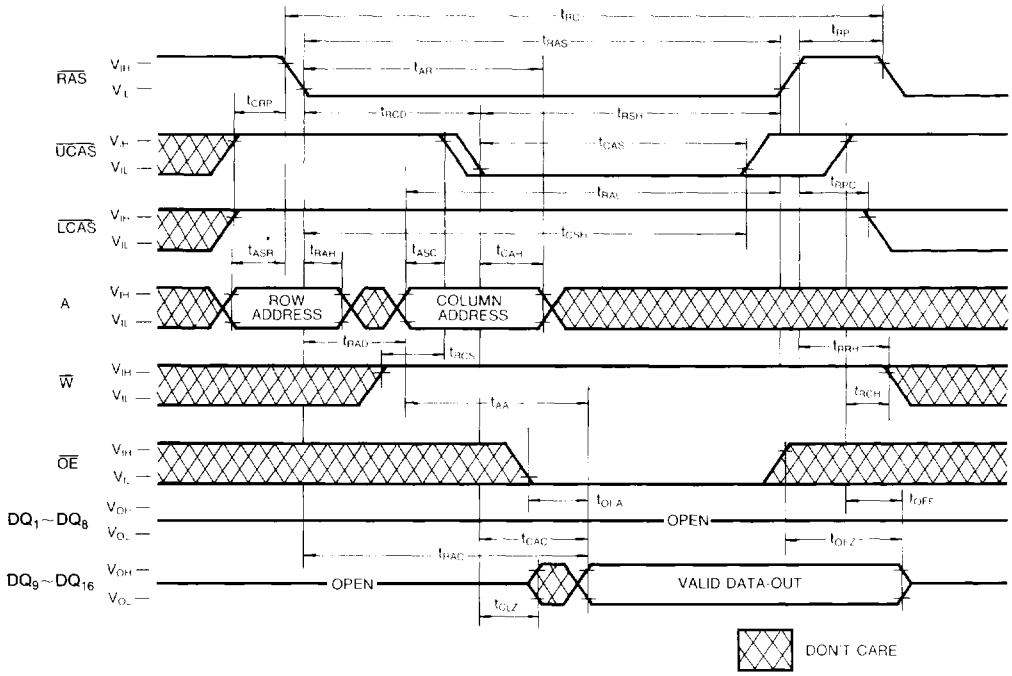
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE

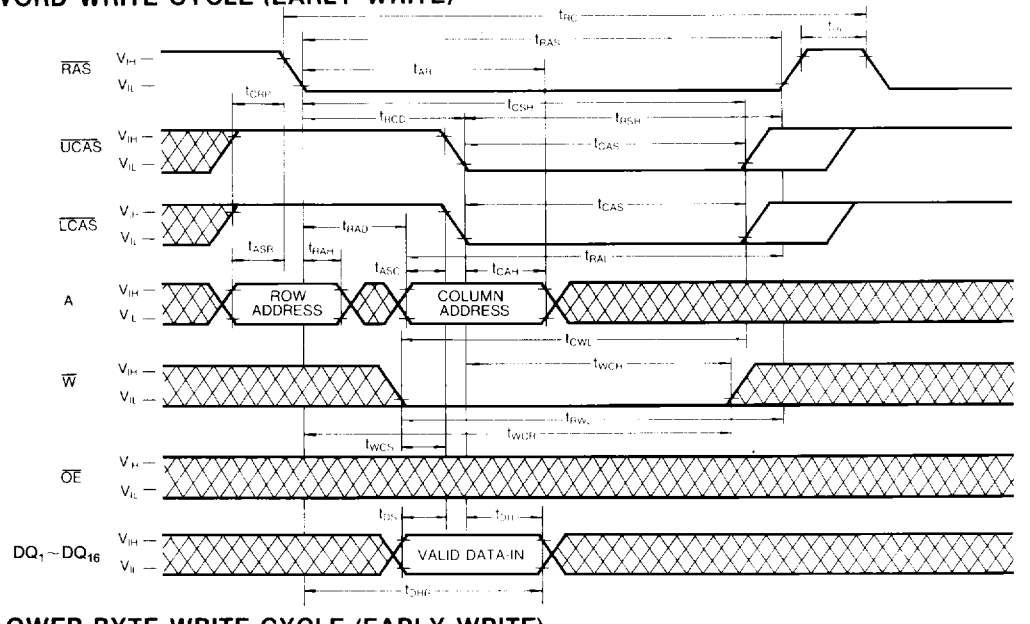


UPPER BYTE READ CYCLE

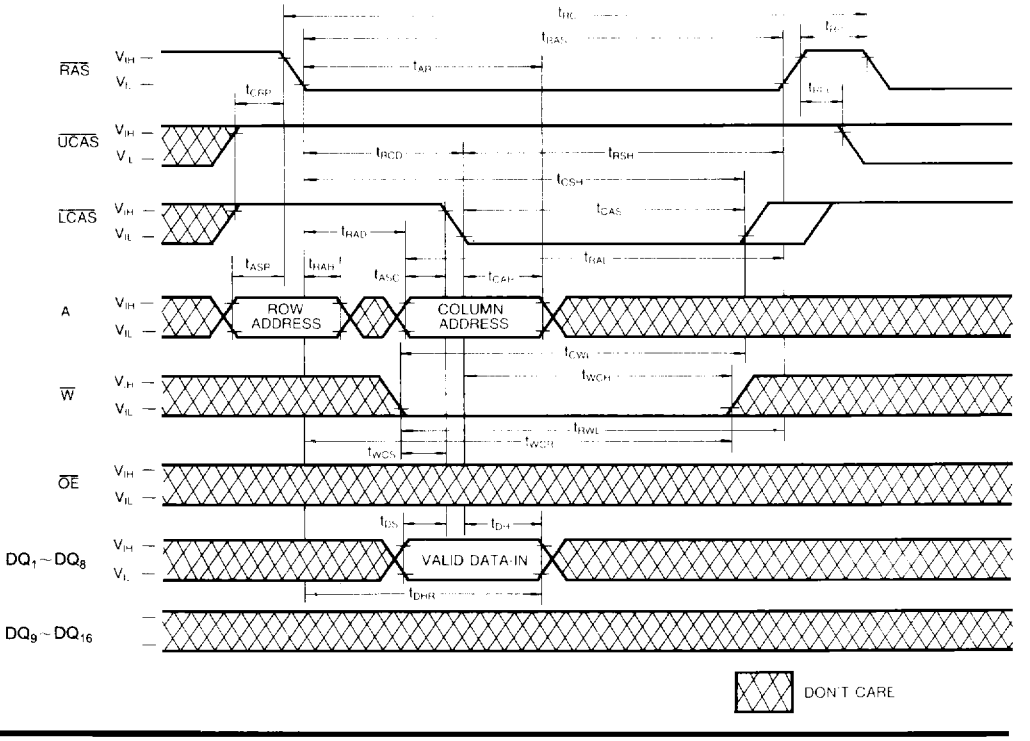


TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)

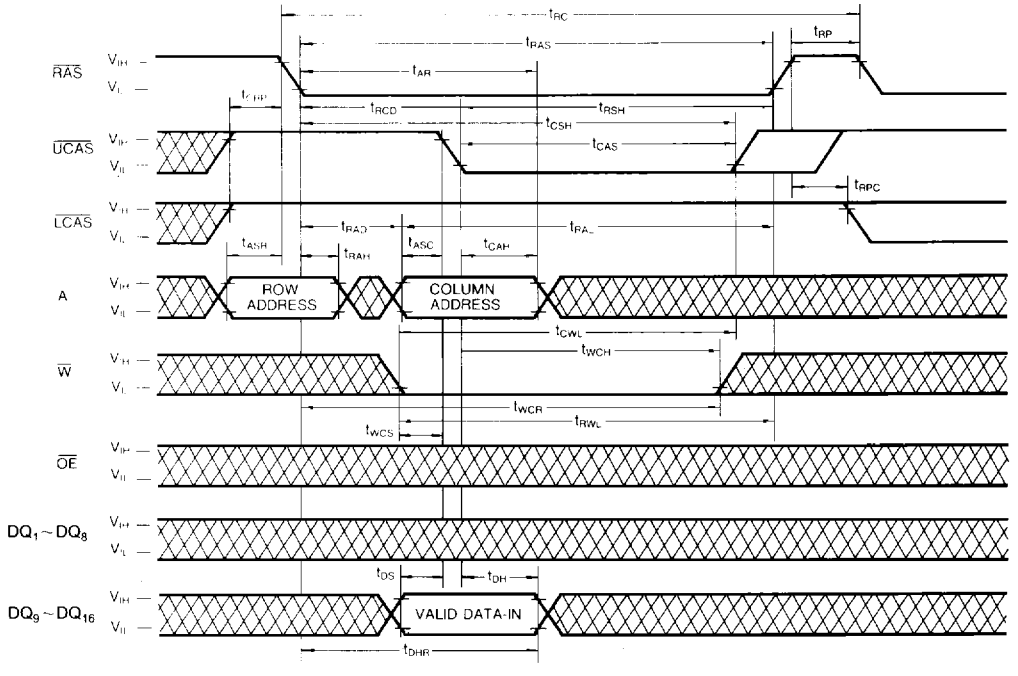


LOWER BYTE WRITE CYCLE (EARLY WRITE)

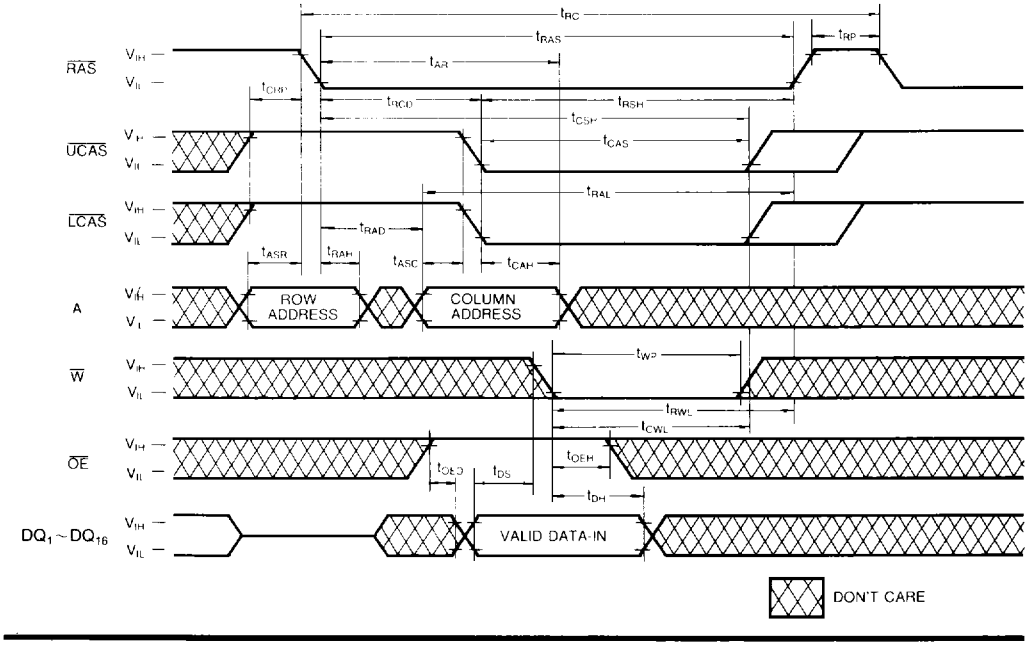


TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)

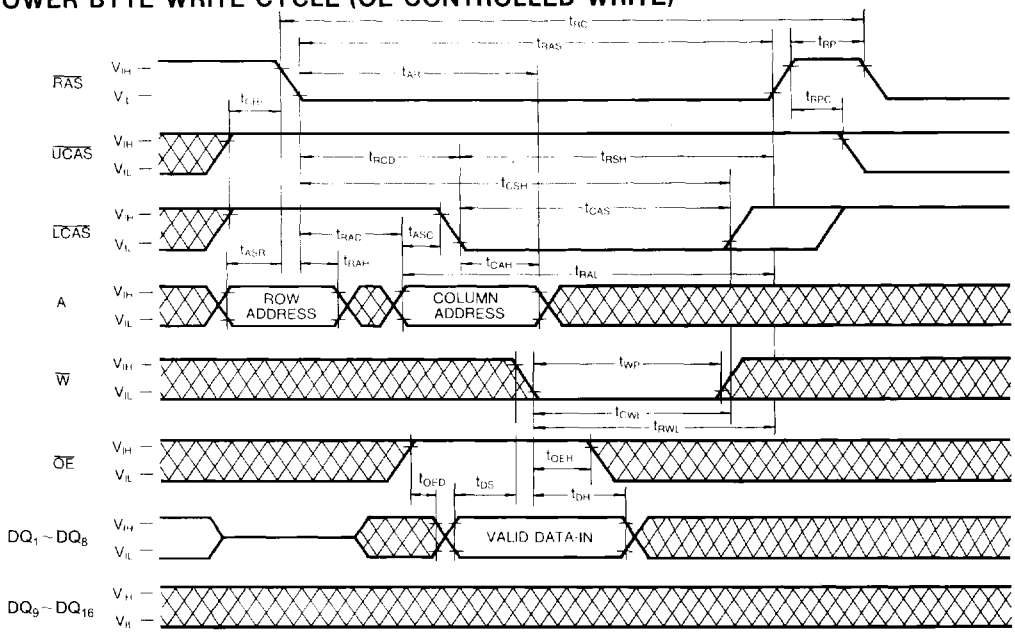


WORD WRITE CYCLE (OE CONTROLLED WRITE)

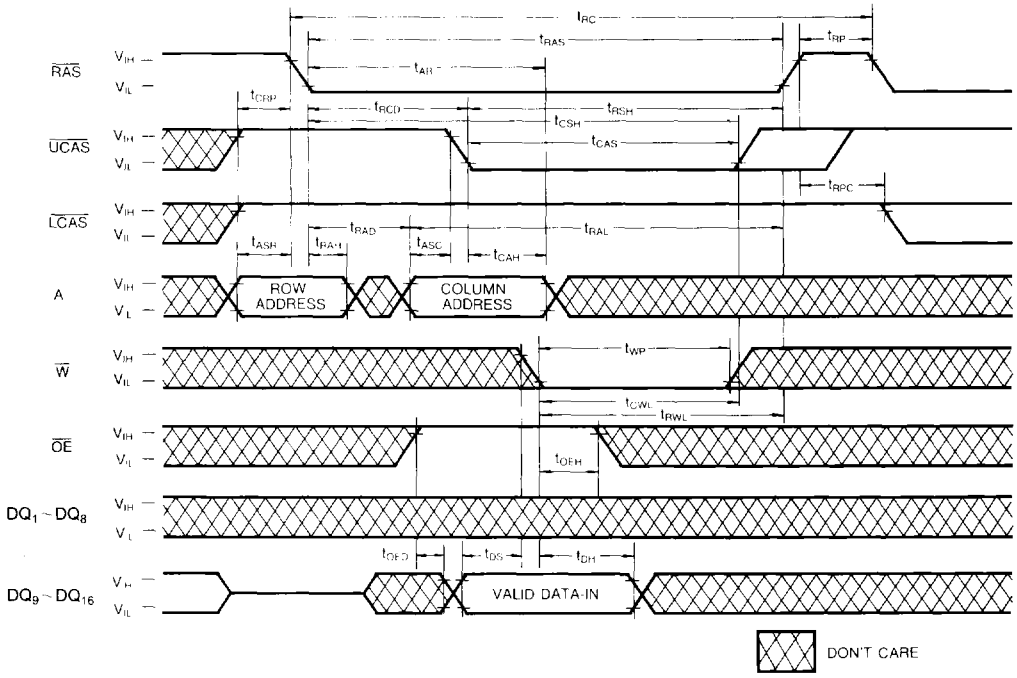


TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

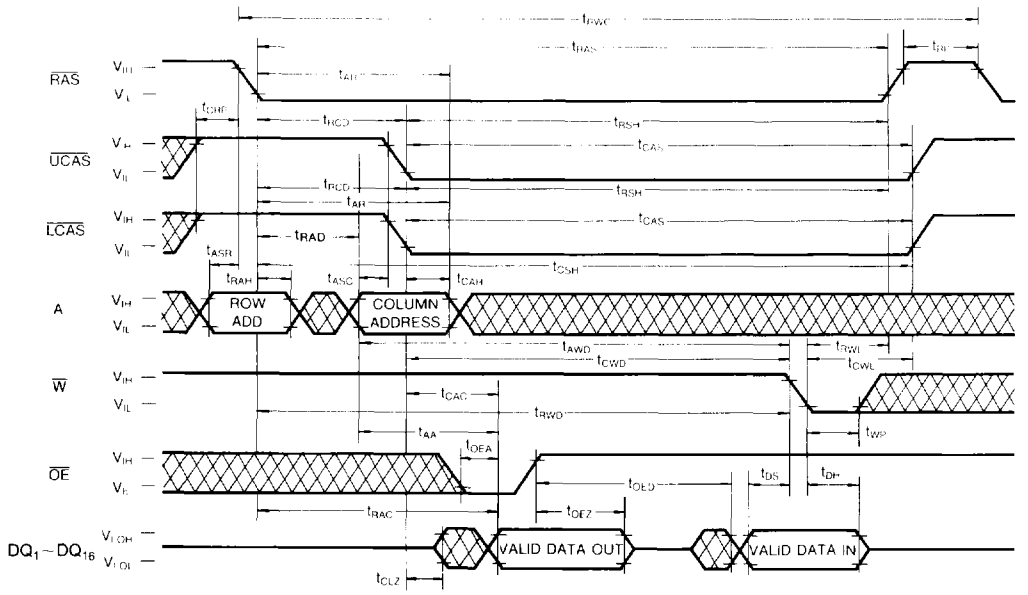


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

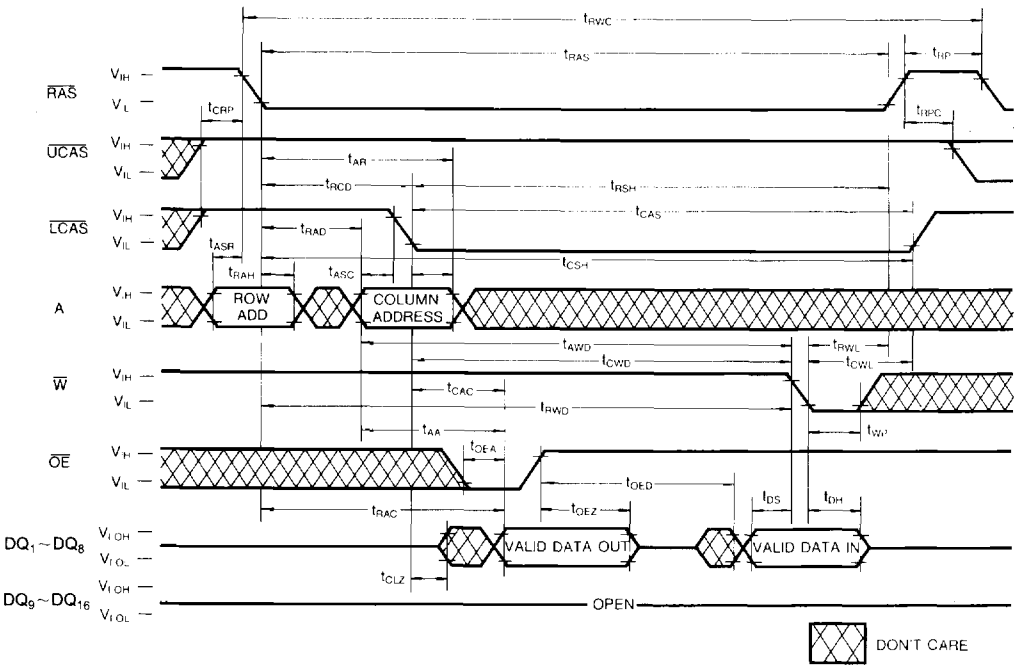


TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE

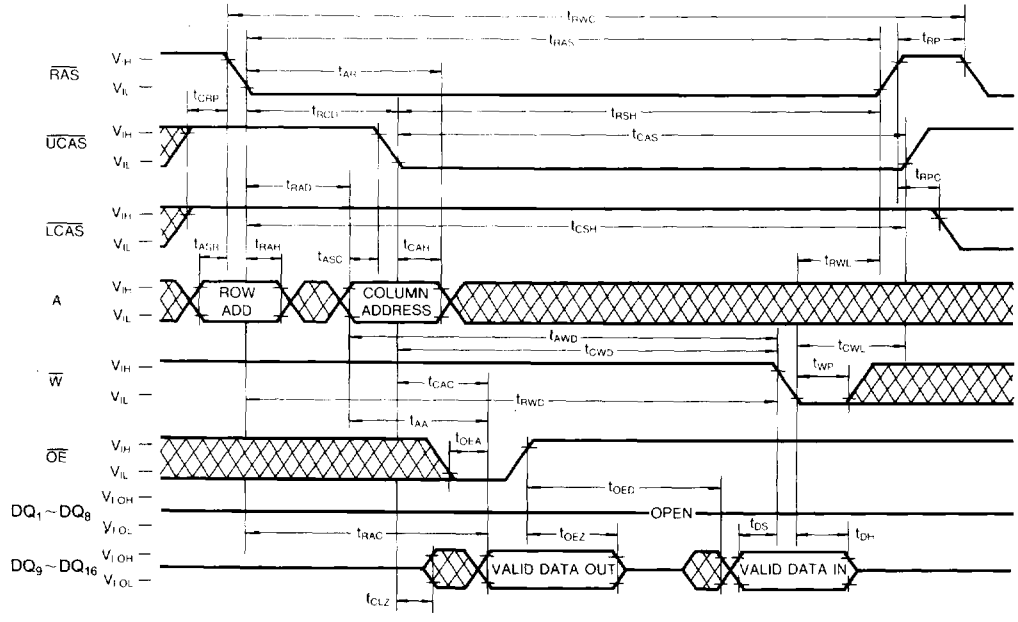


LOWER-BYTE READ-MODIFY-WRITE CYCLE

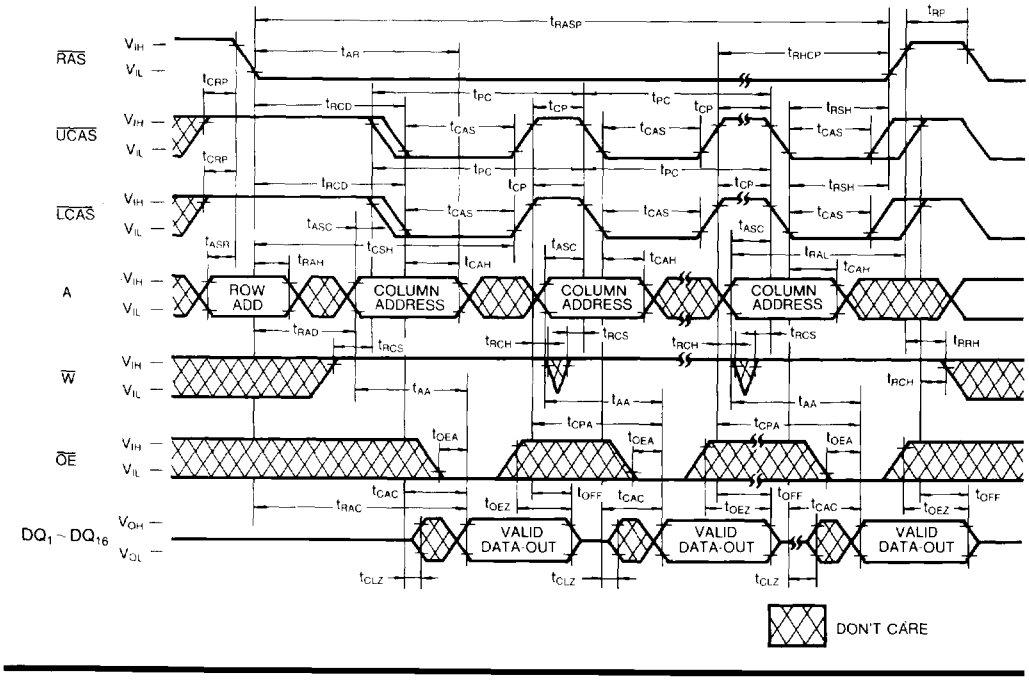


TIMING DIAGRAMS (Continued)

UPPER-BYTE READ-MODIFY-WRITE CYCLE

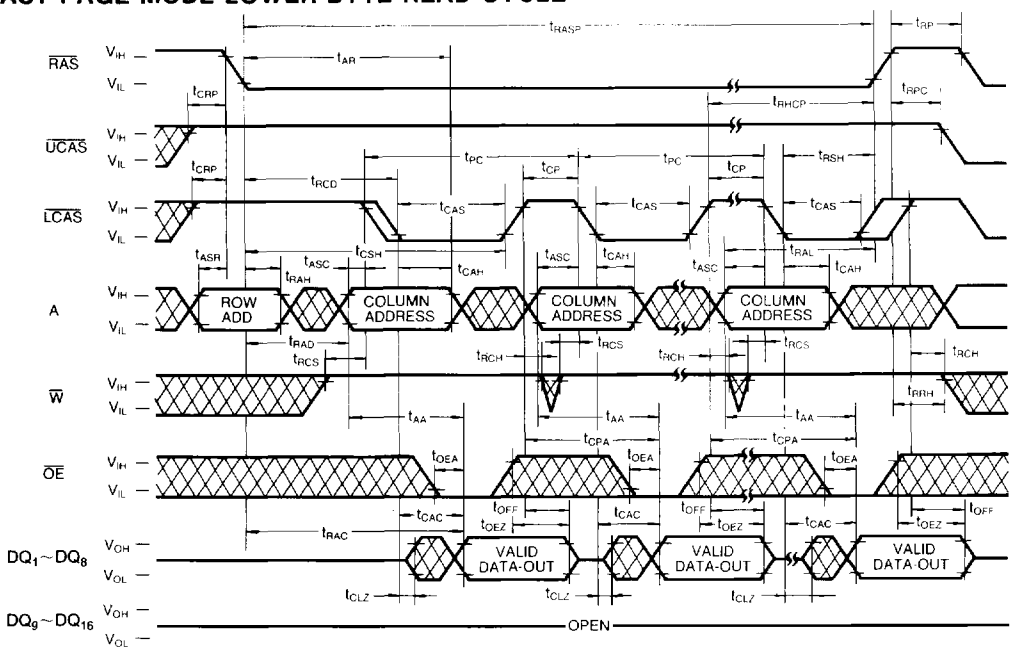


FAST PAGE MODE WORD READ CYCLE

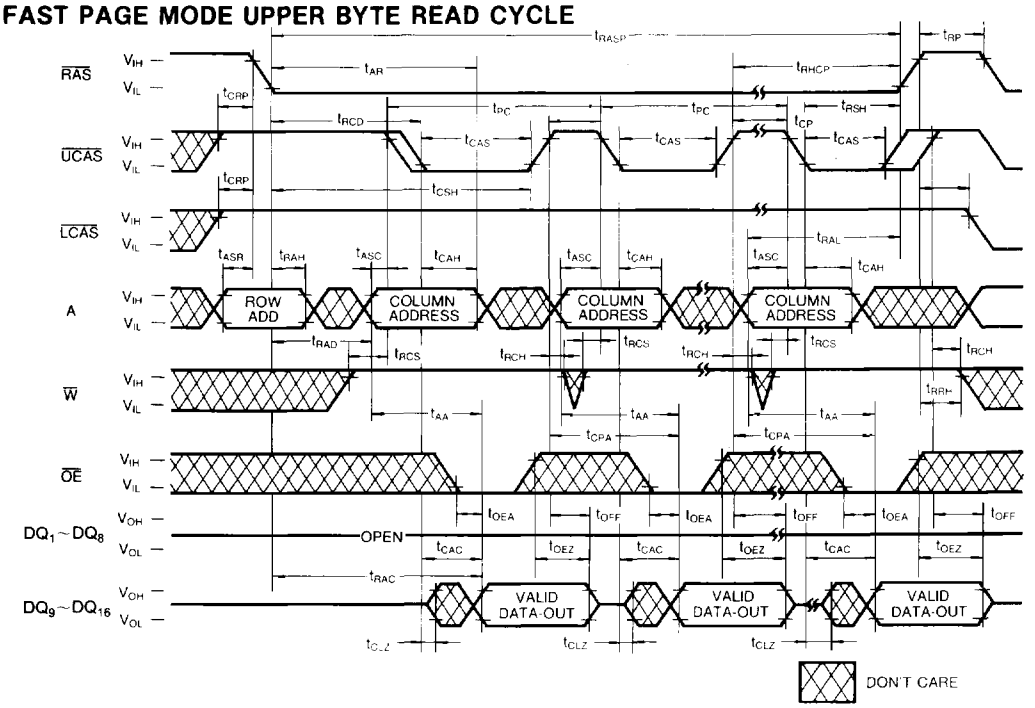


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE

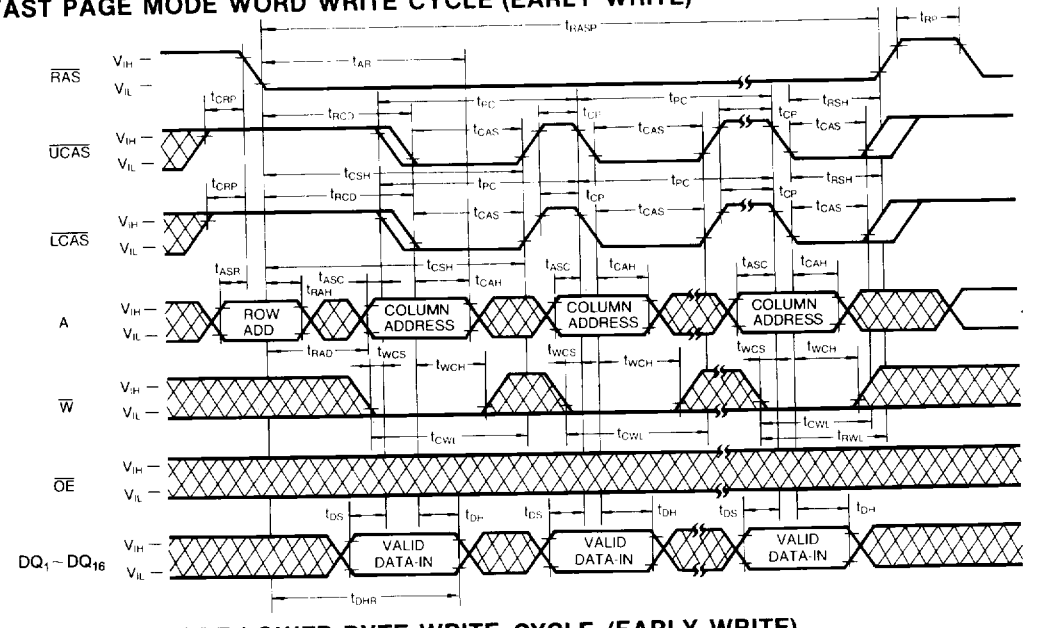


FAST PAGE MODE UPPER BYTE READ CYCLE

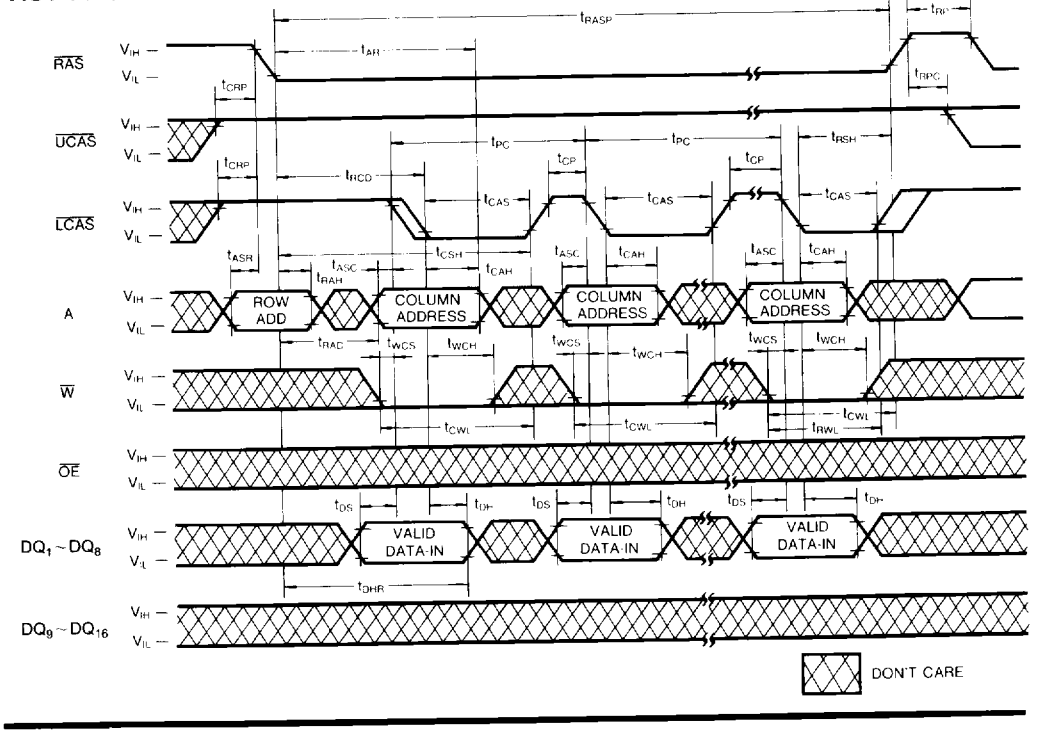


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)



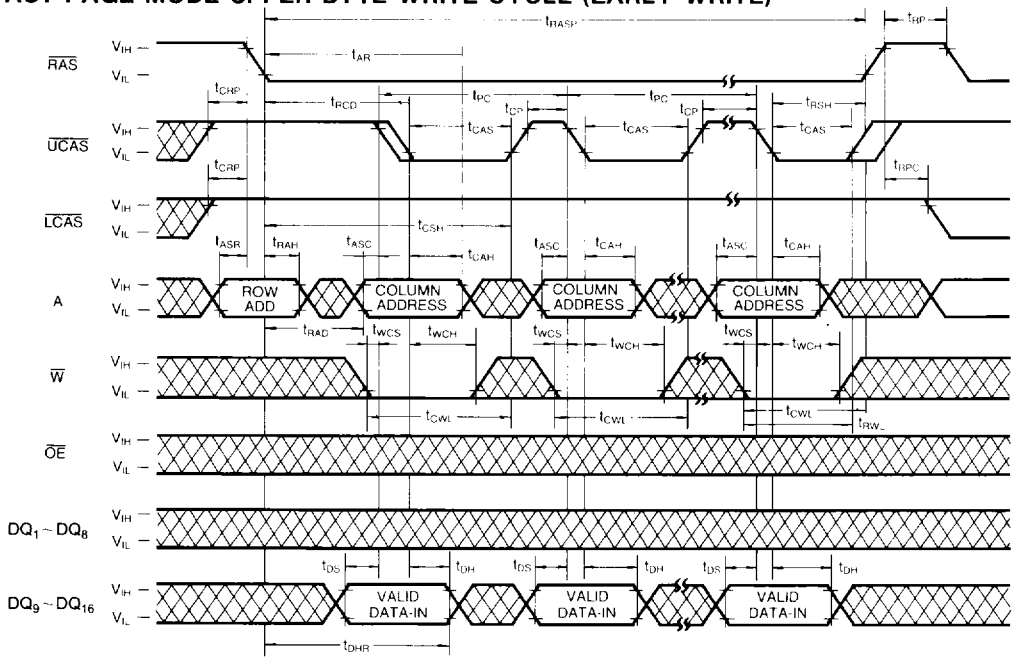
FAST PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)



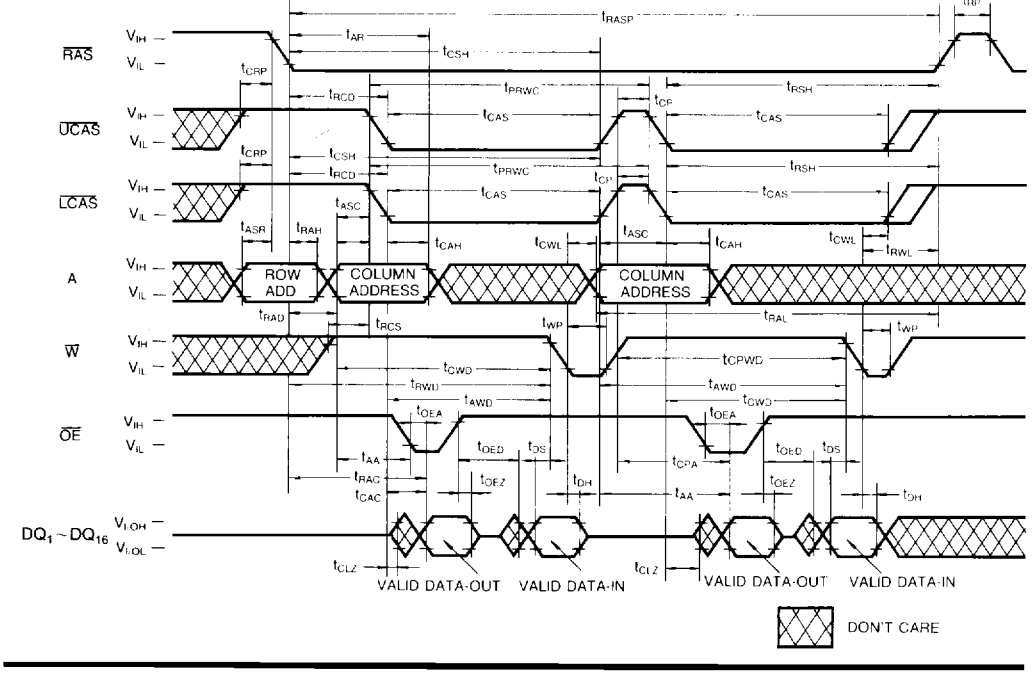
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

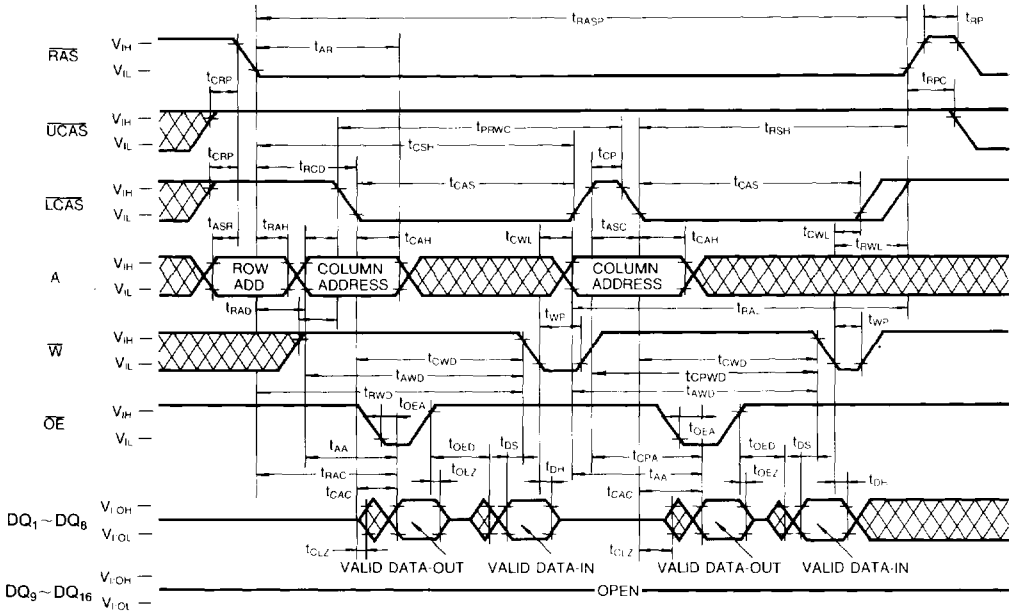


FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE

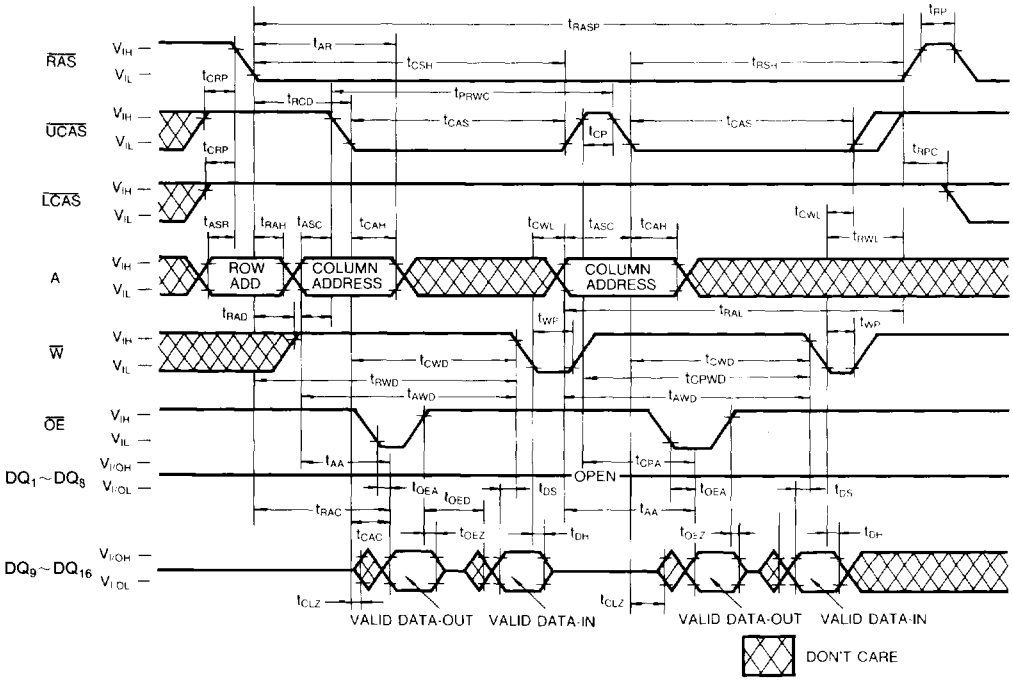


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE



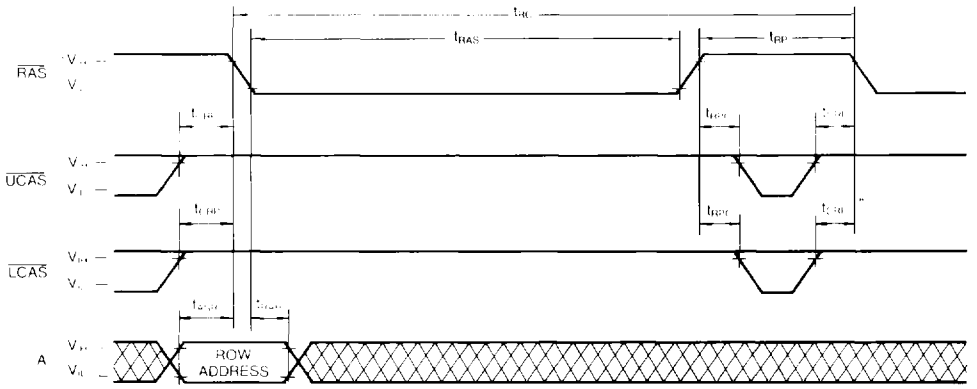
FAST PAGE MODE UPPER-BYTE- READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

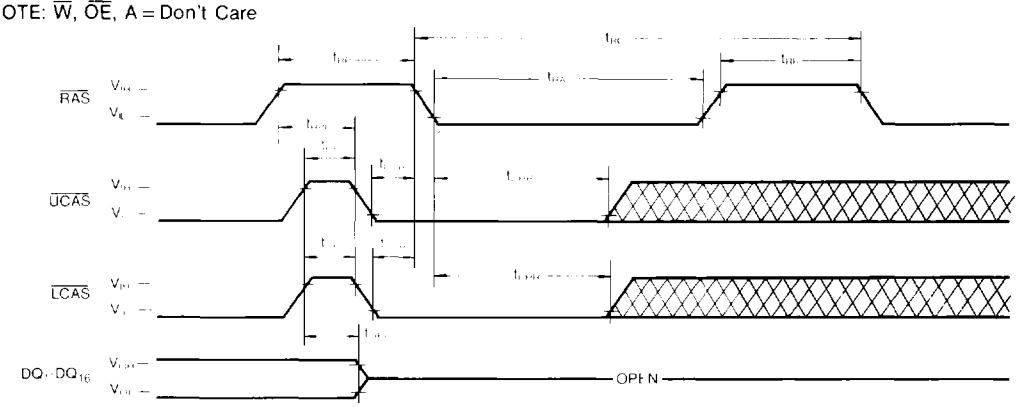
RAS ONLY REFRESH CYCLE

NOTE: W, OE = Don't Care



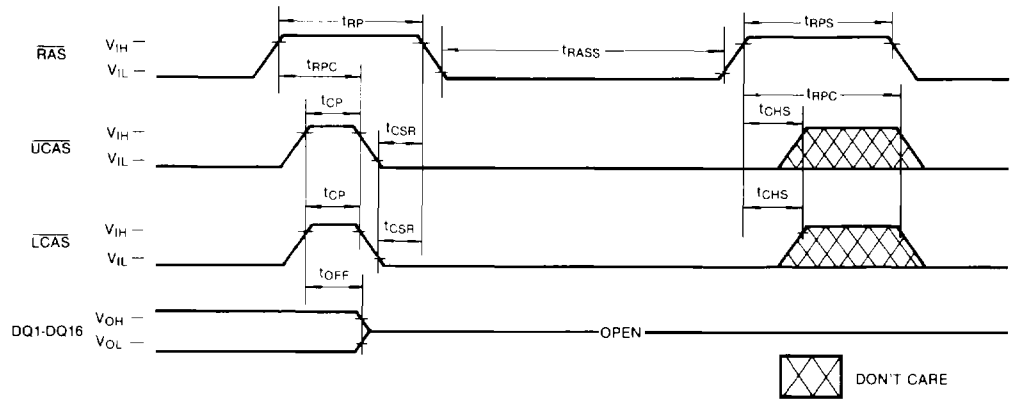
CAS-BEFORE-RAS REFRESH CYCLE

NOTE: W, OE, A = Don't Care



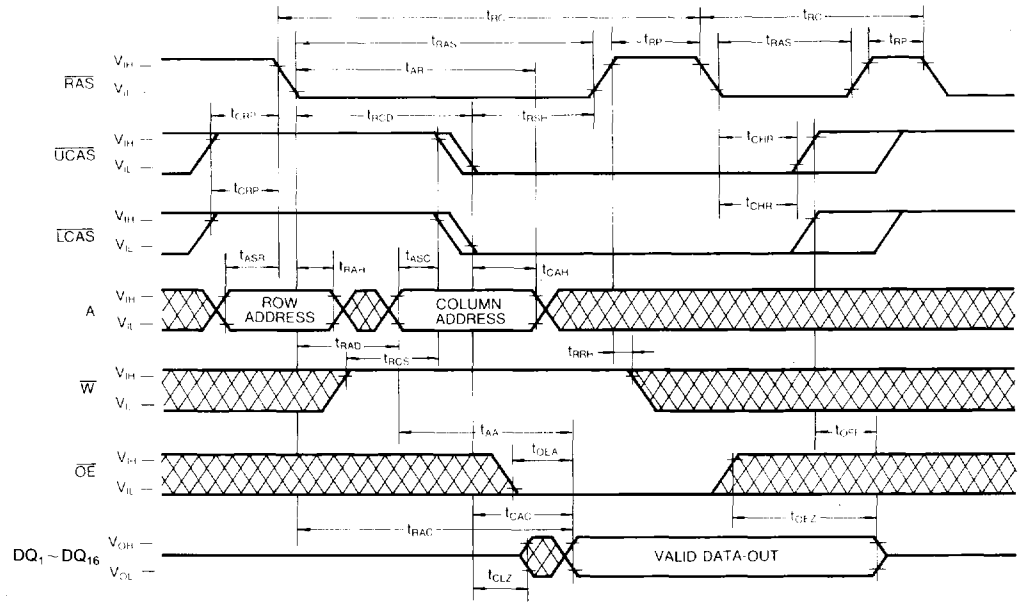
CAS-BEFORE-RAS SELF REFRESH CYCLE (LL-version)

NOTE: W, OE, A = Don't Care

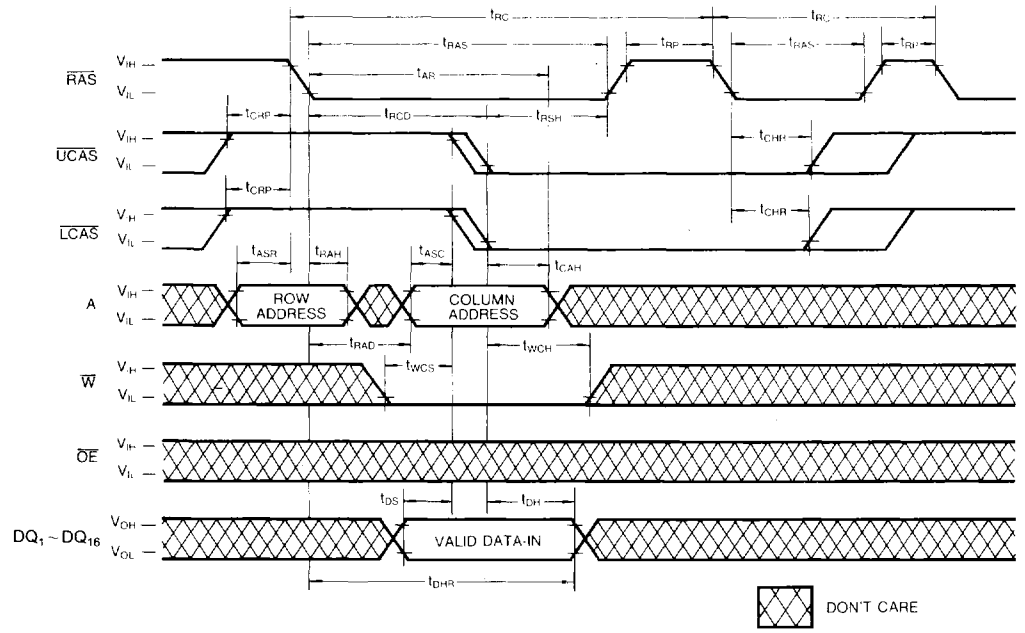


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



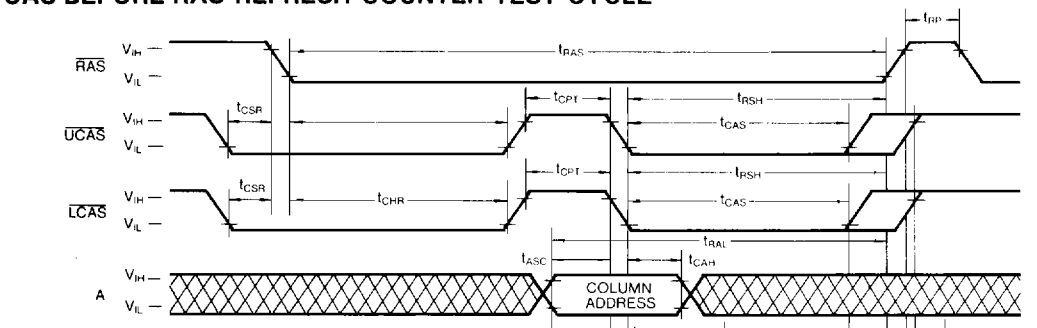
HIDDEN REFRESH CYCLE (WRITE)



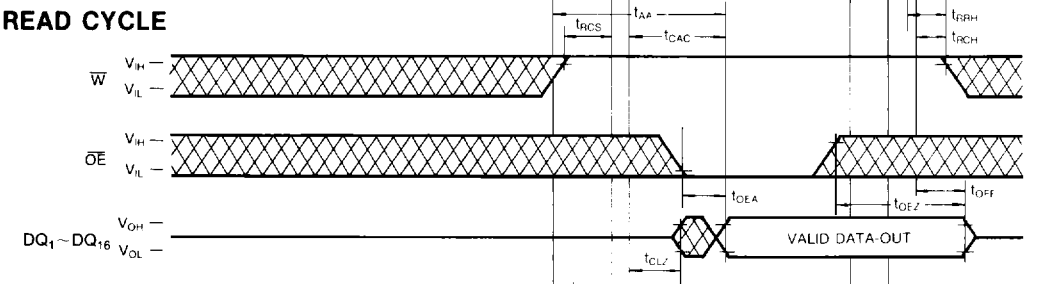
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

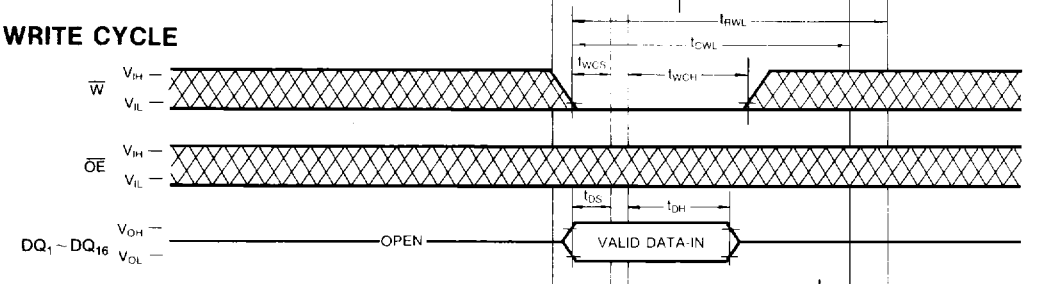
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



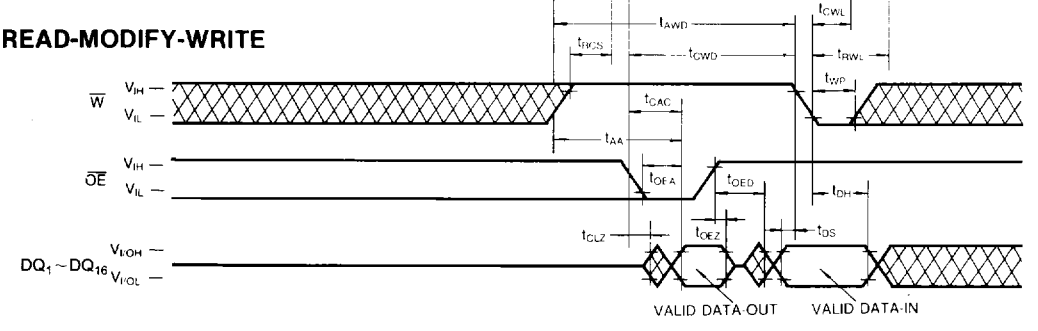
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE

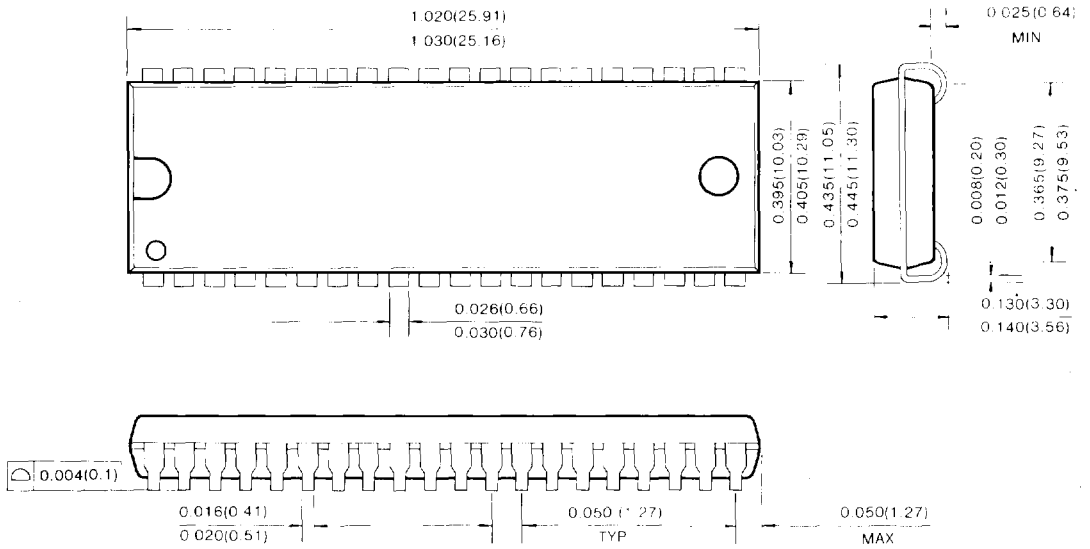


DON'T CARE

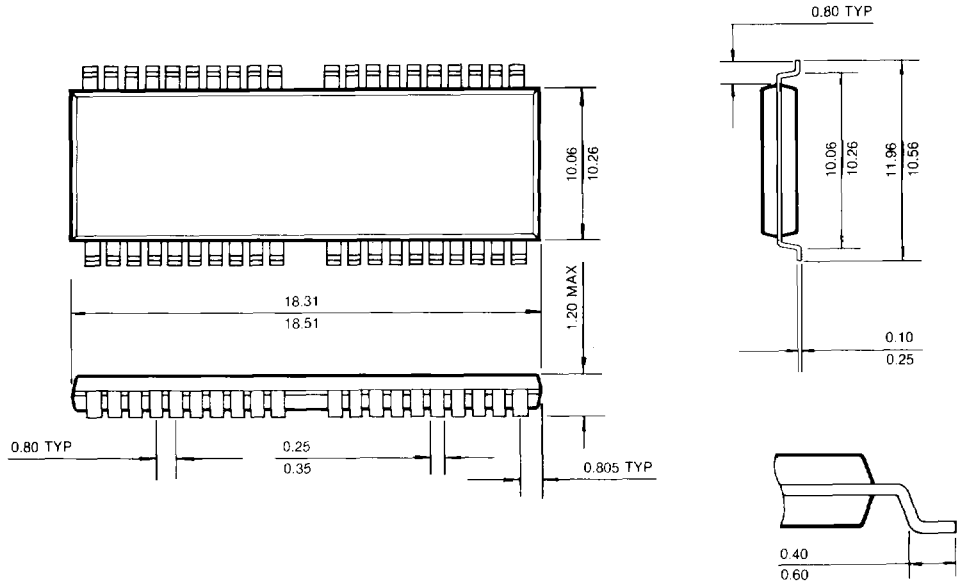
PACKAGE DIMENSION

40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



40 LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)
(Forward and Reverse Type)



SAMSUNG ELECTRONICS