National Semiconductor

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# MM54C905/MM74C905 12-Bit Successive Approximation Register

## General Description

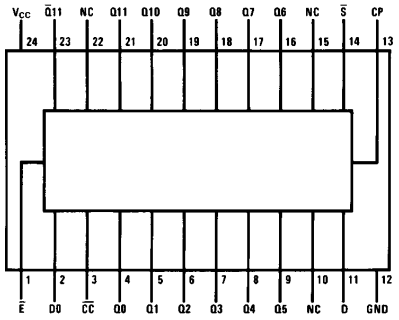
The MM54C905/MM74C905 CMOS 12-bit successive approximation register contains all the digit control and storage necessary for successive approximation analog-to-digital conversion. Because of the unique capability of CMOS to switch to each supply rail without any offset voltage, it can also be used in digital systems as the control and storage element in repetitive routines.

## Features

- Wide supply voltage range 3.0V to15V
- Guaranteed noise margin 1.0V
- High noise immunity $0.45V_{CC}$ typ
- Low power TTL compatibility fan out of 2 driving 74L
- Provision for register extension or truncation
- Operates in START/STOP or continuous conversion mode
- Drive ladder switches directly. For 10 bits or less with 50k/100k R/2R ladder network

## Connection Diagram

**Dual-In-Line Package**




TL/F/5712–1

**Top View**

**Order Number MM74C905N**
**See NS Package Number N24C**

**See the CMOS Logic Databook for Complete Specifications**

## Truth Table

| TIME | INPUTS | | | OUTPUTS | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_n$ | D | $\overline{S}$ | $\overline{E}$ | D0 | Q11 | Q10 | Q9 | Q8 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | 01 | Q0 | $\overline{C}$ |
| 0 | X | L | L | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| 1 | D11 | H | L | X | L | H | H | H | H | H | H | H | H | H | H | H | H |
| 2 | D10 | H | L | D11 | D11 | L | H | H | H | H | H | H | H | H | H | H | H |
| 3 | D9 | H | L | D10 | D11 | D10 | L | H | H | H | H | H | H | H | H | H | H |
| 4 | D8 | H | L | D9 | D11 | D10 | D9 | L | H | H | H | H | H | H | H | H | H |
| 5 | D7 | H | L | D8 | D11 | D10 | D9 | D8 | L | H | H | H | H | H | H | H | H |
| 6 | D6 | H | L | D7 | D11 | D10 | D9 | D8 | D7 | L | H | H | H | H | H | H | H |
| 7 | D5 | H | L | D6 | D11 | D10 | D9 | D8 | D7 | D6 | L | H | H | H | H | H | H |
| 8 | D4 | H | L | D5 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | L | H | H | H | H | H |
| 9 | D3 | H | L | D4 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | L | H | H | H | H |
| 10 | D2 | H | L | D3 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | L | H | H | H |
| 11 | D1 | H | L | D2 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | L | H | H |
| 12 | D0 | H | L | D1 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | L | H |
| 13 | X | H | L | D0 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | L |
| 14 | X | X | L | X | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | L |
|  | X | X | H | X | H | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC |

H = High level
L = Low level
X = Don't care
NC = No change

  RRD-B30M105/Printed in U. S. A.

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Voltage at Any Pin | $-0.3$ to $V_{CC}+0.3V$ |
| Operating Temperature Range | |
| MM74C905 | $-40°C$ to $+85°C$ |
| Storage Temperature Range | $-65°C$ to $+150°C$ |
| ESD Susceptibility (Note 4) | 400V |
| Package Dissipation | 500 mW |
| Operating $V_{CC}$ Range | 3.0V to 15V |
| Absolute Maximum $V_{CC}$ | 16V |
| Lead Temperature (Soldering, 10 seconds) | 260°C |

## DC Electrical Characteristics Min/max limits apply across temperature range, unless otherwise noted.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **CMOS TO CMOS** | | | | | |
| Logical "1" Input Voltage ($V_{IN(1)}$) | $V_{CC}=5.0V$<br>$V_{CC}=10V$ | 3.5<br>8.0 | | | V<br>V |
| Logical "0"Input Voltage ($V_{IN(0)}$) | $V_{CC}=5.0V$<br>$V_{CC}=10V$ | | | 1.5<br>2.0 | V<br>V |
| Logical "1" Output Voltage ($V_{OUT(1)}$) | $V_{CC}=5.0V$, $I_O=-10\mu A$<br>$V_{CC}=10V$, $I_O=-10\mu A$ | 4.5<br>9.0 | | | V<br>V |
| Logical "0" Output Voltage ($V_{OUT(0)}$) | $V_{CC}=5.0V$, $I_O=10\mu A$<br>$V_{CC}=10V$, $I_O=10\mu A$ | | | 0.5<br>1.0 | V<br>V |
| Logical "1" Input Current ($I_{IN(1)}$) | $V_{CC}=15V$, $V_{IN}=15V$ | | 0.005 | 1.0 | $\mu A$ |
| Logical "0" Input Current ($I_{IN(0)}$) | $V_{CC}=15V$, $V_{IN}=0V$ | $-1.0$ | $-0.005$ | | $\mu A$ |
| Supply Current ($I_{CC}$) | $V_{CC}=15V$ | | 0.05 | 300 | $\mu A$ |
| **CMOS/LPTTL INTERFACE** | | | | | |
| Logical "1" Input Voltage ($V_{IN(1)}$) | | | | | |
| MM54C905 | $V_{CC}=4.5V$ | $V_{CC}-1.5$ | | | V |
| MM74C905 | $V_{CC}=4.75V$ | $V_{CC}-1.5$ | | | V |
| Logical "0" Input Voltage ($V_{IN(0)}$) | | | | | |
| MM54C905 | $V_{CC}=4.5V$ | | | 0.8 | V |
| MM74C905 | $V_{CC}=4.75V$ | | | 0.8 | V |
| Logical "1" Output Voltage ($V_{OUT(1)}$) | | | | | |
| MM54C905 | $V_{CC}=4.5V$, $I_O=-360\mu A$ | 2.4 | | | V |
| MM74C905 | $V_{CC}=4.75V$, $I_O=-360\mu A$ | 2.4 | | | V |
| Logical "0" Output Voltage ($V_{OUT(0)}$) | | | | | |
| MM54C905 | $V_{CC}=4.5V$, $I_O=360\mu A$ | | | 0.4 | V |
| MM74C905 | $V_{CC}=4.75V$, $I_O=360\mu A$ | | | 0.4 | V |
| **OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)** | | | | | |
| Output Source Current ($I_{SOURCE}$) (P-Channel) | $V_{CC}=5.0V$, $V_{OUT}=0V$<br>$T_A=25°C$ | $-1.75$ | $-3.3$ | | mA |
| Output Source Current ($I_{SOURCE}$) (P-Channel) | $V_{CC}=10V$, $V_{OUT}=0V$<br>$T_A=25°C$ | $-8.0$ | $-15$ | | mA |
| Output Sink Current ($I_{SINK}$) (N-Channel) | $V_{CC}=5.0V$, $V_{OUT}=V_{CC}$<br>$T_A=25°C$ | 1.75 | 3.6 | | mA |
| Output Sink Current ($I_{SINK}$) (N-Channel) | $V_{CC}=10V$, $V_{OUT}=V_{CC}$<br>$T_A=25°C$ | 8.0 | 16 | | mA |
| Q11–Q0 Outputs<br>$R_{SOURCE}$ | $V_{CC}=10V\pm5\%$<br>$V_{OUT}=V_{CC}-0.3V$<br>$T_A=25°C$ | 150 | | 350 | $\Omega$ |
| $R_{SINK}$ | $V_{CC}=10V\pm5\%$<br>$V_{OUT}=0.3V$<br>$T_A=25°C$ | 80 | | 230 | $\Omega$ |

## AC Electrical Characteristics $T_A = 25°C, C_L = 50pF$, unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Propagation Delay Time From Clock | $V_{CC} = 5.0V$ | | 200 | 350 | ns |
| Input To Outputs (Q0–Q11)($t_{pd(Q)}$) | $V_{CC} = 10V$ | | 80 | 150 | ns |
| Propagation Delay Time From Clock | $V_{CC} = 5.0V$ | | 180 | 325 | ns |
| Input To $D_O$($t_{pd(D_O)}$) | $V_{CC} = 10V$ | | 70 | 125 | ns |
| Propagation Delay Time From Register | $V_{CC} = 5.0V$ | | 190 | 350 | ns |
| Enable ($\overline{E}$) To Output (Q11) ($t_{pd(\overline{E})}$) | $V_{CC} = 10V$ | | 75 | 150 | ns |
| Propagation Delay Time From Clock | $V_{CC} = 5.0V$ | | 190 | 350 | ns |
| To $\overline{CC}$ ($t_{pd(\overline{CC})}$) | $V_{CC} = 10V$ | | 75 | 0.50 | ns |
| Data Input Set-UpTime ($t_{DS}$) | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | 80<br>30 | | | ns<br>ns |
| Start Input Set-Up Time ($t_{SS}$) | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | 80<br>30 | | | ns<br>ns |
| Minimum Clock Pulse Width ($t_{PWL}$,$t_{PWH}$) | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | 250<br>100 | 125<br>40 | | ns<br>ns |
| Maximum Clock Rise and Fall Time ($t_r$, $t_f$) | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | | | 15<br>5 | $\mu$s<br>$\mu$s |
| Maximum Clock Frequency ($f_{MAX}$) | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | 2<br>5 | 4<br>10 | | MHz<br>MHz |
| Clock Input Capacitance ($C_{CLK}$) | Clock Input (Note 2) | | 10 | | pF |
| Input Capacitance ($C_{IN}$) | Any Other Input (Note 2) | | 5 | | pF |
| Power Dissipation Capacitance ($C_{PD}$) | (Note 3) | | 100 | | pF |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

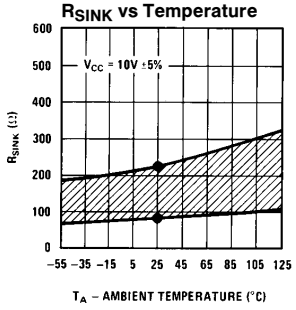
**Note 2:** Capacitance is guaranteed by periodic testing.

**Note 3:** $C_{PD}$ determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

**Note 4:** Human body model, 100 pF discharged through a 1.5 kΩ resistor.

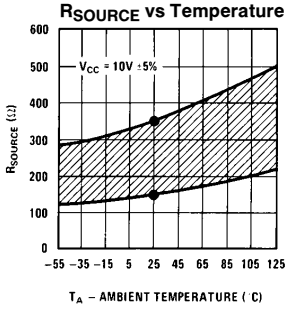
## Typical Performance Characteristics

**$R_{SINK}$ vs Temperature**




•These points are guaranteed by automatic testing

**$R_{SOURCE}$ vs Temperature**




•These points are guaranteed by automatic testing.

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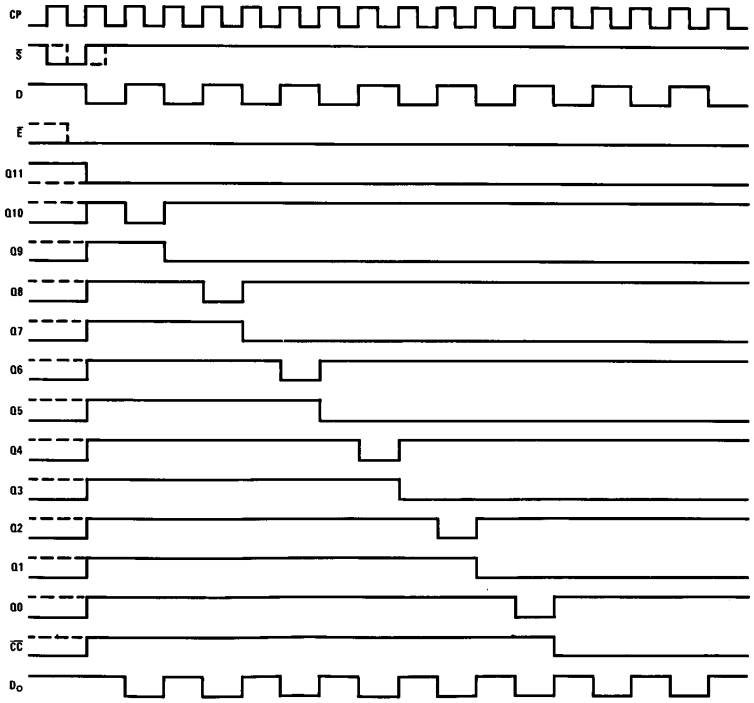
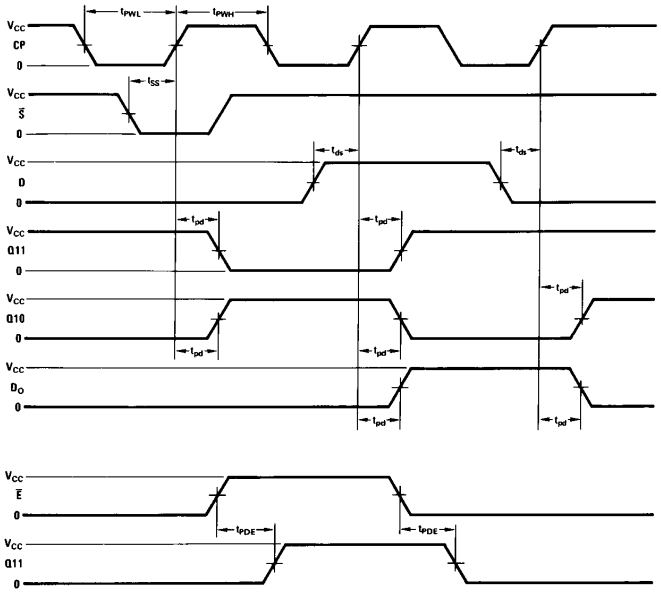
## Timing Diagram




## Switching Time Waveforms

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## Typical Performance Characteristics

**USER NOTES FOR A/D CONVERSION**

The register can be used with either current switches that require a low voltage level to turn the switch ON or current switches that require a high voltage level to turn the switch ON. If current switches are used which turn ON with a low logic level, the resulting digit output from the register is active low. That is, a logic "1" is represented as a low voltage level. If current switches are used which turn ON with a high logic level, the resulting digit output is active high. A logic "1" is represented as a high voltage level.

For a maximum error of $\pm 1/2$ LSB, the comparator must be biased. If current switches that require a high voltage level to turn ON are used, the comparator should be biased $+1/2$ LSB and if the current switches require a low logic level to turn ON, then the comparator must be biased $-1/2$ LSB.

The register can be used to perform 2's complement conversion by offsetting the comparator one half full range $+1/2$ LSB and using the complement of the MSB Q11 as the sign bit.

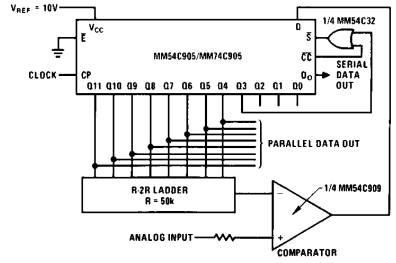
If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power-ON. This situation can be overcome by making the START input the "OR" function of $\overline{CC}$ and the appropriate register output.

The register, by suitable selection of register ladder network, can be used to perform either binary or BCD conversion.

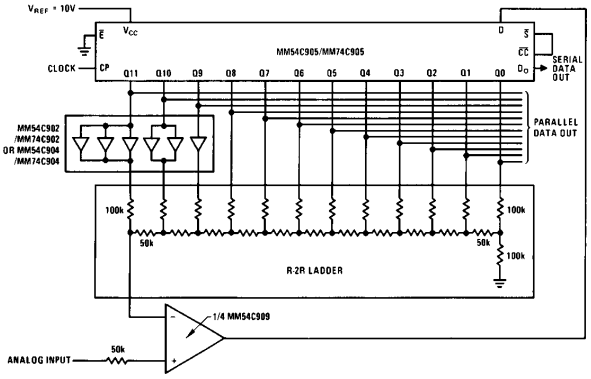
The register outputs can drive the 10 bits or less with 50k/100k R/2R ladder network directly for $V_{CC} = 10V$ or higher. In order to drive the 12-bit 50k/100k ladder network and have the $\pm 1/2$ LSB resolution, the MM54C902/MM74C902 or MM54C904/MM74C904 is used as a buffer, three buffers for MSB (Q11), two buffers for Q10, and one buffer for Q9.

## Typical Applications

**12-Bit Successive Approximation A-to-D Converter Operating in Continuous 8-Bit Truncated Mode**




**12-Bit Successive Approximation A-to-D Converter, Operating in Continuous Mode, Drives the 50k/100k Ladder Network Directly**

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## Definition of Terms

**CP:** Register *clock* input.

**$\overline{CC}$:** *Conversion complete*—this output remains at $V_{OUT(1)}$ during a conversion and goes to $V_{OUT(0)}$ when conversion is complete.

**D:** Serial *data* input—connected to comparator output in A-to-D applications.

**$\overline{E}$:** *Register enable*—this input is used to expand the length of the register. When $\overline{E}$ is at $V_{IN(1)}$ Q11 is forced to $V_{OUT(1)}$ and inhibits conversion. When not used for expansion $\overline{E}$ must be connected to $V_{IN(0)}$ (GND).

**Q11:** True register MSB output.

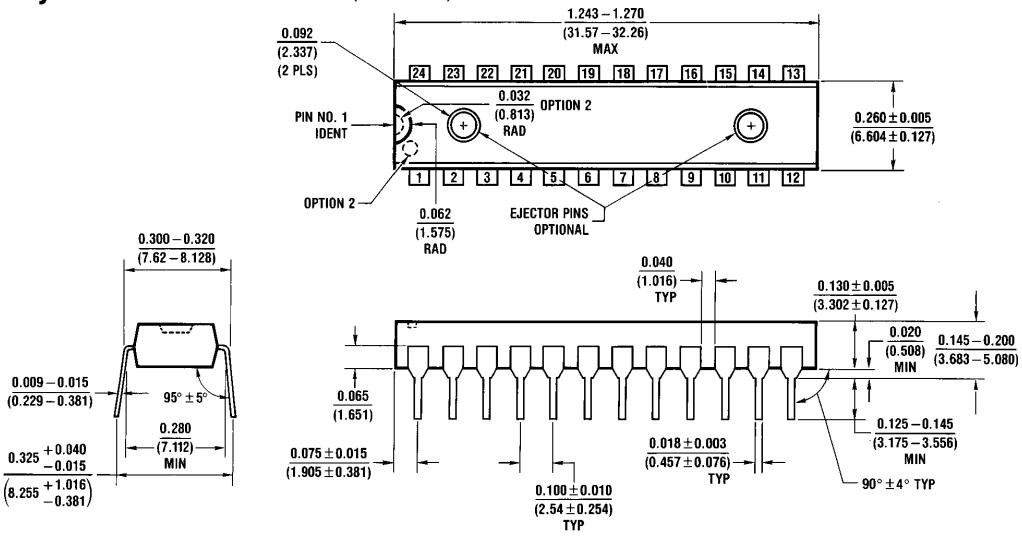
**$\overline{Q}$11:** Complement of register MSB output.

**Qi (i = 0 to 11):** Register outputs.

**$\overline{S}$:** *Start input*—holding start input at $V_{IN(0)}$ for at least one clock period will initiate a conversion by setting MSB (Q11) at $V_{OUT(0)}$ and all other output (Q-10–Q0) at $V_{OUT(1)}$. If set-up time requirements are met, a conversion may be initiated by holding start input at $V_{IN(0)}$ for less than one clock period.

**DO:** *Serial data output*—D input delayed by one clock period.

## Physical Dimensions inches (millimeters)




N24C (REV F)

**Molded Dual-In-Line Package (N)**
**Order Number MM74C905N**
**NS Package Number N24C**

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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