# Analog Switches

## MM450/MM550, MM451/MM551
## MM452/MM552, MM455/MM555 MOS analog switches

### general description

The MM450, and MM550 series each contain four p channel MOS enhancement mode transistors built on a single monolithic chip. The four transistors are arranged as follows:

| | |
|---|---|
| MM450, MM550 | Dual Differential Switch |
| MM451, MM551 | Four Channel Switch |
| MM452, MM552 | Four MOS Transistor Package |
| MM455, MM555 | Three MOS Transistor Package |

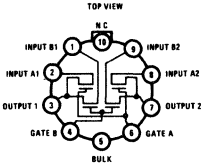
These devices are useful in many airborne and ground support systems requiring multiplexing, analog transmission, and numerous signal routing applications. The use of low threshold transistors ($V_{TH}$ = 2 volts) permits operations with large analog input swings (± 10 volts) at low gate voltages (−20 volts). Significant features, then, include:

- Large Analog Input Swing ±10 Volts
- Low Supply Voltage $V_{BULK}$ = +10 Volts, $V_{GG}$ = −20 Volts
- Low ON Resistance $V_{IN}$ = −10V 150Ω; $V_{IN}$ = +10V 75Ω
- Low Leakage Current 200 pA @ 25°C
- Input Gate Protection
- Zero Offset Voltage

Each gate input is protected from static charge build-up by the incorporation of zener diode protective devices connected between the gate input and device bulk.

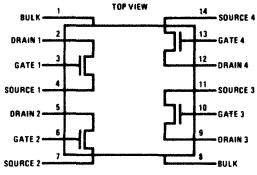
The MM450, MM451, MM452 and MM455 are specified for operation over the −55°C to +125°C military temperature range. The MM550, MM551, MM552 and MM555 are specified for operation over the −25°C to +70°C temperature range.

### schematic and connection diagrams




Note Pin 5 connected to case and device bulk. MM450, MM550

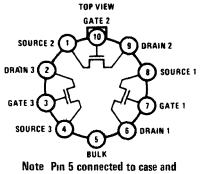
**Order Number MM450H or MM550H**
**See Package 12**




Note 1 Pins 1 and 8 connected to case and device bulk Drain and Source may be interchanged MM452F, MM552F
Note 2 MM452D and MM552D (dual-in-line packages) have same pin connections as MM452F and MM552F shown above

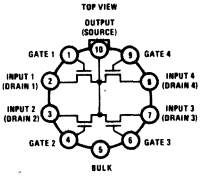
**Order Number MM452F or MM552F**
**See Package 4**

**Order Number MM452D or MM552D**
**See Package 1**




Note Pin 5 connected to case and device bulk Drain and Source may be interchanged MM455, MM555

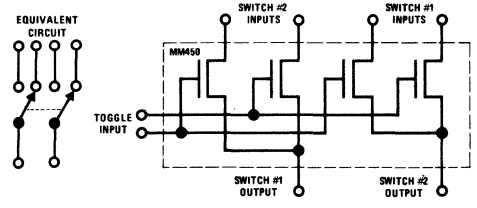
**Order Number MM455H or MM555H**
**See Package 12**




Note Pin 5 connected to case and device bulk MM451, MM551

**Order Number MM451H or MM551H**
**See Package 12**

### typical applications




DPDT Analog Switch

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## absolute maximum ratings

| | MM450, MM451, MM452, MM455 | MM550, MM551, MM552, MM555 |
|---|---|---|
| Gate Voltage ($V_{GG}$) | +10V to -30V | +10V to -30V |
| Bulk Voltage ($V_{BULK}$) | +10V | +10V |
| Analog Input ($V_{IN}$) | +10V to -20V | +10V to -20V |
| Power Dissipation | 200 mW | 200 mW |
| Operating Temperature | -55°C to +125°C | -25°C to 70°C |
| Storage Temperature | -65°C to +150°C | -65°C to +150°C |

## electrical characteristics

STATIC CHARACTERISTICS (Note 1)

| PARAMETER | CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Analog Input Voltage | | | | ±10 | V |
| Threshold Voltage ($V_{GS(T)}$) | $V_{DG}$ = 0, $I_D$ = 1 μA | 1.0 | 2.2 | 3.0 | V |
| ON Resistance | $V_{IN}$ = -10V | | 150 | 600 | Ω |
| ON Resistance | $V_{IN}$ = $V_{SS}$ | | 75 | 200 | Ω |
| OFF Resistance | | | $10^{10}$ | | Ω |
| Gate Leakage Current ($I_{GSB}$) | $V_{GS}$ = -25V, $V_{BS}$ = 0, $T_A$ = 25°C | | 20 | | pA |
| Input (Drain) Leakage Current | | | | | |
| MM450, MM451, MM452, MM455 | $T_A$ = 25°C | | .025 | 100 | nA |
| | $T_A$ = 85°C | | .002 | 1.0 | μA |
| | $T_A$ = 125°C | | .025 | 1.0 | μA |
| Input (Drain) Leakage Current | | | | | |
| MM550, MM551, MM552, MM555 | $T_A$ = 25°C | | 0.1 | 100 | nA |
| | $T_A$ = 70°C | | .030 | 1.0 | μA |
| Output (Source) Leakage Current | | | | | |
| MM450, MM451, MM452, MM455 | $T_A$ = 25°C | | .040 | 100 | nA |
| Output (Source) Leakage Current | | | | | |
| MM450 | $T_A$ = 85°C | | | 1.0 | μA |
| MM451 | $T_A$ = 85°C | | | 1.0 | μA |
| MM452, MM455 | $T_A$ = 85°C | | | 1.0 | μA |
| MM450, MM451, MM452, MM455 | $T_A$ = 125°C | | | 1.0 | μA |
| Output (Source) Leakage Current | | | | | |
| MM550 | $T_A$ = 70°C | | | 1.0 | μA |
| MM551 | $T_A$ = 70°C | | | 1.0 | μA |
| MM552, MM555 | $T_A$ = 70°C | | | 1.0 | μA |
| DYNAMIC CHARACTERISTICS | | | | | |
| Large Signal Transconductance | $V_{DS}$ = -10V, $I_D$ = 10 mA f = 1 kHz | | 4000 | | μmhos |

CAPACITANCE CHARACTERISTICS (Note 2)

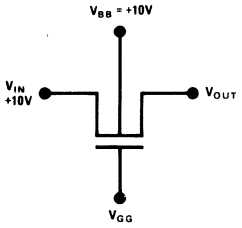
| PARAMETER | DEVICE TYPE | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Analog Input (Drain) Capacitance ($C_{DB}$) | ALL | | 8 | 10 | pF |
| Output (Source) Capacitance ($C_{SB}$) | MM450, MM550 | | 11 | 14 | pF |
| | MM451, MM551 | | 20 | 24 | pF |
| | MM452, MM552 | | 7.5 | 11 | pF |
| | MM455, MM555 | | 7.5 | 11 | pF |
| Gate Input Capacitance ($C_{GB}$) | MM450, MM550 | | 10 | 13 | pF |
| | MM451, MM551 | | 5.5 | 8 | pF |
| | MM452, MM552 | | 5.5 | 9 | pF |
| | MM455, MM555 | | 5.5 | 9 | pF |
| Gate to Output Capacitance ($C_{GS}$) | ALL | | 3.0 | 5 | pF |

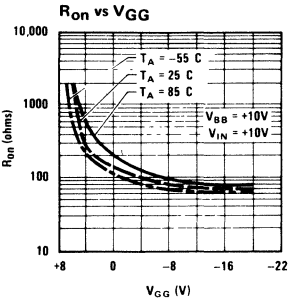
**Note 1:** The resistance specifications apply for -55°C $\leq T_A \leq$ + 85°C, $V_{GG}$ = -20V, $V_{BULK}$ = +10V, and a test current of 1 mA. Leakage current is measured with all pins held at ground except the pin being measured which is biased at -25V.

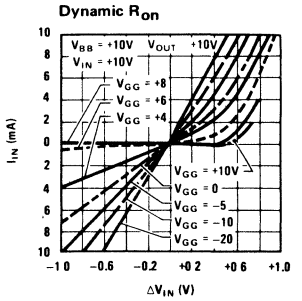
**Note 2:** All capacitance measurements are made at 0 volts bias at 1 MHz.

## typical dynamic input characteristics ($T_A$ = 25°C Unless Otherwise Noted)

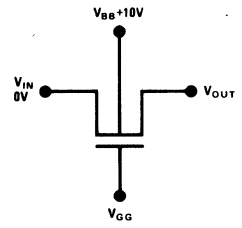
**CONDITION 1**
**ANALOG INPUT VOLTAGE**
**AT +10 VOLTS**

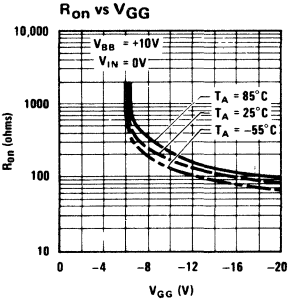


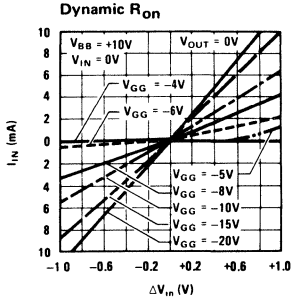



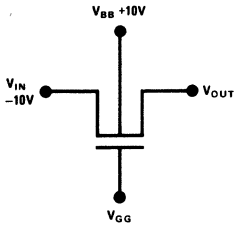

**CONDITION 2**
**ANALOG INPUT VOLTAGE**
**AT 0 VOLTS**

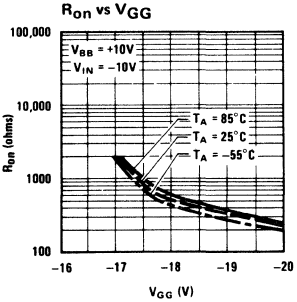


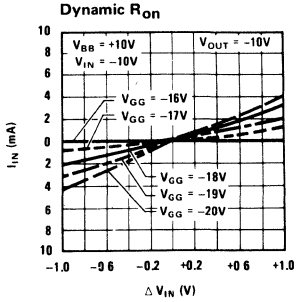



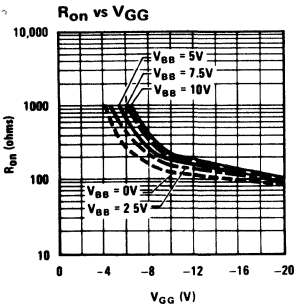



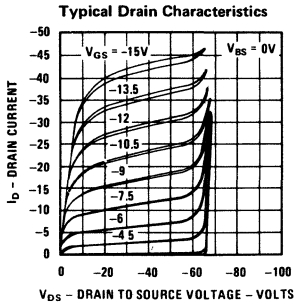

**CONDITION 3:**
**ANALOG INPUT VOLTAGE**
**AT −10 VOLTS**

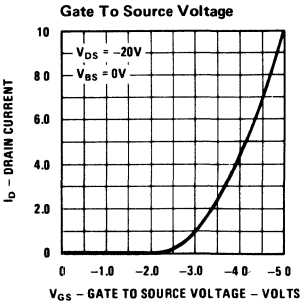
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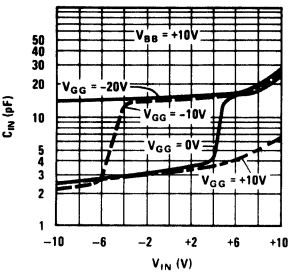
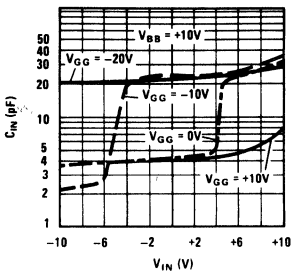
## typical input capacitance characteristics

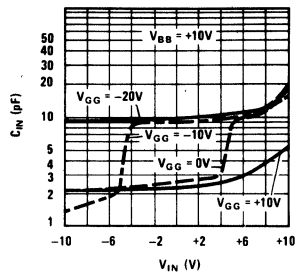
MM450, MM550
$C_{IN}$ vs $V_{IN}$



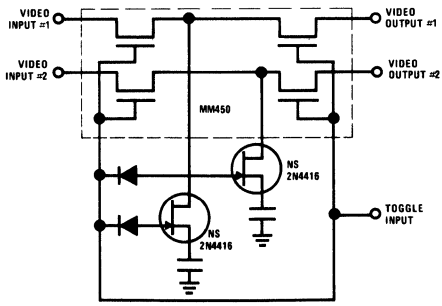

MM451, MM551
$C_{IN}$ vs $V_{IN}$



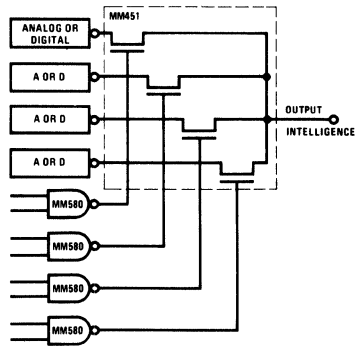

MM452, MM552, MM455, MM555
$C_{IN}$ vs $V_{IN}$




## typical applications (con't)




DPST High-Frequency Switch




4-Channel Multiplexer*

*Expansion in the number of data input lines is possible by using multiple level series switches allowing the same decode gates to be used for all lower rank decoding.