DVB-S2/ABS-S Digital Satellite Tuner

M88TS2022

Data Sheet

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Preface

This data sheet is the primary reference for the M88TS2022 Digital Satellite Tuner. It includes complete pin information, functional description, register description and electrical specifications for engineers who may evaluate or use the M88TS2022.

Terms and Abbreviations

Term	Definition	Term	Definition
ABS-S	Advanced Broadcasting System-Satellite	LPF	Lowpass Filter
AGC	Automatic Gain Control	PLL	Phase Lock Loop
DSP	Digital Signal Process	QPSK	Quadrature Phase Shift Keying
DVB-S	Digital Video Broadcasting over Satellite	RF	Radio Frequency
IF	Intermediate Frequency	8PSK	8 Phase Shift Keying
LNA	Low Noise Amplifier	16-QAM	16 Quadrature Amplitude Modulation
VCO	Voltage Control Oscillator	RMS	Root Mean Square

Conventions

Some conventions are used in this data sheet for easy and effective explanation.

- Number representation
  - A hexadecimal number is represented by XXH – for example, 10H;
  - A binary number with two or more bits is represented by XXXXB – for example, 1100B; A binary number with only one bit is represented by 0 or 1.
  - All other numbers should be considered as decimal numbers unless otherwise stated.
- Signal levels are represented by an uppercase HIGH or LOW.
- Cross-references are highlighted in blue for attention.

Revision History

Revision Number	Revision Date	Changes	
		Page Number	Description
0.0	9/1/2009	-	Initial release

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M88TS2022

Features

- Single-chip tuner
- Compliant with DVB-S2 and ABS-S standards
- Support QPSK, 8PSK and 16APSK
- Direct-conversion from L-band to baseband
- Symbol rate: 1 to 45 Msymbol/s
- Integrated VCOs and PLL, with on-chip inductors, varactors and loop filter
- Integrated baseband filters: 4 MHz to 40 MHz bandwidth
- Integrated RF AGC for optimal performance
- Integrated baseband DC offset cancellation (patent-pending) removes external loop filters
- Excellent immunity to strong adjacent undesired channels
- Integrated clock driver provides auxiliary divided clock output for other devices
- Selectable RF bypass
- Support sleep mode
- 2-wire serial bus with 3.3 V compatible logic levels
- Power supply: +3.3 V
- 28-pin QFN (Quad Flat No-lead) package
- RoHS compliant

Applications

- Digital satellite receiver front-end for DVB-S2 and ABS-S applications

General Description

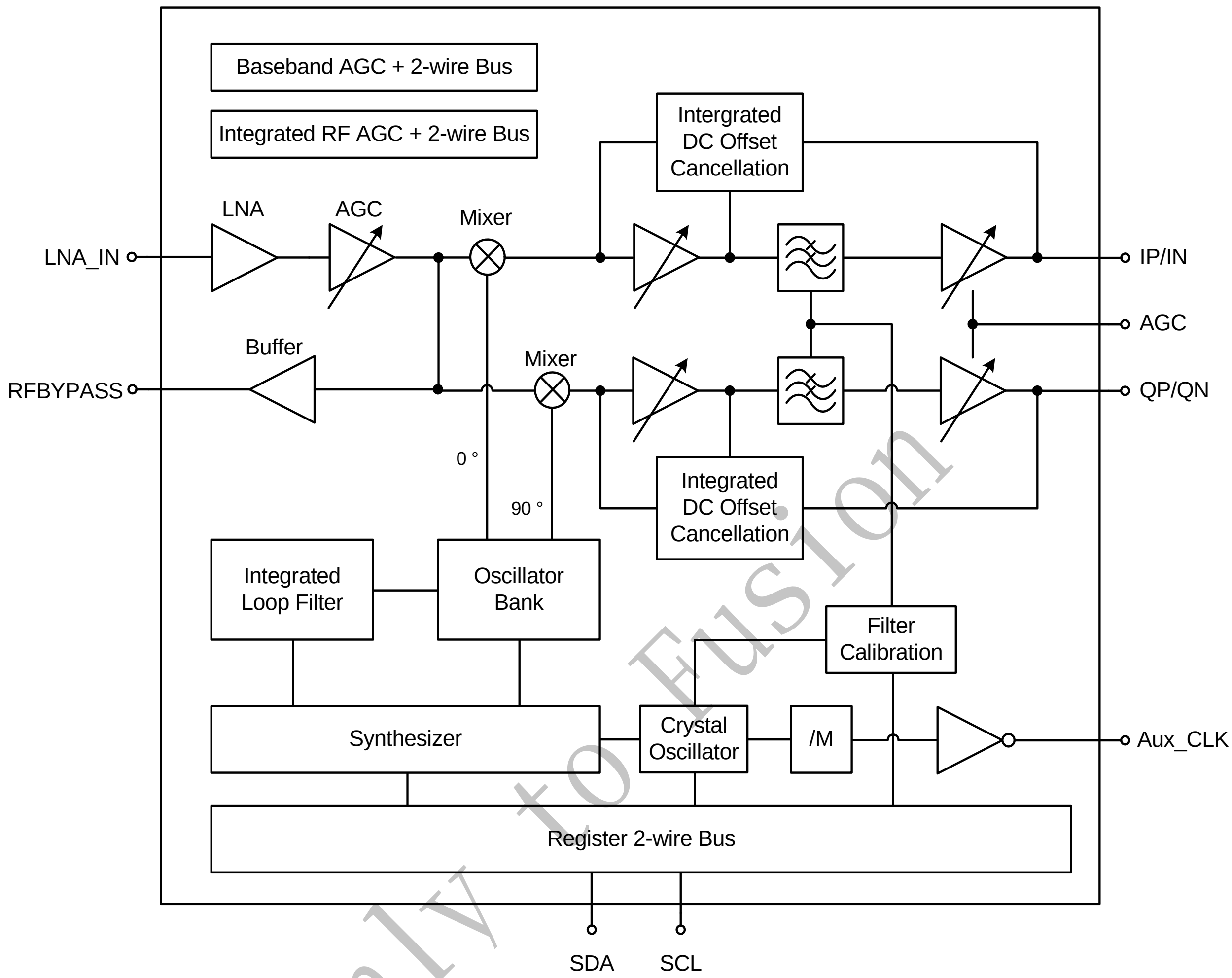
The M88TS2022 is a single-chip, direct-conversion tuner for digital satellite receiver applications. It offers the industry's most integrated solution to a satellite tuner function, simplifying the front-end designs. The device also provides an RF bypass output for driving a second tuner module.

This device incorporates the following functional blocks on a single chip: an LNA, quadrature down-converting mixers, a low phase noise and fast locking frequency synthesizer with on-chip loop filters, a DC offset cancellation loop with integrated loop filters, self-calibrated programmable baseband channel filters, an integrated RF AGC loop, and crystal oscillators with an integrated auxiliary clock output.

As a result of integrating all these blocks, the M88TS2022 has the least number of pins compared with other conventional solutions, and requires the least external components. In typical applications, the M88TS2022 requires only one crystal, one bypass capacitor, one matching network, and a few external resistors. The device also has the industry's smallest latency, as it uses a fast locking PLL and a fast settling DC offset cancellation architecture.

The M88TS2022 can be configured via a 2-wire serial bus. The chip is available in a 28-pin QFN package.

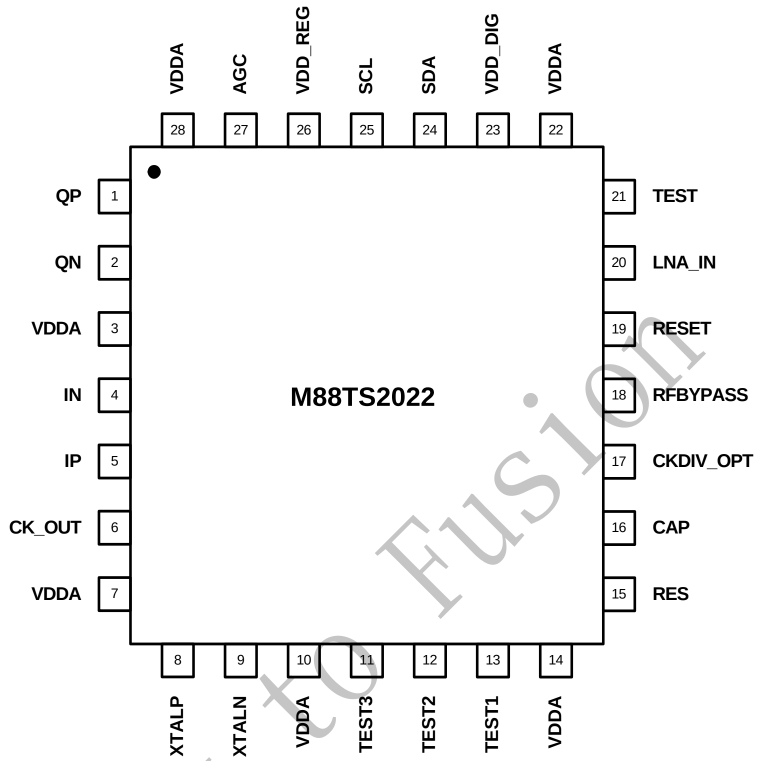
Block Diagram



1 Pin Information

1.1 Pin Assignment

Figure 1. 28-Pin QFN (Quad Flat No-lead) Package



Ground – The exposed pad at the bottom of the package.

1.2 Pin Description

Table 1. Pin Description (Sheet 1 of 3)

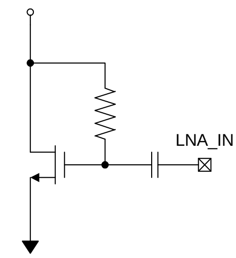
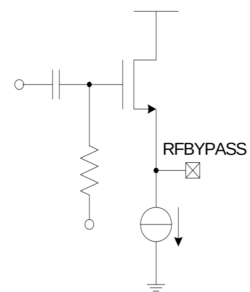
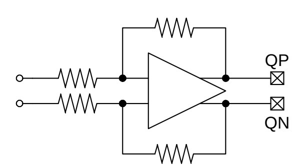
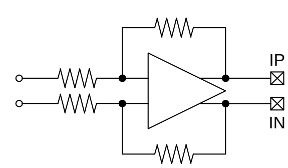
Pin Name	Pin No.	Type	Description	Schematic
RF Interface				
LNA_IN	20	In	**RF Input** The RF (Radio Frequency) signal of 950 MHz to 2150 MHz is fed to the Tuner's LNA (Low Noise Amplifier) input through an appropriate matching circuit.	
RFBYPASS	18	Out	**RF Bypass Output** This is the single-ended RF bypass output.	
CKDIV_OPT	17	Out	**Division Ratio of the Clock Driver** The connection of this pin determines the division ratio of the clock driver: NC: division ratio = 2 VDDA: division ratio = 6 VSS: division ratio = 1	
RES	15	In	**Bandgap Reference Resistor** This pin is to be connected to a 3.3 kΩ resistor.	
CAP	16	In	**Bypass Capacitor** This pin is to be connected to a 10 nF capacitor.	
Baseband Interface				
QP	1	Out	**Differential Quadrature Phase Outputs** QP: Quadrature phase positive output QN: Quadrature phase negative output	
QN	2	Out		
IP	5	Out	**Differential In-Phase Outputs** IP: In-phase positive output IN: In-phase negative output	
IN	4	Out		

Table 1. Pin Description (Sheet 2 of 3)

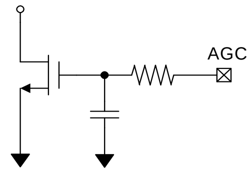
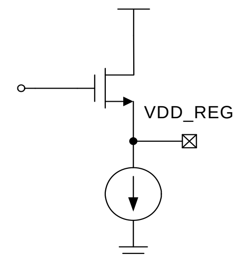
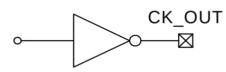
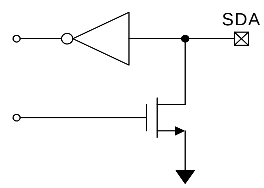
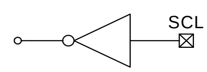
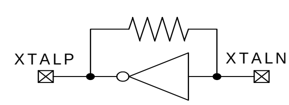
Pin Name	Pin No.	Type	Description	Schematic
AGC	27	In	**AGC (Automatic Gain Control) Voltage Input** This is the feedback voltage from the baseband demodulator chip to control the analog gain of the baseband signal.	
VDD_REG	26	Out	**Regulated Supply for the AGC Sigma-delta Output from Baseband**	
CK_OUT	6	Out	**Auxiliary Output Clock** This is an auxiliary clock for driving an external device (demodulator). This clock is obtained by dividing the crystal oscillator clock. Its frequency is programmable.	
2-wire Bus				
SDA	24	In/Out	**2-wire Bus Data** This is the serial data line for the 2-wire bus. This pin is open-drain and should be pulled up to +3.3 V.	
SCL	25	In	**2-wire Bus Clock** This is the serial clock line for the 2-wire bus. This pin is 3.3 V tolerant.	
Reset and Crystal Pins				
RESET	19	In	**Reset Input (Active HIGH)** This is an active HIGH reset signal that, when asserted, resets all function blocks and registers.	
XTALP	8	In	**Crystal Oscillator Positive Input** The crystal oscillator accepts any crystal with frequency in the range of 8 MHz to 40 MHz.	
XTALN	9	In	**Crystal Oscillator Negative Input** See above for details.	
Test Pins				
TEST	21	In	**Reserved for Testing.** Should be connected to ground.	

Table 1. Pin Description (Sheet 3 of 3)

Pin Name	Pin No.	Type	Description	Schematic
TEST1~3	13, 12, 11	Out	**Reserved for Testing.** Should be connected to ground.	
			Power Supply	
VDDA	3, 7, 10, 14, 22, 28	Power	**+ 3.3 V Analog Power Supply**	
VDD_DIG	23	Power	**+ 3.3 V Power Supply for the Digital 2-Wire Bus**	
VSS	-	Ground	**Ground.** (The exposed pad at the bottom of the package.)	

2 Function Description

The M88TS2022 is a feature-rich, highly-integrated and direct-conversion tuner for DVB-S2 and ABS-S applications. It integrates an LNA (Low Noise Amplifier), direct down-conversion mixers, baseband channel filters, frequency synthesizer, low noise PLL, DC offset cancellation blocks, and gain control stages. In addition, the device provides an RF bypass output for driving a second tuner module. The M88TS2022 requires the smallest pin count and the least external components.

The functionality of the tuner is programmable through a 2-wire bus.

2.1 Signal Path

The M88TS2022 accepts RF (Radio Frequency) signal at the LNA_IN pin, down-converts it to quadrature baseband signals, and outputs the baseband signals at pins QP/QN and IP/IN. This section describes the signal path in detail.

2.1.1 RF Input

The M88TS2022 supports RF signal in the range of 950 MHz to 2150 MHz. The RF signal is fed to the LNA input of the tuner through an appropriate matching network. The tuner is designed such that no tracking filter is required at the LNA input and the linearity performance is good enough to have low distortion even with all the channels present.

The RF signal is amplified by the LNA, and then is fed to a built-in RF AGC (Automatic Gain Control). The RF AGC automatically selects an optimal gain setting for each of the RF gain stages so that the best noise and linearity performances are obtained based on the operating conditions.

The integrated RF AGC ensures that the trade-off between the distortion and noise figure is done internally without the need of external filters or any feedback from the baseband chip. This feature also improves the performance of the system when there is a large cable tilt. This is because it avoids overloading the RF stages with large gain when relatively smaller high-powered signals are desired. Under such conditions, more gain is added at the baseband instead of the RF stages.

The RF AGC and the baseband AGC ensure an operating dynamic range of -92 dBm to -10 dBm. See Section 2.1.3.2, "Baseband AGC" for more details.

2.1.2 Quadrature Down-Conversion

The output of the RF AGC is fed to mixers, where the RF signal is mixed with quadrature local oscillator signals and is directly down-converted to quadrature baseband signals. The local oscillator signals are generated by an integrated voltage control oscillator (VCO). Details about the VCO are available in Section 2.2, "Frequency Synthesizer" on page 9.

2.1.3 Baseband

2.1.3.1 Baseband Lowpass Filter

The quadrature outputs from the mixers are fed to baseband variable gain amplifiers (VGAs) and the 7th order baseband lowpass filters (LPFs) for further processing.

Upon power-on, an RC time constant calibration is automatically performed to make the LPF operate with the correct bias conditions. Hence, the filter is insensitive to temperature and supply voltage variations.

The bandwidth of the LPF is programmable. Once appropriate parameters are set in Reg. 04H and 06H, the M88TS2022 automatically calibrates the LPF and makes its bandwidth to meet the programmed requirement.

2.1.3.1.1 Baseband Lowpass Filter Control Registers

The -3 dB bandwidth of the LPF is calculated using the following equation:

$$f_{3dB} = \frac{f_{xtal}}{M_{LPF}} \times N_{LPF} \times 2.766$$

To determine the two parameters M_{LPF} and N_{LPF}, we re-arrange the above equation to:

$$N_{LPF} = \frac{M_{LPF}}{f_{xtal}} \times \frac{f_{3dB}}{2.766}$$

And, we have the recommended -3 dB filter bandwidth (f_{3dB}) given by:

$$f_{3dB} = \frac{f_{sym}}{2} \times 1.35 + |f_{offset}|$$

So, we can get the following equation:

$$N_{LPF} = \frac{M_{LPF}}{f_{xtal}} \times \frac{\left(\frac{f_{sym}}{2} \times 1.35\right) + |f_{offset}|}{2.766}$$

where,

f_{xtal} is the crystal oscillator frequency in MHz;

f_{sym} is the symbol rate of the channel to be received (provided by the demodulator);

f_{offset} is the frequency offset of the channel (provided by the demodulator);

M_{LPF} is the decimal value of bits M_{LPF}[5:0] (Reg. 04H);

N_{LPF} is the decimal value of register bits N_{LPF}[4:0] (Reg. 06H).

In general, we select M_{LPF} such that

$$1.45\mu s < \frac{M_{LPF}}{f_{xtal}} < 1.70\mu s$$

Typically, $M_{LPF} \cong 1.57\mu s \times f_{xtal}$

Once M_{LPF} has been determined, we can calculate N_{LPF} using the equation mentioned above.

2.1.3.2 Baseband AGC

Following the baseband filters is a baseband AGC stage, which consists of a digital portion and an analog portion. The digital portion is controlled by the internal AGC loop while the analog portion takes the feedback from the baseband demodulator to ensure that the signal output to the demodulator is at optimal range. The baseband AGC together with the RF AGC provides an operating dynamic range of -92 dBm to -10 dBm.

2.1.3.3 DC Offset Cancellation

To avoid output saturation due to DC offsets, the M88TS2022 integrates a DC offset cancellation loop at the baseband. This patent-pending DC offset cancellation architecture makes use of DSP technologies to eliminate the external loop filters, and thus saving board area and cost. In addition, this architecture significantly reduces the settling time required for cancelling the DC offset, and hence reducing the latency of the tuner.

This architecture does not require any external capacitors and is able to settle upon frequency lock within 10 ms, thereby shortening the lock time during channel switching.

2.1.3.4 I/Q Outputs

The I/Q outputs of the M88TS2022 are differential, with high drive capability and extremely low distortion for the DVB-S2 operation.

2.1.4 RF Bypass

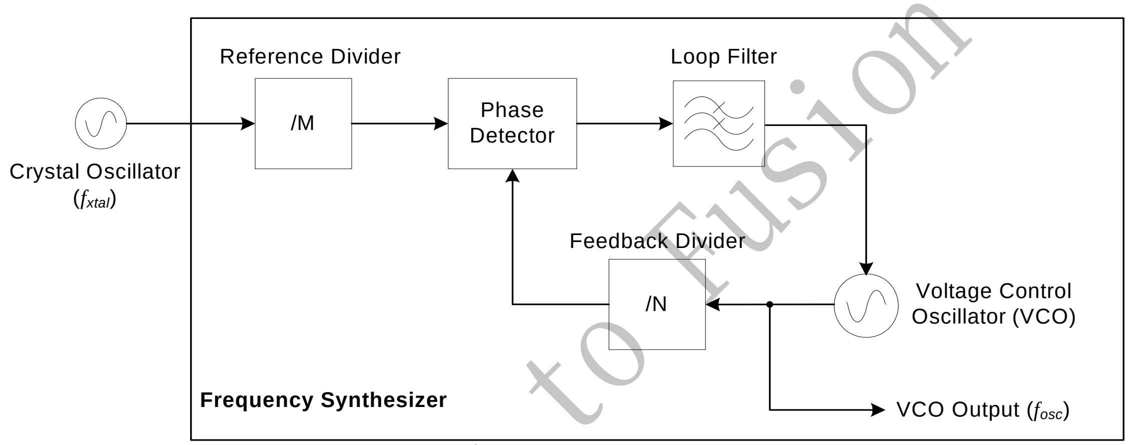
The M88TS2022 provides an RF bypass function to be used for driving a second tuner module. The RF bypass output is singled-ended. No matter the RF bypass is enabled or disabled, the electrical characteristics of the RF input are unchanged.

The RF bypass is enabled by default. When not used, it can be disabled by setting register bit RFBYPASS_EN (Reg. 62H).

2.2 Frequency Synthesizer

The M88TS2022 has a fully integrated PLL-based frequency synthesizer. The frequency synthesizer consists of multiple voltage control oscillators (VCOs), a loop filter, a phase detector, and two frequency dividers. See Figure 2. The synthesizer is designed to provide a low phase-noise clock signal in the range of 950 MHz to 2150 MHz over different temperature and power conditions.

Figure 2. Block Diagram of the Frequency Synthesizer



Inductors and varactors are integrated with the VCOs, making the output frequencies of the VCOs contiguous over the whole tuning range. The VCOs are controlled by an automatic tuning mechanism. The control logic automatically selects an appropriate VCO from the oscillator bank based on the frequency change required. The control logic tracks any changes in the operating conditions and retunes the VCO if necessary.

As shown in Figure 2, the VCO frequency (f_{osc}) is divided down by a programmable feedback divider. The crystal oscillator frequency (f_{xtal}) is divided down to the comparison frequency by a programmable reference divider. The phase detector compares the output of feedback divider with the comparison frequency in both phase and frequency domain, and controls the VCO accordingly. In this way, it is possible for the synthesizer to synthesis a whole range of output frequencies. The division ratios of the dividers are programmed via registers (Reg. 01H ~ 03H). See Section 2.2.1, "Frequency Synthesizer Control Registers" for details.

The frequency synthesizer contains all the required circuitry on the chip with only an external crystal required. The integration of inductors, varactors and loop filters in the M88TS2022 dramatically reduces the number of external components and the pin count, thus allowing the user to reduce the cost of the overall solution.

The output of the frequency synthesizer is converted to quadrature signals (0° and 90°); the quadrature signals are then fed to the mixers as local oscillator signals for direct down-conversion of the RF signal.

2.2.1 Frequency Synthesizer Control Registers

The output frequency of the synthesizer (f_{osc}) is determined by the following equation:

$$f_{OSC} = \frac{(1024 + N_{DIV})f_{xtal}}{(8 + M_{DIV})L_{DIV}}$$

Where,

f_{xtal} is the crystal oscillator frequency in MHz;

N_{DIV} is the decimal value set in bits N_{DIV}[13:0] (Reg. 01H, 02H);

M_{DIV} is the decimal value set in bits M_{DIV}[4:0] (Reg. 03H);

L_{DIV} is a division factor selected by bits DIV8_EN (Reg. 62H) and DIV4_EN (Reg. 10H).

The setting of these registers are based on the following calculations:

$$M_{DIV} = round\left[\frac{f_{xtal}}{2MHz}\right] - 8$$

If $f_{OSC} < \frac{1024 \times f_{xtal}}{4 \times (8 + M_{DIV})}$, L_{DIV} = 8; if $\frac{1024 \times f_{xtal}}{4 \times (8 + M_{DIV})} < f_{OSC} < \frac{1024 \times f_{xtal}}{2 \times (8 + M_{DIV})}$, L_{DIV} = 4; otherwise, L_{DIV} = 2.

$$N_{DIV} = \frac{f_{OSC} \times L_{DIV} \times (8 + M_{DIV})}{f_{xtal}} - 1024$$

The lock status of the synthesizer is indicated in bit PLL_LOCK (Reg. 15H).

2.3 Crystal Oscillator and Auxiliary Clock Output

The crystal oscillator accepts any crystal with frequency in the range of 8 MHz to 40 MHz.

In order to reduce the number of external components, a clock driver is integrated on-chip to provide an auxiliary clock output at the CK_OUT pin. This clock derives from dividing the crystal oscillator clock.

Upon power-up, the frequency of the clock output (f_{CKOUT}) is determined by pin CLKDIV_OPT as follows.

- CLKDIV_OPT = NC: $f_{CKOUT} = f_{xtal} / 2$
- CLKDIV_OPT = VDDA: $f_{CKOUT} = f_{xtal} / 6$
- CLKDIV_OPT = VSS: $f_{CKOUT} = f_{xtal}$

Where, f_{xtal} is the frequency of the crystal oscillator.

In normal operation, the frequency of the clock (f_{CKOUT}) can also be programmable through the 2-wire bus.

$$f_{CKOUT} = f_{xtal} / D_{CKOUT}$$

Where, D_{CKOUT} is the decimal value set in bits D_{CKOUT}[3:0] (Reg. 05H).

The auxiliary clock output is enabled by default. When not used, it can be disabled by setting register bit CK_OUT_EN (Reg. 42H) to 0.

2.4 Sleep Mode

The M88TS2022 supports sleep mode to save the power consumption. The baseband, PLL and mixers can be put into sleep mode by setting the SLEEPB bit in Reg.00H to 0. Also, all analog circuits except the crystal, bandgap and master regulator can be put into sleep mode by setting the SLEEPB_SYS bit in Reg.00H to 0.

3 Programming Description

3.1 2-Wire Bus

The M88TS2022 is programmed via a 2-wire serial bus (pins SDA and SCL). The device functions as a slave receiver and is capable of operating at rates up to 400 kb/s. It is recognized by a unique 7-bit address of 1100000B.

Figure 3 and Figure 4 show the read and write operations of the 2-wire bus.

Figure 3. 2-Wire Bus Read Operation

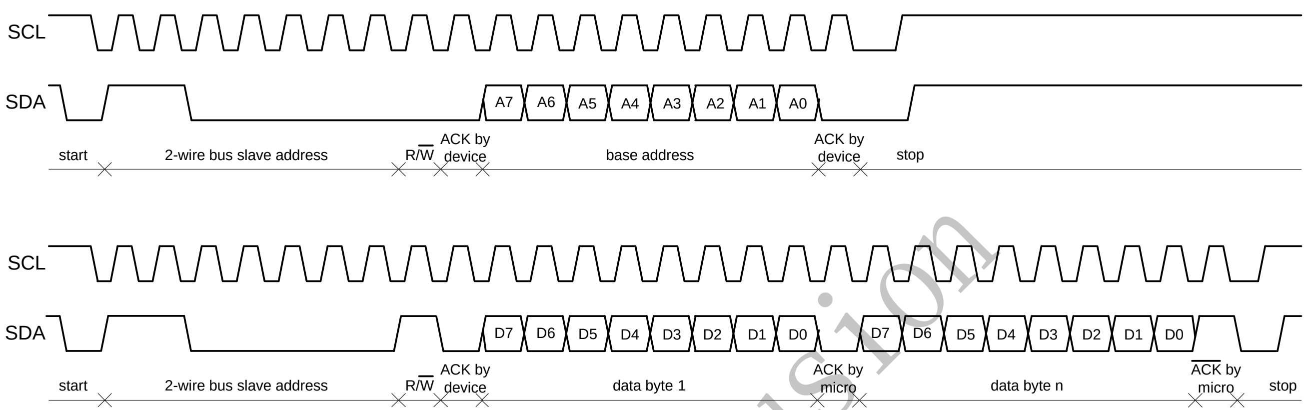
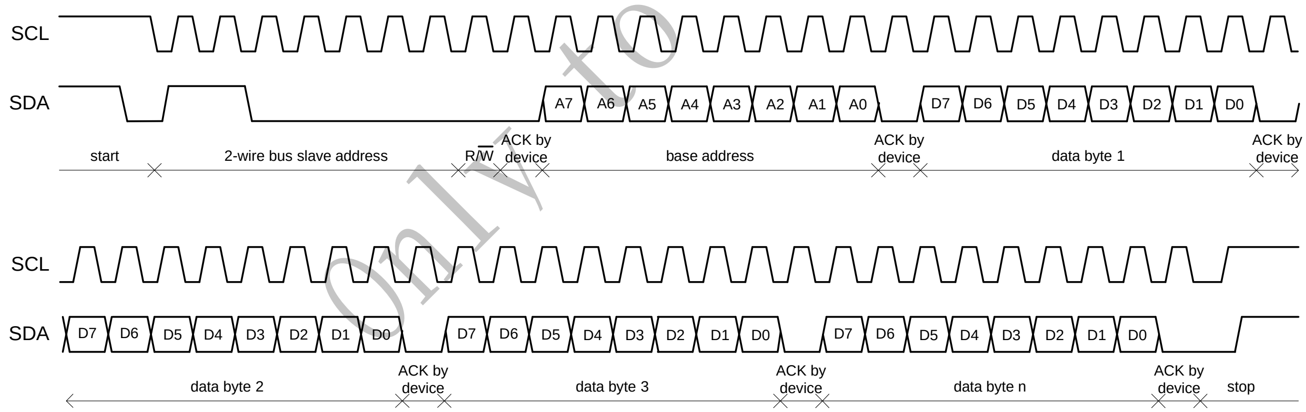


Figure 4. 2-Wire Bus Write Operation



3.2 Register Map

Table 2 shows the register map. The register bits indicated with “R/W” in the Type column can be read or written, and those indicated with “R” are read only. All registers are set to their default values upon power-on reset.

Table 2. Register Map

<table>
<tr><th rowspan="2">Addr.</th><th colspan="8">Bit Name</th><th rowspan="2">Type</th><th rowspan="2">Default</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>00H</td><td colspan="2">VERSION[1:0]</td><td colspan="4">Reserved</td><td>SLEEPB</td><td>SLEEPB_SYS</td><td>R/W</td><td>41H</td></tr>
<tr><td>01H</td><td colspan="2">Reserved</td><td colspan="6">N_{DIV}[13:8]</td><td>R/W</td><td>00H</td></tr>
<tr><td>02H</td><td colspan="8">N_{DIV}[7:0]</td><td>R/W</td><td>00H</td></tr>
<tr><td>03H</td><td colspan="3">Reserved</td><td colspan="5">M_{DIV}[4:0]</td><td>R/W</td><td>00H</td></tr>
<tr><td>04H</td><td colspan="2">Reserved</td><td colspan="6">M_{LPF}[5:0]</td><td>R/W</td><td>05H</td></tr>
<tr><td>05H</td><td colspan="3">Reserved</td><td>EN_CKDIV_OPT</td><td colspan="4">D_{CKOUT}[3:0]</td><td>R/W</td><td>10H</td></tr>
<tr><td>06H</td><td colspan="3">Reserved</td><td colspan="5">N_{LPF}[4:0]</td><td>R/W</td><td>08H</td></tr>
<tr><td>07H</td><td colspan="2">Reserved</td><td colspan="3">DRV_GAIN_MAX[2:0]</td><td colspan="3">LPF_POST_GAIN[2:0]</td><td>R/W</td><td>34H</td></tr>
<tr><td>10H</td><td colspan="3">Reserved</td><td>DIV4_EN</td><td colspan="4">Reserved</td><td>R/W</td><td>00H</td></tr>
<tr><td>15H</td><td>Reserved</td><td>PLL_LOCK</td><td colspan="6">Reserved</td><td>R</td><td>00H</td></tr>
<tr><td>21H</td><td colspan="3">Reserved</td><td colspan="5">BB_GAIN[4:0]</td><td>R</td><td>00H</td></tr>
<tr><td>3DH</td><td colspan="3">Reserved</td><td colspan="5">RF_GAIN[4:0]</td><td>R</td><td>00H</td></tr>
<tr><td>42H</td><td colspan="3">Reserved</td><td>CLK_OUT_EN</td><td colspan="4">Reserved</td><td>R/W</td><td>7CH</td></tr>
<tr><td>62H</td><td>RFBYPASS_EN</td><td colspan="5">Reserved</td><td>DIV8_EN</td><td>Reserved</td><td>R/W</td><td>E4H</td></tr>
</table>

3.3 Register Description

Table 3. Register 00H: Version Number and Sleep Mode Enable

Address: 00H Default: 41H			
Bit	**Name**	**Type**	**Description**
7:6	VERSION[1:0]	R	Version number of the chip (read only).
5:2	-	-	Reserved.
1	SLEEPB	R/W	Baseband sleep mode enable (LOW active). When this bit is 0, the baseband, PLL and mixers are put into sleep mode to save power.
0	SLEEPB_SYS	R/W	Analog sleep mode enable (LOW active). When this bit is 0, the analog part except the crystal, the bandgap and the master regulator are put into sleep mode to save power.

Table 4. Register 01H: Division Ratio of the Feedback Divider (MSB)

Address: 01H Default: 00H			
Bit	**Name**	**Type**	**Description**
7:6	-	-	Reserved.
5:0	N_{DIV}[13:8]	R/W	MSB bits of the division ratio of the feedback divider. Bits N_{DIV}[13:8], combined with bits N_{DIV}[7:0], determine the division ratio of the feedback divider.

Table 5. Register 02H: Division Ratio of the Feedback Divider (LSB)

Address: 02H Default: 00H			
Bit	**Name**	**Type**	**Description**
7:0	N_{DIV}[7:0]	R/W	LSB bits of the division ratio of the feedback divider. Bits N_{DIV}[7:0], combined with bits N_{DIV}[13:8], determine the division ratio of the feedback divider.

Table 6. Register 03H: Division Ratio of the Reference Divider

Address: 03H Default: 00H			
Bit	**Name**	**Type**	**Description**
7:5	-	-	Reserved.
4:0	M_{DIV}[4:0]	R/W	Division ratio of the reference divider. This bit field determines the division ratio of the reference divider.

Table 7. Register 04H: Lowpass Filter Calibration Period

Address: 04H **Default: 05H**			
Bit	**Name**	**Type**	**Description**
7:6	-	-	Reserved.
5:0	M_{LPF}[5:0]	R/W	Period of the internal lowpass filter calibration state machine.

Table 8. Register 05H: Division Ratio of the Output Clock Driver

Address: 05H **Default: 10H**			
Bit	**Name**	**Type**	**Description**
7:5	-	-	Reserved.
4	EN_CKDIV_OPT	R/W	Enable to change the division ratio of the clock driver by bonding option (HIGH active). When this bit is '1', the division ratio of the clock driver is decided by pin CKDIV_OPT as follows: Pin CKDIV_OPT is left open: division ratio = 2; Pin CKDIV_OPT is connected to VDDA: division ratio = 6; Pin CKDIV_OPT is connected to VSS: division ratio = 1.
3:0	D_{CKOUT}[3:0]	R/W	Division ratio of the clock driver. This bit field sets the division ratio for the clock output to the baseband chip.

Table 9. Register 06H: Baseband Lowpass Filter Bandwidth

Address: 06H **Default: 08H**			
Bit	**Name**	**Type**	**Description**
7:5	-	-	Reserved.
4:0	N_{LPF}[4:0]	R/W	Baseband lowpass filter bandwidth. This bit field sets the bandwidth of the lowpass filter.

Table 10. Register 07H: Maximum Driver Gain and Post-filter Gain

Address: 07H **Default: 34H**			
Bit	**Name**	**Type**	**Description**
7:6	-	-	Reserved.
5:3	DRV_GAIN_MAX[2:0]	R/W	Maximum driver gain code specified in software.
2:0	LPF_POST_GAIN[2:0]	R/W	Post-filter Gain. This field sets the gain after the LPF filter.

Table 11. Register 10H: Division Ratio Selection Bit DIV4_EN

<table>
<tr><td colspan="4">Address: 10H
Default: 00H</td></tr>
<tr><th>Bit</th><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>7:5</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>4</td><td>DIV4_EN</td><td>R/W</td><td>Division ratio selection.
This bit together with bit DIV8_EN (Reg. 62H) selects the division ratio L_{DIV} for controlling the output frequency of the synthesizer.
<table>
<tr><td>DIV8_EN (Reg. 62H)</td><td>DIV4_EN</td><td>Division Ratio (L_{DIV})</td></tr>
<tr><td>0</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>Undefined</td></tr>
<tr><td>1</td><td>1</td><td>8</td></tr>
</table></td></tr>
<tr><td>3:0</td><td>-</td><td>-</td><td>Reserved</td></tr>
</table>

Table 12. Register 15H: PLL Lock Indication

Address: 15H **Default: 00H**			
Bit	**Name**	**Type**	**Description**
7	-	-	Reserved.
6	PLL_LOCK	R	PLL lock indication (end flag of the PLL calibration). 0: The PLL is unlocked; 1: The PLL is locked.
5:0	-	-	Reserved

Table 13. Register 21H: Baseband Gain Calibration Result

Address: 21H **Default: 00H**			
Bit	**Name**	**Type**	**Description**
7:5	-	-	Reserved
4:0	BB_GAIN[4:0]	R	Result of the baseband gain calibration.

Table 14. Register 3DH: RF Gain Calibration Result

Address: 3DH Default: 00H			
Bit	**Name**	**Type**	**Description**
7:5	-	-	Reserved
4:0	RF_GAIN[4:0]	R	Result of internal RF gain calibration.

Table 15. Register 42H: Clock Output Enable

Address: 42H Default: 7CH			
Bit	**Name**	**Type**	**Description**
7:5	-	-	Reserved
4	CK_OUT_EN	R/W	Clock output enable. 0: Disable the clock output to the baseband chip. 1: Enable the clock output to the baseband chip.
3:0	-	-	Reserved

Table 16. Register 62H: RF Bypass Enable and Division Select Bit DIV8_EN

<table>
<tr><td colspan="4">Address: 62H
Default: E4H</td></tr>
<tr><th>Bit</th><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>7</td><td>RFBYPASS_EN</td><td>R/W</td><td>RF bypass (LNA loop-through) enable.
0: Disabled. RF bypass is shut down.
1: Enabled. RF bypass works normally.
This bit is set to 1 by default. If the RF bypass output is not used, this bit can be set to 0 to save power.</td></tr>
<tr><td>6:2</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>1</td><td>DIV8_EN</td><td>R/W</td><td>Division ratio selection.
This bit together with bit DIV4_EN (Reg. 10H) selects the division ratio L_{DIV} for controlling the output frequency of the synthesizer.
<table>
<tr><td>DIV8_EN</td><td>DIV4_EN (Reg. 10H)</td><td>Division Ratio (L_{DIV})</td></tr>
<tr><td>0</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>Undefined</td></tr>
<tr><td>1</td><td>1</td><td>8</td></tr>
</table></td></tr>
<tr><td>0</td><td>-</td><td>-</td><td>Reserved</td></tr>
</table>

4 Electrical Characteristics

The following conditions apply to all figures in this chapter, unless otherwise stated.

Ambient temperature = 0°C to 70°C

VSS = 0 V

All power supply = 3.3 V (±10%)

4.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit	Notes
VDDA	Analog power supply	-0.6	5	V	
VDD_DIG	Digital power supply	-0.6	5	V	
$V_{2\text{-wire}}$	Voltage on 2-wire bus pins	-0.6	5	V	
V_{IN}	Voltage on other input pins	-0.6	2.5	V	
V_{OUT}	Output voltage	-0.6	VDDA + 0.5	V	
T_{STG}	Storage temperature	-55	150	°C	
T_{OP}	Operating ambient temperature	0	70	°C	
Note: Stresses above the Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended period may affect device reliability.					

4.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VDDA, VDD_DIG	Analog power supply	3.0	3.3	3.6	V	With respect to VSS
T_{OP}	Operating ambient temperature	0		70	°C	
Note: Device functionality is not guaranteed at any conditions beyond the recommended operating conditions.						

4.3 DC Electrical Characteristics

Parameter	Min.	Typ.	Max.	Unit	Conditions
Supply (All Power Supply Pins)					
Supply Voltage	3.0	3.3	3.6	V	
Supply Current	140	150	160	mA	Normal Mode
Baseband Outputs (QP/QN, IP/IN Pins)					
Nominal Output Voltage Swing		1		V_{PP}	R_{LOAD} = 10 pF
Output Clipping Voltage		2		V_{PP}	
Common Mode Voltage	1.20	1.25	1.35	V	
DC Offset Voltage	-10	0	10	mV	
Analog Regulator Outputs (VDD_REG Pin)					
Output Voltage	2.55	2.70	2.85	V	
Source Current			3	mA	
2-Wire Bus (SDA and SCL Pins)					
Input Logic Level LOW			1.0	V	
Input Logic Level HIGH	2.0			V	
Input Hysteresis		0.2		V	
Input Current	-10		10	µA	
Output Logic Level LOW		0.6		V	

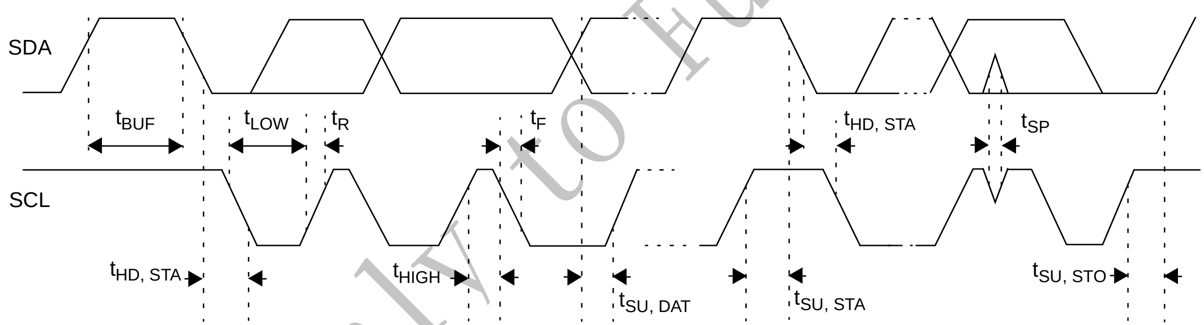
4.4 AC Electrical Characteristics

Parameter	Min.	Typ.	Max.	Unit	Conditions
RF Front End					
Input Carrier	950		2150	MHz	
Input Noise Figure		3.0		dB	RF Gain = Maximum
RF Input Return Loss			-10	dB	
In-band LO Leakage			-90	dBm	
Baseband Outputs					
Baseband Highpass -3 dB Point		850		Hz	
Baseband Lowpass Filter Bandwidth Range	4		33	MHz	Baseband -3 dB Cutoff Frequency
Synthesizer					
Phase Detector Comparison Frequency	1.5	2	2.5	MHz	
Crystal Frequency	8	27	40	MHz	

4.5 2-Wire Bus Timing Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{SCL}	SCL clock frequency			400	kHz
t_{BUF}	Bus free time between a stop and start condition	5.0			µs
$t_{HD, STA}$	Hold time (repeated) start condition. After this period, the first clock pulse is generated.	1.0			µs
t_{LOW}	Low period of the SCL clock	1.0			µs
t_{HIGH}	High period of the SCL clock	1.0			µs
t_R	Rise time for SDA and SCL signals			200	ns
t_F	Fall time for SDA and SCL signals			200	ns
$t_{SU, STA}$	Setup time for a repeated start condition	1.0			µs
$t_{SU, STO}$	Setup time for stop condition	1.0			µs
$t_{SU, DAT}$	Data setup time	200			ns
t_{SP}	Pulse width of spikes to be suppressed by input filter	0		50	ns

Figure 5. 2-Wire Bus Timing Diagram



5 Typical Performance Data

Figure 6. RF Gain with respect to Gain Setting

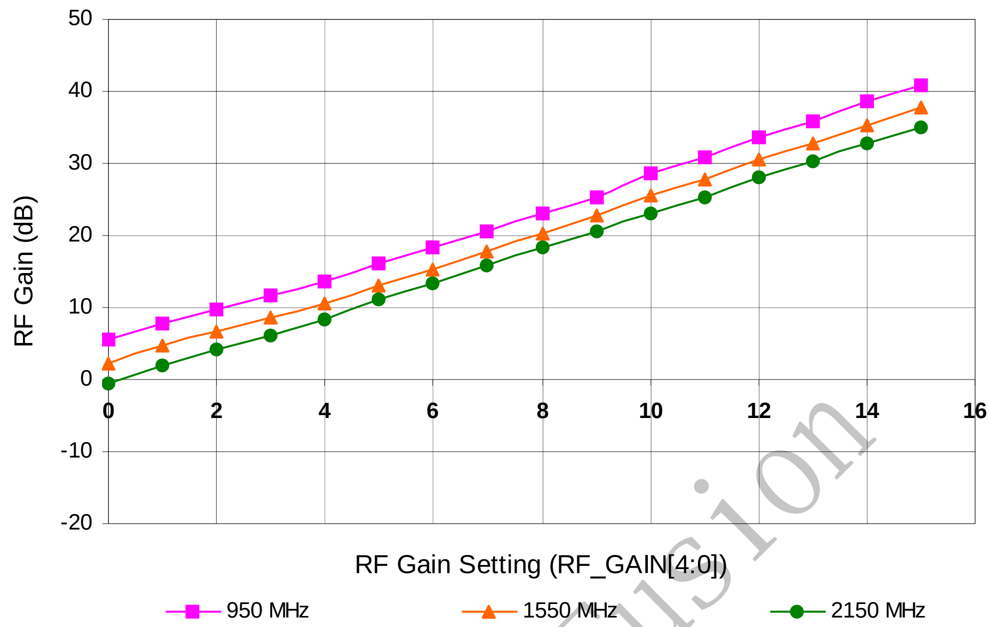


Figure 7. Baseband Gain with Respect to Gain Setting & Control Voltage

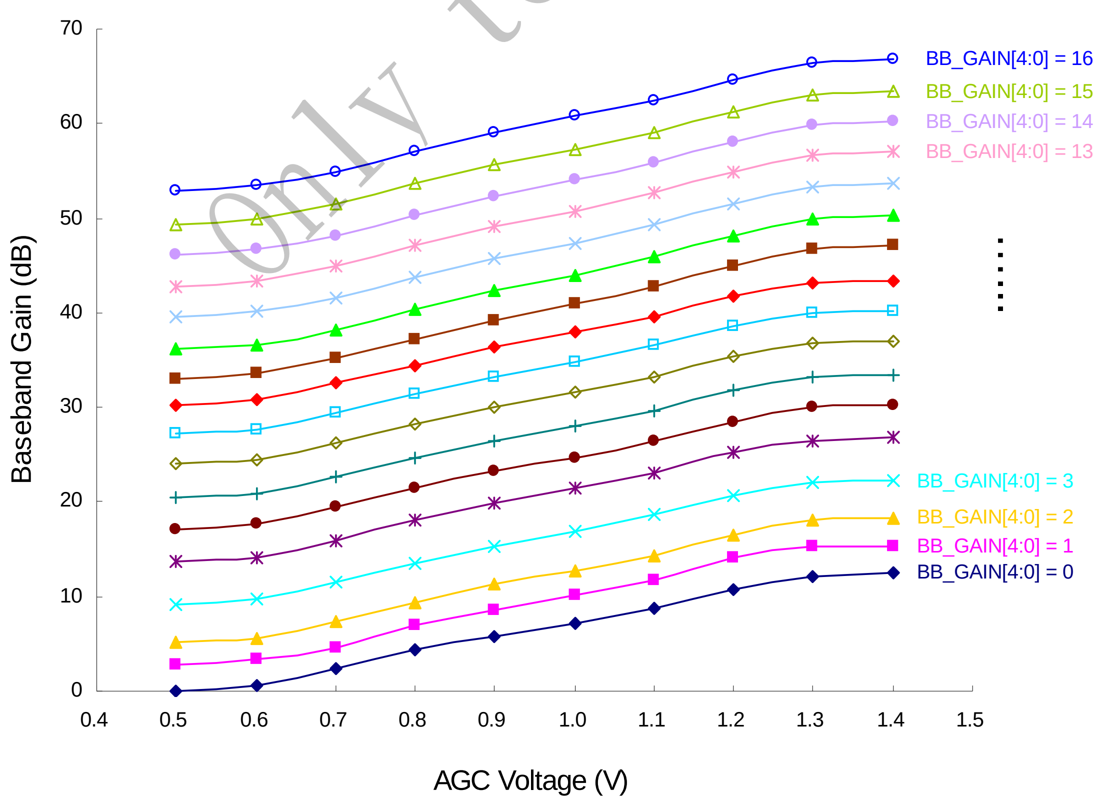
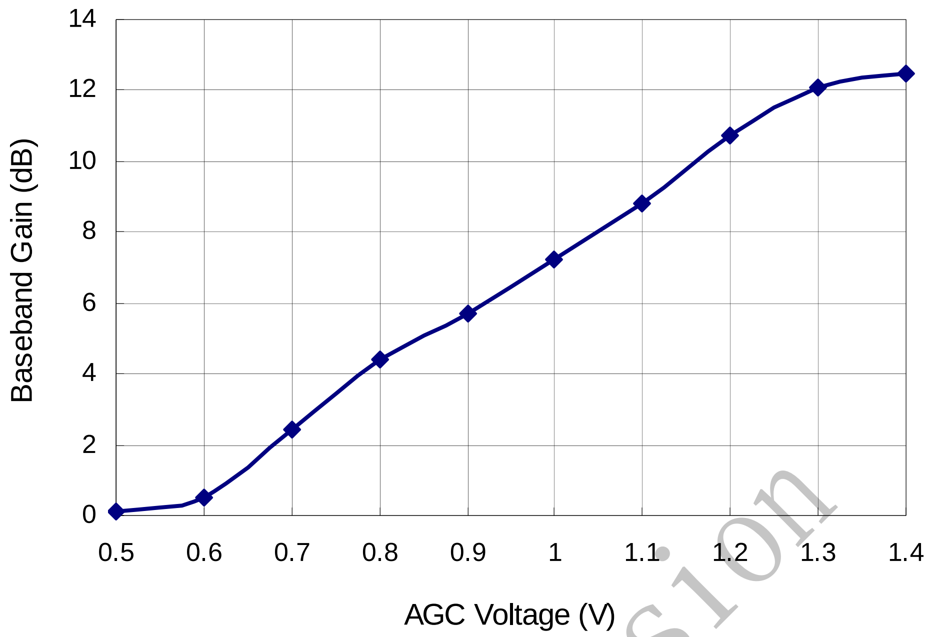
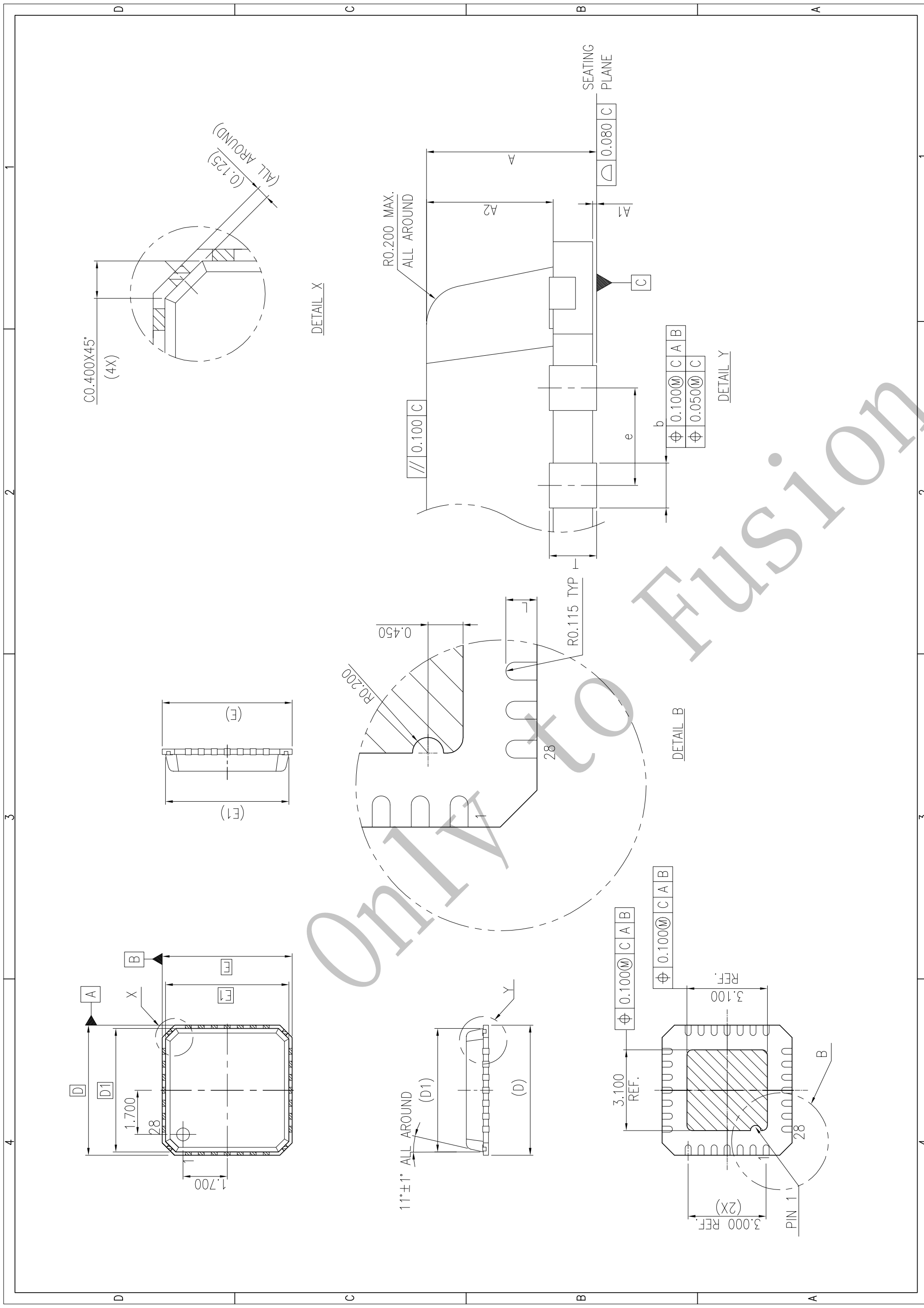


Figure 8. Baseband Gain for a Single Gain Setting (Slope of Graph = 16.6 dB/V)



6 Mechanical Package Data

Figure 9. Package Outline



DIMENSION LIST (FOOTPRINT: 1.10)

S/N	SYM	DIMENSIONS	REMARKS
1	A	0.850±0.050	OVERALL HEIGHT
2	A1	0.025±0.020	STANDOFF
3	A2	0.650±0.050	CAVITY THICKNESS
4	D	5.000±0.100	PKG. LENGTH
5	D1	4.750±0.100	CAVITY LENGTH
6	E	5.000±0.100	PKG. WIDTH
7	E1	4.750±0.100	CAVITY WIDTH
8	L	0.550±0.100	FOOT LENGTH
9	T	0.190~0.245	FRAME THICKNESS
10	b	$0.230^{+0.070}_{-0.050}$	LEAD WIDTH
11	e	0.500 BASE	LEAD PITCH

NOTES :

S/N	DESCRIPTION		SPEC.
1	GENERAL TOLERANCE.	DISTANCE	±0.100
		ANGLE	±2.5°
2	MATTE FINISH ON PACKAGE BODY SURFACE EXCEPT EJECTION AND PIN 1 MARKING.		Ra 0.3~1.2 um
3	FRAME BASE METAL THICKNESS		0.203 BASE
4	ALL MOLDED BODY SHARP CORNER RADII UNLESS OTHERWISE SPECIFIED.		MAX. R0.200
5	DRAWING DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OR CUTTING BURR.		
6	COMPLIANT TO JEDEC STANDARD: MO-220		