Leiditech

Thyristor Surge Suppressors

P0060~P3500LA_B_C Series

Description

The L Series are designed to protect baseband equipment such as modems, line cards, CPE and DSL from damaging overvoltage transients.
The series provides a cost-effective through-hole solution that enables equipment to comply with global regulatory standards.

Features and Benefits

- Low voltagr overeshoot
- Low on-state voltage
- Does not degrade with use
- Fails short circuit when surged in excess of ratings
- Low Capacitance

Applicable Global Standards

- TIA-968-A
- ITU K.20/21 Enhanced level*
- ITU K.20/21 Basic Level
- GR 1089 Inter building*
- GR 1089 Inter building
- IEC 6100-4-5
- YD/T 1082
- YD/T 993
- YD/T 950

Electrical Characteristics

Part Number	V_{DRM}@ I_{DRM}=5μA	V_S@ 100V/μS	V_T@ I_T=2.2Amps	I_S	I_T	I_H	Capacitance @1MHz, 2V bias	
	V min	V max	V max	mA max	A max	mA min	pF min	pF max
P0060LA	6	15	4	800	2.2	50	25	50
P0080LA	6	25	4	800	2.2	50	25	50
P0300LA	25	40	4	800	2.2	50	55	70
P0640LA	58	77	4	800	2.2	150	40	60
P0720LA	65	88	4	800	2.2	150	35	55
P0900LA	75	98	4	800	2.2	150	35	55
P1100LA	90	130	4	800	2.2	150	30	60
P1300LA	120	160	4	800	2.2	150	25	40
P1500LA	140	180	4	800	2.2	150	25	40
P1800LA	170	220	4	800	2.2	150	25	30
P2300LA	190	260	4	800	2.2	150	25	30
P2600LA	220	300	4	800	2.2	150	25	30
P3100LA	275	350	4	800	2.2	150	20	30
P3500LA	320	400	4	800	2.2	150	20	30

Electrical Characteristics

Part Number	V_{DRM}@ I_{DRM}=5μA	V_S@ 100V/μS	V_T@ I_T=2.2Amps	I_S	I_T	I_H	Capacitance @1MHz, 2V bias	
	V min	V max	V max	mA max	A max	mA min	pF min	pF max
P0060LB	6	15	4	800	2.2	50	40	85
P0080LB	6	25	4	800	2.2	50	40	85
P0300LB	25	40	4	800	2.2	50	40	85
P0640LB	58	77	4	800	2.2	150	40	60
P0720LB	65	88	4	800	2.2	150	35	60
P0900LB	75	98	4	800	2.2	150	35	60
P1100LB	90	130	4	800	2.2	150	30	60
P1300LB	120	160	4	800	2.2	150	25	40
P1500LB	140	180	4	800	2.2	150	25	40
P1800LB	170	220	4	800	2.2	150	25	40
P2300LB	190	260	4	800	2.2	150	25	30
P2600LB	220	300	4	800	2.2	150	20	30
P3100LB	275	350	4	800	2.2	150	20	30
P3500LB	320	400	4	800	2.2	150	20	30
P0060LC	6	15	4	800	2.2	50	60	260
P0080LC	6	25	4	800	2.2	50	60	260
P0300LC	25	40	4	800	2.2	50	60	250
P0640LC	58	77	4	800	2.2	150	55	155
P0720LC	65	88	4	800	2.2	150	50	150
P0900LC	75	98	4	800	2.2	150	45	140
P1100LC	90	130	4	800	2.2	150	45	115
P1300LC	120	160	4	800	2.2	150	40	105
P1500LC	140	180	4	800	2.2	150	35	95
P1800LC	170	220	4	800	2.2	150	35	90
P2300LC	190	260	4	800	2.2	150	30	80
P2600LC	220	300	4	800	2.2	150	30	80
P3100LC	275	350	4	800	2.2	150	30	70
P3500LC	320	400	4	800	2.2	150	25	65

Notes:
- Absolute maximum ratings measured at TA= 25ºC (unless otherwise noted).
- Devices are bi-directional (unless otherwise noted)

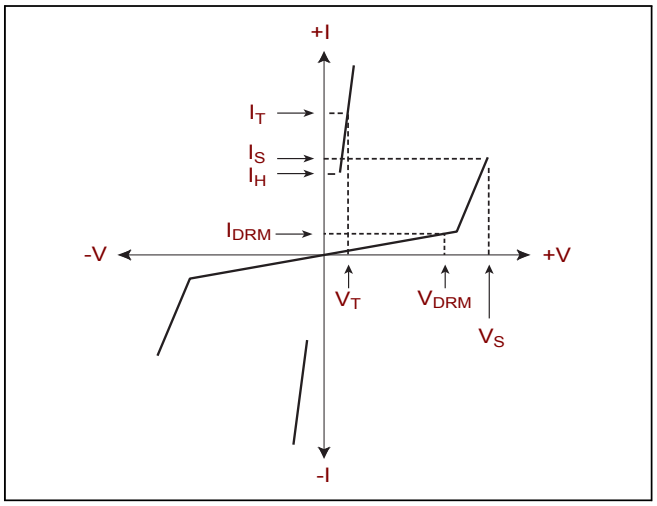
Surge Ratings

Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2x310 [1] 0.5x700 [2]	2x10 [1] 2x10 [2]	8x20 [1] 1.2x50 [2]	10x160 [1] 10x160 [2]	10x560 [1] 10x560 [2]	5x320 [1] 9x720 [2]	10x360 [1] 10x360 [2]	10x1000 [1] 10x1000 [2]	5x310 [1] 10x700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/μs max
A	20	150	150	90	50	75	75	45	75	20	500
B	25	250	250	150	100	100	125	80	100	25	500
C	50	500	400	200	150	200	175	100	200	30	500

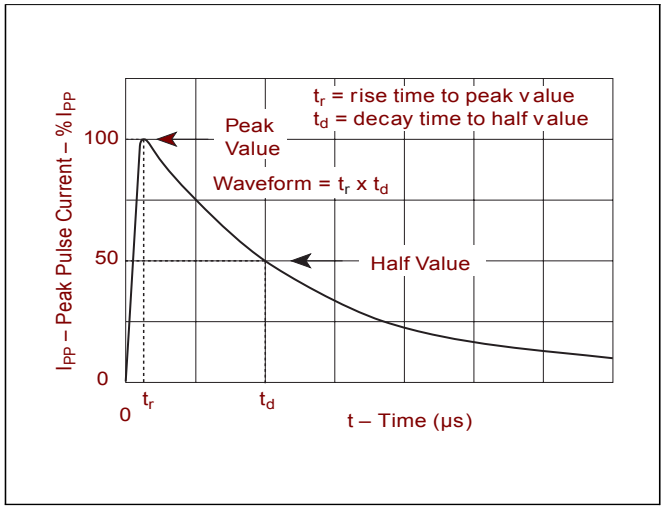
Notes:

1 Current waveform in μs
2 Voltage waveform in μs

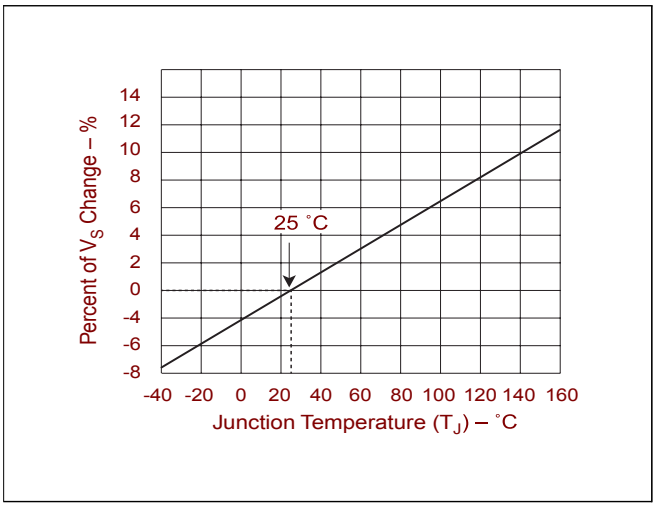
- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product.
- I_{PP} ratings applicable over temperature range of -40ºC to +85ºC
- The device must initially be in thermal equilibrium with -40°C $\leq T_J \leq$ +150°C



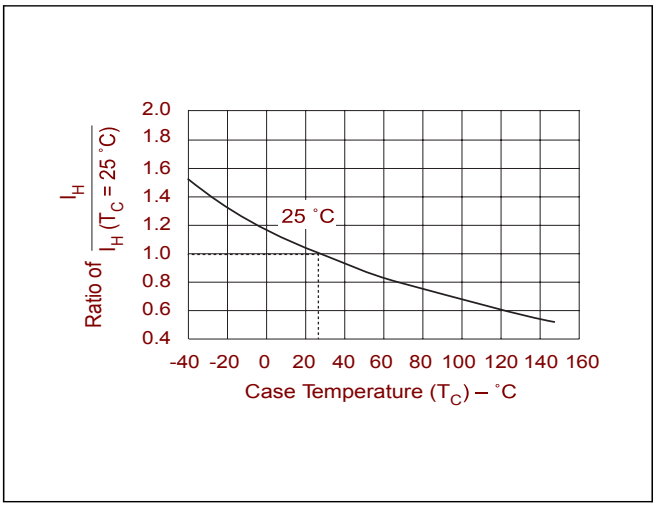
V-I Characteristics



t_r x t_d Pulse Wave-form

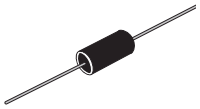


Normalized V_S Change versus Junction Temperature



Normalized DC Holding Current versus Case Temperature

Thermal Considerations

Package	Symbol	Parameter	Value	Unit
DO-15 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	60	°C/W

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T)		8 min. Max.

Figure 1

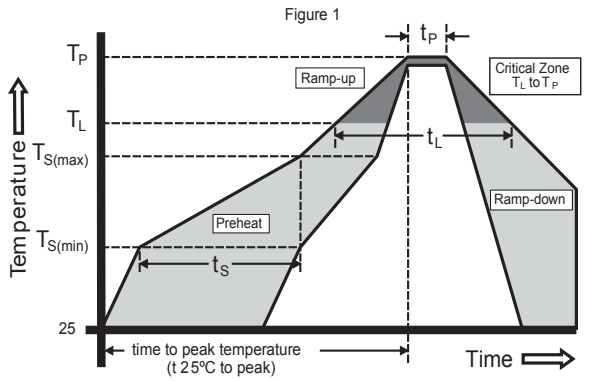
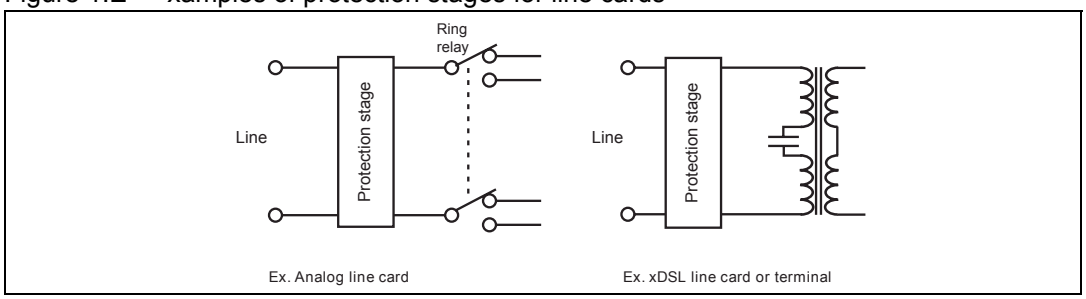


Figure 1.E xamples of protection stages for line cards



In such a stage, parallel function is assumed by one or several Trisil, and is used to protect against short duration surge (lightning). During this kind of surges the Trisil limits the voltage across the device to be protected at its break over value and then fires. The fuse assumes the series function, and is used to protect the module against long duration or very high current mains disturbances (50/60Hz). It acts by safe circuit opening. Lightning surge and mains disturbance surges are defined by standards like GR1089, FCC part 68, ITU-T K20.

Figure 2. Typical circuits

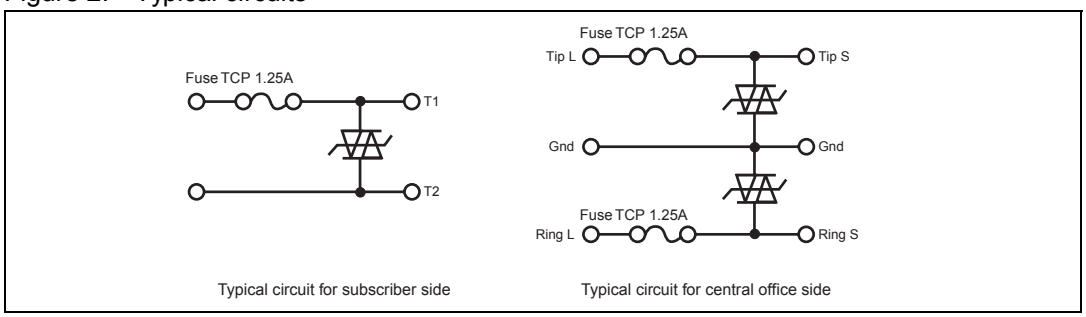


Figure 3.T est circuit 1 for Dynamic I_{BO} and V_{BO} parameters

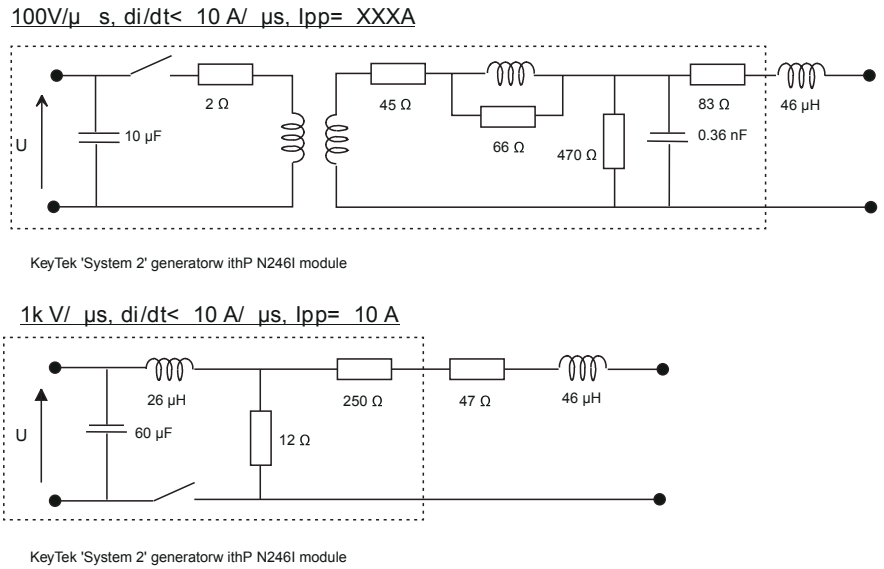
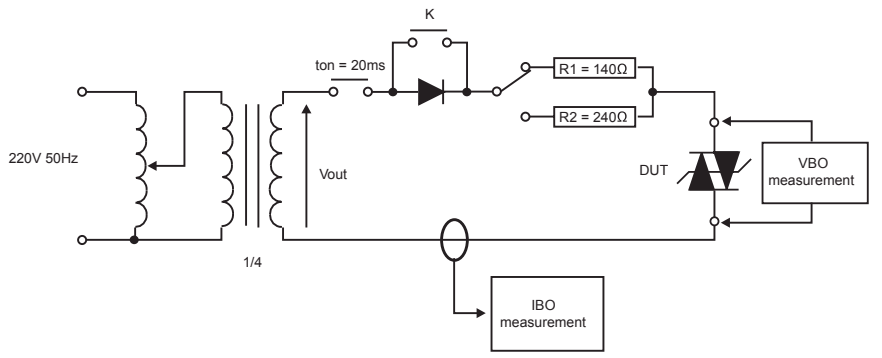


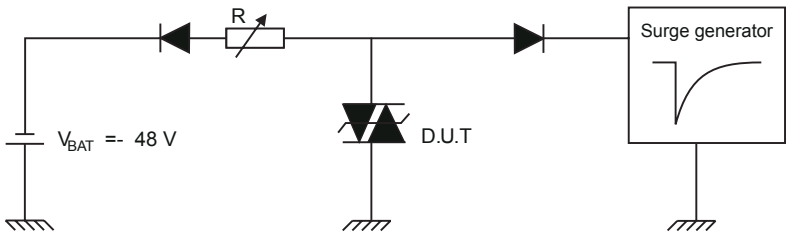
Figure 4. Test circuit 2 for I_{BO} and V_{BO} parameters



TEST PROCEDURE
Pulse test duration (tp = 20ms):
- for Bidirectional devices = Switch K is closed
- for Unidirectional devices = Switch K is open

V_{OUT} selection:
- Device with V_{BO} 200V→ V_{OUT} 250V MS, R1 = 140Ω
- Device with V_{BO} ≥ 200V→ V_{OUT} 480V MS, R2 = 240Ω

Figure 5. Test circuit 3 for dynamic I_H parameter



This is a GO-NOGO test which allows to confirm the holding current (I_H) level in a functional test circuit.

TEST PROCEDURE

1/ Adjust the current level at the Iv alue by short circuiting the AK of the D.U.T.

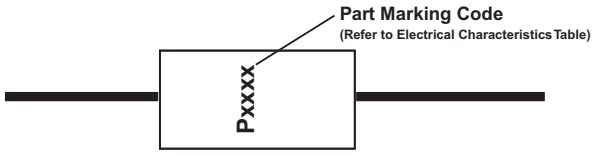
2/ Fire the D.U.T.w ith a surge current → I_{PP} 10A, 10/1000µs.

3/ The D.U.T.w ill come back off-state within 50ms maximum.

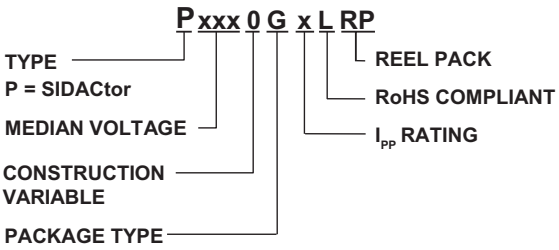
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL recognized epoxy meeting flammability classification 94V-0

Part Marking



Part Numbering



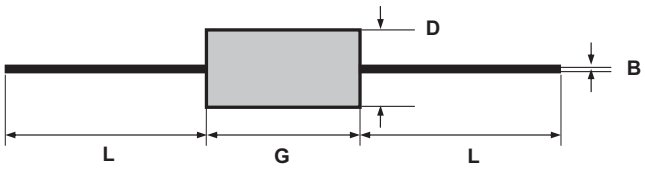
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Packing Options

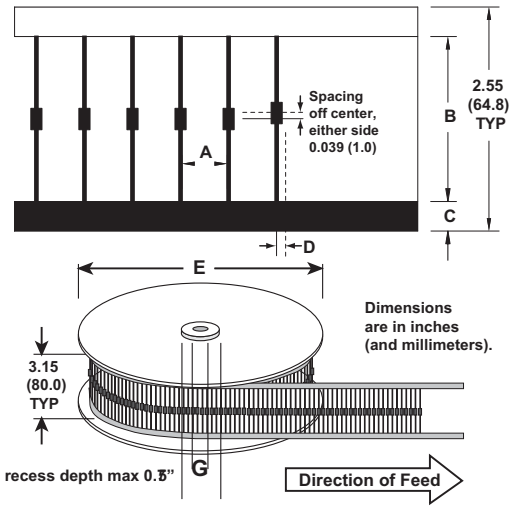
Package Type	Description	Quantity	Added Suffix	Industry Standard
G	DO-15 Axial Tape & Reel	2000	RP	EIA-RS-296-D

Dimensions — DO-15



Dimension	Inches		Millimeters	
	MIN	MAX	MIN	MAX
B	0.028	0.034	0.711	0.864
D	0.12	0.14	3.048	3.556
G	0.235	0.27	5.969	6.858
L	1		25.4	

Tape and Reel Specification — DO-15



Symbols	Description	Inches	MM
A	Component Spacing (lead to lead)	0.200 ± 0.020"	5.08 ± 0.508
B	Inner Tape Pitch	2.062 ± 0.059"	52.37 ± 1.498
C	Tape Width	0.250"	6.35
D	Max. Off Alignment	0.048"	1.219
E	Reel Dimension	13"	330.2
F	Max. Hub Recess	3"	76.19
G	Max. Abor Hole	0.68"	17.27

SHANGHAI LEIDITECH ELECTRONICS TECHNOLOGY CO., LTD
Phone: +86- 021-50828806
Email:sale1@leiditech.com
http://www.leiditech.com