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ILI9338B

a-Si TFT LCD Single Chip Driver
240RGBx320 Resolution and 262K color

Specification
Preliminary

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1. Introduction

ILI9338B is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 240RGBx320 dots, comprising a 720-channel source driver, a 320-channel gate driver, 172,800 bytes GRAM for graphic display data of 240RGBx320 dots, and power supply circuit.

ILI9338B supports parallel 8-/9-/16-/18-bit data bus MCU interface, 6-/16-/18-bit data bus RGB interface and 3-/4-line serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

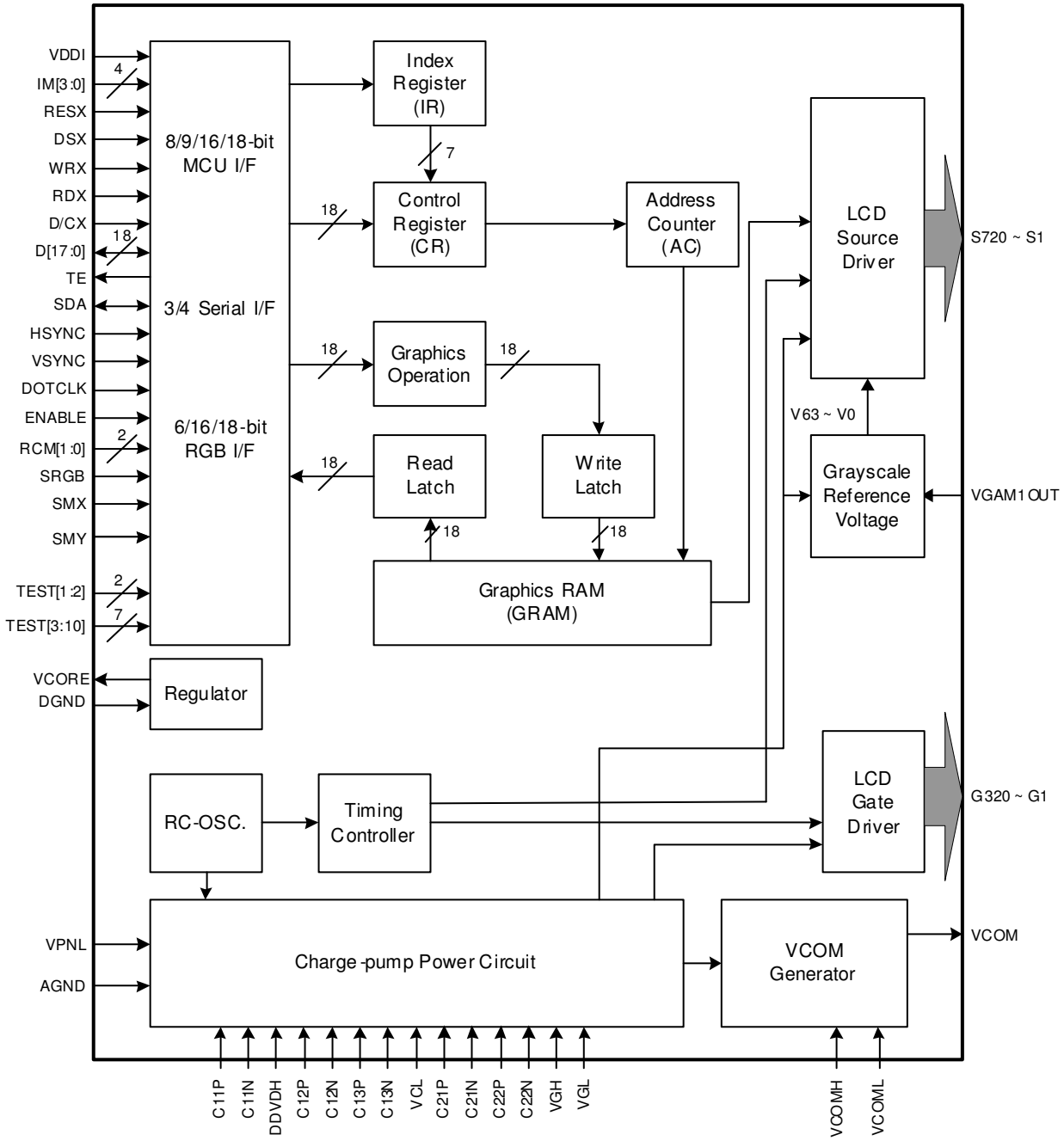
ILI9338B can operate with 1.65V ~ 3.3V I/O interface voltage, and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. ILI9338B supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the ILI9338B an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- Display resolution: [240xRGB](H) x 320(V)
- Output:
  - 720 source outputs
  - 320 gate outputs
  - Common electrode output (VCOM)
- a-TFT LCD driver with on-chip full display RAM: 172,800 bytes
- System Interface
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080-series MCU
  - 6-bits, 16-bits, 18-bits RGB interface with graphic controller
  - 3-line / 4-line serial interface
- Display mode:
  - Full color mode (Idle mode OFF): 262K-color (selectable color depth mode by software)
  - Reduce color mode (Idle mode ON) : 8-color
- Power saving mode:
  - Sleep mode
  - Deep standby mode
- On chip functions:
  - VCOM generator and adjustment
  - Timing generator
  - Oscillator
  - DC/DC converter
  - Line/frame inversion
  - 4 preset selectable gamma curves
- OTP (4 times):
  - 7-bits for ID2
  - 8-bits for ID3
  - 7-bits for VCOM adjustment

- Low -power consumption architecture
  - Low operating power supplies:
    - VDDI = 1.65V ~ 3.3V (logic)
    - VDD = 2.5V ~ 3.3V (analog)
- LCD Voltage drive:
  - Source/VCOM power supply voltage
    - DDVDH - GND = 4.5V ~ 6.0V
    - VCL - GND = -2.0V ~ -3.0V
    - VCI1 - VCL ≦ 6.0V
  - Gate driver output voltage
    - VGH - GND = 10.0V ~ 20.0V
    - VGL - GND = -5.0V ~ -15.0V
    - VGH - VGL ≦ 32V
  - VCOM driver output voltage
    - VCOMH = 3.0V ~ (DDVDH – 0.5)V
    - VCOML = (VCL+0.5)V ~ 0V
    - VCOMH - VCOML ≦ 6.0V
- Operate temperature range: -40℃ to 80℃
- a-Si TFT LCD storage capacitor : Cst on Common structure only

3. Block Diagram



4. Pin Descriptions

<table>
<tr><th colspan="4">Interface Logic Signals</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Type</th><th>Descriptions</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>(VDDI/DGND)</td><td>- Select the MPU system interface mode
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU-Interface Mode</th><th>DB Pin in use</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 16-bits Parallel type Ⅰ</td><td>D[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8080 MCU 8-bits Parallel type Ⅰ</td><td>D[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 16-bits Parallel type Ⅱ</td><td>D[8:1]、D[17:10]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 8-bits Parallel type Ⅱ</td><td>D[17:10]</td></tr>
<tr><td>0</td><td>1</td><td>X</td><td>X</td><td>3-wire Serial interface</td><td>CSX, SCL, SDA</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 18-bits Parallel type Ⅰ</td><td>D[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>8080 MCU 9-bits Parallel type Ⅰ</td><td>D[8:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 18-bits Parallel type Ⅱ</td><td>D[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 9-bits Parallel type Ⅱ</td><td>D[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>X</td><td>X</td><td>4-wire Serial interface</td><td>CSX, SCL, SDA, D/CX</td></tr>
<tr><td colspan="6">If not used, please fix this pin to VDDI or DGND level</td></tr>
</table></td></tr>
<tr><td>TE</td><td>O</td><td>MPU
(VDDI/DGND)</td><td>- Tearing effect output.
Leave the pin to open when not in use.</td></tr>
<tr><td>CSX</td><td>I</td><td>MPU
(VDDI/DGND)</td><td>- A chip selection signal.
Low: the chip is selected and accessible
High: the chip is not selected and not accessible
Fix to VDDI level when not in use.</td></tr>
<tr><td>D/CX (SCL)</td><td>I</td><td>MPU
(VDDI/DGND)</td><td>- Parallel interface (D/CX):
The signal for command or parameter select.
Low: Command.
High: Parameter.
- Serial interface (SCL): Serial clock input.</td></tr>
<tr><td>WRX (R/WX)
(D/CX)</td><td>I</td><td>MPU
(VDDI/DGND)</td><td>- 8080 system (WRX): Serves as a write signal and writes data at the rising edge.
- 4-line system (D/CX): Serves as command or parameter select.
Fix to VDDI or DGND level when not in use.</td></tr>
<tr><td>RDX</td><td>I</td><td>MPU
(VDDI/DGND)</td><td>- 8080 system (RDX): Serves as a read signal and read data at the rising edge.
Fix to VDDI or DGND level when not in use.</td></tr>
<tr><td>SDA</td><td>I/O</td><td>MPU
(VDDI/DGND)</td><td>Serial data input / output.
Fix to VDDI or DGND level when not in use.</td></tr>
<tr><td>RESX</td><td>I</td><td>MPU
(VDDI/DGND)</td><td>The external reset input.
Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.</td></tr>
<tr><td>DE</td><td>I</td><td>MPU
(VDDI/DGND)</td><td>Data enable signal for RGB interface operation.
Fix to VDDI or DGND level when not in use.</td></tr>
<tr><td>D[17:0]</td><td>I/O</td><td>MPU
(VDDI/DGND)</td><td>18-bit parallel bi-directional data bus for MCU system and RGB interface mode
<table>
<tr><th>Interface Mode</th><th>Data Pin in Use</th></tr>
<tr><td>8-bit type Ⅰ MCU System Interface Mode</td><td>D[7:0]</td></tr>
<tr><td>8-bit type Ⅱ MCU System Interface Mode</td><td>D[17:10]</td></tr>
<tr><td>9-bit type Ⅰ MCU System Interface Mode</td><td>D[8:0]</td></tr>
<tr><td>9-bit type Ⅱ MCU System Interface Mode</td><td>D[17:9]</td></tr>
<tr><td>16-bit type Ⅰ MCU System Interface Mode</td><td>D[15:0]</td></tr>
<tr><td>16-bit type Ⅱ MCU System Interface Mode</td><td>D[8:1]、D[17:10]</td></tr>
<tr><td>18-bit type Ⅰ MCU System Interface Mode</td><td>D[17:0]</td></tr>
<tr><td>18-bit type Ⅱ MCU System Interface Mode</td><td>D[17:0]</td></tr>
</table></td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td>
<table>
<tr><td>6-bit RGB Interface Mode</td><td>D[7:2]</td></tr>
<tr><td>16-bit RGB Interface Mode</td><td>D[17:13], D[11:1]</td></tr>
<tr><td>18-bit RGB Interface Mode</td><td>D[17:0]</td></tr>
</table>
Fix to DGND level when not in use</td></tr>
<tr><td>VSYNC</td><td>I</td><td>MPU
(VDDI/DGND)</td><td>Frame synchronizing signal for RGB interface operation.
Fix to VDDI or DGND level when not in use.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>MPU
(VDDI/DGND)</td><td>Line synchronizing signal for RGB interface operation.
Fix to VDDI or DGND level when not in use.</td></tr>
<tr><td>DOTCLK</td><td>I</td><td>MPU
(VDDI/DGND)</td><td>Dot clock signal for RGB interface operation.
Fix to VDDI or DGND level when not in use.</td></tr>
<tr><td>Dummy_EXTC</td><td>I</td><td>MPU
(VDDI/DGND)</td><td>Please connect Dummy_EXTC to VDDI or DGND</td></tr>
<tr><td>RCM[1:0]</td><td>I</td><td>MPU
(VDDI/DGND)</td><td>MCU/RGB interface mode external selection pin.
<table>
<tr><th>RCM[1]</th><th>RCM[0]</th><th>Interface Mode</th></tr>
<tr><td>0</td><td>0</td><td>MCU interface</td></tr>
<tr><td>0</td><td>1</td><td>MCU interface</td></tr>
<tr><td>1</td><td>0</td><td>RGB interface DE mode</td></tr>
<tr><td>1</td><td>1</td><td>RGB interface SYNC mode</td></tr>
</table>
Fixed to DGND level or VDDI when not in use</td></tr>
<tr><td>SRGB</td><td>I</td><td>MPU
(VDDI/DGND)</td><td>RGB color map selection pin.
<table>
<tr><th>SRGB</th><th>RGB Filter Order for Color Filter</th></tr>
<tr><td>0</td><td>S1,S2,S3 filter order =’R’ ‘G’ ‘B’</td></tr>
<tr><td>1</td><td>S1,S2,S3 filter order =’B’ ‘G’ ‘R’</td></tr>
</table></td></tr>
<tr><td>SMX</td><td>I</td><td>MPU
(VDDI/DGND)</td><td>Source output direction selection pin.
<table>
<tr><th>SMX</th><th>Module Source Output Direction</th></tr>
<tr><td>0</td><td>S1 ➔ S720</td></tr>
<tr><td>1</td><td>S720 ➔ S1</td></tr>
</table></td></tr>
<tr><td>SMY</td><td>I</td><td>MPU
(VDDI/DGND)</td><td>Gate output direction selection pin.
<table>
<tr><th>SMY</th><th>Module Source Output Direction</th></tr>
<tr><td>0</td><td>G1 ➔ G320</td></tr>
<tr><td>1</td><td>G320 ➔ G1</td></tr>
</table></td></tr>
<tr><td colspan="4">LCD Driving signals</td></tr>
<tr><td>S720~S1</td><td>O</td><td>LCD</td><td>Source output signals..
Leave the pin to open when not in use.</td></tr>
<tr><td>G320~G1</td><td>O</td><td>LCD</td><td>Gate output signals.
Leave the pin to open when not in use.</td></tr>
<tr><td>VCOM</td><td>O</td><td>TFT common Electrode</td><td>A supply voltage to the common electrode of TFT panel
VCOM is AC voltage alternating signal between the VCOMH and VCOML levels.</td></tr>
<tr><td colspan="4">Charge-pump and Regulator Circuit</td></tr>
<tr><td>VCORE</td><td>P</td><td>Power</td><td>Regulated power output pad.
This power is applied to the digital core circuit.
Connect this pad with a stabilizing capacitor.</td></tr>
<tr><td>VREG1OUT</td><td>P</td><td>Stabilizing Capacitor</td><td>Internal generated reference voltage for source driver and VCOM
The voltage level can be set by VRH [5:0].
VREG1OUT = 3.0~ (DDVDH-0.5)V</td></tr>
<tr><td>VCL</td><td>P</td><td>Stabilizing capacitor</td><td>Power supply for VCOML.
VCL = 0~ - VDD
Connect this pad with a stabilizing capacitor.</td></tr>
<tr><td>DDVDH</td><td>P</td><td>Stabilizing capacitor</td><td>Power supply for the source driver and VCOM driver.
Connect this pad with a stabilizing capacitor.</td></tr>
<tr><td>VGH</td><td>P</td><td>Stabilizing capacitor</td><td>Power supply for the gate driver.
Adjust the VGH level with the BT[2:0] bits.</td></tr>
</table>

			Connect this pad with a stabilizing capacitor.
VGL	P	Stabilizing capacitor	Power supply for the gate driver. Adjust the VGL level with the BT[2:0] bits. Connect this pad with a stabilizing capacitor.
C11P, C11N C12P, C12N	P	Step-up capacitor	Capacitor connection pins for the step-up circuit 1.
C21P, C21N C22P, C22N C31P, C31N	P	Step-up Capacitor	Capacitor connection pins for the step-up circuit 2/3/4.
Power Pads			
VDDI	P	Power supply	Power supply for the I/O interface. Connect to an external power supply of 1.65V ~ 3.3V.
VDD	P	Power supply	Power supply for the analog circuit. Connect to an external power supply of 2.5V ~ 3.3V.
AGND	P	Power supply	Ground level for the analog side: AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
DGND	P	Power supply	Ground level for the logic side: DGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
VPP_OTP	P	Power supply	Power supply for OTP Programming. **Connect to an external power supply of 7.0V ~ 7.5V when programming OTP and leave this pad open when it's not used.**
Test Pads			
TEST_EN	I	DGND	Test pins. (internal pull low) ***Leave the pin to be open.***
TEST0~8	I/O	DGND	Test pins. (internal pull low) ***Leave the pin to be open.***
DUMMY	-	Open	Dummy pads. ***Leave the pin to be open.***
DUMMYR 1~2	-	Short	Both of dummy pads are used to measure the COG contact resistance. They are short-circuited within the chip.

Liquid crystal power supply specifications Table

No.	Item		Description
1	TFT Source Driver		720 pins (240 x RGB)
2	TFT Gate Driver		320 pins
3	TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
4	Liquid Crystal Drive Output	S1 ~ S720	V0 ~ V63 grayscales
		G1 ~ G320	VGH - VGL
		VCOM	VCOMH - VCOML: Amplitude = electronic volumes
5	Input Voltage	VDDI	1.65V ~ 3.30V
		VDD	2.50V ~ 3.30V
6	Liquid Crystal Drive Voltages	DDVDH	4.5V ~ 6.0V
		VGH	10.0V ~ 20.0V
		VGL	-5.0V ~ -15.0V
		VCL	-1.9V ~ -3.0V
		VGH - VGL	Max. 32.0V
		VCI1 - VCL	Max. 6.0V
7	Internal Step-up Circuits	DDVDH	VCI1 x2, x3
		VGH	VCI1 x4, x5, x6, x7, x9
		VGL	VCI1 x-3, x-4, x-5, x-6, x-7
		VCL	VCI1 x-1

Note: VCI1 is an internal reference voltage for the step-up circuit1.

5. Pad Arrangement and Coordination

Chip Size: 15616um x 705um

Chip thickness : 280um (typ.)

Pad Location: Pad Center.

Coordinate Origin: Chip center

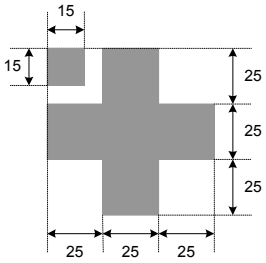
Au bump height: 12um (typ.)

Au Bump Size:

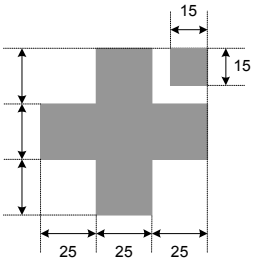
1. 18um x 80um
   Gate: G[1] ~ G[320]
   Source: S[1] ~ S[720]

2. 40um x 56um
   Input Pads
   Pad 1 to 235

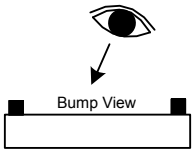
Alignment Marks

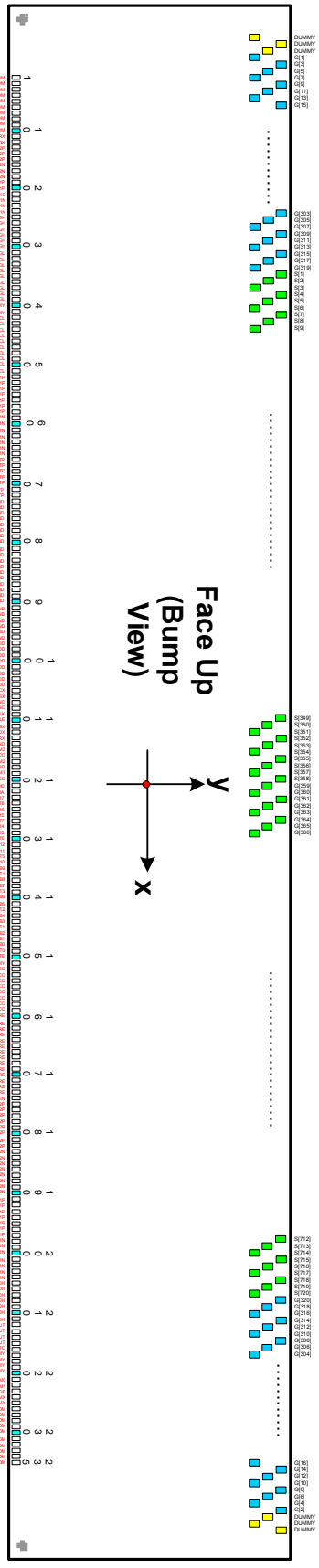


Alignment Mark: A1



Alignment Mark: A2





No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	VCOM	-7307.5	-265	61	C31N	-3707	-265	121	IM0	-107.5	-265	181	C12P	4067.5	-265
2	VCOM	-7247.5	-265	62	C31N	-3647	-265	122	SDA	-47.5	-265	182	C12P	4127.5	-265
3	VCOM	-7187.5	-265	63	C31N	-3587	-265	123	D[17]	37.5	-265	183	C12N	4187.5	-265
4	VCOM	-7127.5	-265	64	C31N	-3527	-265	124	TEST8	122.5	-265	184	C12N	4247.5	-265
5	VCOM	-7067.5	-265	65	C31N	-3467	-265	125	D[16]	182.5	-265	185	C12N	4307.5	-265
6	VCOM	-7007.5	-265	66	VPP_OTP	-3407	-265	126	D[15]	267.5	-265	186	C12N	4367.5	-265
7	VCOM	-6947.5	-265	67	VPP_OTP	-3347	-265	127	TEST7	352.5	-265	187	C12N	4427.5	-265
8	VCOM	-6887.5	-265	68	VPP_OTP	-3287	-265	128	D[14]	412.5	-265	188	C12N	4487.5	-265
9	VCOM	-6827.5	-265	69	VPP_OTP	-3227	-265	129	D[13]	497.5	-265	189	C12N	4547.5	-265
10	VCOM	-6767.5	-265	70	VPP_OTP	-3167	-265	130	TEST6	582.5	-265	190	C12N	4607.5	-265
11	DUMMYRX	-6707.5	-265	71	VPP_OTP	-3107	-265	131	D[12]	642.5	-265	191	C11P	4667.5	-265
12	DUMMYRX	-6647.5	-265	72	VPP_OTP	-3047	-265	132	D[11]	727.5	-265	192	C11P	4727.5	-265
13	C22P	-6587.5	-265	73	AGND	-2987	-265	133	TEST5	812.5	-265	193	C11P	4787.5	-265
14	C22P	-6527.5	-265	74	AGND	-2927	-265	134	D[10]	872.5	-265	194	C11P	4847.5	-265
15	C22P	-6467.5	-265	75	AGND	-2867	-265	135	D[9]	957.5	-265	195	C11P	4907.5	-265
16	C22N	-6407.5	-265	76	AGND	-2807	-265	136	TEST4	1042.5	-265	196	C11P	4967.5	-265
17	C22N	-6347.5	-265	77	AGND	-2747	-265	137	D[8]	1102.5	-265	197	C11P	5027.5	-265
18	C22N	-6287.5	-265	78	AGND	-2687	-265	138	D[7]	1187.5	-265	198	C11N	5087.5	-265
19	C21P	-6227.5	-265	79	AGND	-2627	-265	139	TEST3	1272.5	-265	199	C11N	5147.5	-265
20	C21P	-6167.5	-265	80	AGND	-2567	-265	140	D[6]	1332.5	-265	200	C11N	5207.5	-265
21	C21P	-6107.5	-265	81	AGND	-2507	-265	141	D[5]	1417.5	-265	201	C11N	5267.5	-265
22	C21N	-6047.5	-265	82	AGND	-2447	-265	142	TEST2	1502.5	-265	202	C11N	5327.5	-265
23	C21N	-5987.5	-265	83	AGND	-2387	-265	143	D[4]	1562.5	-265	203	C11N	5387.5	-265
24	C21N	-5927.5	-265	84	AGND	-2327	-265	144	D[3]	1647.5	-265	204	C11N	5447.5	-265
25	VGH	-5867.5	-265	85	AGND	-2267	-265	145	TEST1	1732.5	-265	205	DDVDH	5507.5	-265
26	VGH	-5807.5	-265	86	DGND	-2207	-265	146	D[2]	1792.5	-265	206	DDVDH	5567.5	-265
27	VGH	-5747.5	-265	87	DGND	-2147	-265	147	D[1]	1877.5	-265	207	DDVDH	5627.5	-265
28	VGH	-5687.5	-265	88	DGND	-2087	-265	148	D[0]	1962.5	-265	208	DDVDH	5687.5	-265
29	VGH	-5627.5	-265	89	DGND	-2027	-265	149	TEST0	2047.5	-265	209	DDVDH	5747.5	-265
30	VGH	-5567.5	-265	90	DGND	-1967	-265	150	TE	2132.5	-265	210	DDVDH	5807.5	-265
31	VGL	-5507.5	-265	91	DGND	-1907	-265	151	DUMMY	2217.5	-265	211	DDVDH	5867.5	-265
32	VGL	-5447.5	-265	92	DGND	-1847	-265	152	TESTOSC	2302.5	-265	212	VREG1OUT	5927.5	-265
33	VGL	-5387.5	-265	93	DGND	-1787	-265	153	VDDI	2387.5	-265	213	VREG1OUT	5987.5	-265
34	VGL	-5327.5	-265	94	DGND	-1727	-265	154	VDDI	2447.5	-265	214	VREG1OUT	6047.5	-265
35	VGL	-5267.5	-265	95	DGND	-1667	-265	155	VDDI	2507.5	-265	215	VREG1OUT	6107.5	-265
36	VGL	-5207.5	-265	96	DGND	-1607	-265	156	VDDI	2567.5	-265	216	DUMMY_EXTC	6167.5	-265
37	VGL	-5147.5	-265	97	VDD	-1547	-265	157	VDDI	2627.5	-265	217	DUMMY	6227.5	-265
38	VGL	-5087.5	-265	98	VDD	-1487	-265	158	VDDI	2687.5	-265	218	DUMMY	6287.5	-265
39	VGL	-5027.5	-265	99	VDD	-1427	-265	159	VDDI	2747.5	-265	219	DUMMY	6347.5	-265
40	DUMMY	-4967.5	-265	100	VDD	-1367	-265	160	VCORE	2807.5	-265	220	DUMMY	6407.5	-265
41	DUMMY	-4907.5	-265	101	VDD	-1307	-265	161	VCORE	2867.5	-265	221	RCM0	6467.5	-265
42	VCL	-4847.5	-265	102	VDD	-1247	-265	162	VCORE	2927.5	-265	222	RCM1	6527.5	-265
43	VCL	-4787.5	-265	103	VDD	-1187	-265	163	VCORE	2987.5	-265	223	SRGB	6587.5	-265
44	VCL	-4727.5	-265	104	VDD	-1127	-265	164	VCORE	3047.5	-265	224	SMX	6647.5	-265
45	VCL	-4667.5	-265	105	DCX	-1067	-265	165	VCORE	3107.5	-265	225	SMY	6707.5	-265
46	VCL	-4607.5	-265	106	CSX	-1007	-265	166	VCORE	3167.5	-265	226	VCOM	6767.5	-265
47	VCL	-4547.5	-265	107	VSYNC	-948	-265	167	VCORE	3227.5	-265	227	VCOM	6827.5	-265
48	VCL	-4487.5	-265	108	HSYNC	-888	-265	168	VCORE	3287.5	-265	228	VCOM	6887.5	-265
49	VCL	-4427.5	-265	109	DOTCLK	-828	-265	169	VCORE	3347.5	-265	229	VCOM	6947.5	-265
50	VCL	-4367.5	-265	110	DE	-768	-265	170	VCORE	3407.5	-265	230	VCOM	7007.5	-265
51	VCL	-4307.5	-265	111	RESX	-708	-265	171	VCORE	3467.5	-265	231	VCOM	7067.5	-265
52	C31P	-4247.5	-265	112	RDX	-648	-265	172	VCORE	3527.5	-265	232	VCOM	7127.5	-265
53	C31P	-4187.5	-265	113	WRX	-588	-265	173	VCORE	3587.5	-265	233	VCOM	7187.5	-265
54	C31P	-4127.5	-265	114	DGND	-528	-265	174	TEST_EN	3647.5	-265	234	VCOM	7247.5	-265
55	C31P	-4067.5	-265	115	IM3	-468	-265	175	C12P	3707.5	-265	235	VCOM	7307.5	-265
56	C31P	-4007.5	-265	116	VDDI	-408	-265	176	C12P	3767.5	-265	236	DUMMY	7399	253
57	C31P	-3947.5	-265	117	IM2	-348	-265	177	C12P	3827.5	-265	237	DUMMY	7385	61
58	C31P	-3887.5	-265	118	DGND	-288	-265	178	C12P	3887.5	-265	238	DUMMY	7371	157
59	C31N	-3827.5	-265	119	IM1	-228	-265	179	C12P	3947.5	-265	239	G[2]	7357	253
60	C31N	-3767.5	-265	120	VDDI	-168	-265	180	C12P	4007.5	-265	240	G[4]	7343	61

No.	Pad name	X	Y
241	G[6]	7329	157
242	G[8]	7315	253
243	G[10]	7301	61
244	G[12]	7287	157
245	G[14]	7273	253
246	G[16]	7259	61
247	G[18]	7245	157
248	G[20]	7231	253
249	G[22]	7217	61
250	G[24]	7203	157
251	G[26]	7189	253
252	G[28]	7175	61
253	G[30]	7161	157
254	G[32]	7147	253
255	G[34]	7133	61
256	G[36]	7119	157
257	G[38]	7105	253
258	G[40]	7091	61
259	G[42]	7077	157
260	G[44]	7063	253
261	G[46]	7049	61
262	G[48]	7035	157
263	G[50]	7021	253
264	G[52]	7007	61
265	G[54]	6993	157
266	G[56]	6979	253
267	G[58]	6965	61
268	G[60]	6951	157
269	G[62]	6937	253
270	G[64]	6923	61
271	G[66]	6909	157
272	G[68]	6895	253
273	G[70]	6881	61
274	G[72]	6867	157
275	G[74]	6853	253
276	G[76]	6839	61
277	G[78]	6825	157
278	G[80]	6811	253
279	G[82]	6797	61
280	G[84]	6783	157
281	G[86]	6769	253
282	G[88]	6755	61
283	G[90]	6741	157
284	G[92]	6727	253
285	G[94]	6713	61
286	G[96]	6699	157
287	G[98]	6685	253
288	G[100]	6671	61
289	G[102]	6657	157
290	G[104]	6643	253
291	G[106]	6629	61
292	G[108]	6615	157
293	G[110]	6601	253
294	G[112]	6587	61
295	G[114]	6573	157
296	G[116]	6559	253
297	G[118]	6545	61
298	G[120]	6531	157
299	G[122]	6517	253
300	G[124]	6503	61

No.	Pad name	X	Y
301	G[126]	6489	157
302	G[128]	6475	253
303	G[130]	6461	61
304	G[132]	6447	157
305	G[134]	6433	253
306	G[136]	6419	61
307	G[138]	6405	157
308	G[140]	6391	253
309	G[142]	6377	61
310	G[144]	6363	157
311	G[146]	6349	253
312	G[148]	6335	61
313	G[150]	6321	157
314	G[152]	6307	253
315	G[154]	6293	61
316	G[156]	6279	157
317	G[158]	6265	253
318	G[160]	6251	61
319	G[162]	6237	157
320	G[164]	6223	253
321	G[166]	6209	61
322	G[168]	6195	157
323	G[170]	6181	253
324	G[172]	6167	61
325	G[174]	6153	157
326	G[176]	6139	253
327	G[178]	6125	61
328	G[180]	6111	157
329	G[182]	6097	253
330	G[184]	6083	61
331	G[186]	6069	157
332	G[188]	6055	253
333	G[190]	6041	61
334	G[192]	6027	157
335	G[194]	6013	253
336	G[196]	5999	61
337	G[198]	5985	157
338	G[200]	5971	253
339	G[202]	5957	61
340	G[204]	5943	157
341	G[206]	5929	253
342	G[208]	5915	61
343	G[210]	5901	157
344	G[212]	5887	253
345	G[214]	5873	61
346	G[216]	5859	157
347	G[218]	5845	253
348	G[220]	5831	61
349	G[222]	5817	157
350	G[224]	5803	253
351	G[226]	5789	61
352	G[228]	5775	157
353	G[230]	5761	253
354	G[232]	5747	61
355	G[234]	5733	157
356	G[236]	5719	253
357	G[238]	5705	61
358	G[240]	5691	157
359	G[242]	5677	253
360	G[244]	5663	61

No.	Pad name	X	Y
361	G[246]	5649	157
362	G[248]	5635	253
363	G[250]	5621	61
364	G[252]	5607	157
365	G[254]	5593	253
366	G[256]	5579	61
367	G[258]	5565	157
368	G[260]	5551	253
369	G[262]	5537	61
370	G[264]	5523	157
371	G[266]	5509	253
372	G[268]	5495	61
373	G[270]	5481	157
374	G[272]	5467	253
375	G[274]	5453	61
376	G[276]	5439	157
377	G[278]	5425	253
378	G[280]	5411	61
379	G[282]	5397	157
380	G[284]	5383	253
381	G[286]	5369	61
382	G[288]	5355	157
383	G[290]	5341	253
384	G[292]	5327	61
385	G[294]	5313	157
386	G[296]	5299	253
387	G[298]	5285	61
388	G[300]	5271	157
389	G[302]	5257	253
390	G[304]	5243	61
391	G[306]	5229	157
392	G[308]	5215	253
393	G[310]	5201	61
394	G[312]	5187	157
395	G[314]	5173	253
396	G[316]	5159	61
397	G[318]	5145	157
398	G[320]	5131	253
399	S[720]	5075	61
400	S[719]	5061	157
401	S[718]	5047	253
402	S[717]	5033	61
403	S[716]	5019	157
404	S[715]	5005	253
405	S[714]	4991	61
406	S[713]	4977	157
407	S[712]	4963	253
408	S[711]	4949	61
409	S[710]	4935	157
410	S[709]	4921	253
411	S[708]	4907	61
412	S[707]	4893	157
413	S[706]	4879	253
414	S[705]	4865	61
415	S[704]	4851	157
416	S[703]	4837	253
417	S[702]	4823	61
418	S[701]	4809	157
419	S[700]	4795	253
420	S[699]	4781	61

No.	Pad name	X	Y
421	S[698]	4767	157
422	S[697]	4753	253
423	S[696]	4739	61
424	S[695]	4725	157
425	S[694]	4711	253
426	S[693]	4697	61
427	S[692]	4683	157
428	S[691]	4669	253
429	S[690]	4655	61
430	S[689]	4641	157
431	S[688]	4627	253
432	S[687]	4613	61
433	S[686]	4599	157
434	S[685]	4585	253
435	S[684]	4571	61
436	S[683]	4557	157
437	S[682]	4543	253
438	S[681]	4529	61
439	S[680]	4515	157
440	S[679]	4501	253
441	S[678]	4487	61
442	S[677]	4473	157
443	S[676]	4459	253
444	S[675]	4445	61
445	S[674]	4431	157
446	S[673]	4417	253
447	S[672]	4403	61
448	S[671]	4389	157
449	S[670]	4375	253
450	S[669]	4361	61
451	S[668]	4347	157
452	S[667]	4333	253
453	S[666]	4319	61
454	S[665]	4305	157
455	S[664]	4291	253
456	S[663]	4277	61
457	S[662]	4263	157
458	S[661]	4249	253
459	S[660]	4235	61
460	S[659]	4221	157
461	S[658]	4207	253
462	S[657]	4193	61
463	S[656]	4179	157
464	S[655]	4165	253
465	S[654]	4151	61
466	S[653]	4137	157
467	S[652]	4123	253
468	S[651]	4109	61
469	S[650]	4095	157
470	S[649]	4081	253
471	S[648]	4067	61
472	S[647]	4053	157
473	S[646]	4039	253
474	S[645]	4025	61
475	S[644]	4011	157
476	S[643]	3997	253
477	S[642]	3983	61
478	S[641]	3969	157
479	S[640]	3955	253
480	S[639]	3941	61

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
481	S[638]	3927	157	541	S[578]	3087	157	601	S[518]	2247	157	661	S[458]	1407	157
482	S[637]	3913	253	542	S[577]	3073	253	602	S[517]	2233	253	662	S[457]	1393	253
483	S[636]	3899	61	543	S[576]	3059	61	603	S[516]	2219	61	663	S[456]	1379	61
484	S[635]	3885	157	544	S[575]	3045	157	604	S[515]	2205	157	664	S[455]	1365	157
485	S[634]	3871	253	545	S[574]	3031	253	605	S[514]	2191	253	665	S[454]	1351	253
486	S[633]	3857	61	546	S[573]	3017	61	606	S[513]	2177	61	666	S[453]	1337	61
487	S[632]	3843	157	547	S[572]	3003	157	607	S[512]	2163	157	667	S[452]	1323	157
488	S[631]	3829	253	548	S[571]	2989	253	608	S[511]	2149	253	668	S[451]	1309	253
489	S[630]	3815	61	549	S[570]	2975	61	609	S[510]	2135	61	669	S[450]	1295	61
490	S[629]	3801	157	550	S[569]	2961	157	610	S[509]	2121	157	670	S[449]	1281	157
491	S[628]	3787	253	551	S[568]	2947	253	611	S[508]	2107	253	671	S[448]	1267	253
492	S[627]	3773	61	552	S[567]	2933	61	612	S[507]	2093	61	672	S[447]	1253	61
493	S[626]	3759	157	553	S[566]	2919	157	613	S[506]	2079	157	673	S[446]	1239	157
494	S[625]	3745	253	554	S[565]	2905	253	614	S[505]	2065	253	674	S[445]	1225	253
495	S[624]	3731	61	555	S[564]	2891	61	615	S[504]	2051	61	675	S[444]	1211	61
496	S[623]	3717	157	556	S[563]	2877	157	616	S[503]	2037	157	676	S[443]	1197	157
497	S[622]	3703	253	557	S[562]	2863	253	617	S[502]	2023	253	677	S[442]	1183	253
498	S[621]	3689	61	558	S[561]	2849	61	618	S[501]	2009	61	678	S[441]	1169	61
499	S[620]	3675	157	559	S[560]	2835	157	619	S[500]	1995	157	679	S[440]	1155	157
500	S[619]	3661	253	560	S[559]	2821	253	620	S[499]	1981	253	680	S[439]	1141	253
501	S[618]	3647	61	561	S[558]	2807	61	621	S[498]	1967	61	681	S[438]	1127	61
502	S[617]	3633	157	562	S[557]	2793	157	622	S[497]	1953	157	682	S[437]	1113	157
503	S[616]	3619	253	563	S[556]	2779	253	623	S[496]	1939	253	683	S[436]	1099	253
504	S[615]	3605	61	564	S[555]	2765	61	624	S[495]	1925	61	684	S[435]	1085	61
505	S[614]	3591	157	565	S[554]	2751	157	625	S[494]	1911	157	685	S[434]	1071	157
506	S[613]	3577	253	566	S[553]	2737	253	626	S[493]	1897	253	686	S[433]	1057	253
507	S[612]	3563	61	567	S[552]	2723	61	627	S[492]	1883	61	687	S[432]	1043	61
508	S[611]	3549	157	568	S[551]	2709	157	628	S[491]	1869	157	688	S[431]	1029	157
509	S[610]	3535	253	569	S[550]	2695	253	629	S[490]	1855	253	689	S[430]	1015	253
510	S[609]	3521	61	570	S[549]	2681	61	630	S[489]	1841	61	690	S[429]	1001	61
511	S[608]	3507	157	571	S[548]	2667	157	631	S[488]	1827	157	691	S[428]	987	157
512	S[607]	3493	253	572	S[547]	2653	253	632	S[487]	1813	253	692	S[427]	973	253
513	S[606]	3479	61	573	S[546]	2639	61	633	S[486]	1799	61	693	S[426]	959	61
514	S[605]	3465	157	574	S[545]	2625	157	634	S[485]	1785	157	694	S[425]	945	157
515	S[604]	3451	253	575	S[544]	2611	253	635	S[484]	1771	253	695	S[424]	931	253
516	S[603]	3437	61	576	S[543]	2597	61	636	S[483]	1757	61	696	S[423]	917	61
517	S[602]	3423	157	577	S[542]	2583	157	637	S[482]	1743	157	697	S[422]	903	157
518	S[601]	3409	253	578	S[541]	2569	253	638	S[481]	1729	253	698	S[421]	889	253
519	S[600]	3395	61	579	S[540]	2555	61	639	S[480]	1715	61	699	S[420]	875	61
520	S[599]	3381	157	580	S[539]	2541	157	640	S[479]	1701	157	700	S[419]	861	157
521	S[598]	3367	253	581	S[538]	2527	253	641	S[478]	1687	253	701	S[418]	847	253
522	S[597]	3353	61	582	S[537]	2513	61	642	S[477]	1673	61	702	S[417]	833	61
523	S[596]	3339	157	583	S[536]	2499	157	643	S[476]	1659	157	703	S[416]	819	157
524	S[595]	3325	253	584	S[535]	2485	253	644	S[475]	1645	253	704	S[415]	805	253
525	S[594]	3311	61	585	S[534]	2471	61	645	S[474]	1631	61	705	S[414]	791	61
526	S[593]	3297	157	586	S[533]	2457	157	646	S[473]	1617	157	706	S[413]	777	157
527	S[592]	3283	253	587	S[532]	2443	253	647	S[472]	1603	253	707	S[412]	763	253
528	S[591]	3269	61	588	S[531]	2429	61	648	S[471]	1589	61	708	S[411]	749	61
529	S[590]	3255	157	589	S[530]	2415	157	649	S[470]	1575	157	709	S[410]	735	157
530	S[589]	3241	253	590	S[529]	2401	253	650	S[469]	1561	253	710	S[409]	721	253
531	S[588]	3227	61	591	S[528]	2387	61	651	S[468]	1547	61	711	S[408]	707	61
532	S[587]	3213	157	592	S[527]	2373	157	652	S[467]	1533	157	712	S[407]	693	157
533	S[586]	3199	253	593	S[526]	2359	253	653	S[466]	1519	253	713	S[406]	679	253
534	S[585]	3185	61	594	S[525]	2345	61	654	S[465]	1505	61	714	S[405]	665	61
535	S[584]	3171	157	595	S[524]	2331	157	655	S[464]	1491	157	715	S[404]	651	157
536	S[583]	3157	253	596	S[523]	2317	253	656	S[463]	1477	253	716	S[403]	637	253
537	S[582]	3143	61	597	S[522]	2303	61	657	S[462]	1463	61	717	S[402]	623	61
538	S[581]	3129	157	598	S[521]	2289	157	658	S[461]	1449	157	718	S[401]	609	157
539	S[580]	3115	253	599	S[520]	2275	253	659	S[460]	1435	253	719	S[400]	595	253
540	S[579]	3101	61	600	S[519]	2261	61	660	S[459]	1421	61	720	S[399]	581	61

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
721	S[398]	567	157	781	S[338]	-357	157	841	S[278]	-1197	157	901	S[218]	-2037	157
722	S[397]	553	253	782	S[337]	-371	253	842	S[277]	-1211	253	902	S[217]	-2051	253
723	S[396]	539	61	783	S[336]	-385	61	843	S[276]	-1225	61	903	S[216]	-2065	61
724	S[395]	525	157	784	S[335]	-399	157	844	S[275]	-1239	157	904	S[215]	-2079	157
725	S[394]	511	253	785	S[334]	-413	253	845	S[274]	-1253	253	905	S[214]	-2093	253
726	S[393]	497	61	786	S[333]	-427	61	846	S[273]	-1267	61	906	S[213]	-2107	61
727	S[392]	483	157	787	S[332]	-441	157	847	S[272]	-1281	157	907	S[212]	-2121	157
728	S[391]	469	253	788	S[331]	-455	253	848	S[271]	-1295	253	908	S[211]	-2135	253
729	S[390]	455	61	789	S[330]	-469	61	849	S[270]	-1309	61	909	S[210]	-2149	61
730	S[389]	441	157	790	S[329]	-483	157	850	S[269]	-1323	157	910	S[209]	-2163	157
731	S[388]	427	253	791	S[328]	-497	253	851	S[268]	-1337	253	911	S[208]	-2177	253
732	S[387]	413	61	792	S[327]	-511	61	852	S[267]	-1351	61	912	S[207]	-2191	61
733	S[386]	399	157	793	S[326]	-525	157	853	S[266]	-1365	157	913	S[206]	-2205	157
734	S[385]	385	253	794	S[325]	-539	253	854	S[265]	-1379	253	914	S[205]	-2219	253
735	S[384]	371	61	795	S[324]	-553	61	855	S[264]	-1393	61	915	S[204]	-2233	61
736	S[383]	357	157	796	S[323]	-567	157	856	S[263]	-1407	157	916	S[203]	-2247	157
737	S[382]	343	253	797	S[322]	-581	253	857	S[262]	-1421	253	917	S[202]	-2261	253
738	S[381]	329	61	798	S[321]	-595	61	858	S[261]	-1435	61	918	S[201]	-2275	61
739	S[380]	315	157	799	S[320]	-609	157	859	S[260]	-1449	157	919	S[200]	-2289	157
740	S[379]	301	253	800	S[319]	-623	253	860	S[259]	-1463	253	920	S[199]	-2303	253
741	S[378]	287	61	801	S[318]	-637	61	861	S[258]	-1477	61	921	S[198]	-2317	61
742	S[377]	273	157	802	S[317]	-651	157	862	S[257]	-1491	157	922	S[197]	-2331	157
743	S[376]	259	253	803	S[316]	-665	253	863	S[256]	-1505	253	923	S[196]	-2345	253
744	S[375]	245	61	804	S[315]	-679	61	864	S[255]	-1519	61	924	S[195]	-2359	61
745	S[374]	231	157	805	S[314]	-693	157	865	S[254]	-1533	157	925	S[194]	-2373	157
746	S[373]	217	253	806	S[313]	-707	253	866	S[253]	-1547	253	926	S[193]	-2387	253
747	S[372]	203	61	807	S[312]	-721	61	867	S[252]	-1561	61	927	S[192]	-2401	61
748	S[371]	189	157	808	S[311]	-735	157	868	S[251]	-1575	157	928	S[191]	-2415	157
749	S[370]	175	253	809	S[310]	-749	253	869	S[250]	-1589	253	929	S[190]	-2429	253
750	S[369]	161	61	810	S[309]	-763	61	870	S[249]	-1603	61	930	S[189]	-2443	61
751	S[368]	147	157	811	S[308]	-777	157	871	S[248]	-1617	157	931	S[188]	-2457	157
752	S[367]	133	253	812	S[307]	-791	253	872	S[247]	-1631	253	932	S[187]	-2471	253
753	S[366]	119	61	813	S[306]	-805	61	873	S[246]	-1645	61	933	S[186]	-2485	61
754	S[365]	105	157	814	S[305]	-819	157	874	S[245]	-1659	157	934	S[185]	-2499	157
755	S[364]	91	253	815	S[304]	-833	253	875	S[244]	-1673	253	935	S[184]	-2513	253
756	S[363]	77	61	816	S[303]	-847	61	876	S[243]	-1687	61	936	S[183]	-2527	61
757	S[362]	63	157	817	S[302]	-861	157	877	S[242]	-1701	157	937	S[182]	-2541	157
758	S[361]	49	253	818	S[301]	-875	253	878	S[241]	-1715	253	938	S[181]	-2555	253
759	S[360]	-49	61	819	S[300]	-889	61	879	S[240]	-1729	61	939	S[180]	-2569	61
760	S[359]	-63	157	820	S[299]	-903	157	880	S[239]	-1743	157	940	S[179]	-2583	157
761	S[358]	-77	253	821	S[298]	-917	253	881	S[238]	-1757	253	941	S[178]	-2597	253
762	S[357]	-91	61	822	S[297]	-931	61	882	S[237]	-1771	61	942	S[177]	-2611	61
763	S[356]	-105	157	823	S[296]	-945	157	883	S[236]	-1785	157	943	S[176]	-2625	157
764	S[355]	-119	253	824	S[295]	-959	253	884	S[235]	-1799	253	944	S[175]	-2639	253
765	S[354]	-133	61	825	S[294]	-973	61	885	S[234]	-1813	61	945	S[174]	-2653	61
766	S[353]	-147	157	826	S[293]	-987	157	886	S[233]	-1827	157	946	S[173]	-2667	157
767	S[352]	-161	253	827	S[292]	-1001	253	887	S[232]	-1841	253	947	S[172]	-2681	253
768	S[351]	-175	61	828	S[291]	-1015	61	888	S[231]	-1855	61	948	S[171]	-2695	61
769	S[350]	-189	157	829	S[290]	-1029	157	889	S[230]	-1869	157	949	S[170]	-2709	157
770	S[349]	-203	253	830	S[289]	-1043	253	890	S[229]	-1883	253	950	S[169]	-2723	253
771	S[348]	-217	61	831	S[288]	-1057	61	891	S[228]	-1897	61	951	S[168]	-2737	61
772	S[347]	-231	157	832	S[287]	-1071	157	892	S[227]	-1911	157	952	S[167]	-2751	157
773	S[346]	-245	253	833	S[286]	-1085	253	893	S[226]	-1925	253	953	S[166]	-2765	253
774	S[345]	-259	61	834	S[285]	-1099	61	894	S[225]	-1939	61	954	S[165]	-2779	61
775	S[344]	-273	157	835	S[284]	-1113	157	895	S[224]	-1953	157	955	S[164]	-2793	157
776	S[343]	-287	253	836	S[283]	-1127	253	896	S[223]	-1967	253	956	S[163]	-2807	253
777	S[342]	-301	61	837	S[282]	-1141	61	897	S[222]	-1981	61	957	S[162]	-2821	61
778	S[341]	-315	157	838	S[281]	-1155	157	898	S[221]	-1995	157	958	S[161]	-2835	157
779	S[340]	-329	253	839	S[280]	-1169	253	899	S[220]	-2009	253	959	S[160]	-2849	253
780	S[339]	-343	61	840	S[279]	-1183	61	900	S[219]	-2023	61	960	S[159]	-2863	61

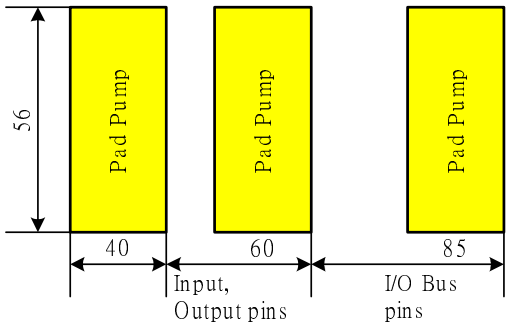
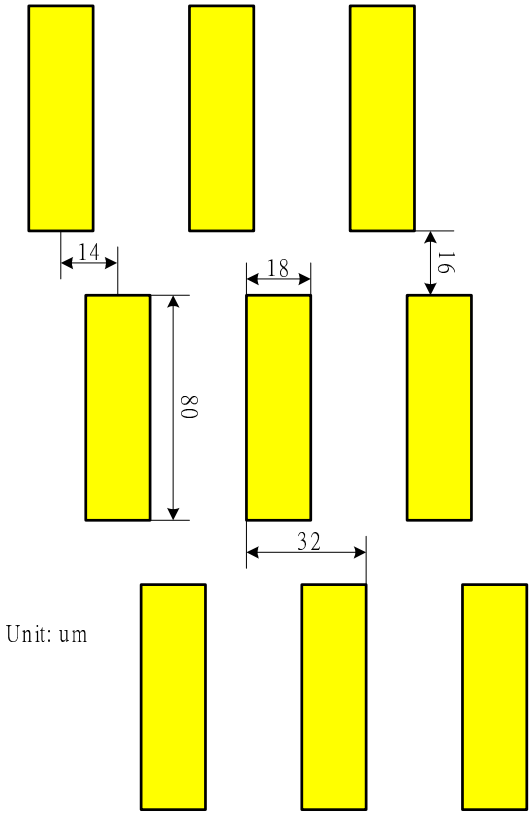
No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
961	S[158]	-2877	157	1021	S[98]	-3717	157	1081	S[38]	-4557	157	1141	G[275]	-5439	157
962	S[157]	-2891	253	1022	S[97]	-3731	253	1082	S[37]	-4571	253	1142	G[273]	-5453	253
963	S[156]	-2905	61	1023	S[96]	-3745	61	1083	S[36]	-4585	61	1143	G[271]	-5467	61
964	S[155]	-2919	157	1024	S[95]	-3759	157	1084	S[35]	-4599	157	1144	G[269]	-5481	157
965	S[154]	-2933	253	1025	S[94]	-3773	253	1085	S[34]	-4613	253	1145	G[267]	-5495	253
966	S[153]	-2947	61	1026	S[93]	-3787	61	1086	S[33]	-4627	61	1146	G[265]	-5509	61
967	S[152]	-2961	157	1027	S[92]	-3801	157	1087	S[32]	-4641	157	1147	G[263]	-5523	157
968	S[151]	-2975	253	1028	S[91]	-3815	253	1088	S[31]	-4655	253	1148	G[261]	-5537	253
969	S[150]	-2989	61	1029	S[90]	-3829	61	1089	S[30]	-4669	61	1149	G[259]	-5551	61
970	S[149]	-3003	157	1030	S[89]	-3843	157	1090	S[29]	-4683	157	1150	G[257]	-5565	157
971	S[148]	-3017	253	1031	S[88]	-3857	253	1091	S[28]	-4697	253	1151	G[255]	-5579	253
972	S[147]	-3031	61	1032	S[87]	-3871	61	1092	S[27]	-4711	61	1152	G[253]	-5593	61
973	S[146]	-3045	157	1033	S[86]	-3885	157	1093	S[26]	-4725	157	1153	G[251]	-5607	157
974	S[145]	-3059	253	1034	S[85]	-3899	253	1094	S[25]	-4739	253	1154	G[249]	-5621	253
975	S[144]	-3073	61	1035	S[84]	-3913	61	1095	S[24]	-4753	61	1155	G[247]	-5635	61
976	S[143]	-3087	157	1036	S[83]	-3927	157	1096	S[23]	-4767	157	1156	G[245]	-5649	157
977	S[142]	-3101	253	1037	S[82]	-3941	253	1097	S[22]	-4781	253	1157	G[243]	-5663	253
978	S[141]	-3115	61	1038	S[81]	-3955	61	1098	S[21]	-4795	61	1158	G[241]	-5677	61
979	S[140]	-3129	157	1039	S[80]	-3969	157	1099	S[20]	-4809	157	1159	G[239]	-5691	157
980	S[139]	-3143	253	1040	S[79]	-3983	253	1100	S[19]	-4823	253	1160	G[237]	-5705	253
981	S[138]	-3157	61	1041	S[78]	-3997	61	1101	S[18]	-4837	61	1161	G[235]	-5719	61
982	S[137]	-3171	157	1042	S[77]	-4011	157	1102	S[17]	-4851	157	1162	G[233]	-5733	157
983	S[136]	-3185	253	1043	S[76]	-4025	253	1103	S[16]	-4865	253	1163	G[231]	-5747	253
984	S[135]	-3199	61	1044	S[75]	-4039	61	1104	S[15]	-4879	61	1164	G[229]	-5761	61
985	S[134]	-3213	157	1045	S[74]	-4053	157	1105	S[14]	-4893	157	1165	G[227]	-5775	157
986	S[133]	-3227	253	1046	S[73]	-4067	253	1106	S[13]	-4907	253	1166	G[225]	-5789	253
987	S[132]	-3241	61	1047	S[72]	-4081	61	1107	S[12]	-4921	61	1167	G[223]	-5803	61
988	S[131]	-3255	157	1048	S[71]	-4095	157	1108	S[11]	-4935	157	1168	G[221]	-5817	157
989	S[130]	-3269	253	1049	S[70]	-4109	253	1109	S[10]	-4949	253	1169	G[219]	-5831	253
990	S[129]	-3283	61	1050	S[69]	-4123	61	1110	S[9]	-4963	61	1170	G[217]	-5845	61
991	S[128]	-3297	157	1051	S[68]	-4137	157	1111	S[8]	-4977	157	1171	G[215]	-5859	157
992	S[127]	-3311	253	1052	S[67]	-4151	253	1112	S[7]	-4991	253	1172	G[213]	-5873	253
993	S[126]	-3325	61	1053	S[66]	-4165	61	1113	S[6]	-5005	61	1173	G[211]	-5887	61
994	S[125]	-3339	157	1054	S[65]	-4179	157	1114	S[5]	-5019	157	1174	G[209]	-5901	157
995	S[124]	-3353	253	1055	S[64]	-4193	253	1115	S[4]	-5033	253	1175	G[207]	-5915	253
996	S[123]	-3367	61	1056	S[63]	-4207	61	1116	S[3]	-5047	61	1176	G[205]	-5929	61
997	S[122]	-3381	157	1057	S[62]	-4221	157	1117	S[2]	-5061	157	1177	G[203]	-5943	157
998	S[121]	-3395	253	1058	S[61]	-4235	253	1118	S[1]	-5075	253	1178	G[201]	-5957	253
999	S[120]	-3409	61	1059	S[60]	-4249	61	1119	G[319]	-5131	61	1179	G[199]	-5971	61
1000	S[119]	-3423	157	1060	S[59]	-4263	157	1120	G[317]	-5145	157	1180	G[197]	-5985	157
1001	S[118]	-3437	253	1061	S[58]	-4277	253	1121	G[315]	-5159	253	1181	G[195]	-5999	253
1002	S[117]	-3451	61	1062	S[57]	-4291	61	1122	G[313]	-5173	61	1182	G[193]	-6013	61
1003	S[116]	-3465	157	1063	S[56]	-4305	157	1123	G[311]	-5187	157	1183	G[191]	-6027	157
1004	S[115]	-3479	253	1064	S[55]	-4319	253	1124	G[309]	-5201	253	1184	G[189]	-6041	253
1005	S[114]	-3493	61	1065	S[54]	-4333	61	1125	G[307]	-5215	61	1185	G[187]	-6055	61
1006	S[113]	-3507	157	1066	S[53]	-4347	157	1126	G[305]	-5229	157	1186	G[185]	-6069	157
1007	S[112]	-3521	253	1067	S[52]	-4361	253	1127	G[303]	-5243	253	1187	G[183]	-6083	253
1008	S[111]	-3535	61	1068	S[51]	-4375	61	1128	G[301]	-5257	61	1188	G[181]	-6097	61
1009	S[110]	-3549	157	1069	S[50]	-4389	157	1129	G[299]	-5271	157	1189	G[179]	-6111	157
1010	S[109]	-3563	253	1070	S[49]	-4403	253	1130	G[297]	-5285	253	1190	G[177]	-6125	253
1011	S[108]	-3577	61	1071	S[48]	-4417	61	1131	G[295]	-5299	61	1191	G[175]	-6139	61
1012	S[107]	-3591	157	1072	S[47]	-4431	157	1132	G[293]	-5313	157	1192	G[173]	-6153	157
1013	S[106]	-3605	253	1073	S[46]	-4445	253	1133	G[291]	-5327	253	1193	G[171]	-6167	253
1014	S[105]	-3619	61	1074	S[45]	-4459	61	1134	G[289]	-5341	61	1194	G[169]	-6181	61
1015	S[104]	-3633	157	1075	S[44]	-4473	157	1135	G[287]	-5355	157	1195	G[167]	-6195	157
1016	S[103]	-3647	253	1076	S[43]	-4487	253	1136	G[285]	-5369	253	1196	G[165]	-6209	253
1017	S[102]	-3661	61	1077	S[42]	-4501	61	1137	G[283]	-5383	61	1197	G[163]	-6223	61
1018	S[101]	-3675	157	1078	S[41]	-4515	157	1138	G[281]	-5397	157	1198	G[161]	-6237	157
1019	S[100]	-3689	253	1079	S[40]	-4529	253	1139	G[279]	-5411	253	1199	G[159]	-6251	253
1020	S[99]	-3703	61	1080	S[39]	-4543	61	1140	G[277]	-5425	61	1200	G[157]	-6265	61

No.	Pad name	X	Y
1201	G[155]	-6279	157
1202	G[153]	-6293	253
1203	G[151]	-6307	61
1204	G[149]	-6321	157
1205	G[147]	-6335	253
1206	G[145]	-6349	61
1207	G[143]	-6363	157
1208	G[141]	-6377	253
1209	G[139]	-6391	61
1210	G[137]	-6405	157
1211	G[135]	-6419	253
1212	G[133]	-6433	61
1213	G[131]	-6447	157
1214	G[129]	-6461	253
1215	G[127]	-6475	61
1216	G[125]	-6489	157
1217	G[123]	-6503	253
1218	G[121]	-6517	61
1219	G[119]	-6531	157
1220	G[117]	-6545	253
1221	G[115]	-6559	61
1222	G[113]	-6573	157
1223	G[111]	-6587	253
1224	G[109]	-6601	61
1225	G[107]	-6615	157
1226	G[105]	-6629	253
1227	G[103]	-6643	61
1228	G[101]	-6657	157
1229	G[99]	-6671	253
1230	G[97]	-6685	61
1231	G[95]	-6699	157
1232	G[93]	-6713	253
1233	G[91]	-6727	61
1234	G[89]	-6741	157
1235	G[87]	-6755	253
1236	G[85]	-6769	61
1237	G[83]	-6783	157
1238	G[81]	-6797	253
1239	G[79]	-6811	61
1240	G[77]	-6825	157
1241	G[75]	-6839	253
1242	G[73]	-6853	61
1243	G[71]	-6867	157
1244	G[69]	-6881	253
1245	G[67]	-6895	61
1246	G[65]	-6909	157
1247	G[63]	-6923	253
1248	G[61]	-6937	61
1249	G[59]	-6951	157
1250	G[57]	-6965	253
1251	G[55]	-6979	61
1252	G[53]	-6993	157
1253	G[51]	-7007	253
1254	G[49]	-7021	61
1255	G[47]	-7035	157
1256	G[45]	-7049	253
1257	G[43]	-7063	61
1258	G[41]	-7077	157
1259	G[39]	-7091	253
1260	G[37]	-7105	61

No.	Pad name	X	Y
1261	G[35]	-7119	157
1262	G[33]	-7133	253
1263	G[31]	-7147	61
1264	G[29]	-7161	157
1265	G[27]	-7175	253
1266	G[25]	-7189	61
1267	G[23]	-7203	157
1268	G[21]	-7217	253
1269	G[19]	-7231	61
1270	G[17]	-7245	157
1271	G[15]	-7259	253
1272	G[13]	-7273	61
1273	G[11]	-7287	157
1274	G[9]	-7301	253
1275	G[7]	-7315	61
1276	G[5]	-7329	157
1277	G[3]	-7343	253
1278	G[1]	-7357	61
1279	DUMMY	-7371	157
1280	DUMMY	-7385	253
1281	DUMMY	-7399	61

Alignment mark	X	Y
A1	-7377.5	-247.5
A2	7377.5	-247.5

BUMP Size

Input Pad	
Output Pad	

6. Block Function Description

MCU System Interface

ILI9338B provides four kinds of MCU system interface with 8080-series parallel interface and 3-/4-line serial interface. The selection of the given interfaces are done by external IM [3:0] pins and shown as below:

IM3	IM2	IM1	IM0	MPU-Interface Mode	Data Pin in use	
					Register / Content	GRAM
0	0	0	0	8080 MCU 16-bits Parallel type Ⅰ	D7-D0	D[15:0]：16-bit data
0	0	0	1	8080 MCU 8-bits Parallel type Ⅰ	D7-D0	D[7:0]：8-bit data
0	0	1	0	8080 MCU 16-bits Parallel type Ⅱ	D8-D1	D[17:10]、D[8:1]：16-bit data
0	0	1	1	8080 MCU 8-bits Parallel type Ⅱ	D17-D10	D[17:10]：8-bit data
0	1	0	ID	3-wire Serial interface	SDA	
1	0	0	0	8080 MCU 18-bits Parallel type Ⅰ	D7-D0	D[17:0]：18-bit data
1	0	0	1	8080 MCU 9-bits Parallel type Ⅰ	D7-D0	D[8:0]：9-bit data
1	0	1	0	8080 MCU 18-bits Parallel type Ⅱ	D8-D1	D[17:0]：18-bit data
1	0	1	1	8080 MCU 9-bits Parallel type Ⅱ	D17-D10	D[17:9]：9-bit data
0	1	1	X	4-wire Serial interface	SDA	
If not used, please fix this pin to VDDI or DGND level						

In 8080-series parallel interface, the registers are accessed by the D[7:0] data pins.

8080-Series				Operation
CSX	D/CX	RDX	WRX	
"L"	"L"	"H"	↑	Write command
"L"	"H"	↑	"H"	Read parameter
"L"	"H"	"H"	↑	Write parameter

Parallel RGB Interface

ILI9338B also supports the RGB interface for displaying a moving picture. When the RGB interface is selected, display operation is synchronized with externally signals, VSYNC, HSYNC, and DOTCLK and input display data is written in synchronization with these signals according to the polarity of enable signal (DE).

Graphic RAM (GRAM)

GRAM is a graphic RAM to store display data. GRAM size is 172,800 bytes with 18 bits per pixel for a maximum 240(RGB) x320 dot graphic display.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a liquid crystal drive voltage, which corresponds to grayscale level set in the gamma correction register. ILI9338B can display maximum 262,144 colors.

Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels as VREG1OUT, VGH, VGL and VCOM for

driving TFT LCD panel.

Timing controller

The timing controller generates all the timing signals for display and GRAM access.

Oscillator

ILI9338B incorporates RC oscillator circuit and output a stable output frequency for operation.

Panel Driver Circuit

Liquid crystal display driver circuit consists of 720-output source driver (S1~S720), 320-output gate driver (G1~G320), and VCOM signal.

7. Function Description

7.1. MCU interfaces

ILI9338B provides the 8-/9-/16-/18-bit parallel system interface for 8080 series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins as IM [3:0] and the bit formal per pixel color order is selected by DBI [2:0] bits of 3Ah register.

7.1.1. MCU interface selection

The selection of interface is done by setting external pins IM [3:0] as shown in the following table.

IM3	IM2	IM1	IM0	MPU-Interface Mode	Pins in use
0	0	0	0	8080 MCU 16-bits Parallel type Ⅰ	D[15:0], WRX, RDX, CSX, D/CX
0	0	0	1	8080 MCU 8-bits Parallel type Ⅰ	D[7:0] , WRX, RDX, CSX, D/CX
0	0	1	0	8080 MCU 16-bits Parallel type Ⅱ	D[8:1]、D[17:10] , WRX, RDX, CSX, D/CX
0	0	1	1	8080 MCU 8-bits Parallel type Ⅱ	D[17:10] , WRX, RDX, CSX, D/CX
0	1	X	X	3-line Serial interface	SCL,SDA,CSX
1	0	0	0	8080 MCU 18-bits Parallel type Ⅰ	D[17:0] , WRX, RDX, CSX, D/CX
1	0	0	1	8080 MCU 9-bits Parallel type Ⅰ	D[8:0] , WRX, RDX, CSX, D/CX
1	0	1	0	8080 MCU 18-bits Parallel type Ⅱ	D[17:0] , WRX, RDX, CSX, D/CX
1	0	1	1	8080 MCU 9-bits Parallel type Ⅱ	D[17:9] , WRX, RDX, CSX, D/CX
1	1	X	X	4-line serial interface	SCL,SDA,CSX,D/CX
If not used, please fix this pin to VDDI or DGND level					

7.1.2. 8080-Series Parallel Interface

ILI9338B can be accessed via 8-/9-/16-/18-bit MCU 8080-series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9338B chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

ILI9338B latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D [17:0] bits are commands.

The 8080-series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080-interface selection is done when IM3 pin is low state (DGND level). Interface bus width can be selected by IM [2:0] bits.

The selection of 8080-series parallel interface is shown as the table in the following.

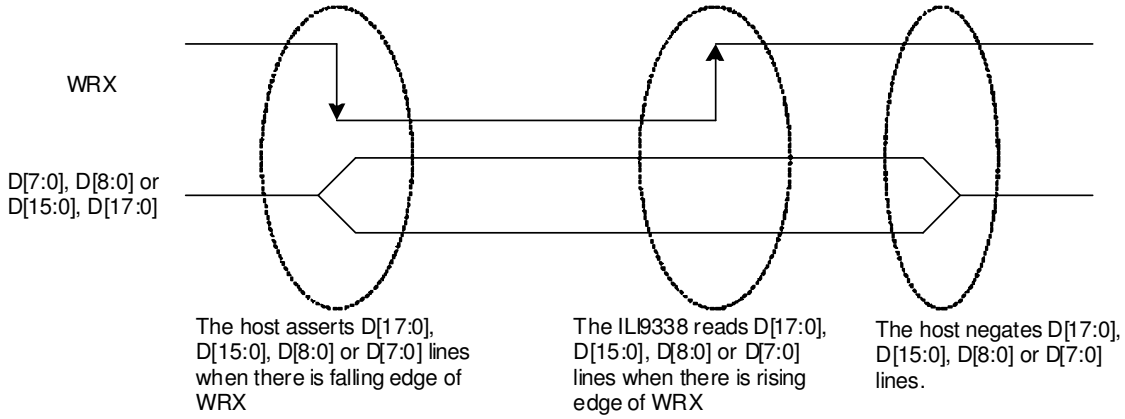
IM3	IM2	IM1	IM0	MPU-Interface Mode	WRX	RDX	D/CX	Function
0	0	0	0	8080 MCU 16-bits Parallel type Ⅰ	↑	"H"	"L"	Write command code.
					"H"	↑	"H"	Read internal status.
					↑	"H"	"H"	Write parameter or display data.
					"H"	↑	"H"	Reads parameter or display data.
0	0	0	1	8080 MCU 8-bits Parallel type Ⅰ	↑	"H"	"L"	Write command code.
					"H"	↑	"H"	Read internal status.
					↑	"H"	"H"	Write parameter or display data.
					"H"	↑	"H"	Reads parameter or display data.
0	0	1	0	8080 MCU 16-bits Parallel type Ⅱ	↑	"H"	"L"	Write command code.
					"H"	↑	"H"	Read internal status.
					↑	"H"	"H"	Write parameter or display data.
					"H"	↑	"H"	Reads parameter or display data.
0	0	1	1	8080 MCU 8-bits Parallel type Ⅱ	↑	"H"	"L"	Write command code.
					"H"	↑	"H"	Read internal status.
					↑	"H"	"H"	Write parameter or display data.
					"H"	↑	"H"	Reads parameter or display data.
1	0	0	0	8080 MCU 18-bits Parallel type Ⅰ	↑	"H"	"L"	Write command code.
					"H"	↑	"H"	Read internal status.
					↑	"H"	"H"	Write parameter or display data.
					"H"	↑	"H"	Reads parameter or display data.
1	0	0	1	8080 MCU 9-bits Parallel type Ⅰ	↑	"H"	"L"	Write command code.
					"H"	↑	"H"	Read internal status.
					↑	"H"	"H"	Write parameter or display data.
					"H"	↑	"H"	Reads parameter or display data.
1	0	1	0	8080 MCU 18-bits Parallel type Ⅱ	↑	"H"	"L"	Write command code.
					"H"	↑	"H"	Read internal status.

					↑	“H”	“H”	Write parameter or display data.
					“H”	↑	“H”	Reads parameter or display data.
1	0	1	1	8080 MCU 9-bits Parallel type Ⅱ	↑	“H”	“L”	Write command code.
					“H”	↑	“H”	Read internal status.
					↑	“H”	“H”	Write parameter or display data.
					“H”	↑	“H”	Reads parameter or display data.

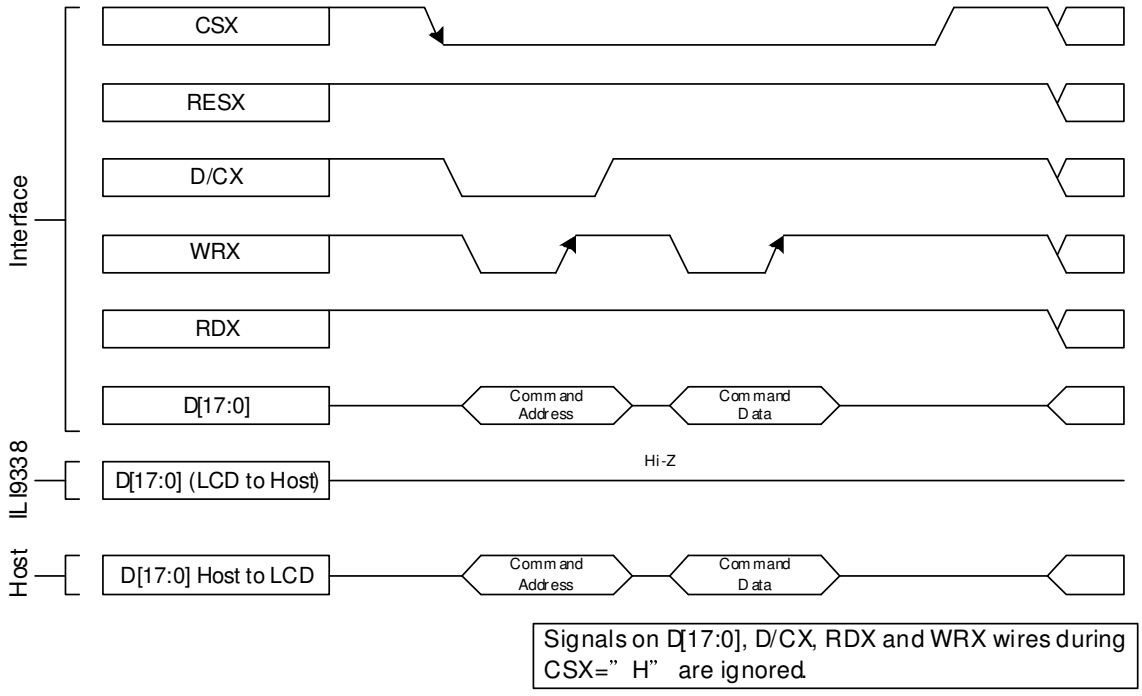
7.1.3. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080 MCU interface.



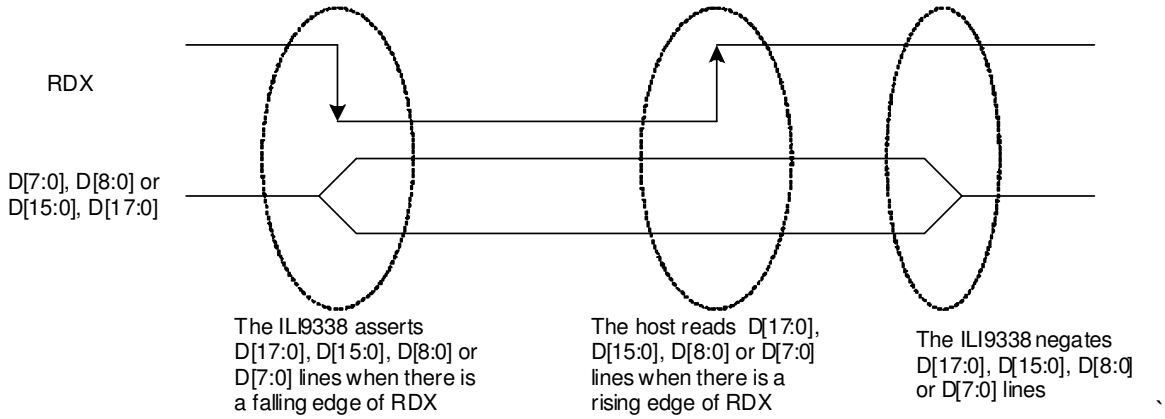
Note: WRX is an unsynchronized signal (It can be stopped)



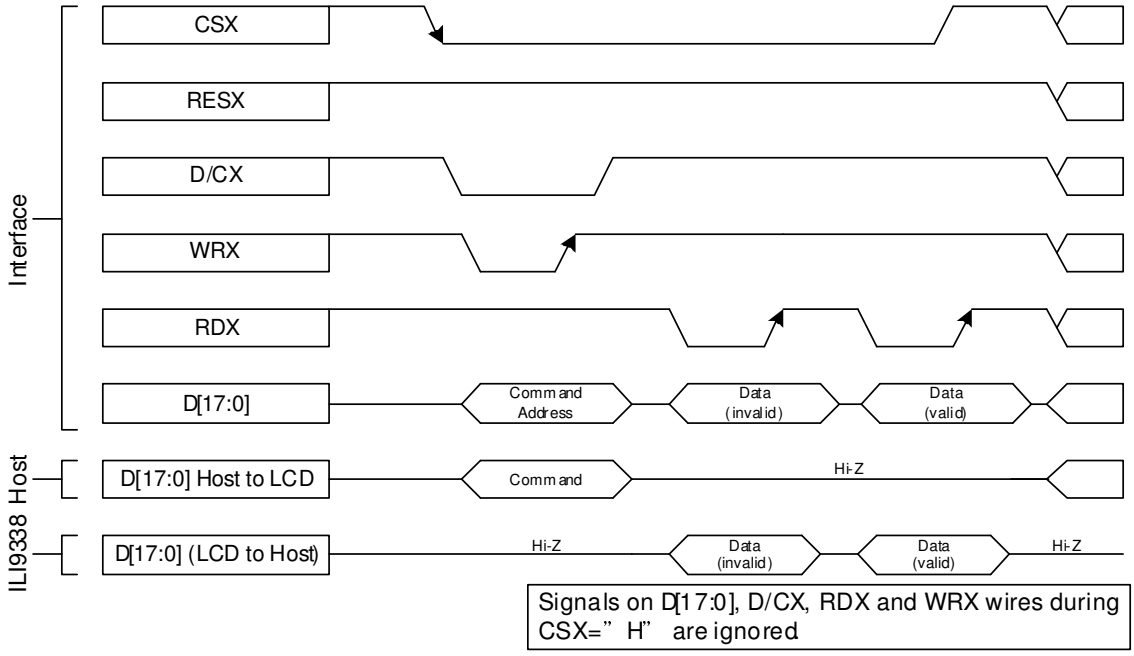
7.1.4. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080 MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

7.1.5. Serial Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

IM3	IM2	IM1	IM0	MPU-Interface Mode	CSX	D/CX	SCL	Function
0	1	0	ID	3-line serial interface	"L"	"L"	⎍	Read/Write command, parameter or display data.
1	1	1	X	4-line serial interface	"L"	"L"/"H"	⎍	Read/Write command, parameter or display data.

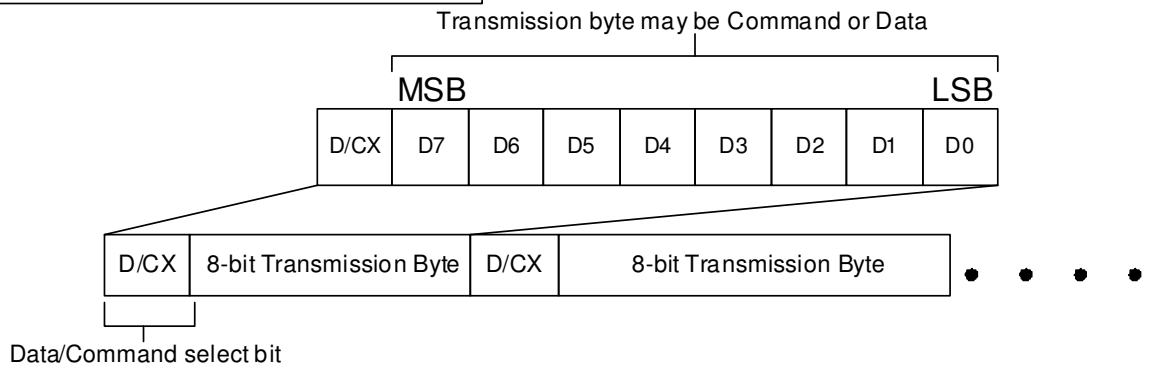
ILI9338B supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and ILI9338B. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA). The 4-line serial mode consists of the Data/Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA) for data transmission. The data bus (D [17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

7.1.6. Write Cycle Sequence

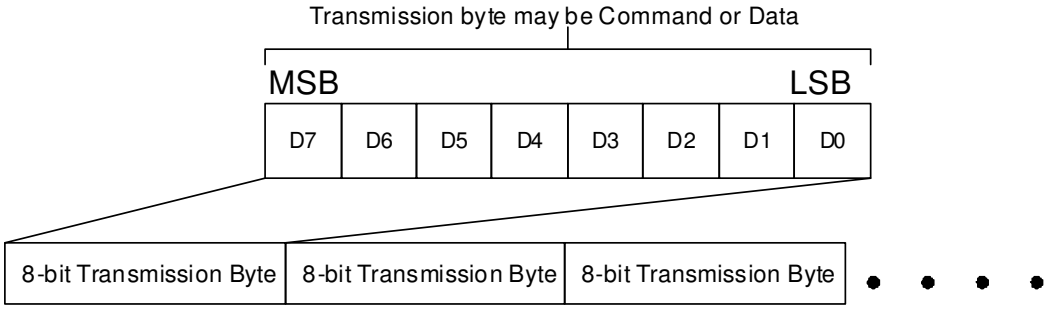
The write mode of the interface means that host writes commands or data to ILI9338B. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is "low", the transmission byte is interpreted as a command byte. If the D/CX bit is "high", the transmission byte is stored as the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to ILI9338B and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.

Data Format for 3-line Serial Interface

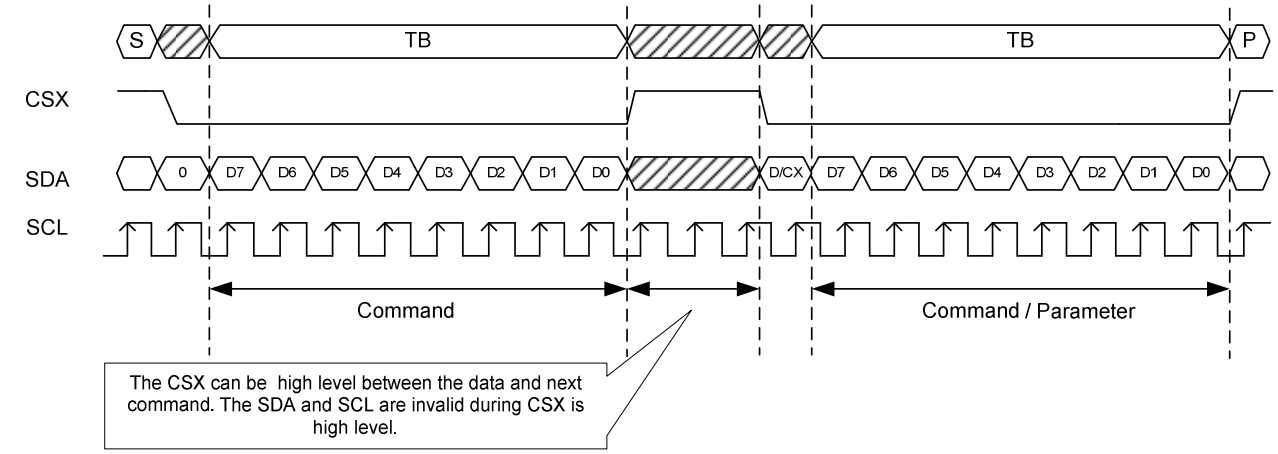


Data Format for 4-line Serial Interface

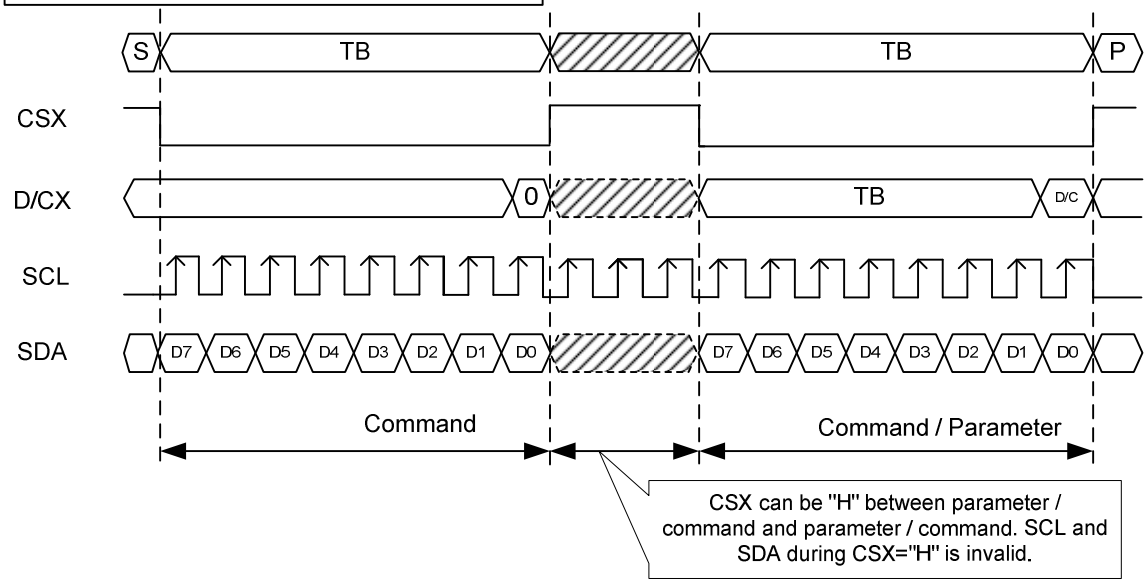


Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by ILI9338B on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

3-line Serial Interface Protocol



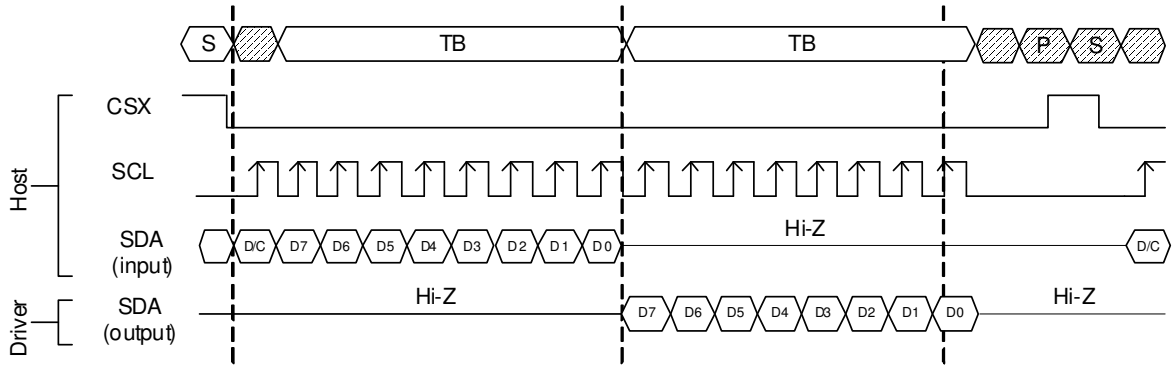
4-line Serial Interface Protocol



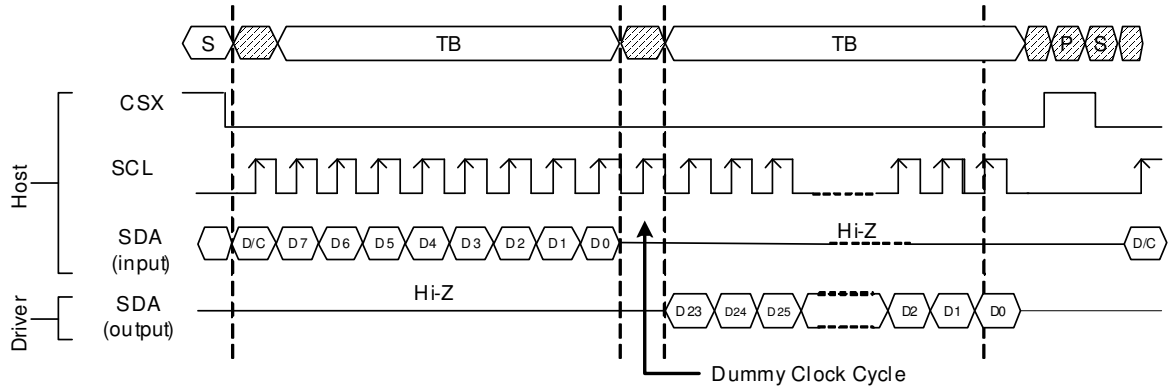
7.1.7. Read Cycle Sequence

The read mode of interface means that the host reads register's parameter or display data from ILI9338B. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. ILI9338B latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

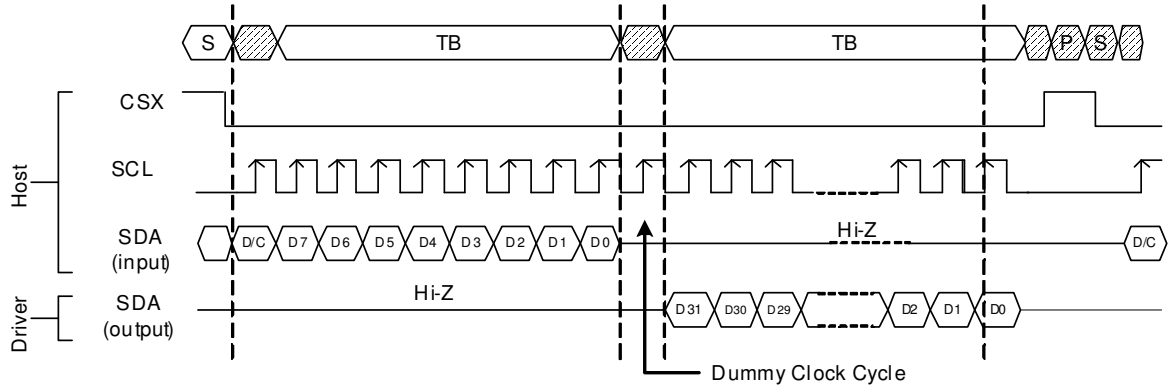
3-line Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



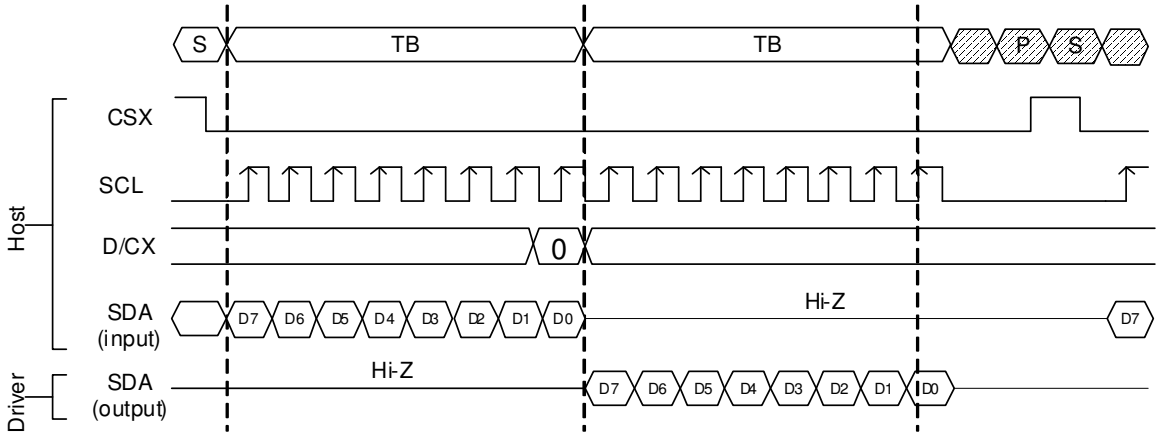
3-line Serial Protocol (for RDDID command: 24-bit read)



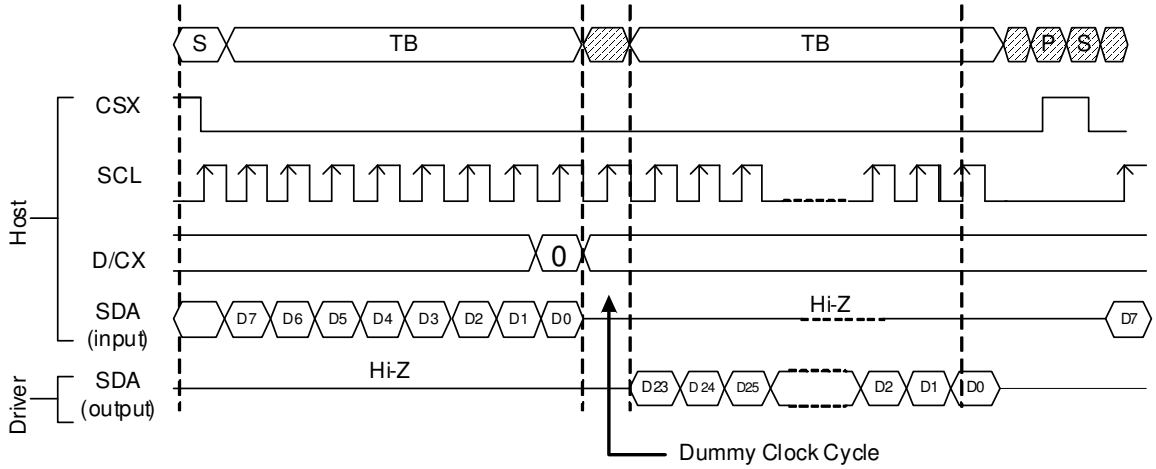
3-line Serial Protocol (for RDDST command: 32-bit read)



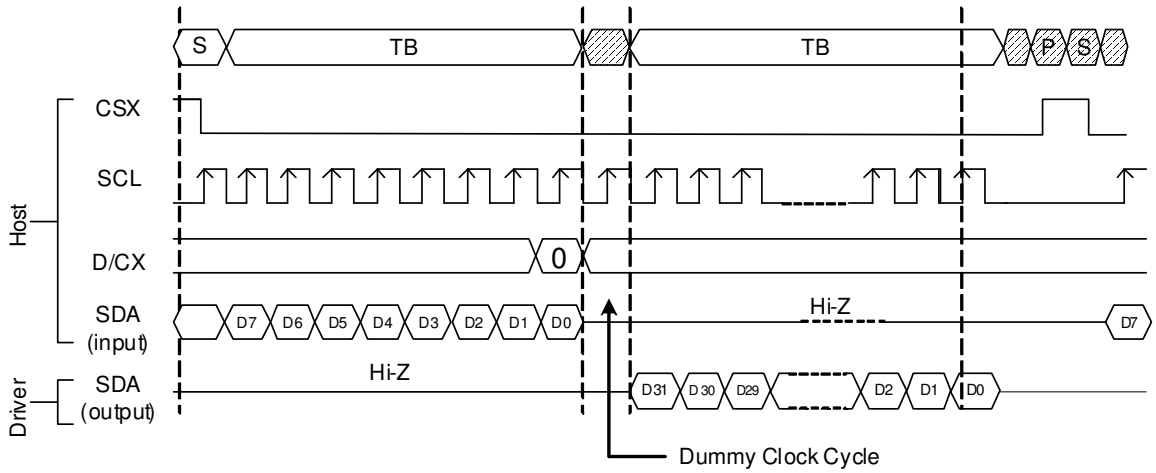
4-line Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



4-line Serial Protocol (for RDDID command: 24-bit read)

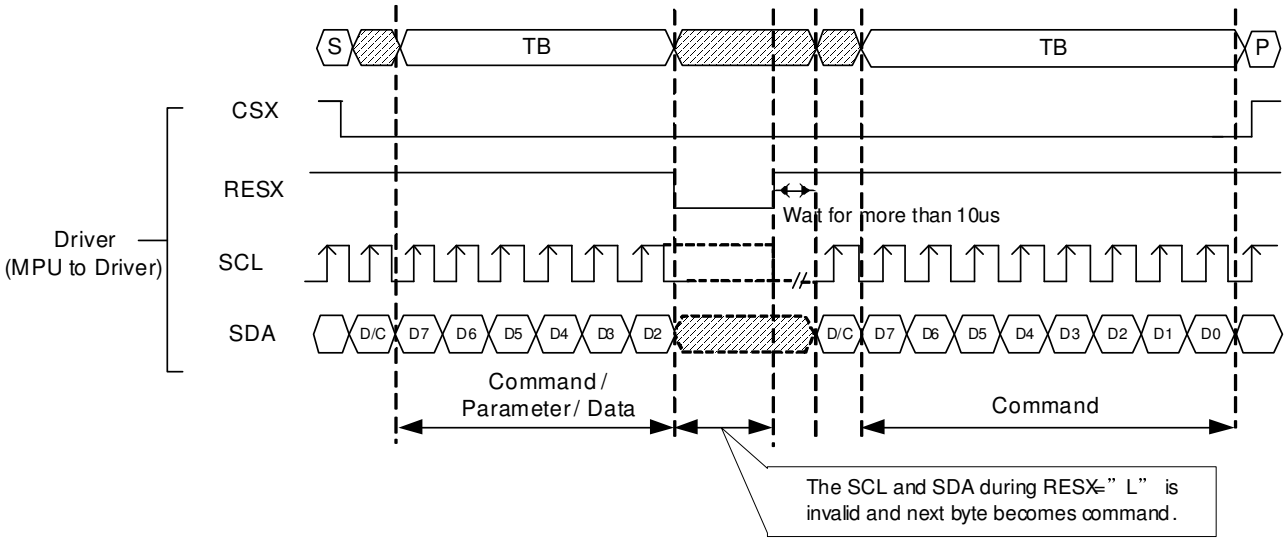


4-line Serial Protocol (for RDDST command: 32-bit read)

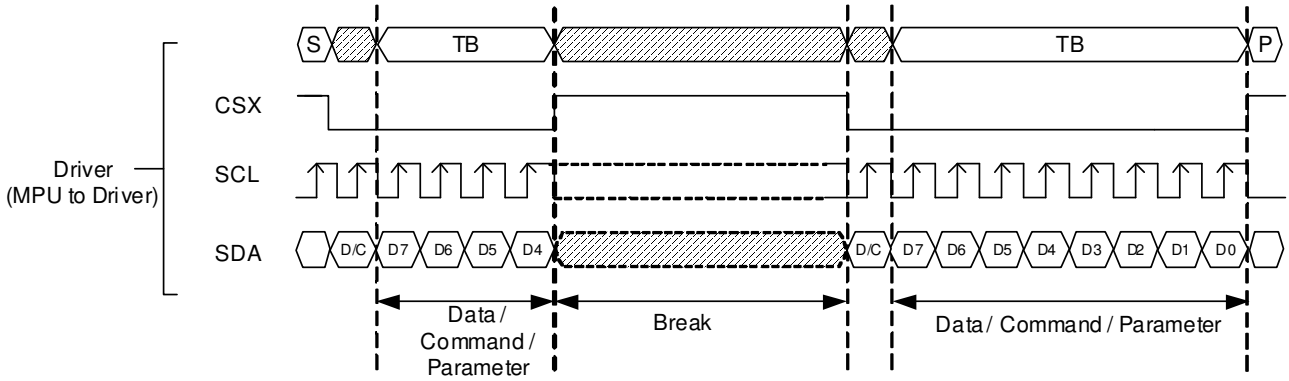


7.1.8. Data Transfer Break and Recovery

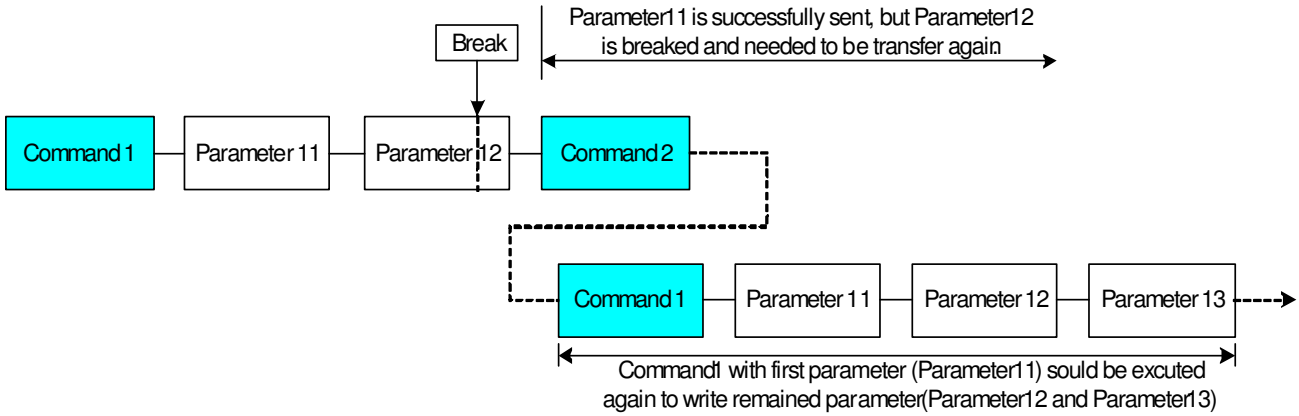
If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.



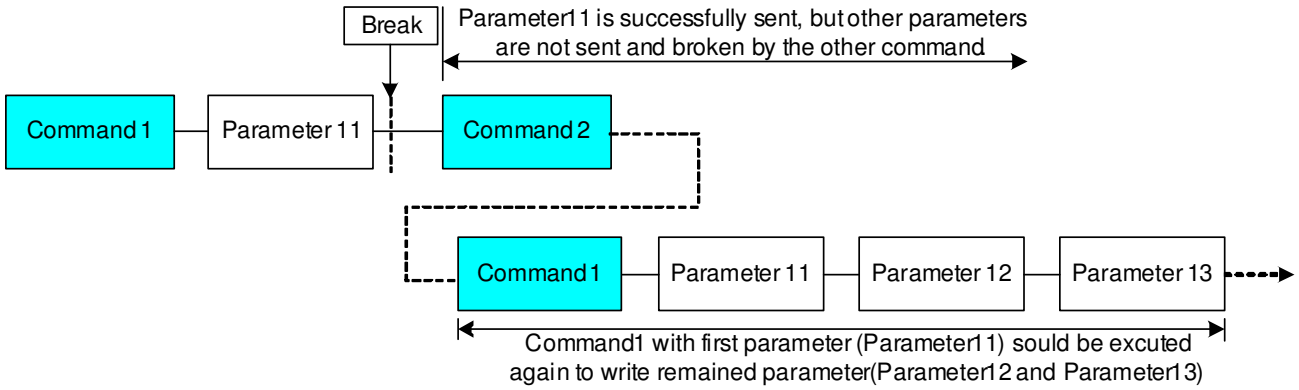
If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.



If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.

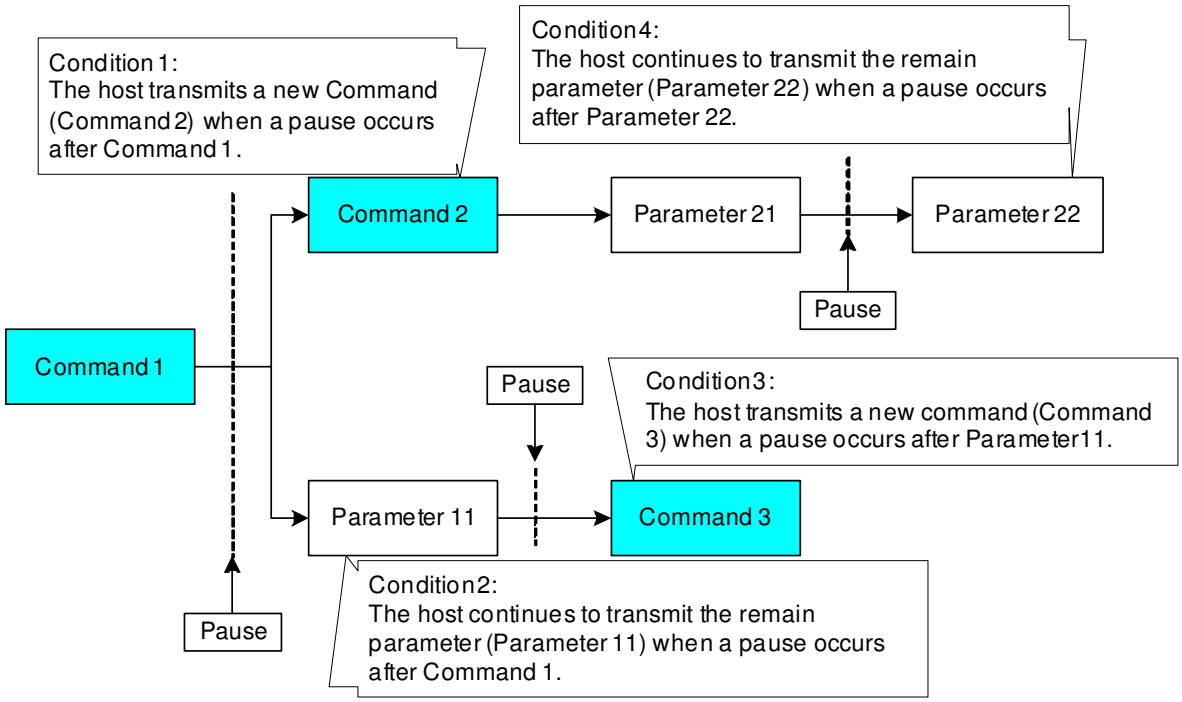


7.1.9. Data Transfer Pause

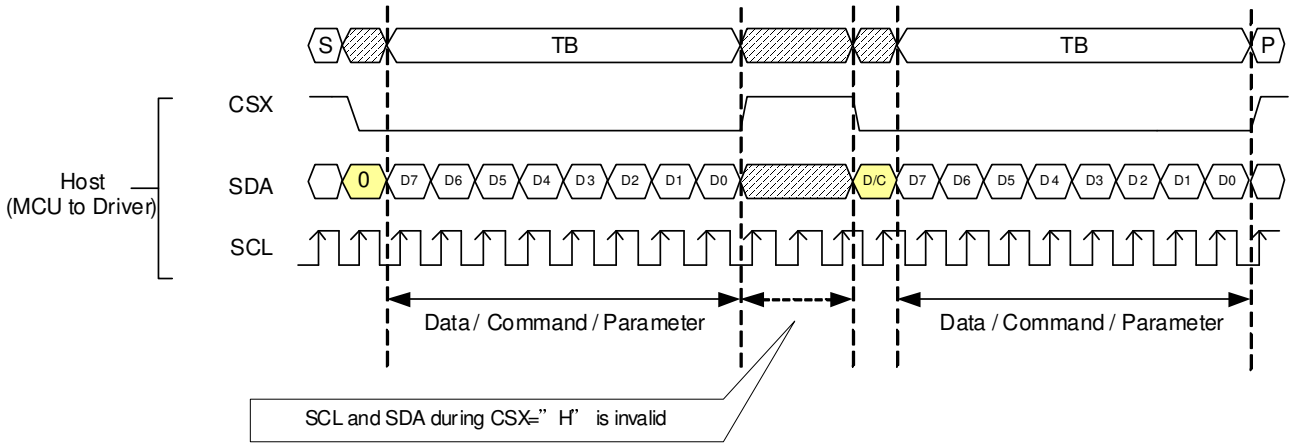
It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then ILI9338B will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select pin is next enabled as shown below.

This applies to the following 4 conditions:

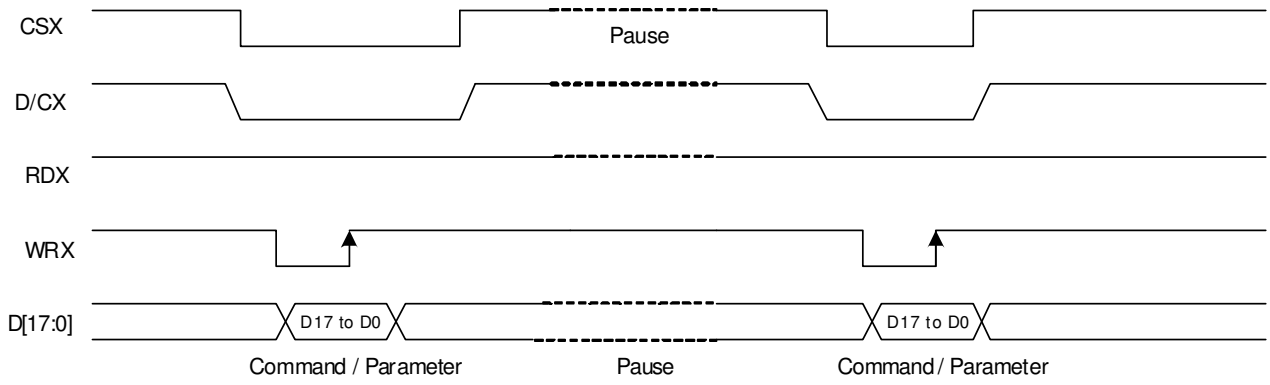
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter



7.1.10. Serial Interface Pause



7.1.11. Parallel Interface Pause

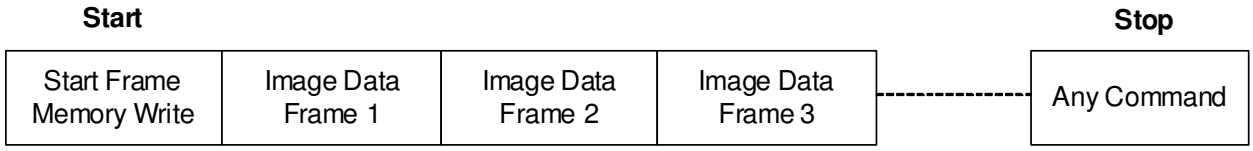


7.1.12. Data Transfer Mode

ILI9338B can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

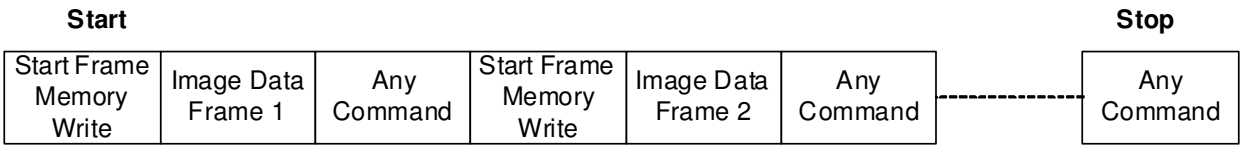
7.1.13. Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.



7.1.14. Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

7.2. RGB Interface

7.2.1. RGB Interface Selection

ILI9338B has two kinds of RGB interface and these interfaces can be selected by external RCM [1:0] pins. When RCM [1:0] bits are set to “10”, the DE mode is selected which utilizes VSYNC, HSYNC, DOTCLK, DE, D [17:0] pins; when RCM [1:0] bits are set to “11”, the SYNC mode is selected which utilizes which utilizes VSYNC, HSYNC, DOTCLK, D [17:0] pins.

ILI9338B supports several pixel formats that can be selected by DPI [3:0] bits of “Pixel Format Set (3Ah)” command. The selection of a given interfaces is done by setting RCM [1:0] and DPI [3:0] as show in the following table.

RCM[1:0]		DPI[3:0]				RGB Interface Mode	RGB Mode	Used Pins
1	0	0	1	1	0	18-bit RGB interface	**DE Mode** Valid data is determined by the DE signal	VSYNC, HSYNC, DE, DOTCLK, D[17:0]
1	0	0	1	0	1	16-bit RGB interface		VSYNC, HSYNC, DE, DOTCLK, D[17:13] & D[11:1]
1	0	1	1	1	0	6-bitRGB interface		VSYNC, HSYNC, DE, DOTCLK, D[7:2]
1	1	0	1	1	0	18-bit RGB interface	**SYNC Mode** In SYNC mode, DE signal is ignored; blanking porch is determined by B5h command.	VSYNC, HSYNC, DOTCLK, D[17:0]
1	1	0	1	0	1	16-bit RGB interface		VSYNC, HSYNC, DOTCLK, D[17:13] & D[11:1]
1	1	1	1	1	0	6-bitRGB interface		VSYNC, HSYNC, DOTCLK, D[7:2]

Parallel RGB Interface Set Table

18-bit data bus interface (D[17:0] is used) , DPI[3:0] = 0110

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

16-bit data bus interface (D[17:13] and D[11:1] are used) , DPI[3:0] = 0101

	D17	D16	D15	D14	D13	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
16bpp Frame Memory Write	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

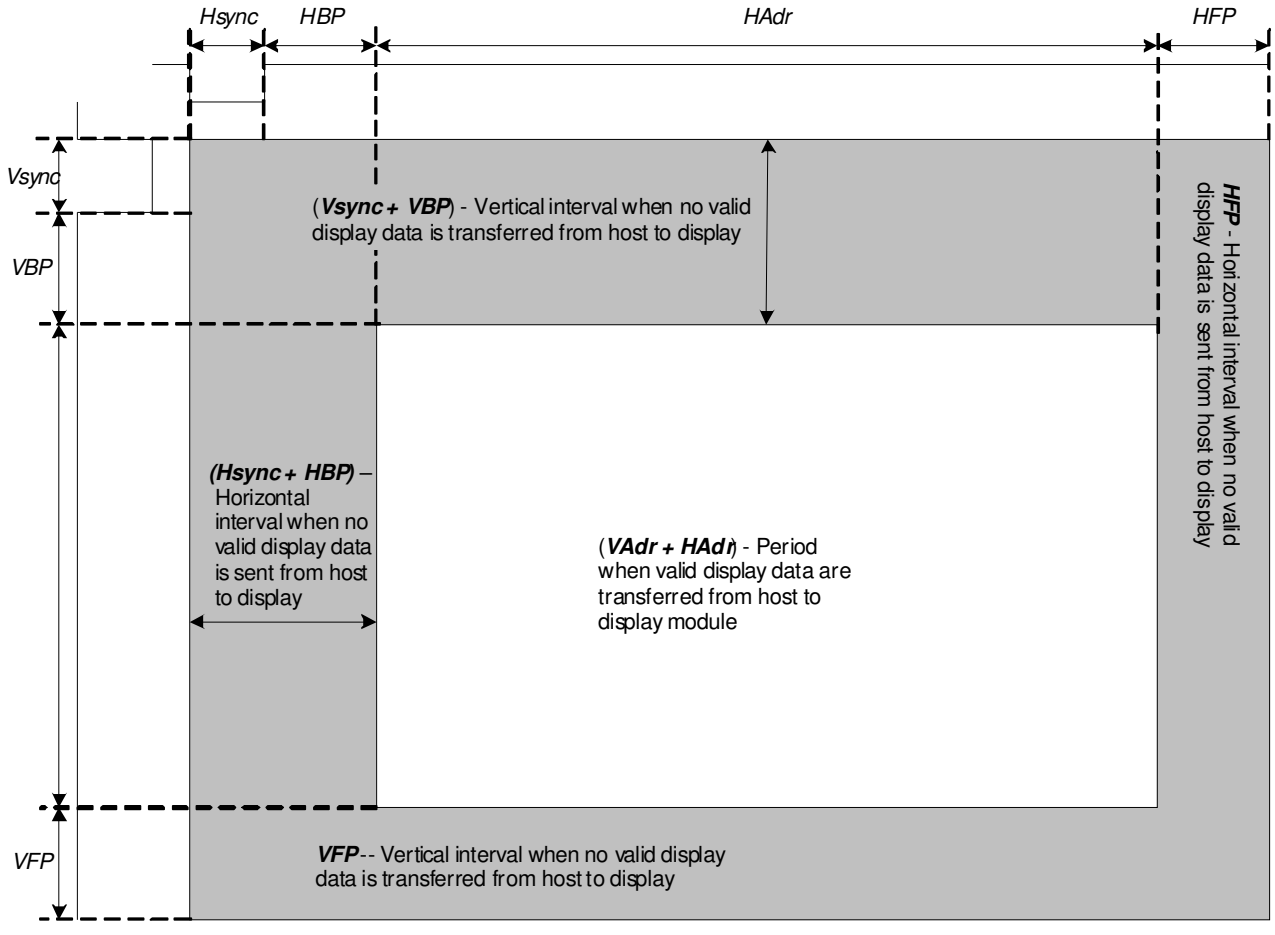
6-bit data bus interface (D[7:2] is used) , DPI[3:0] = 1110

	First Transfer						Second Transfer						Third Transfer					
	D7	D6	D5	D4	D3	D2	D7	D6	D5	D4	D3	D2	D7	D6	D5	D4	D3	D2
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

Pixel clock (DOTCLK) is running all the time without stopping and used to enter VSYNC, HSYNC, DE and D [17:0] states when there is a rising edge of the DOTCLK. The DOTCLK cannot be used as continues internal clock for other functions of the display module. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

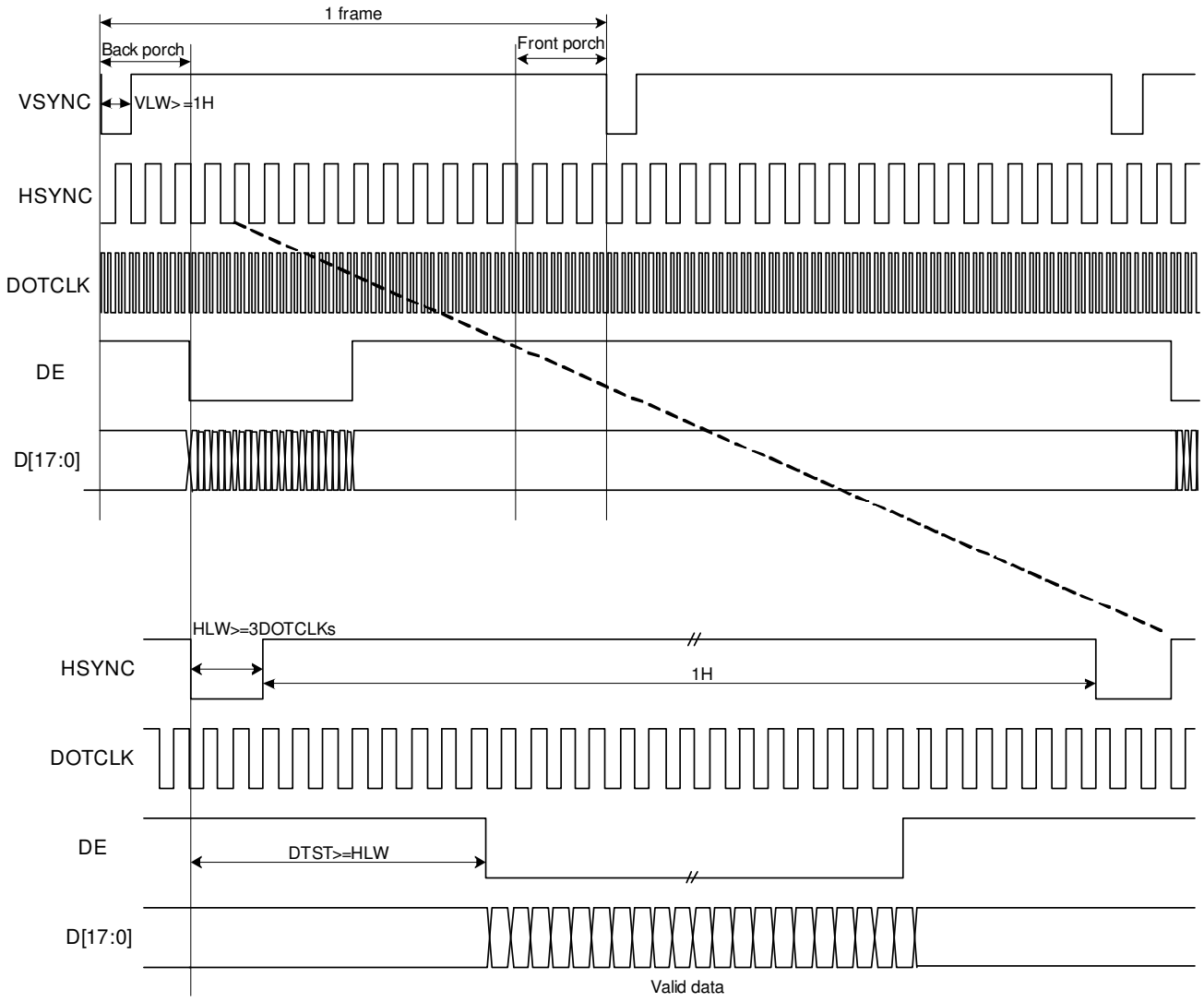
Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

In DE mode, Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal. D [17:0] are used to tell what is the information of the image that is transferred on the display (When DE= '0' (low) and there is a rising edge of DOTCLK). D [17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the DOTCLK signal. In SYNC mode, the valid display data in inputted in pixel unit via D [17:0] according to HFP/HBP settings of HSYNC signal and VFP/VBP setting of VSYNC. In both RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.



7.2.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as below.

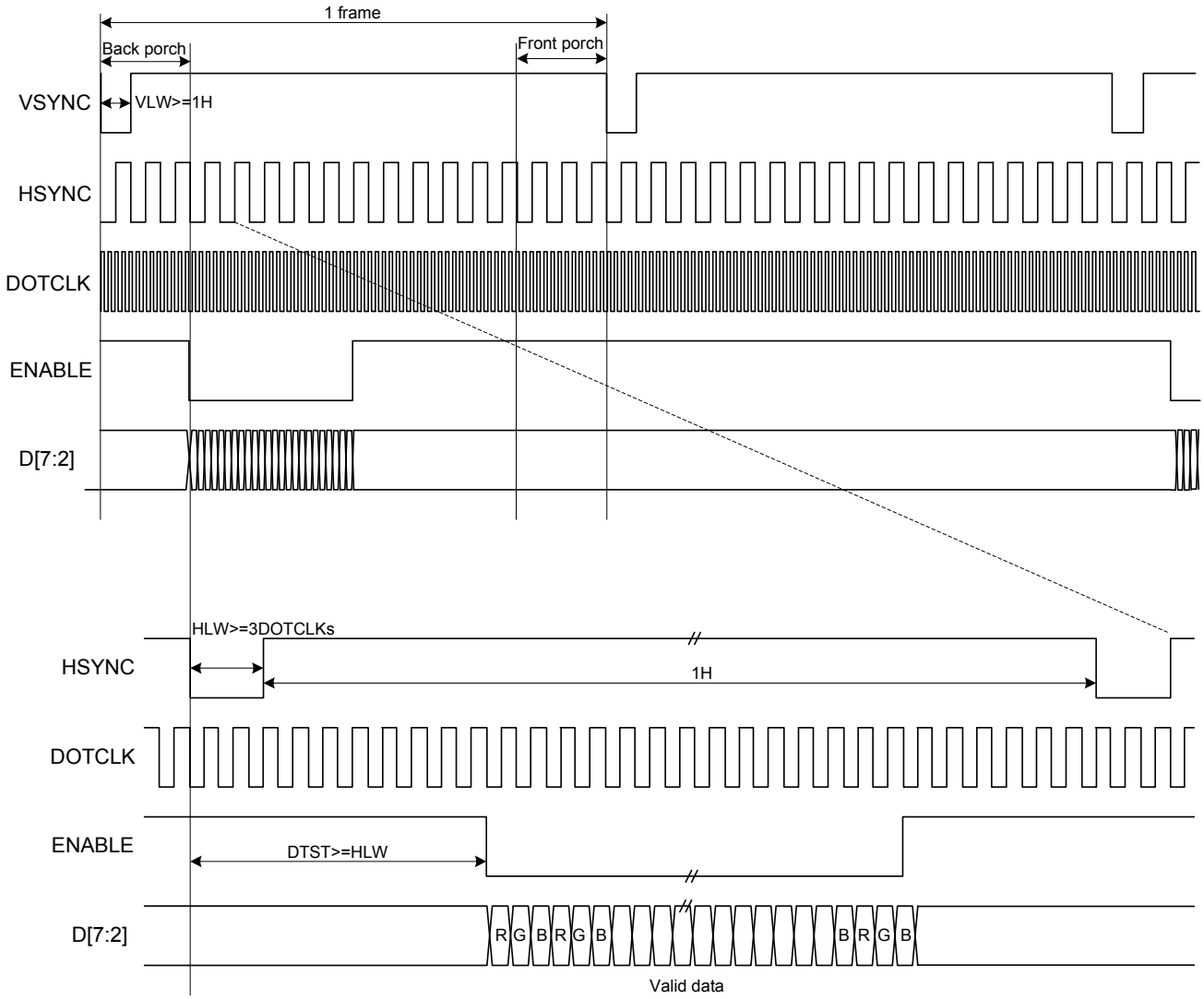


VLW : VSYNC Low Width
HLW : HSYNC Low Width
DTST : Data Transfer Startup Time

Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='1' of "Interface Mode Control (B0h)" command.

The timing chart of 6-bit RGB interface mode is shown as below:



VLW : VSYNC Low Width
HLW : HSYNC Low Width
DTST : Data Transfer Startup Time

Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='1' of "Interface Mode Control (B0h)" command.

Note 3: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.

Note 4: In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and DE to 3 multiples of DOTCLK.

7.3. Color Depth Conversion Look Up Table

When ILI9338B operates in parallel 16-bit interface, the color depth conversion is done by look-up table and extend input data format to 18-bit. See the detail for look-up table of color depth conversion.

R input (5-bit) 16-bit/pixel –mode 65,536 colors	R output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
00000	R_{005} R_{004} R_{003} R_{002} R_{001} R_{000}	1
00001	R_{015} R_{014} R_{013} R_{012} R_{011} R_{010}	2
00010	R_{025} R_{024} R_{023} R_{022} R_{021} R_{020}	3
00011	R_{035} R_{034} R_{033} R_{032} R_{031} R_{030}	4
00100	R_{045} R_{044} R_{043} R_{042} R_{041} R_{040}	5
00101	R_{055} R_{054} R_{053} R_{052} R_{051} R_{050}	6
00110	R_{065} R_{064} R_{063} R_{062} R_{061} R_{060}	7
00111	R_{075} R_{074} R_{073} R_{072} R_{071} R_{070}	8
01000	R_{085} R_{084} R_{083} R_{082} R_{081} R_{080}	9
01001	R_{095} R_{094} R_{093} R_{092} R_{091} R_{090}	10
01010	R_{105} R_{104} R_{103} R_{102} R_{101} R_{100}	11
01011	R_{115} R_{114} R_{113} R_{112} R_{111} R_{110}	12
01100	R_{125} R_{124} R_{123} R_{122} R_{121} R_{120}	13
01101	R_{135} R_{134} R_{133} R_{132} R_{131} R_{130}	14
01110	R_{145} R_{144} R_{143} R_{142} R_{141} R_{140}	15
01111	R_{155} R_{154} R_{153} R_{152} R_{151} R_{150}	16
10000	R_{165} R_{164} R_{163} R_{162} R_{161} R_{160}	17
10001	R_{175} R_{174} R_{173} R_{172} R_{171} R_{170}	18
10010	R_{185} R_{184} R_{183} R_{182} R_{181} R_{180}	19
10011	R_{195} R_{194} R_{193} R_{192} R_{191} R_{190}	20
10100	R_{205} R_{204} R_{203} R_{202} R_{201} R_{200}	21
10101	R_{215} R_{214} R_{213} R_{212} R_{211} R_{210}	22
10110	R_{225} R_{224} R_{223} R_{222} R_{221} R_{220}	23
10111	R_{235} R_{234} R_{233} R_{232} R_{231} R_{230}	24
11000	R_{245} R_{244} R_{243} R_{242} R_{241} R_{240}	25
11001	R_{255} R_{254} R_{253} R_{252} R_{251} R_{250}	26
11010	R_{265} R_{264} R_{263} R_{262} R_{261} R_{260}	27
11011	R_{275} R_{274} R_{273} R_{272} R_{271} R_{270}	28
11100	R_{285} R_{284} R_{283} R_{282} R_{281} R_{280}	29
11101	R_{295} R_{294} R_{293} R_{292} R_{291} R_{290}	30
11110	R_{305} R_{304} R_{303} R_{302} R_{301} R_{300}	31
11111	R_{315} R_{314} R_{313} R_{312} R_{311} R_{310}	32

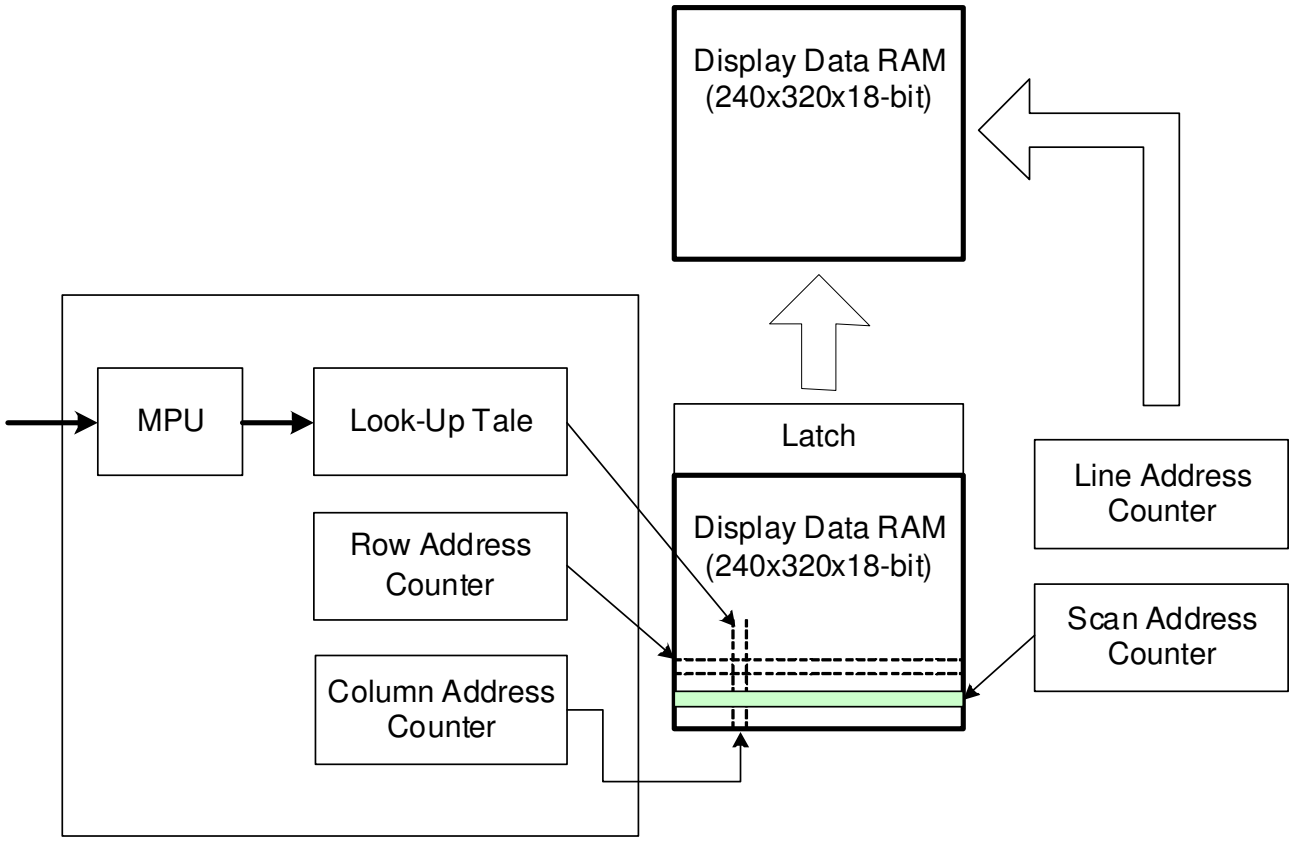
G input (5-bit) 16-bit/pixel –mode 65,536 colors	G output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
000000	G_{005} G_{004} G_{003} G_{002} G_{001} G_{000}	33
000001	G_{015} G_{014} G_{013} G_{012} G_{011} G_{010}	34
000010	G_{025} G_{024} G_{023} G_{022} G_{021} G_{020}	35
000011	G_{035} G_{034} G_{033} G_{032} G_{031} G_{030}	36
000100	G_{045} G_{044} G_{043} G_{042} G_{041} G_{040}	37
000101	G_{055} G_{054} G_{053} G_{052} G_{051} G_{050}	38
000110	G_{065} G_{064} G_{063} G_{062} G_{061} G_{060}	39
000111	G_{075} G_{074} G_{073} G_{072} G_{071} G_{070}	40
001000	G_{085} G_{084} G_{083} G_{082} G_{081} G_{080}	41
001001	G_{095} G_{094} G_{093} G_{092} G_{091} G_{090}	42
001010	G_{105} G_{104} G_{103} G_{102} G_{101} G_{100}	43
001011	G_{115} G_{114} G_{113} G_{112} G_{111} G_{110}	44
001100	G_{125} G_{124} G_{123} G_{122} G_{121} G_{120}	45
001101	G_{135} G_{134} G_{133} G_{132} G_{131} G_{130}	46
001110	G_{145} G_{144} G_{143} G_{142} G_{141} G_{140}	47
001111	G_{155} G_{154} G_{153} G_{152} G_{151} G_{150}	48
010000	G_{165} G_{164} G_{163} G_{162} G_{161} G_{160}	49
010001	G_{175} G_{174} G_{173} G_{172} G_{171} G_{170}	50
010010	G_{185} G_{184} G_{183} G_{182} G_{181} G_{180}	51
010011	G_{195} G_{194} G_{193} G_{192} G_{191} G_{190}	52
010100	G_{205} G_{204} G_{203} G_{202} G_{201} G_{200}	53
010101	G_{215} G_{214} G_{213} G_{212} G_{211} G_{210}	54
010110	G_{225} G_{224} G_{223} G_{222} G_{221} G_{220}	55
010111	G_{235} G_{234} G_{233} G_{232} G_{231} G_{230}	56
011000	G_{245} G_{244} G_{243} G_{242} G_{241} G_{240}	57
011001	G_{255} G_{254} G_{253} G_{252} G_{251} G_{250}	58
011010	G_{265} G_{264} G_{263} G_{262} G_{261} G_{260}	59
011011	G_{275} G_{274} G_{273} G_{272} G_{271} G_{270}	60
011100	G_{285} G_{284} G_{283} G_{282} G_{281} G_{280}	61
011101	G_{295} G_{294} G_{293} G_{292} G_{291} G_{290}	62
011110	G_{305} G_{304} G_{303} G_{302} G_{301} G_{300}	63
011111	G_{315} G_{314} G_{313} G_{312} G_{311} G_{310}	64
100000	G_{325} G_{324} G_{323} G_{322} G_{321} G_{320}	65
100001	G_{335} G_{334} G_{333} G_{332} G_{331} G_{330}	66

G input (5-bit) 16-bit/pixel –mode 65,536 colors	G output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
100010	G_{345} G_{344} G_{343} G_{342} G_{341} G_{340}	67
100011	G_{355} G_{354} G_{353} G_{352} G_{351} G_{350}	68
100100	G_{365} G_{364} G_{363} G_{362} G_{361} G_{360}	69
100101	G_{375} G_{374} G_{373} G_{372} G_{371} G_{370}	70
100110	G_{385} G_{384} G_{383} G_{382} G_{381} G_{380}	71
100111	G_{395} G_{394} G_{393} G_{392} G_{391} G_{390}	72
101000	G_{405} G_{404} G_{403} G_{402} G_{401} G_{400}	73
101001	G_{415} G_{414} G_{413} G_{412} G_{411} G_{410}	74
101010	G_{425} G_{424} G_{423} G_{422} G_{421} G_{420}	75
101011	G_{435} G_{434} G_{433} G_{432} G_{431} G_{430}	76
101100	G_{445} G_{444} G_{443} G_{442} G_{441} G_{440}	77
101101	G_{455} G_{454} G_{453} G_{452} G_{451} G_{450}	78
101110	G_{465} G_{464} G_{463} G_{462} G_{461} G_{460}	79
101111	G_{475} G_{474} G_{473} G_{472} G_{471} G_{470}	80
110000	G_{485} G_{484} G_{483} G_{482} G_{481} G_{480}	81
110001	G_{495} G_{494} G_{493} G_{492} G_{491} G_{490}	82
110010	G_{505} G_{504} G_{503} G_{502} G_{501} G_{500}	83
110011	G_{515} G_{514} G_{513} G_{512} G_{511} G_{510}	84
110100	G_{525} G_{524} G_{523} G_{522} G_{521} G_{520}	85
110101	G_{535} G_{534} G_{533} G_{532} G_{531} G_{530}	86
110110	G_{545} G_{544} G_{543} G_{542} G_{541} G_{540}	87
110111	G_{555} G_{554} G_{553} G_{552} G_{551} G_{550}	88
111000	G_{565} G_{564} G_{563} G_{562} G_{561} G_{560}	89
111001	G_{575} G_{574} G_{573} G_{572} G_{571} G_{570}	90
111010	G_{585} G_{584} G_{583} G_{582} G_{581} G_{580}	91
111011	G_{595} G_{594} G_{593} G_{592} G_{591} G_{590}	92
111100	G_{605} G_{604} G_{603} G_{602} G_{601} G_{600}	93
111101	G_{615} G_{614} G_{613} G_{612} G_{611} G_{610}	94
111110	G_{625} G_{624} G_{623} G_{622} G_{621} G_{620}	95
111111	G_{635} G_{634} G_{633} G_{632} G_{631} G_{630}	96

B input (5-bit) 16-bit/pixel –mode 65,536 colors	B output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
00000	B_{005} B_{004} B_{003} B_{002} B_{001} B_{000}	97
00001	B_{015} B_{014} B_{013} B_{012} B_{011} B_{010}	98
00010	B_{025} B_{024} B_{023} B_{022} B_{021} B_{020}	99
00011	B_{035} B_{034} B_{033} B_{032} B_{031} B_{030}	100
00100	B_{045} B_{044} B_{043} B_{042} B_{041} B_{040}	101
00101	B_{055} B_{054} B_{053} B_{052} B_{051} B_{050}	102
00110	B_{065} B_{064} B_{063} B_{062} B_{061} B_{060}	103
00111	B_{075} B_{074} B_{073} B_{072} B_{071} B_{070}	104
01000	B_{085} B_{084} B_{083} B_{082} B_{081} B_{080}	105
01001	B_{095} B_{094} B_{093} B_{092} B_{091} B_{090}	106
01010	B_{105} B_{104} B_{103} B_{102} B_{101} B_{100}	107
01011	B_{115} B_{114} B_{113} B_{112} B_{111} B_{110}	108
01100	B_{125} B_{124} B_{123} B_{122} B_{121} B_{120}	109
01101	B_{135} B_{134} B_{133} B_{132} B_{131} B_{130}	110
01110	B_{145} B_{144} B_{143} B_{142} B_{141} B_{140}	111
01111	B_{155} B_{154} B_{153} B_{152} B_{151} B_{150}	112
10000	B_{165} B_{164} B_{163} B_{162} B_{161} B_{160}	113
10001	B_{175} B_{174} B_{173} B_{172} B_{171} B_{170}	114
10010	B_{185} B_{184} B_{183} B_{182} B_{181} B_{180}	115
10011	B_{195} B_{194} B_{193} B_{192} B_{191} B_{190}	116
10100	B_{205} B_{204} B_{203} B_{202} B_{201} B_{200}	117
10101	B_{215} B_{214} B_{213} B_{212} B_{211} B_{210}	118
10110	B_{225} B_{224} B_{223} B_{222} B_{221} B_{220}	119
10111	B_{235} B_{234} B_{233} B_{232} B_{231} B_{230}	120
11000	B_{245} B_{244} B_{243} B_{242} B_{241} B_{240}	121
11001	B_{255} B_{254} B_{253} B_{252} B_{251} B_{250}	122
11010	B_{265} B_{264} B_{263} B_{262} B_{261} B_{260}	123
11011	B_{275} B_{274} B_{273} B_{272} B_{271} B_{270}	124
11100	B_{285} B_{284} B_{283} B_{282} B_{281} B_{280}	125
11101	B_{295} B_{294} B_{293} B_{292} B_{291} B_{290}	126
11110	B_{305} B_{304} B_{303} B_{302} B_{301} B_{300}	127
11111	B_{315} B_{314} B_{313} B_{312} B_{311} B_{310}	128

7.4. Display Data RAM (DDRAM)

ILI9338B has an integrated 240x320x18-bit graphic type static RAM. This 172,800-byte memory allows storing a 240xRGBx320 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read or write to the same location of the frame memory.

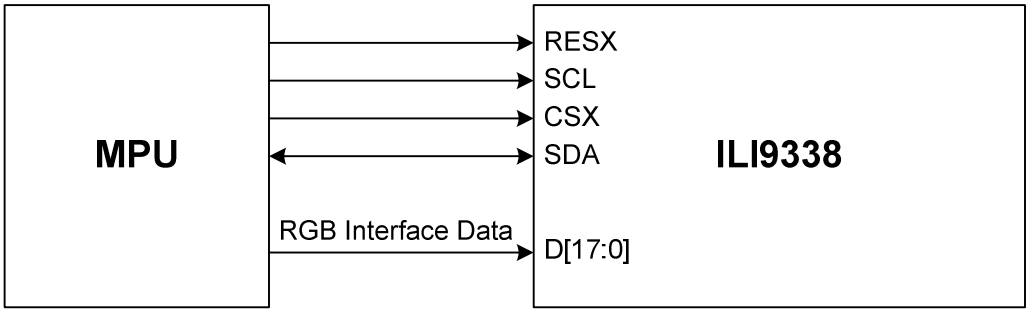


7.5. Display Data Format

ILI9338B supplies 18-/16-/9-/8-bit parallel MCU interface with 8080-series, 3-/4-line serial interface and 6-/16-/18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters RCM[1:0].

7.5.1. 3-line Serial Interface

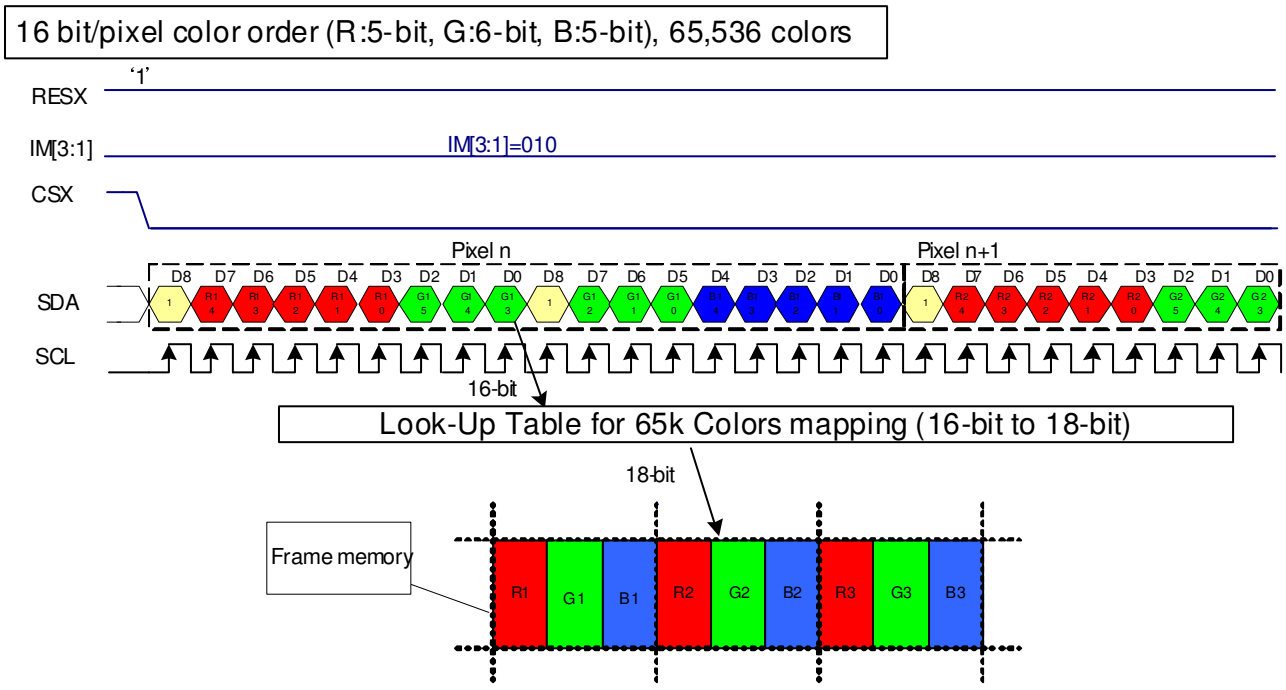
The 3-line/9-bit serial bus interface of ILI9338B can be used by setting external pin as IM [3:1] to "010". The shown figure is the example of SPI interface.



In 3-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bits input

-262k colors, RGB 6, 6, 6 -bits input.



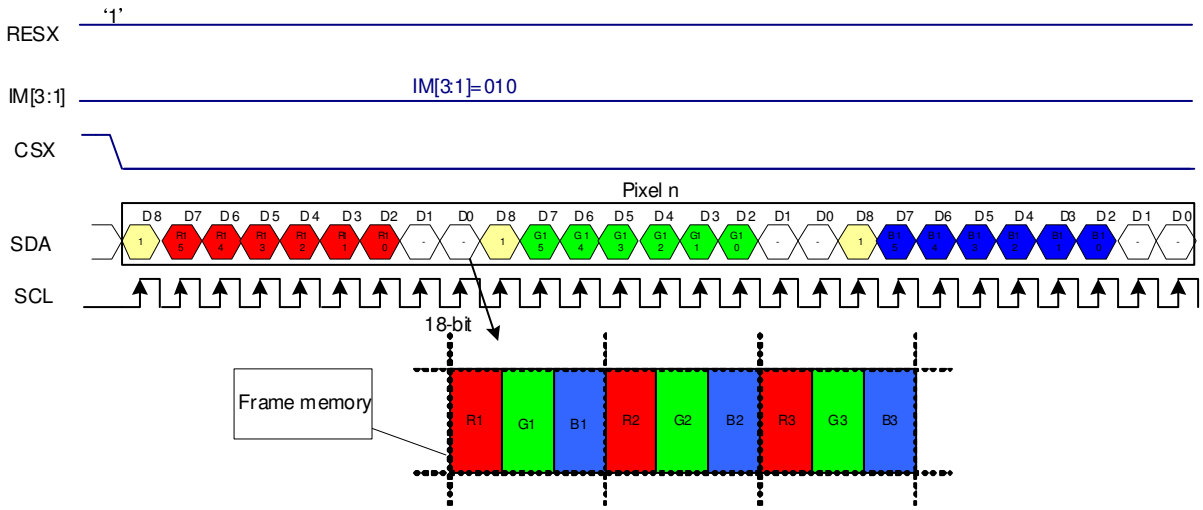
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care – Leave these pins to Open.

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



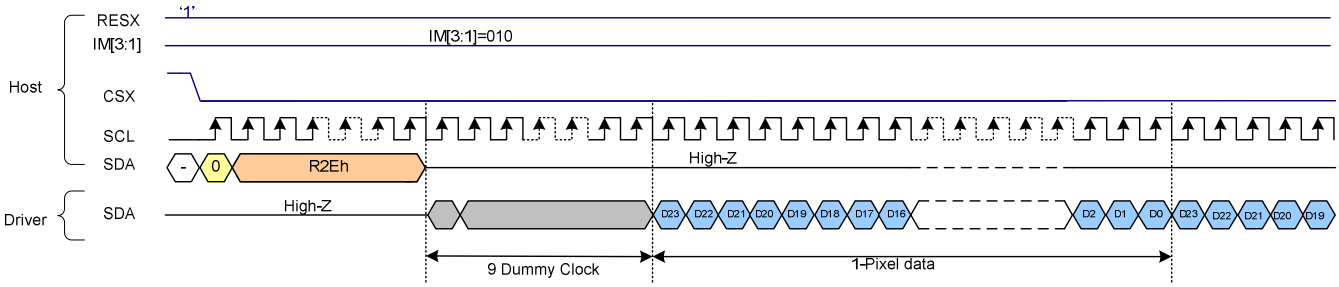
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care - Leave these pins to Open.

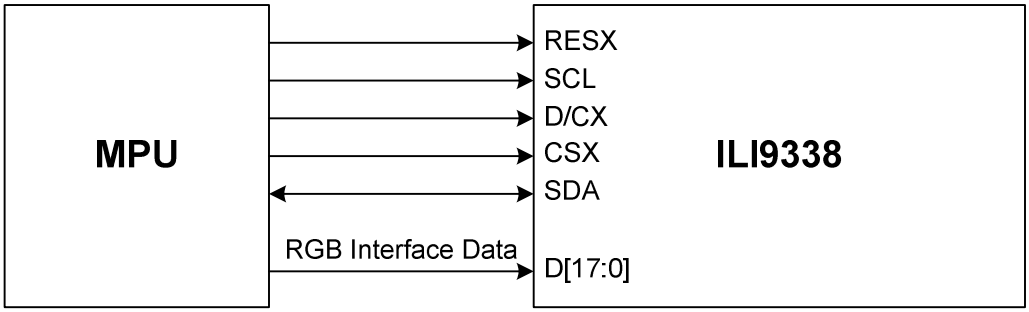
Read data through 3-line SPI mode



Note 1: '-'= Don't care – Leave these pins to Open.

7.5.2. 4-line Serial Interface

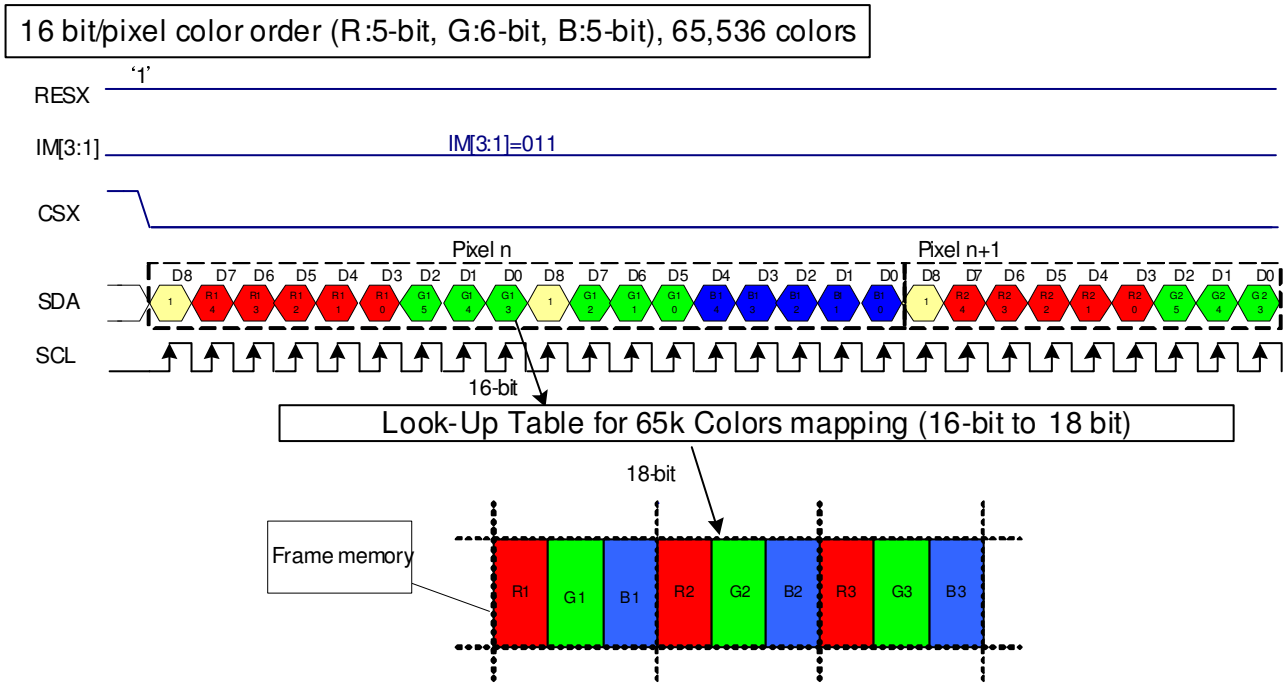
The 4-line/8-bit serial bus interface of ILI9338B can be used by setting external pin as IM [3:1] to "011". The shown figure is the example of interface with 8080 microcomputer system interface.



In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bits input.

-262k colors, RGB 6, 6, 6 -bits input.



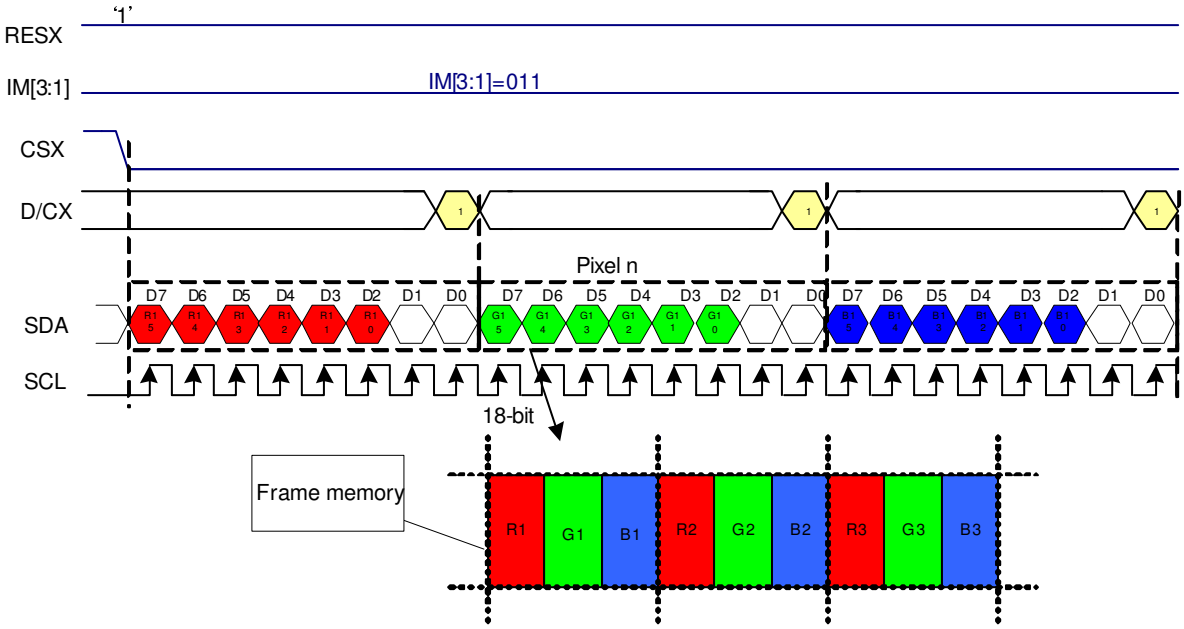
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care – Leave these pins to Open.

18 bit/pixel color order (R:6-bit, G:6-bit, B:5-bit), 262,144 colors



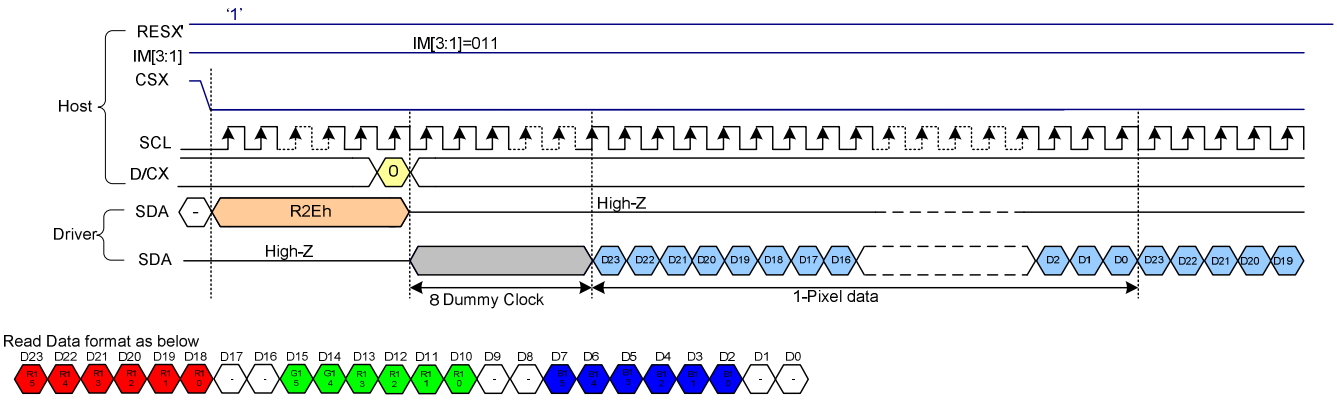
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and B5x.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care – Leave these pins to Open.

Read data through 4-line SPI mode

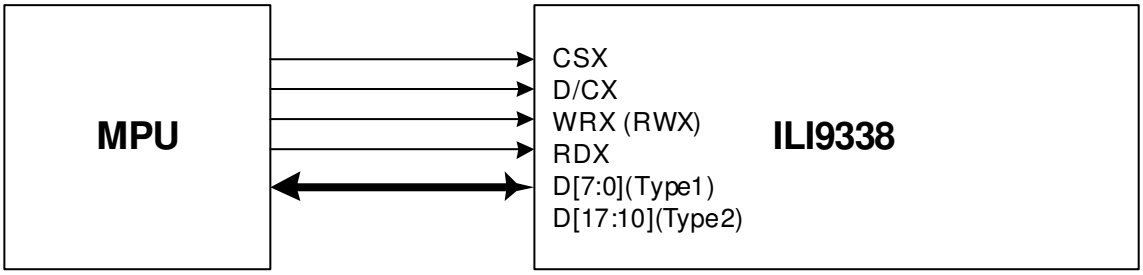


Note 1: '-'= Don't care – Leave these pins to Open.

7.5.3. 8-bit Parallel MCU Interface

The 8080-system 8-bit type Ⅰ parallel bus interface of ILI9338B can be used by setting external pin as IM [3:0] to "0001"; the 8080-system 8-bit type Ⅱ parallel bus interface mode can be used by settings as IM [3:0] ="0011".

The following shown figure is the example of interface with 8080-system 8-bit microcomputer system interface.

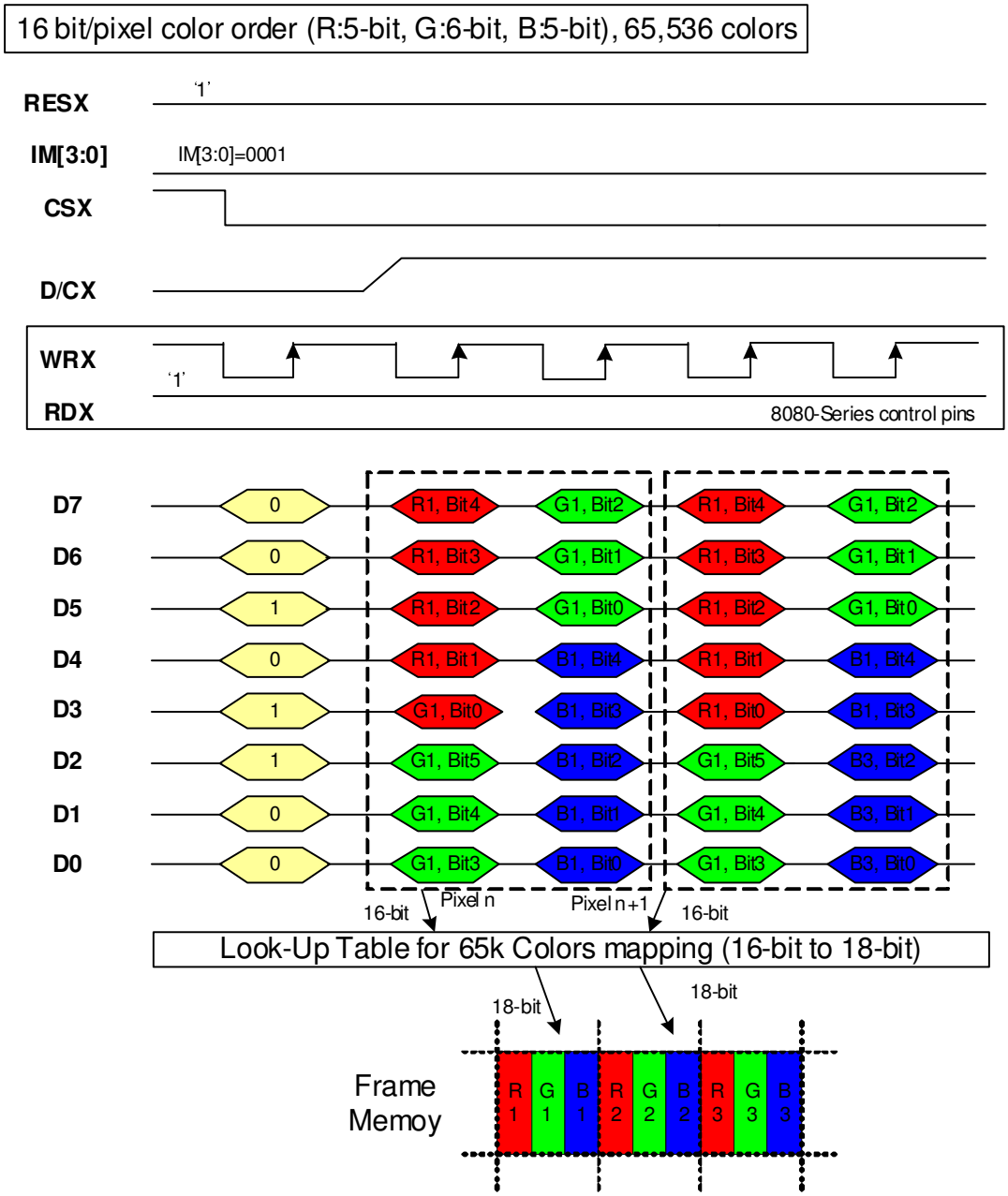


Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

7.5.4. 8-bit type I Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits are set to "101".

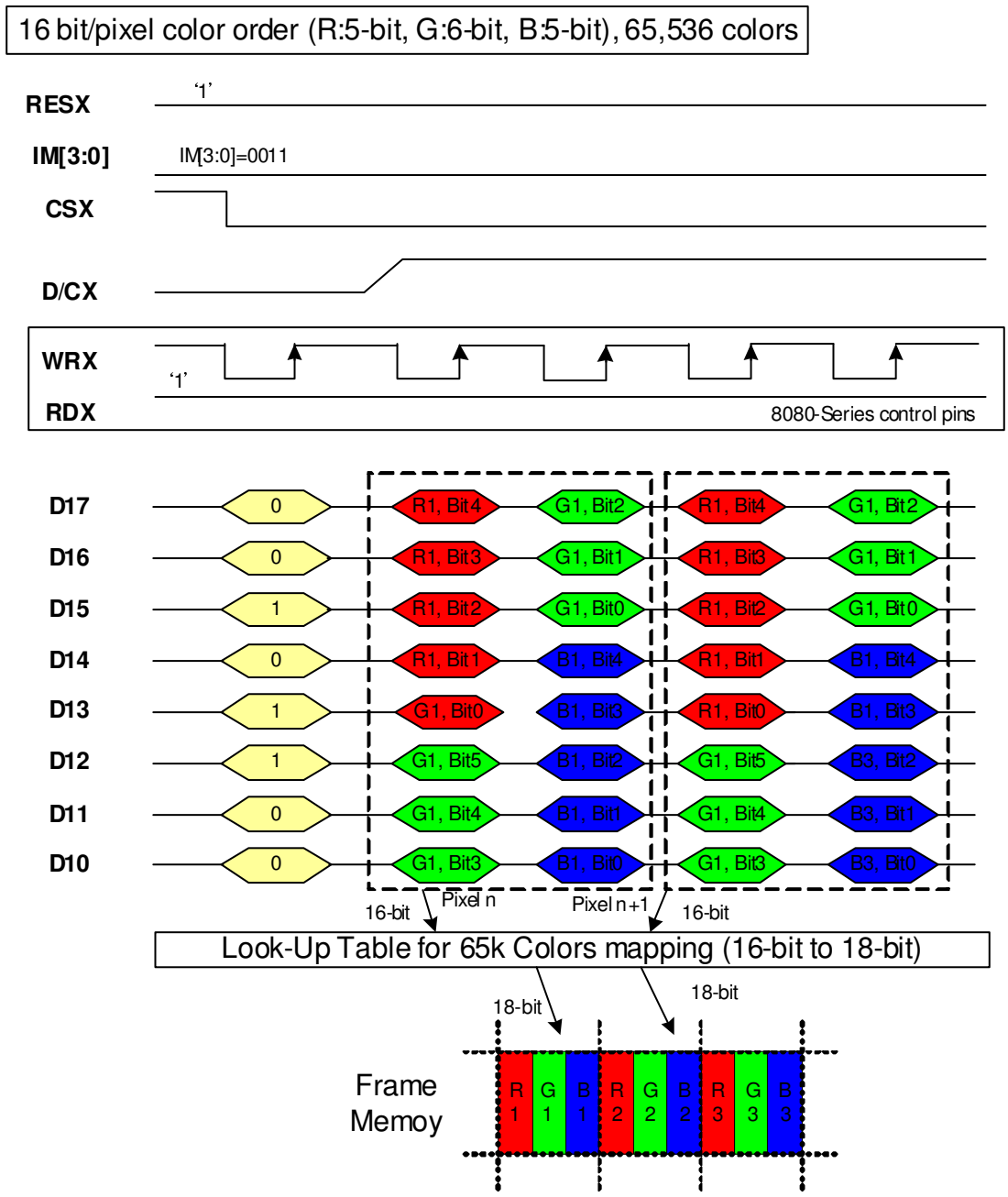


Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green data and MSB=Bit 4, LSB=Bit0 for Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

7.5.5. 8-bit type Ⅱ Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits are set to "101"

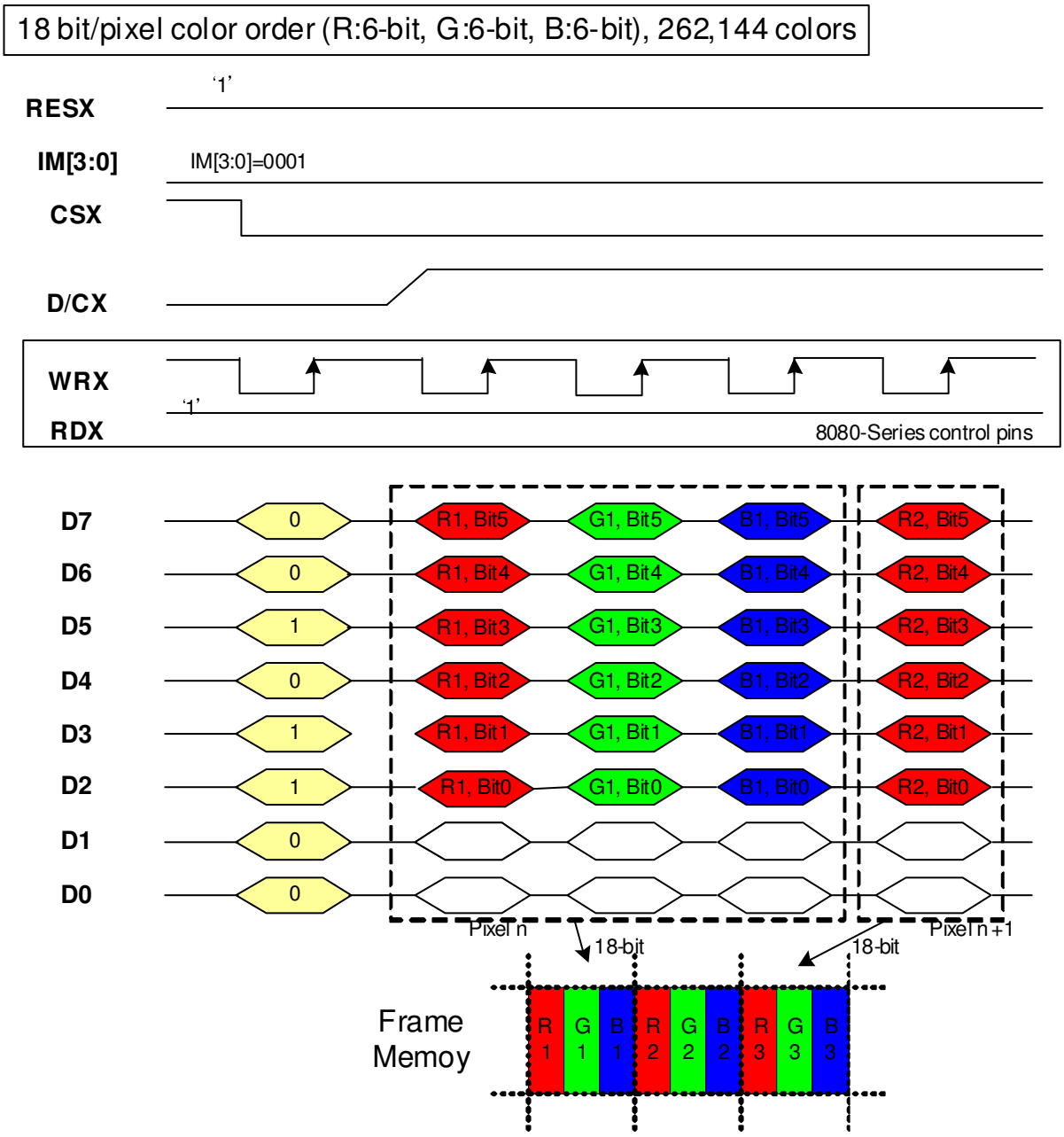


Note 1: The data order is as follows, MSB=D17, LSB=D10 and picture data is MSB=Bit 5, LSB=Bit 0 for Green data and MSB=Bit 4, LSB=Bit0 for Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

7.5.6. 8-bit type I Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits are set to “110”.

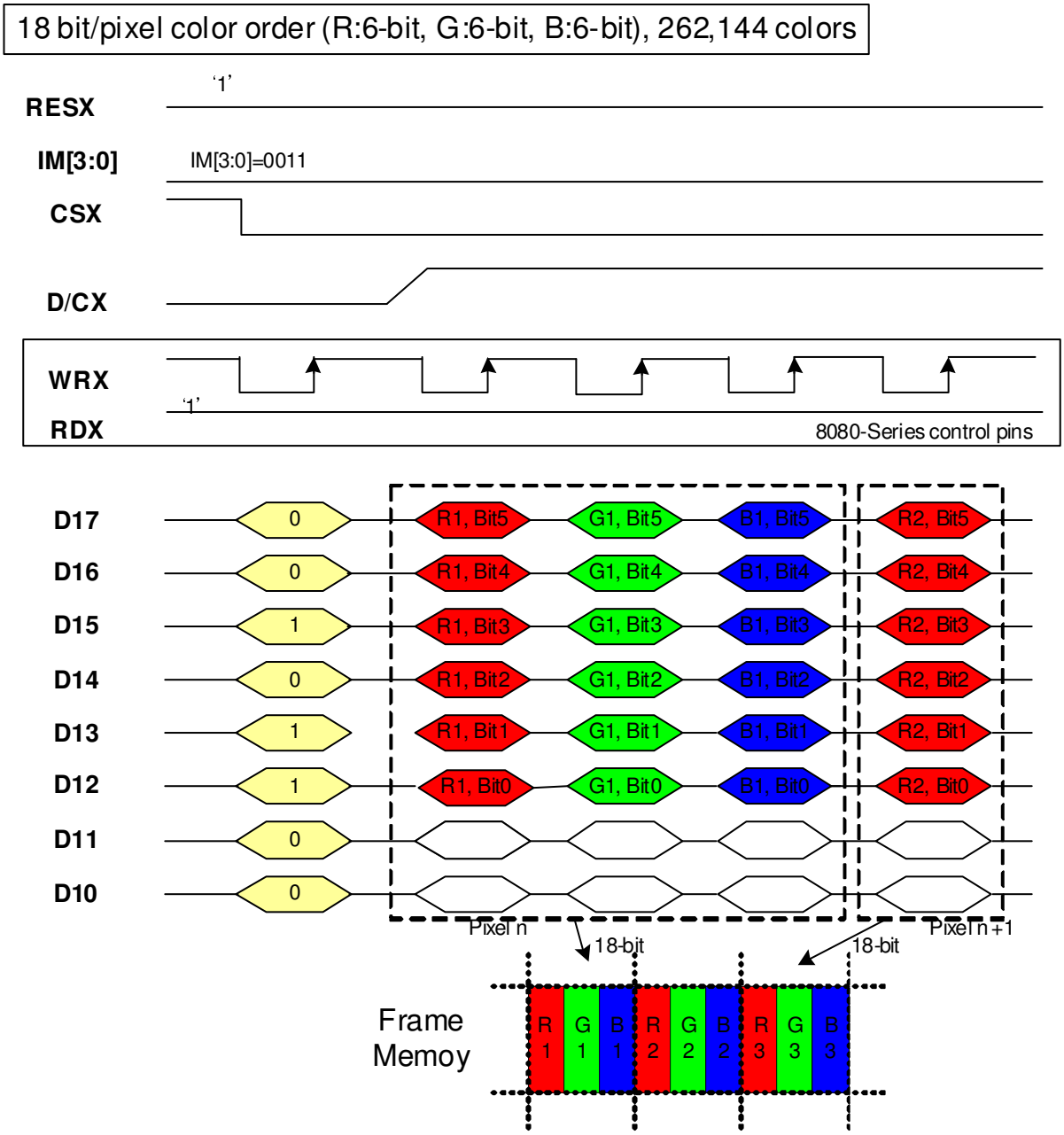


Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, Red and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

7.5.7. 8-bit type Ⅱ Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits are set to “110”.

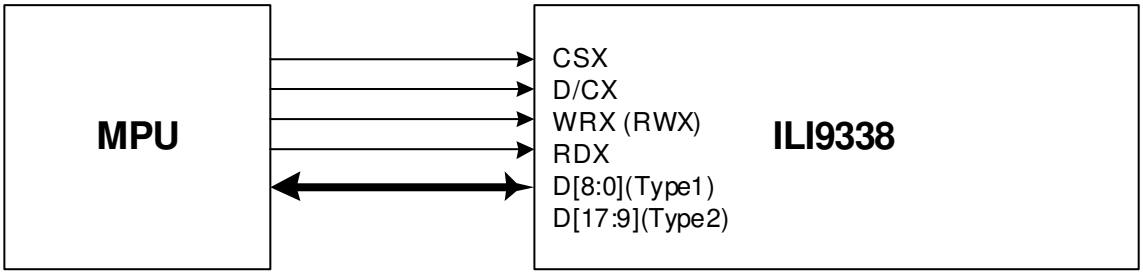


Note 1: The data order is as follows, MSB=D17, LSB=D10 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, Red and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

7.5.8. 9-bit Parallel MCU Interface

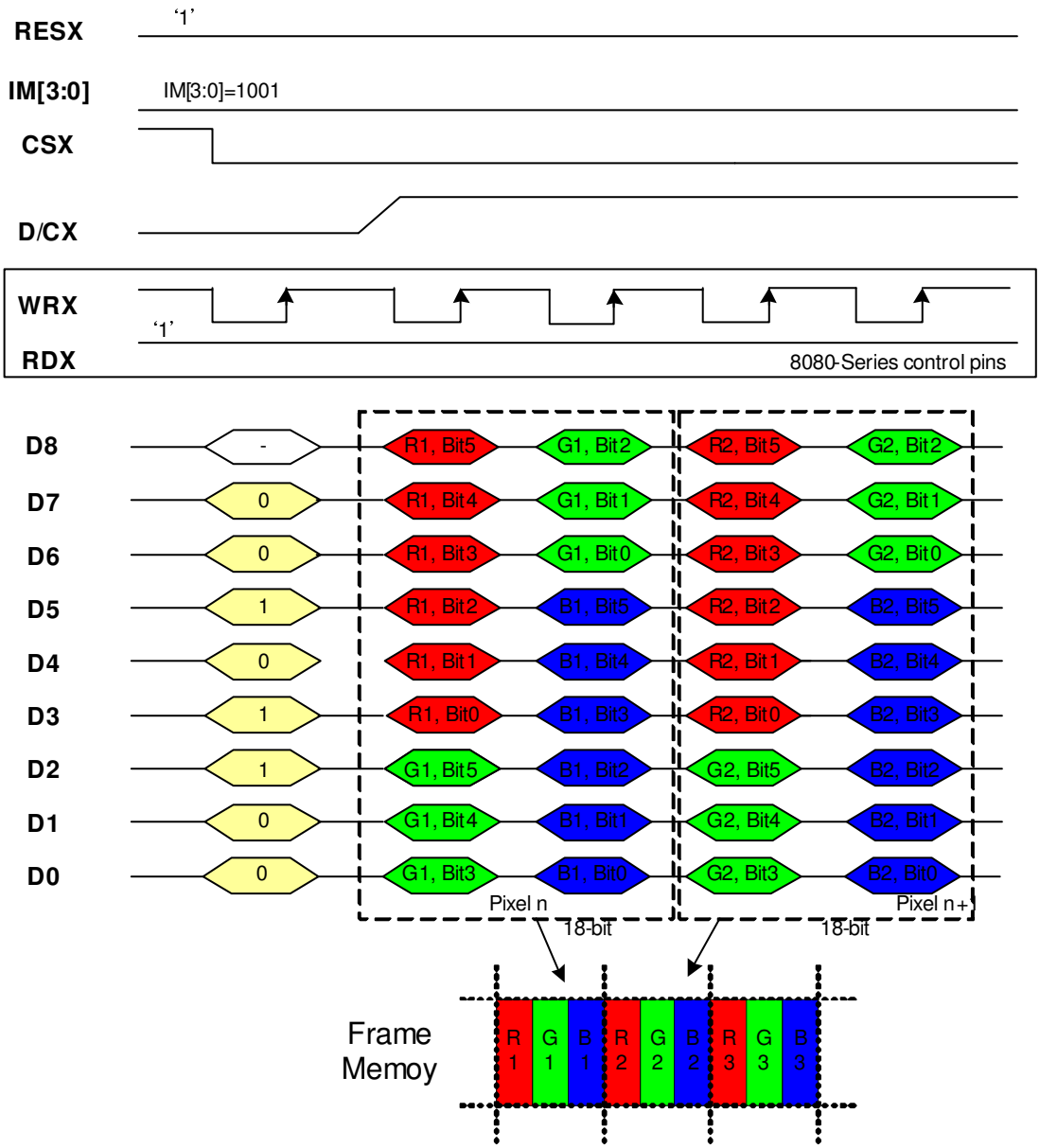
The 8080-system 9-bit type Ⅰ parallel bus interface of ILI9338B can be selected by setting hardware pin IM [3:0] to “1001”. And the 8080-system 9-bit type Ⅱ parallel bus interface mode can be selected by settings IM [3:0] =”1011”. The following shown figure is the example of interface with 8080 9-bit microcomputer system interface.



7.5.9. 9-bit type I Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

There are 2 pixels (6 sub-pixels) display data per 4 transfers, when DBI [2:0] bits are set to “110”.

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



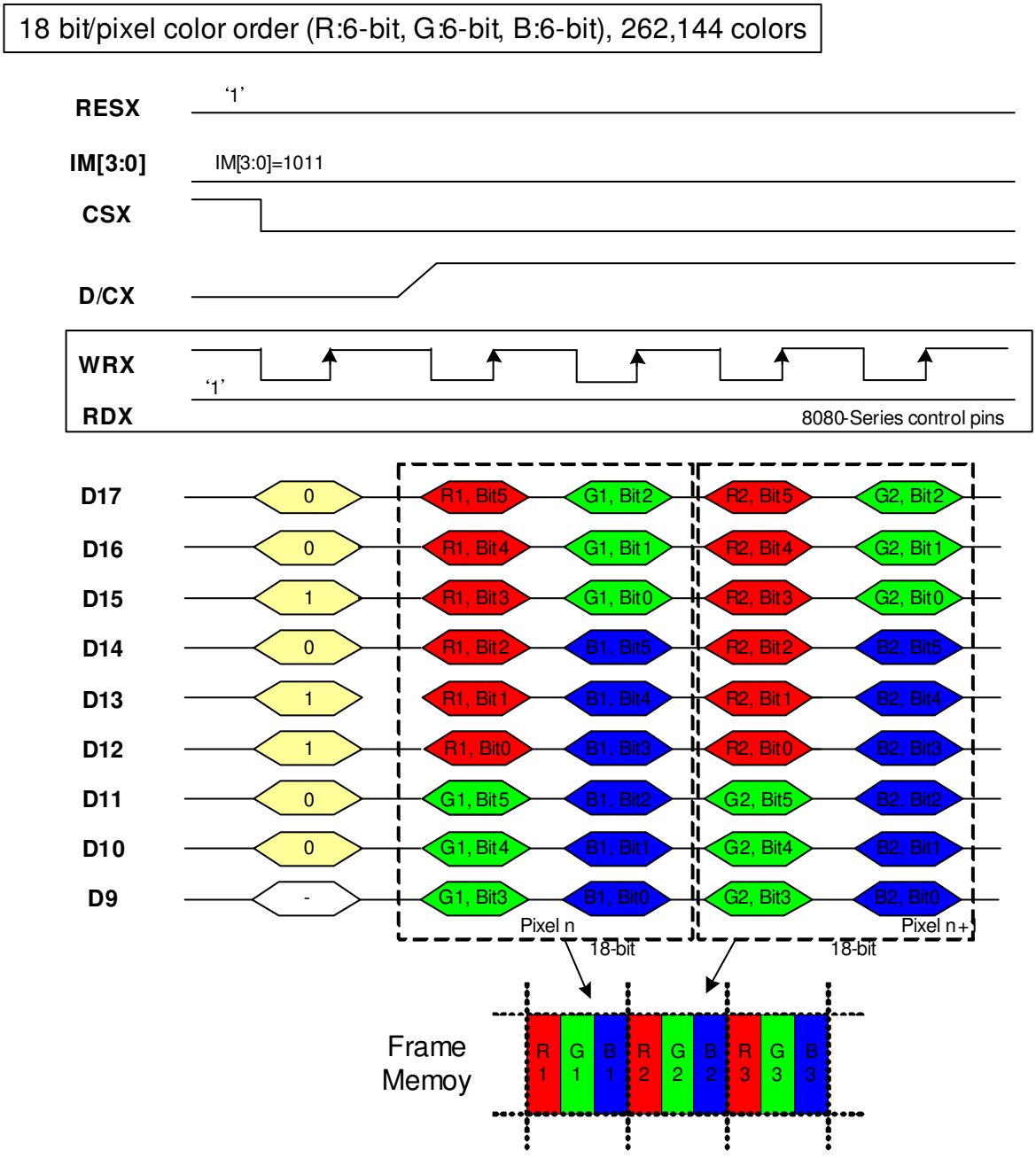
Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3: '-'= Don't care – Leave these pins to Open.

7.5.10. 9-bit type Ⅱ Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

There are 2 pixels (6 sub-pixels) display data per 4 transfers, when DBI [2:0] bits are set to “110”.



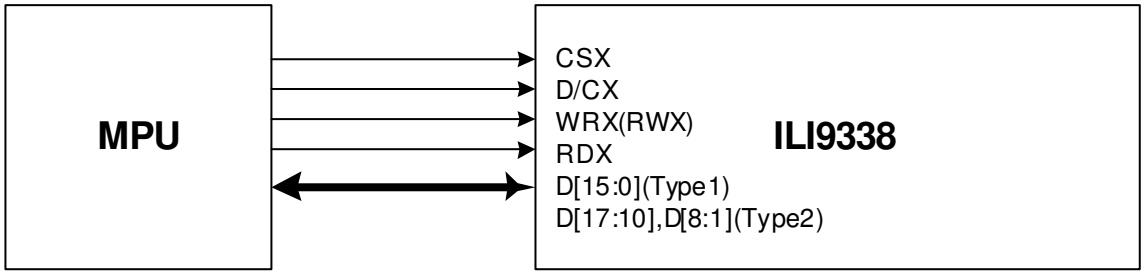
Note 1: The data order is as follows, MSB=D17, LSB=D9 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3: '-'= Don't care – Leave these pins to Open.

7.5.11. 16-bit Parallel MCU Interface

The 8080-system 16-bit type Ⅰ parallel bus interface of ILI9338B can be selected by setting hardware pin IM[3:0] to “0000”. And the 8080-system 16-bit type Ⅱ parallel bus interface mode can be selected by settings IM [3:0] =”0010”. The following shown figure is the example of interface with 8080 16-bit microcomputer system interface.

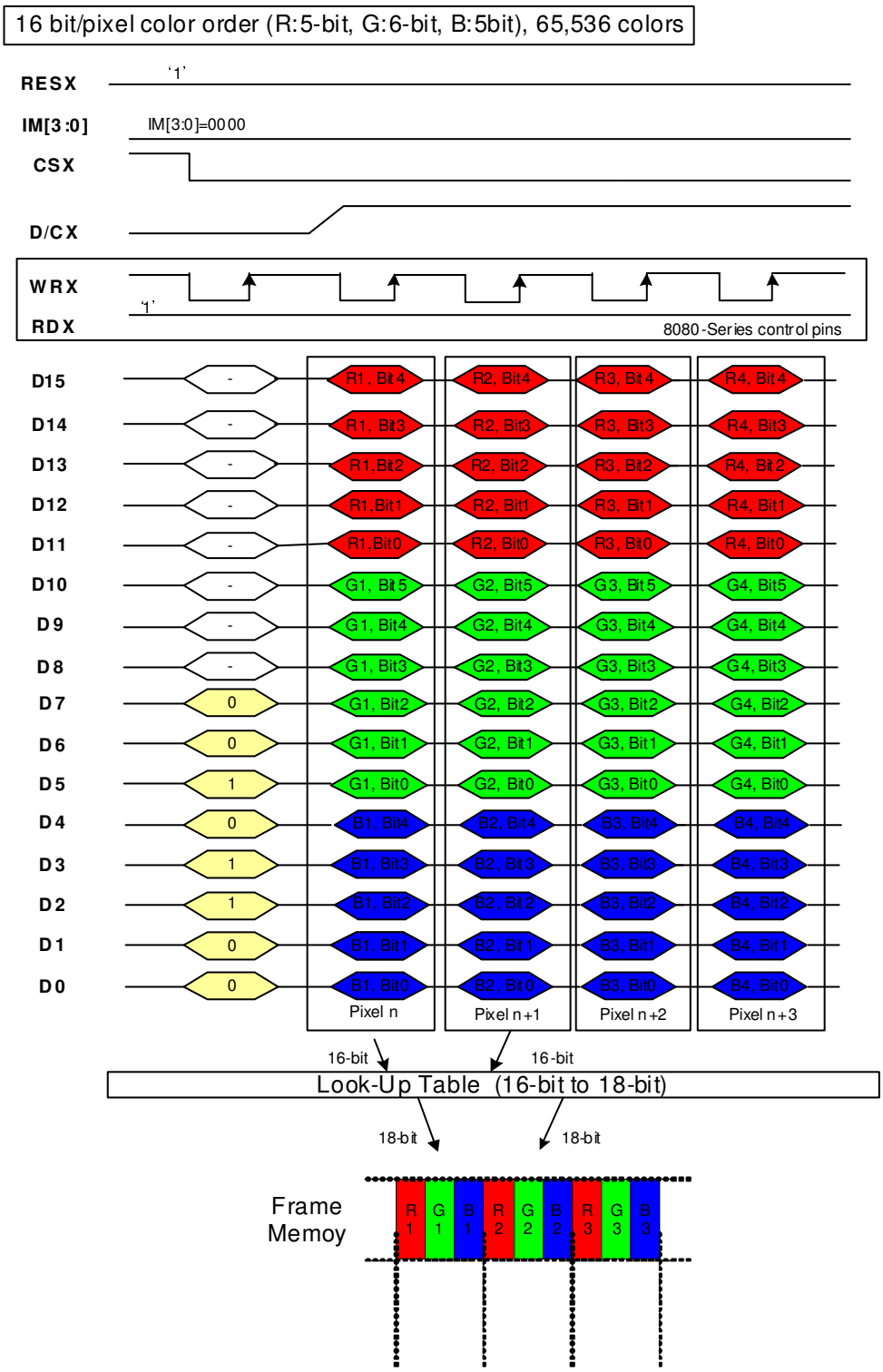


Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

7.5.12. 16-bit type I Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color

One pixel (3 sub-pixels) display data is sent by 2 bytes transfer when DBI [2:0] bits are set to “101”.



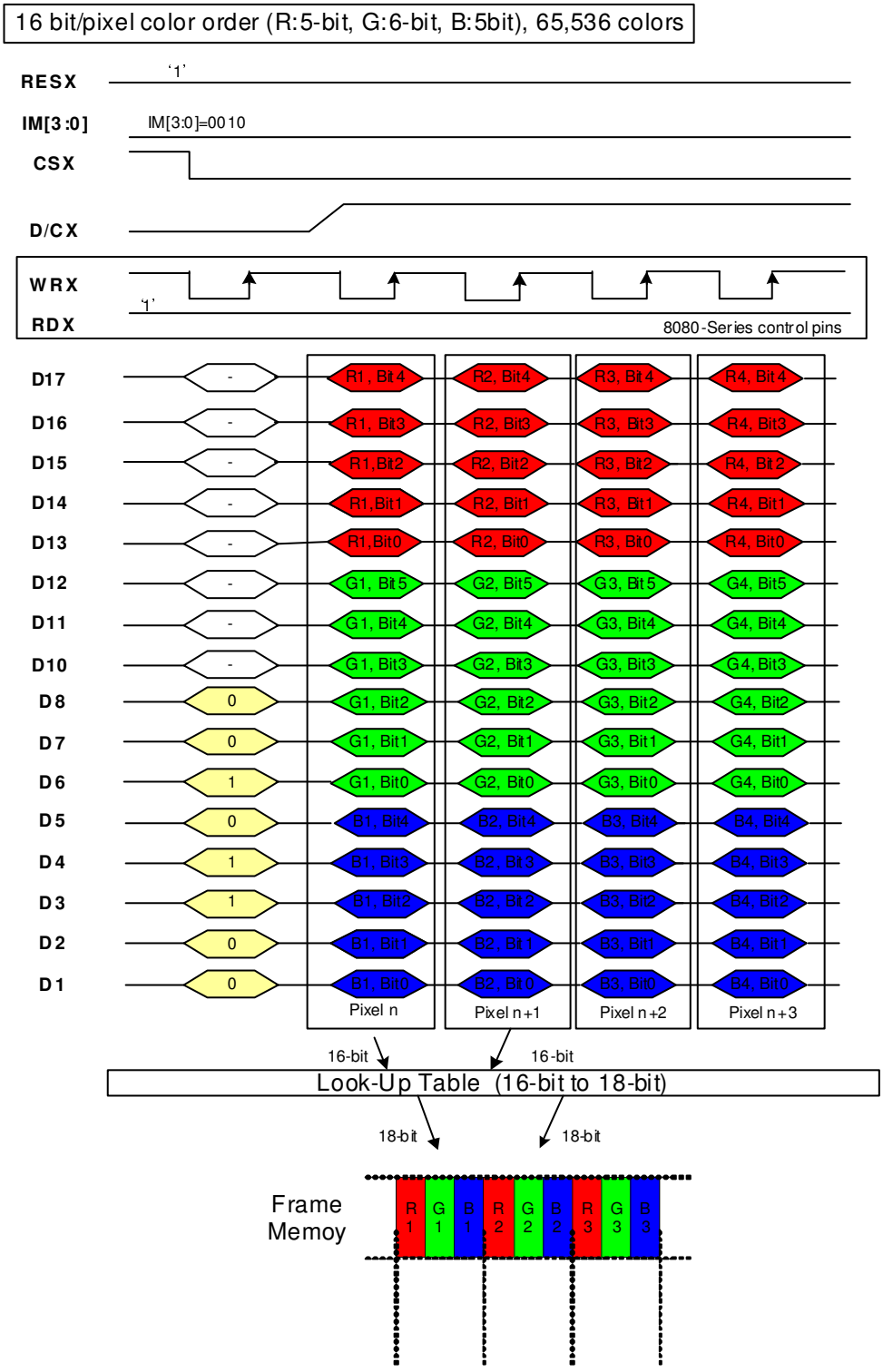
Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green data and MSB=Bit 4, LSB=Bit0 for Red and Blue data.

Note 2: 1-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3: '-'= Don't care – Leave these pins to Open.

7.5.13. 16-bit type Ⅱ Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color

One pixel (3 sub-pixels) display data is sent by 2 bytes transfer when DBI [2:0] bits are set to "101"



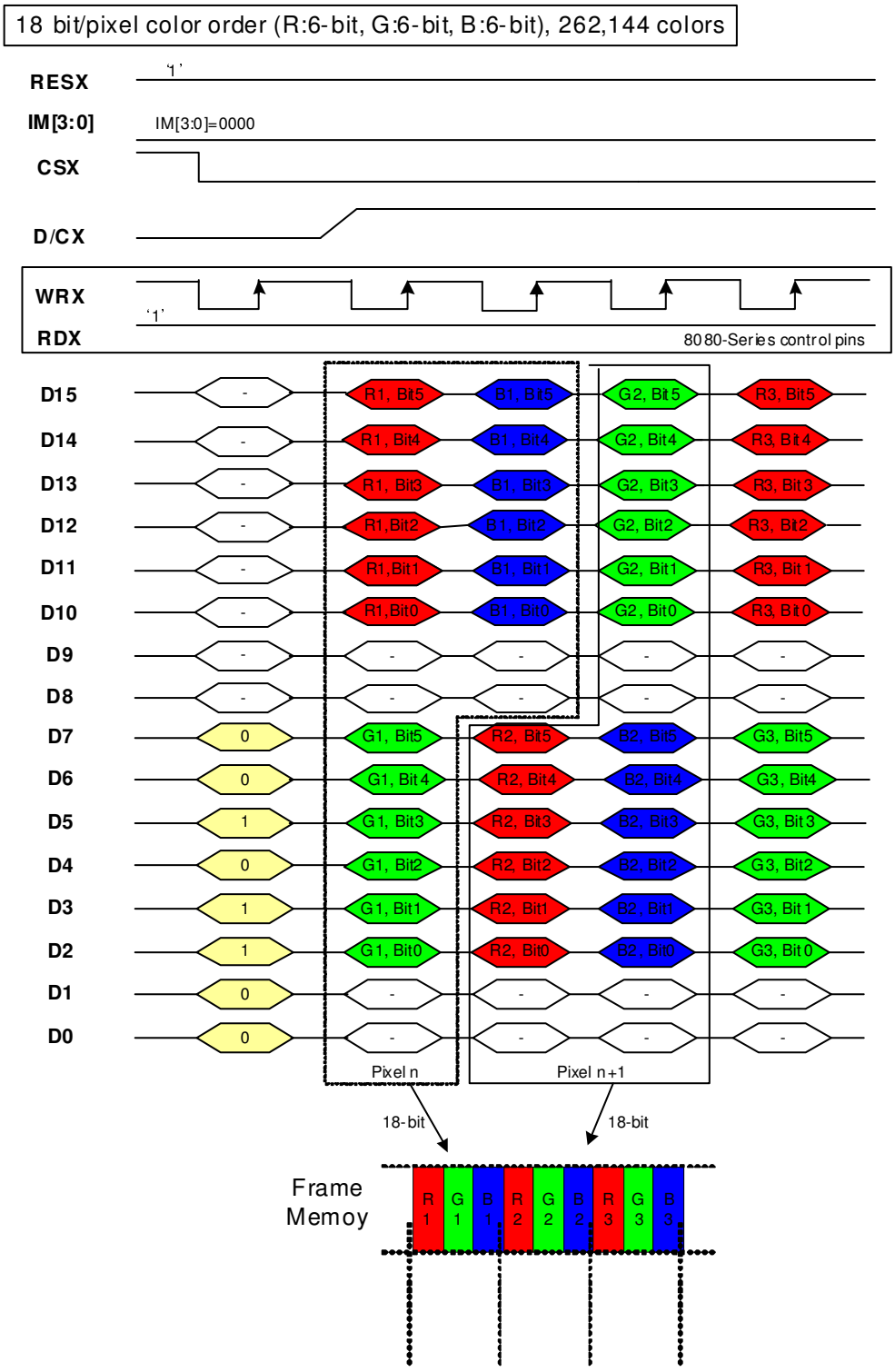
Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green data and MSB=Bit 4, LSB=Bit0 for Red and Blue data.

Note 2: 1-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3: '-'= Don't care – Leave these pins to Open.

7.5.14. 16-bit Data type I Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits are set to “110”.



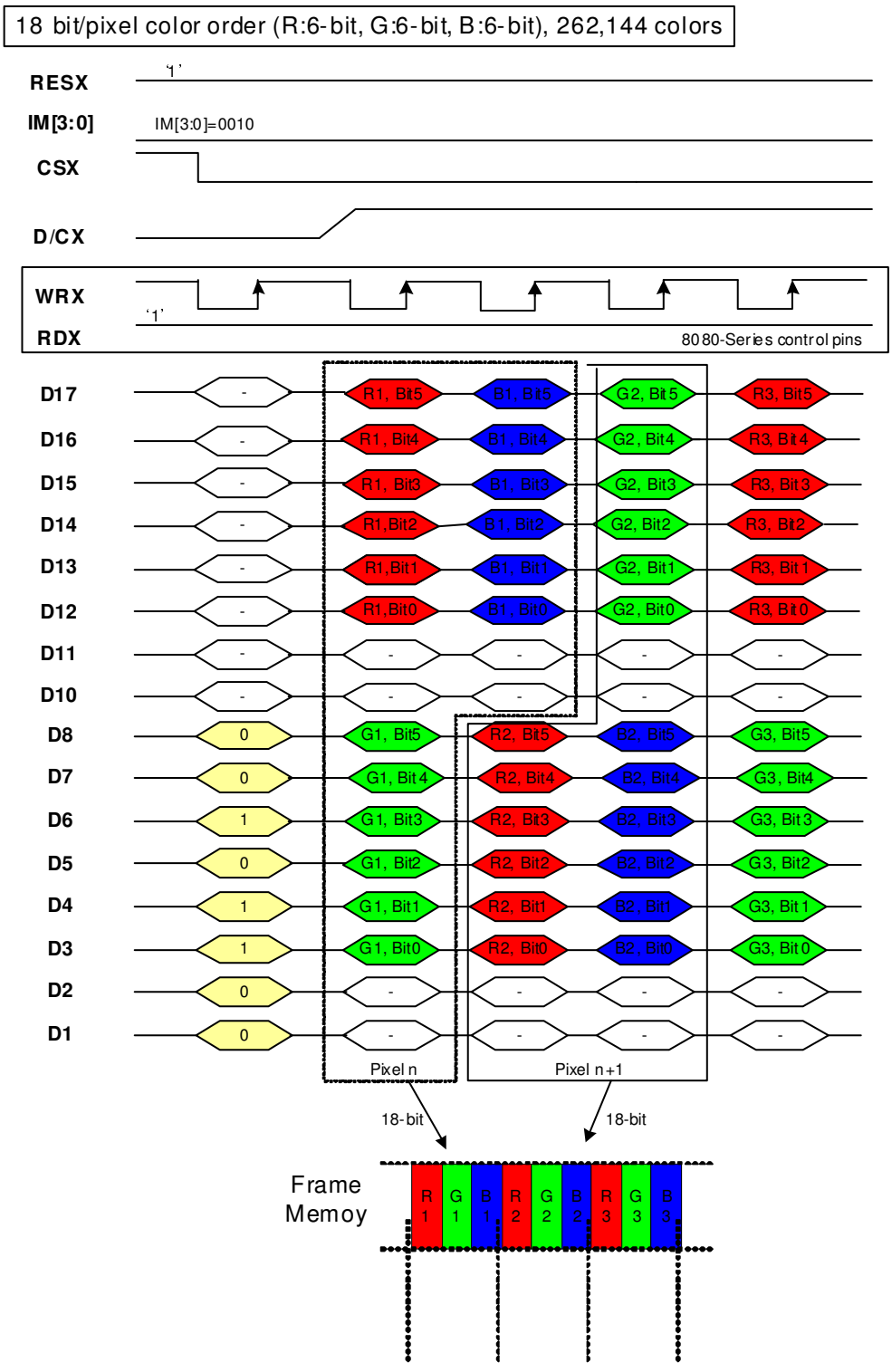
Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, Red and Blue data.

Note 2: 3-times transfer is used to transmit 2 pixel data with the 18-bits color depth information.

Note 3: '-'= Don't care – Leave these pins to Open.

7.5.15. 16-bit Data type Ⅱ Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits are set to “110”.



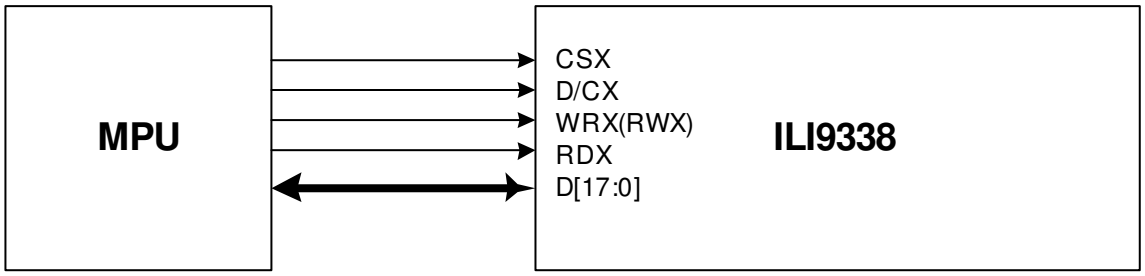
Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, Red and Blue data.

Note 2: 3-times transfer is used to transmit 2 pixel data with the 18-bits color depth information.

Note 3: ‘-‘= Don’t care – Leave these pins to Open.

7.5.16. 18-bit Parallel MCU Interface

The 8080-system 18-bit type Ⅰ parallel bus interface of ILI9338B can be selected by setting hardware pin IM[3:0] to “1000”. And the 8080-system 18-bit type Ⅱ parallel bus interface mode can be selected by settings IM [3:0] =”1010”. The following shown figure is the example of interface with 8080 18-bit microcomputer system interface.

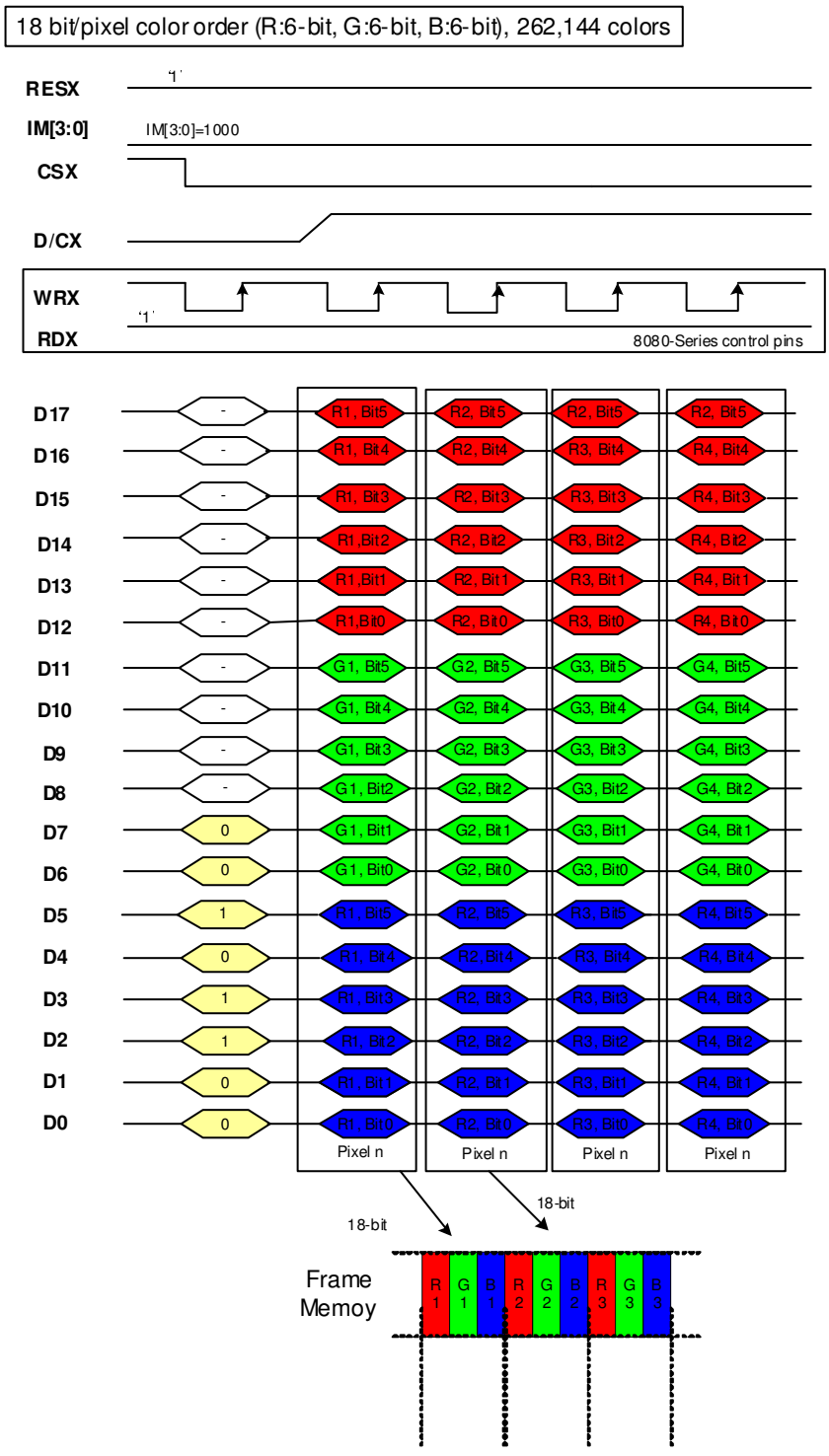


Different display data format is available for one color depth only supported by listed below.

- 262K-Colors, RGB 6, 6, 6 -bits input data.

7.5.17. 18-bit type I Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

There is 1 pixel (3 sub-pixels) display data per 1 transfer, when DBI [2:0] bits are set to “110”



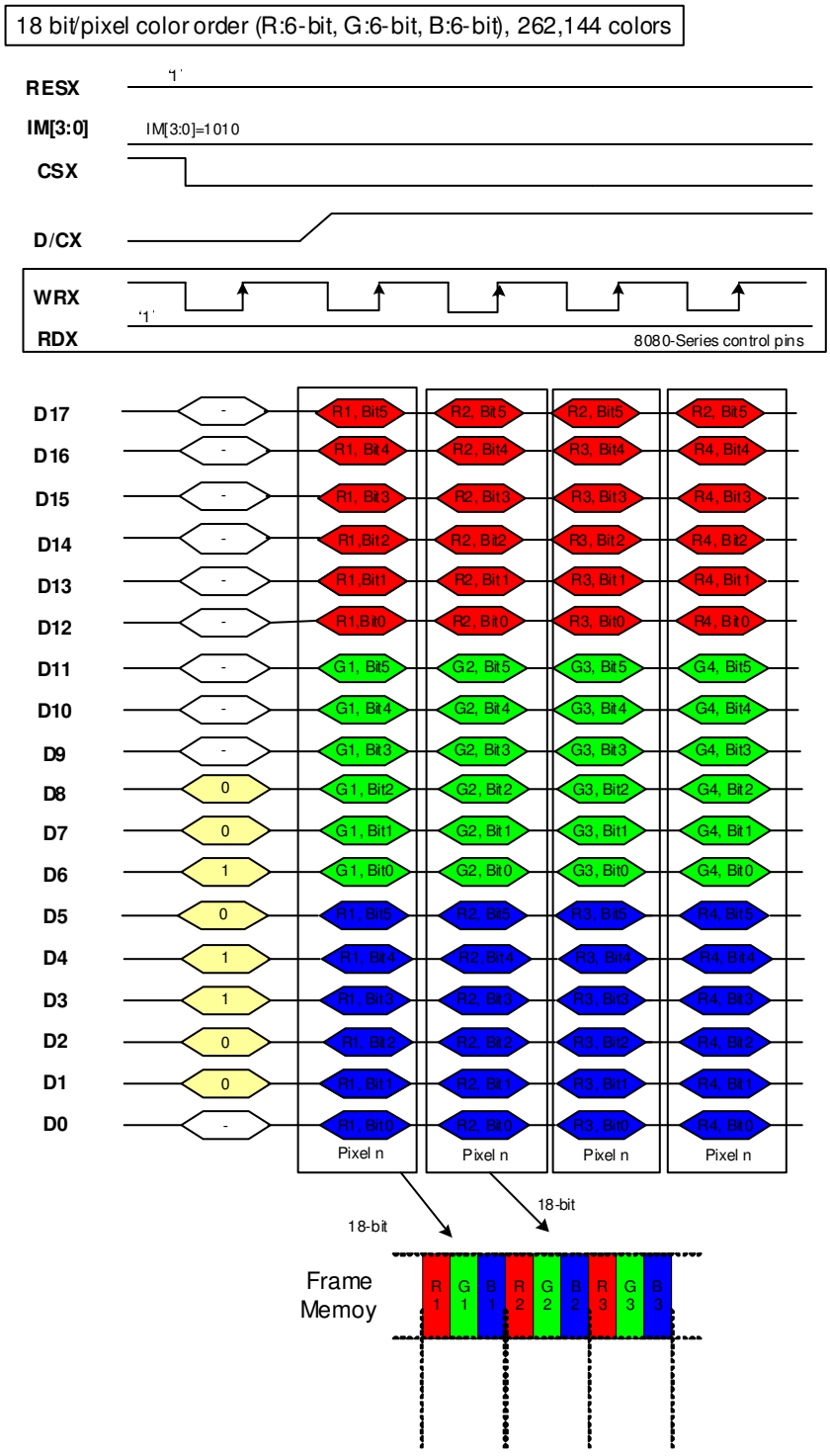
Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, Red and Blue data.

Note 2: 1-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3: ‘-‘= Don’t care – Leave these pins to Open.

7.5.18. 18-bit type Ⅱ Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

There is 1 pixel (3 sub-pixels) display data per 1 transfer, when DBI [2:0] bits are set to “110”



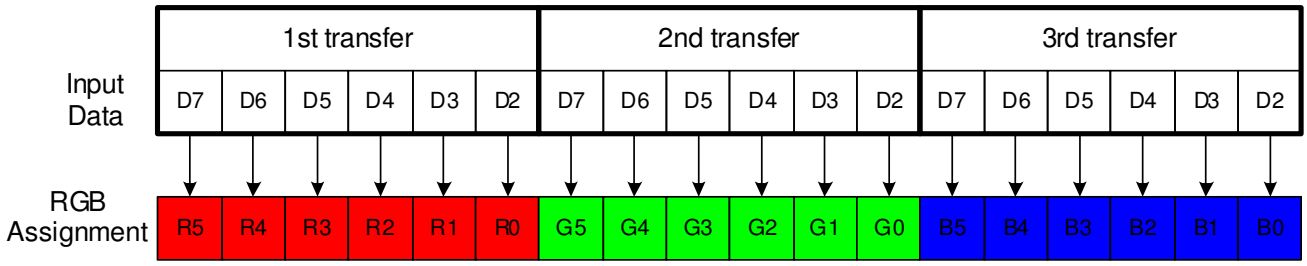
Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, Red and Blue data.

Note 2: 1-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3: ‘-‘= Don’t care – Leave these pins to Open.

7.5.19. 6-bit Parallel RGB Interface

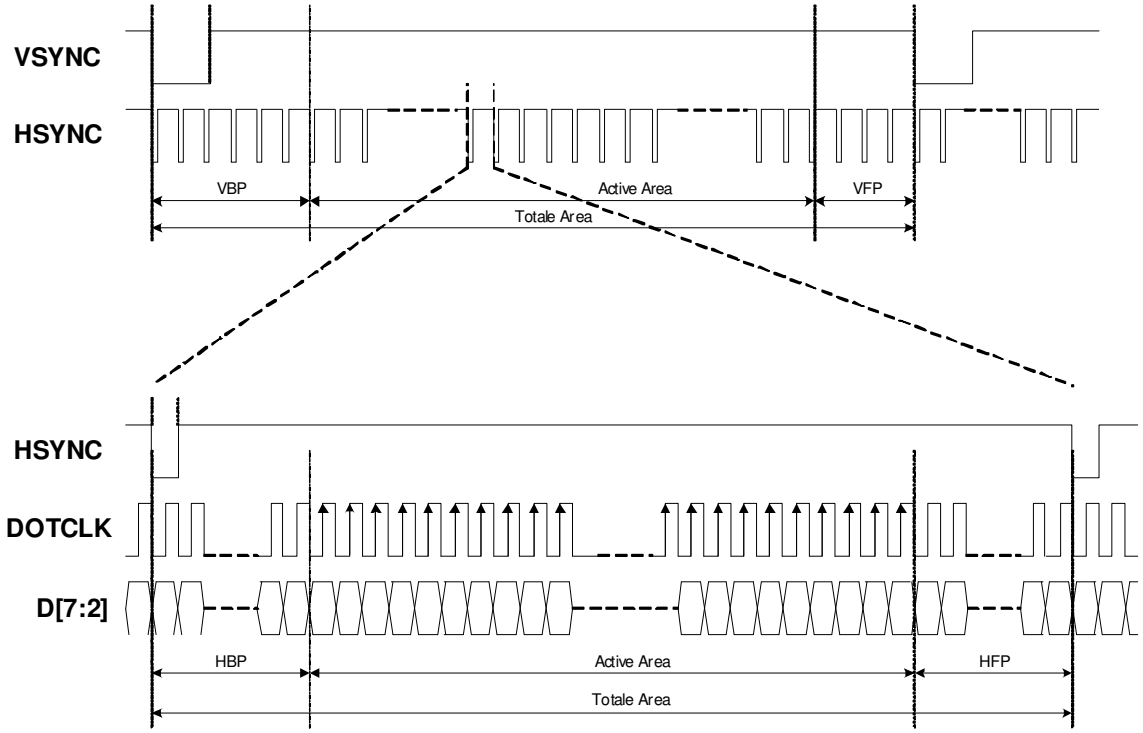
The 6-bit RGB interface is selected by setting the DPI [3:0] bit to “1110”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (D [7:2]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D [7:2] according to the VFP/VBP and HFP/HBP settings. Unused pins must be connected to GND to ensure normally operation. Registers can be set by the SPI system interface.



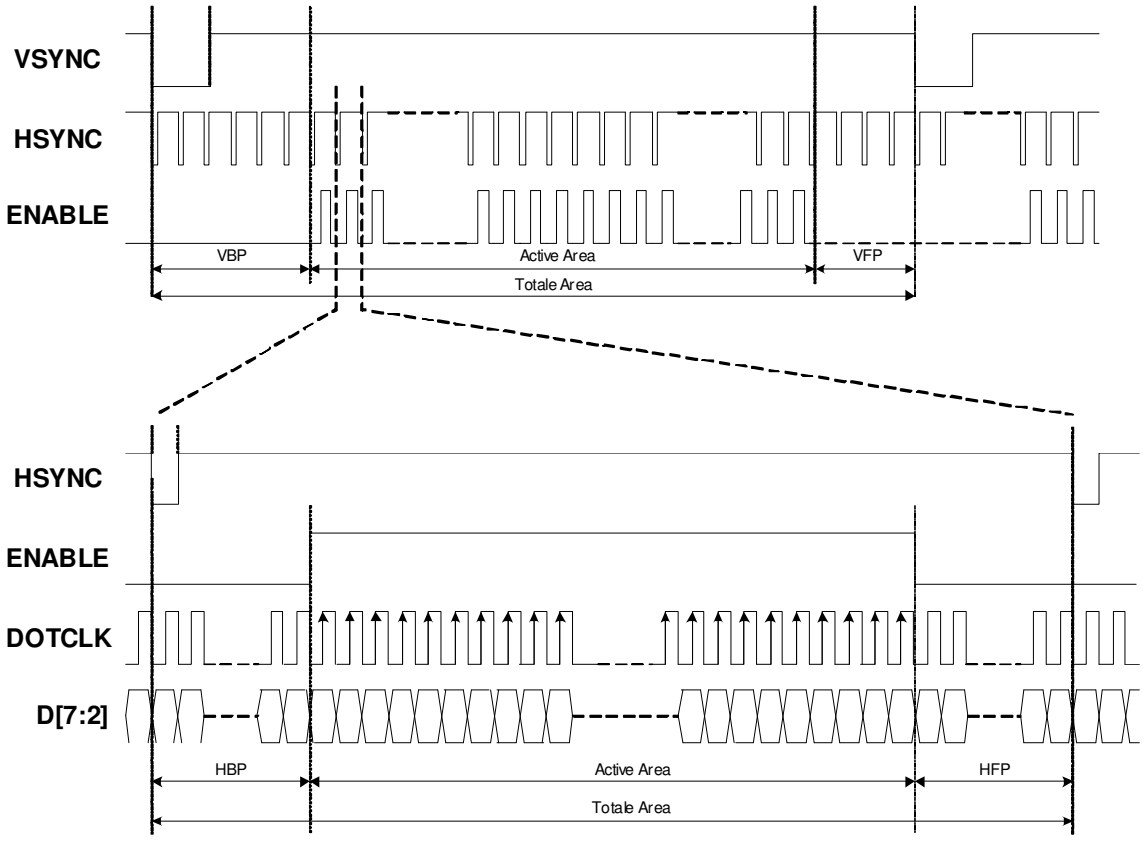
ILI9338B has data transfer counters to count the first, second, third data transfer in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.

SYNC Mode, RCM[1:0]=“11”

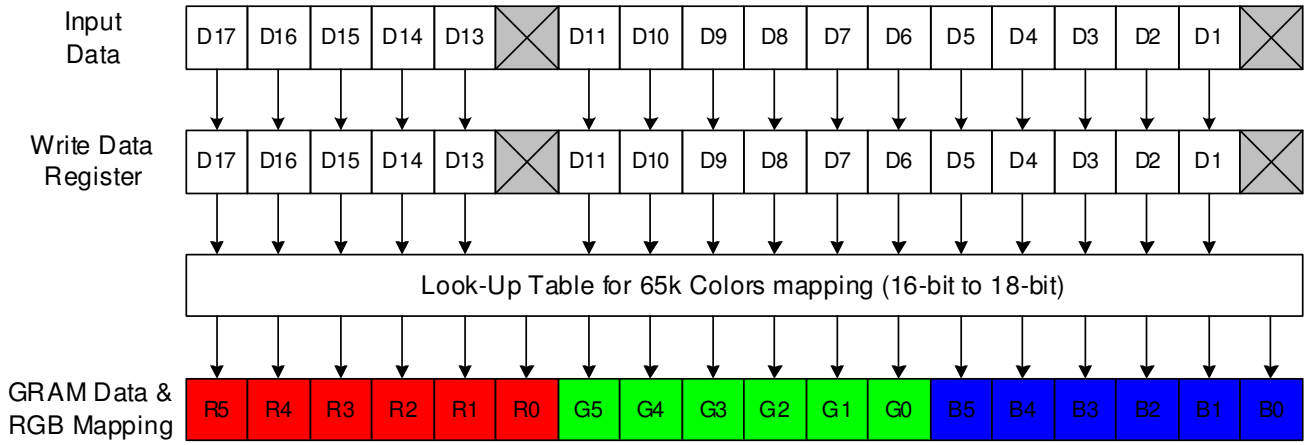


DE Mode, RCM[1:0]=“10”



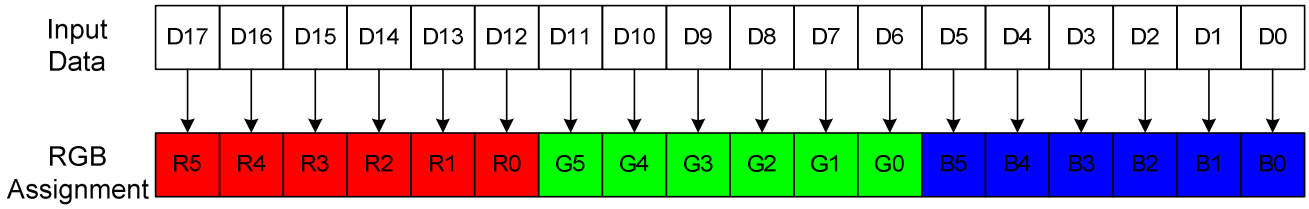
7.5.20. 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI [3:0] bits to “0101”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data is transferred to the internal GRAM in synchronization with the display operation via 16-bit RGB data bus (D [17:13] & D [11:1]) according to the data enable signal (DE). The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D [17:13] and D [11:1] according to the VFP/VBP and HFP/HBP settings. The unused D12 and D0 pins must be connected to GND for ensure normally operation. Registers can be set by the system interface.



7.5.21. 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI [3:0] bits to “0110”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 18-bit RGB data bus (D [17:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D [17:0] according to the VFP/VBP and HFP/HBP settings. Registers can be set by the system interface.



8. Command

8.1. Command List

Regulative Command Set													
Command Function	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
No Operation	0	1	↑	XXXXXXXX	0	0	0	0	0	0	0	0	00h
Software Reset	0	1	↑	XXXXXXXX	0	0	0	0	0	0	0	1	01h
Read Display Identification Information	0	1	↑	XXXXXXXX	0	0	0	0	0	1	0	0	04h
	1	↑	1	XXXXXXXX	ID1 [7:0]								XX
	1	↑	1	XXXXXXXX	ID2 [7:0]								XX
	1	↑	1	XXXXXXXX	ID3 [7:0]								XX
Read Display Status	0	1	↑	XXXXXXXX	0	0	0	0	1	0	0	1	09h
	1	↑	1	XXXXXXXX	D [31:25]							0	XX
	1	↑	1	XXXXXXXX	0	D [22:20]			D [19:16]				XX
	1	↑	1	XXXXXXXX	0	0	0	0	0	D [10:8]			XX
	1	↑	1	XXXXXXXX	D [7:5]			0	0	0	0	0	XX
Read Display Power Mode	0	1	↑	XXXXXXXX	0	0	0	0	1	0	1	0	0Ah
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	D [7:2]						0	0	XX
Read Display MADCTL	0	1	↑	XXXXXXXX	0	0	0	0	1	0	1	1	0Bh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	D [7:2]						0	0	XX
Read Display Pixel Format	0	1	↑	XXXXXXXX	0	0	0	0	1	1	0	0	0Ch
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	D [7:4]				X	D [2:0]			XX
Read Display Image Mode	0	1	↑	XXXXXXXX	0	0	0	0	1	1	0	1	0Dh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	X	X	X	X	X	D [2:0]			XX
Read Display Signal Mode	0	1	↑	XXXXXXXX	0	0	0	0	1	1	1	0	0Eh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	D [7:6]		X	X	X	X	X	X	XX
Read Display Self-Diagnostic Result	0	1	↑	XXXXXXXX	0	0	0	0	1	1	1	1	0Fh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	D [7:6]		X	X	X	X	X	X	XX
Sleep IN	0	1	↑	XXXXXXXX	0	0	0	1	0	0	0	0	10h
Sleep OUT	0	1	↑	XXXXXXXX	0	0	0	1	0	0	0	1	11h
Partial Mode ON	0	1	↑	XXXXXXXX	0	0	0	1	0	0	1	0	12h
Normal Display Mode ON	0	1	↑	XXXXXXXX	0	0	0	1	0	0	1	1	13h
Display Inversion OFF	0	1	↑	XXXXXXXX	0	0	1	0	0	0	0	0	20h
Display Inversion ON	0	1	↑	XXXXXXXX	0	0	1	0	0	0	0	1	21h
Gamma Set	0	1	↑	XXXXXXXX	0	0	1	0	0	1	1	0	26h
	1	1	↑	XXXXXXXX	GC [7:0]								XX
Display OFF	0	1	↑	XXXXXXXX	0	0	1	0	1	0	0	0	28h
Display ON	0	1	↑	XXXXXXXX	0	0	1	0	1	0	0	1	29h
Column Address Set	0	1	↑	XXXXXXXX	0	0	1	0	1	0	1	0	2Ah
	1	1	↑	XXXXXXXX	SC [15:8]								XX
	1	1	↑	XXXXXXXX	SC [7:0]								XX
	1	1	↑	XXXXXXXX	EC [15:8]								XX
	1	1	↑	XXXXXXXX	EC [7:0]								XX
Page Address Set	0	1	↑	XXXXXXXX	0	0	1	0	1	0	1	1	2Bh
	1	1	↑	XXXXXXXX	SP [15:8]								XX
	1	1	↑	XXXXXXXX	SP [7:0]								XX
	1	1	↑	XXXXXXXX	EP [15:8]								XX
	1	1	↑	XXXXXXXX	EP [7:0]								XX

Memory Write	0	1	↑	XXXXXXXX	0	0	1	0	1	1	0	0	2Ch
	1	1	↑	D [15:0]									XX
RGBSET	0	1	↑	XXXXXXXX	0	0	1	0	1	1	0	1	2Dh
	1	↑	1	XXXXXXXX	R00[5:0]								XX
	1	↑	1	XXXXXXXX	Rnn[5:0]								XX
	1	↑	1	XXXXXXXX	R31[5:0]								XX
	1	↑	1	XXXXXXXX	G00[5:0]								XX
	1	↑	1	XXXXXXXX	Gnn[5:0]								XX
	1	↑	1	XXXXXXXX	G63[5:0]								XX
	1	↑	1	XXXXXXXX	B00[5:0]								XX
	1	↑	1	XXXXXXXX	Bnn[5:0]								XX
	1	↑	1	XXXXXXXX	B31[5:0]								XX
Memory Read	0	1	↑	XXXXXXXX	0	0	1	0	1	1	1	0	2Eh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	D[15:0]									XX
Partial Area	0	1	↑	XXXXXXXX	0	0	1	1	0	0	0	0	30h
	1	1	↑	XXXXXXXX	SR[15:8]								XX
	1	1	↑	XXXXXXXX	SR[7:0]								XX
	1	1	↑	XXXXXXXX	ER[15:8]								XX
	1	1	↑	XXXXXXXX	ER[7:0]								XX
Vertical Scrolling Definition	0	1	↑	XXXXXXXX	0	0	1	1	0	0	1	1	33h
	1	1	↑	XXXXXXXX	TFA[15:9]								XX
	1	1	↑	XXXXXXXX	TFA[7:0]								XX
	1	1	↑	XXXXXXXX	VSA[15:8]								XX
	1	1	↑	XXXXXXXX	VSA[7:0]								XX
	1	1	↑	XXXXXXXX	BFA[15:8]								XX
	1	1	↑	XXXXXXXX	BFA[7:0]								XX
Tearing Effect Line OFF	0	1	↑	XXXXXXXX	0	0	1	1	0	1	0	0	34h
Tearing Effect Line ON	0	1	↑	XXXXXXXX	0	0	1	1	0	1	0	1	35h
	1	1	↑	XXXXXXXX	X	X	X	X	X	X	X	M	XX
Memory Access Control	0	1	↑	XXXXXXXX	0	0	1	1	0	1	1	0	36h
	1	1	↑	XXXXXXXX	D[7:2]						X	X	XX
Vertical Scrolling Start Address	0	1	↑	XXXXXXXX	0	0	1	1	0	1	1	1	37h
	1	1	↑	XXXXXXXX	VSP[15:8]								XX
	1	1	↑	XXXXXXXX	VSP[7:0]								XX
Idle Mode OFF	0	1	↑	XXXXXXXX	0	0	1	1	1	0	0	0	38h
Idle Mode ON	0	1	↑	XXXXXXXX	0	0	1	1	1	0	0	1	39h
Pixel Format Set	0	1	↑	XXXXXXXX	0	0	1	1	1	0	1	0	3Ah
	1	1	↑	XXXXXXXX	DPI[3:0]				X	DBI[2:0]			XX
Read ID1	0	1	↑	XXXXXXXX	1	1	0	1	1	1	1	1	DAh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	Module's Manufacture[7:0]								XX
Read ID2	0	1	↑	XXXXXXXX	1	1	0	1	1	0	1	0	DBh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	LCD Module / Driver Version[7:0]								XX
Read ID3	0	1	↑	XXXXXXXX	1	1	0	1	1	0	1	1	DCh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	LCD Module / Driver ID[7:0]								XX

Extended Command Set													
Command Function	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Interface Control	0	1	↑	XXXXXXXX	1	0	1	1	0	0	0	0	B0h
	1	1	↑	XXXXXXXX	0	0	0	0	VSPL	HSPL	DPL	EPL	XX
Frame Control 1	0	1	↑	XXXXXXXX	1	0	1	1	0	0	0	1	B1h
	1	1	↑	XXXXXXXX	0	0	0	0	0	0	DIVA[1:0]		XX
	1	1	↑	XXXXXXXX	0	0	0	RTNA[4:0]					XX
Frame Control 2	0	1	↑	XXXXXXXX	1	0	1	1	0	0	1	0	B2h
	1	1	↑	XXXXXXXX	0	0	0	0	0	0	DIVB[1:0]		XX
	1	1	↑	XXXXXXXX	0	0	0	RTNB[4:0]					XX
Frame Control 3	0	1	↑	XXXXXXXX	1	0	1	1	0	0	1	1	B3h
	1	1	↑	XXXXXXXX	0	0	0	0	0	0	DIVC[1:0]		XX
	1	1	↑	XXXXXXXX	0	0	0	RTNC[4:0]					XX
Display Inversion Control	0	1	↑	XXXXXXXX	1	0	1	1	0	1	0	0	B4h
	1	1	↑	XXXXXXXX	0	0	0	0	0	NLA	NLB	NLC	XX
	1	1	↑	XXXXXXXX	0	0	NW[5:0]						XX
Blanking Porch Control	0	1	↑	XXXXXXXX	1	0	1	1	0	1	0	1	B5h
	1	1	↑	XXXXXXXX	0	VFP[6:0]							XX
	1	1	↑	XXXXXXXX	0	VBP[6:0]							XX
	1	1	↑	XXXXXXXX	0	0	0	HFP[4:0]					XX
	1	1	↑	XXXXXXXX	0	0	0	HBP[4:0]					XX
Display Function Control	0	1	↑	XXXXXXXX	1	0	1	1	0	1	1	0	B6h
	1	1	↑	XXXXXXXX	0	0	0	0	PTG[1:0]		PT[1:0]		XX
	1	1	↑	XXXXXXXX	0	GS	SS	SM	ISC[3:0]				XX
	1	1	↑	XXXXXXXX	0	0	NL[5:0]						XX
Entry Mode Set	0	1	↑	XXXXXXXX	1	0	1	1	0	1	1	1	B7h
	1	1	↑	XXXXXXXX	0	0	0	0	DSTB	GON	DTE	GAS	XX
Power Control 1	0	1	↑	XXXXXXXX	1	1	0	0	0	0	0	0	C0h
	1	1	↑	XXXXXXXX	0	0	VRH[5:0]						XX
	1	1	↑	XXXXXXXX	0	0	0	0	0	VC[2:0]			XX
Power Control 2	0	1	↑	XXXXXXXX	1	1	0	0	0	0	0	1	C1h
	1	1	↑	XXXXXXXX	0	SAP[2:0]			0	BT[2:0]			XX
Power Control 3	0	1	↑	XXXXXXXX	1	1	0	0	0	0	1	0	C2h
	1	1	↑	XXXXXXXX	0	DCA1[2:0]			0	DCA0[2:0]			XX
Power Control 4	0	1	↑	XXXXXXXX	1	1	0	0	0	0	1	1	C3h
	1	1	↑	XXXXXXXX	0	DCB1[2:0]			0	DCB0[2:0]			XX
Power Control 5	0	1	↑	XXXXXXXX	1	1	0	0	0	1	0	0	C4h
	1	1	↑	XXXXXXXX	0	DCC2[2:0]			0	DCC0[2:0]			XX
VCOM Control 1	0	1	↑	XXXXXXXX	1	1	0	0	0	1	0	1	C5h
	1	1	↑	XXXXXXXX	0	VMH[6:0]							XX
	1	1	↑	XXXXXXXX	0	VML[6:0]							XX
VCOM Control 2	0	1	↑	XXXXXXXX	1	1	0	0	0	1	1	1	C7h
	1	1	↑	XXXXXXXX	nVM	VMF[6:0]							XX
NV Memory Write	0	1	↑	XXXXXXXX	1	1	0	1	0	0	0	0	D0h
	1	1	↑	XXXXXXXX	0	0	0	0	0	PGM_ADR[2:0]			XX
	1	1	↑	XXXXXXXX	PGM_DATA[7:0]								XX
NV Memory Protection Key	0	1	↑	XXXXXXXX	1	1	0	1	0	0	0	1	D1h
	1	1	↑	XXXXXXXX	KEY[23:16]								XX
	0	↑	1	XXXXXXXX	KEY[15:8]								XX
	1	↑	1	XXXXXXXX	KEY[7:0]								XX
NV Memory Status Read	1	↑	1	XXXXXXXX	1	1	0	1	0	0	1	0	D2h
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	0	1	↑	XXXXXXXX	ID3_CNT[3:0]				ID2_CNT[3:0]				XX
	1	1	↑	XXXXXXXX	BUSY	X	X	X	VMF_CNT[3:0]				XX
	1	1	↑	XXXXXXXX	OTP_DATA[7:0]								XX

Read ID4	0	↑	1	XXXXXXXX	1	1	0	1	0	0	1	1	D3h
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	0	0	0	0	0	0	0	0	00h
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	0	0	1	1	1	0	0	0	38h
Positive Gamma Correction	0	1	↑	XXXXXXXX	1	1	1	0	0	0	0	0	E0h
	1	1	↑	XXXXXXXX	0	0	0	0	VP63[3:0]				XX
	1	1	↑	XXXXXXXX	0	0	VP62[5:0]						XX
	1	1	↑	XXXXXXXX	0	0	VP61[5:0]						XX
	1	1	↑	XXXXXXXX	0	0	0	0	VP59[3:0]				XX
	1	1	↑	XXXXXXXX	0	0	0	VP57[4:0]					XX
	1	1	↑	XXXXXXXX	0	0	0	0	VP50[3:0]				XX
	1	1	↑	XXXXXXXX	0	VP20[6:0]							XX
	1	1	↑	XXXXXXXX	VP36[3:0]				VP27[3:0]				XX
	1	1	↑	XXXXXXXX	0	VP20[6:0]							XX
	1	1	↑	XXXXXXXX	0	0	0	0	VP13[3:0]				XX
	1	1	↑	XXXXXXXX	0	0	0	VP6[4:0]					XX
	1	1	↑	XXXXXXXX	0	0	0	0	VP4[3:0]				XX
	1	1	↑	XXXXXXXX	0	0	VP2[5:0]						XX
	1	1	↑	XXXXXXXX	0	0	VP1[5:0]						XX
	1	1	↑	XXXXXXXX	0	0	0	0	VP0[3:0]				XX
Negative Gamma Correction	0	1	↑	XXXXXXXX	1	1	1	0	0	0	0	1	E1h
	1	1	↑	XXXXXXXX	0	0	0	0	VN63[3:0]				XX
	1	1	↑	XXXXXXXX	0	0	VN62[5:0]						XX
	1	1	↑	XXXXXXXX	0	0	VN61[5:0]						XX
	1	1	↑	XXXXXXXX	0	0	0	0	VN59[3:0]				XX
	1	1	↑	XXXXXXXX	0	0	0	VN57[4:0]					XX
	1	1	↑	XXXXXXXX	0	0	0	0	VN50[3:0]				XX
	1	1	↑	XXXXXXXX	0	VN43[6:0]							XX
	1	1	↑	XXXXXXXX	VN36[3:0]				VN27[3:0]				XX
	1	1	↑	XXXXXXXX	0	VN20[6:0]							XX
	1	1	↑	XXXXXXXX	0	0	0	0	VN13[3:0]				XX
	1	1	↑	XXXXXXXX	0	0	0	VN6[4:0]					XX
	1	1	↑	XXXXXXXX	0	0	0	0	VN4[3:0]				XX
	1	1	↑	XXXXXXXX	0	0	VN2[5:0]						XX
	1	1	↑	XXXXXXXX	0	0	VN1[5:0]						XX
	1	1	↑	XXXXXXXX	0	0	0	0	VN0[5:0]				XX

Note 1: Undefined commands are treated as NOP (00h) command.

Note 2: B0 to D9 and DE to FF are for factory use of display supplier. USER can decide if these commands are available or they are treated as NOP (00h) commands before shipping to USER. Default value is NOP (00h).

Note 3: Commands 10h, 12h, 13h, 26h, 28h, 29h, 30h, 36h (Bit B4 only), 38h and 39h are updated during V-SYNC when ILI9338B is in Sleep OUT mode to avoid abnormal visual effects. During Sleep IN mode, these commands are updated immediately. Read status (09h), Read display power mode (0Ah), Read display MADCTL (0Bh), Read display pixel format (0Ch), Read display image mode (0Dh), Read display signal mode (0Eh) and Read display self diagnostic result (0Fh) of these commands are updated immediately both in Sleep IN mode and Sleep OUT mode.

8.2. Command Description

8.2.1. NOP (00h)

<table>
<tr><th>00h</th><th colspan="12">NOP (No Operation)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D [15:8]</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XXXXXXXX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter.</td></tr>
<tr><td>Description</td><td colspan="13">This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">None</td></tr>
</table>

8.2.2. Software Reset (01h)

01h	SWRESET												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	0	0	0	0	1	01h
Parameter	No Parameter.												
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are unaffected by this command X = Don't care.												
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.												

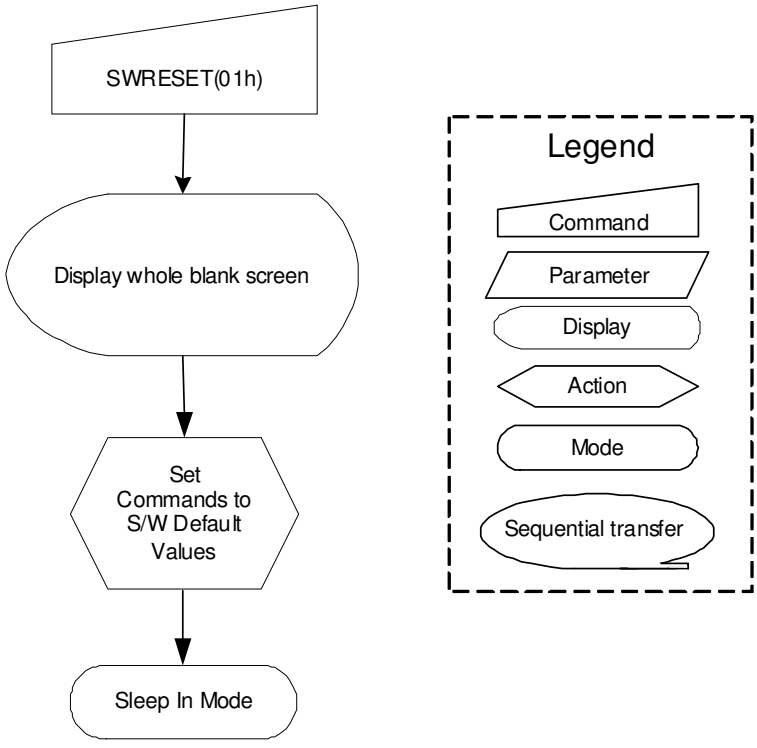
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A

Flow Chart



8.2.3. Read display identification information (04h)

04h	RDDIDIF (Read Display Identification Information)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	0	0	1	0	0	04h
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	X
2ndParameter	1	↑	1	XXXXXXXX	ID1 [7:0]								XX
3rd Parameter	1	↑	1	XXXXXXXX	ID2 [7:0]								XX
4th Parameter	1	↑	1	XXXXXXXX	ID3 [7:0]								XX

Description

This read byte returns 24 bits display identification information.

The 1st parameter is dummy data.

The 2nd parameter (ID1 [7:0]): LCD module's manufacturer ID.

The 3rd parameter (ID2 [7:0]): LCD module/driver version ID.

The 4th parameter (ID3 [7:0]): LCD module/driver ID.

Restriction

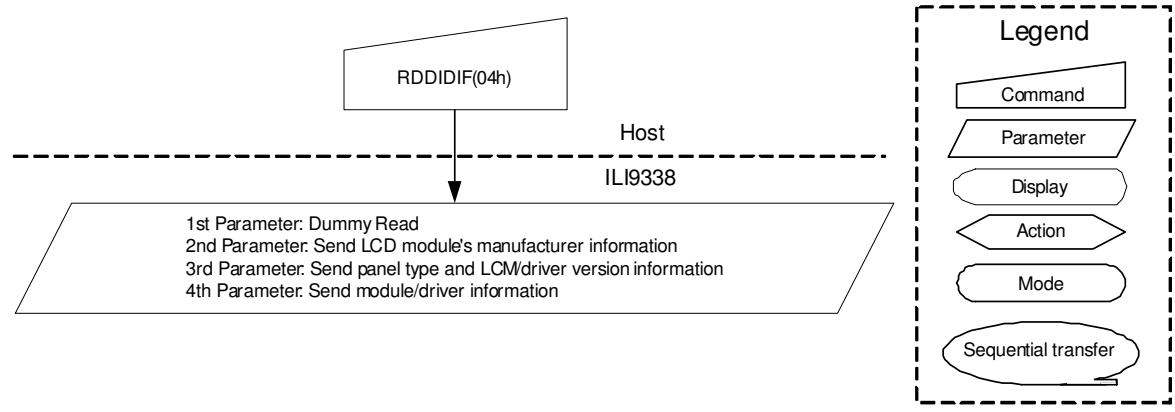
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	See description
SW Reset	See description
HW Reset	See description

Flow Chart



8.2.4. Read Display Status (09h)

09h	RDDST (Read Display Status)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	0	1	0	0	1	09h
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XXXXXXXX	D [31:25]							0	XX
3rd Parameter	1	↑	1	XXXXXXXX	0	D [22:20]			D [19:16]				XX
4th Parameter	1	↑	1	XXXXXXXX	0	0	0	0	0	D [10:8]			XX
5th Parameter	1	↑	1	XXXXXXXX	D [7:5]			0	0	0	0	0	XX

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value	Status
D31	Booster voltage status	0	Booster OFF
		1	Booster ON
D30	Row address order	0	Top to Bottom (When MADCTL B7='0')
		1	Bottom to Top (When MADCTL B7='1')
D29	Column address order	0	Left to Right (When MADCTL B6='0').
		1	Right to Left (When MADCTL B6='1').
D28	Row/column exchange	0	Normal Mode (When MADCTL B5='0').
		1	Reverse Mode (When MADCTL B5='1').
D27	Vertical refresh	0	LCD Refresh Top to Bottom (When MADCTL B4='0')
		1	LCD Refresh Bottom to Top (When MADCTL B4='1').
D26	RGB/BGR order	0	RGB (When MADCTL B3='0')
		1	BGR (When MADCTL B3='1')
D25	Horizontal refresh order	0	LCD Refresh Left to Right (When MADCTL B2='0')
		1	LCD Refresh Right to Left (When MADCTL B2='1')
D24	Not used	0	---
D23	Not used	0	---
D22 D21 D20	Interface color pixel format definition	101	16-bit/pixel
		110	18-bit/pixel
D19	Idle mode ON/OFF	0	Idle Mode OFF
		1	Idle Mode ON
D18	Partial mode ON/OFF	0	Partial Mode OFF
		1	Partial Mode ON.
D17	Sleep IN/OUT	0	Sleep IN Mode
		1	Sleep OUT Mode.
D16	Display normal mode ON/OFF	0	Display Normal Mode OFF.
		1	Display Normal Mode ON.
D15	Vertical scrolling status	0	Scroll OFF
D14	Not used	0	---
D13	Inversion status	0	Not defined
D12	All pixel ON	0	Not defined
D11	All pixel OFF	0	Not defined
D10	Display ON/OFF	0	Display is OFF
		1	Display is ON
D9	Tearing effect line ON/OFF	0	Tearing Effect Line OFF
		1	Tearing Effect ON
D[8:6]	Gamma curve selection	000	GC0
		001	GC1
		010	GC2
		011	GC3
		other	Not defined
D5	Tearing effect line mode	0	Mode 1, V-Blanking only
		1	Mode 2, both H-Blanking and V-Blanking.
D4	Not used	0	---

D3	Not used	0	---
D2	Not used	0	---
D1	Not used	0	---
D0	Not used	0	---

X = Don't care

Restriction

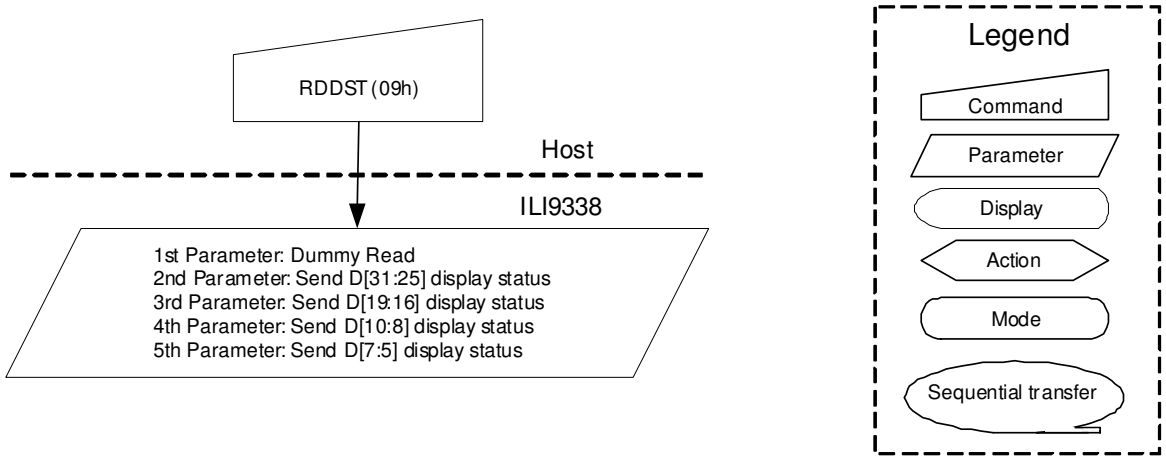
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	See description
SW Reset	See description
HW Reset	See description

Flow Chart



8.2.5. Read Display Power Mode (0Ah)

0Ah	RDDPM (Read Display Power Mode)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	0	1	0	1	0	0Ah
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XXXXXXXX	D7	D6	D5	D4	D3	D2	D1	D0	XX

Description

This command indicates the current status of the display as described in the table below::

Bit	Value	Description	Comment
D7	0	Booster Off or has a fault.	---
	1	Booster On and working OK	---
D6	0	Idle Mode Off.	---
	1	Idle Mode On.	---
D5	0	Partial Mode Off.	---
	1	Partial Mode On.	---
D4	0	Sleep In Mode	---
	1	Sleep Out Mode	---
D3	0	Display Normal Mode Off.	---
	1	Display Normal Mode On	---
D2	0	Display is Off.	---
	1	Display is On	---
D1	--	Not Defined	Set to '0'
D0	--	Not Defined	Set to '0'

X = Don't care

Restriction

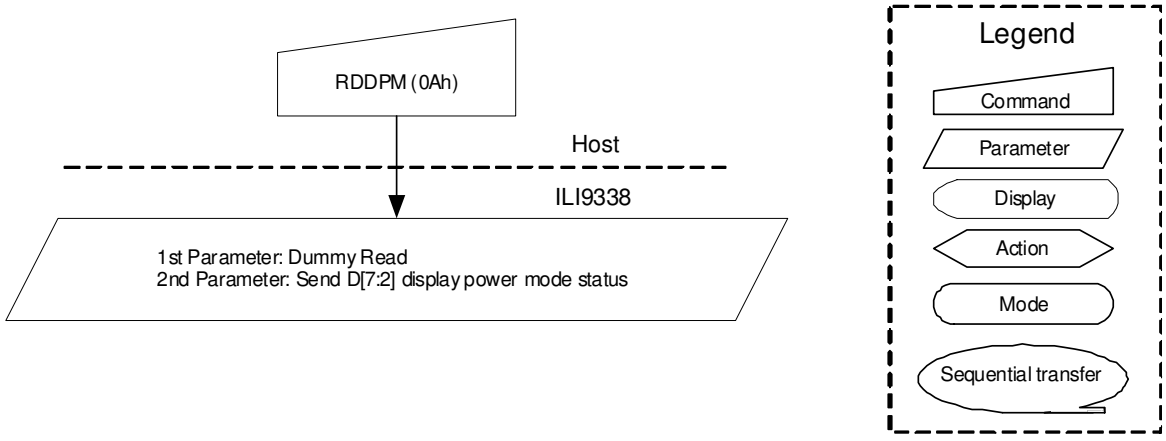
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08h
SW Reset	08h
HW Reset	08h

Flow Chart



8.2.6. Read Display MADCTL (0Bh)

0Bh	RDDMADCTL (Read Display MADCTL)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	0	1	0	1	1	0Bh
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XXXXXXXX	D7	D6	D5	D4	D3	D2	D1	D0	XX

Description

This command indicates the current status of the display as described in the table below:

Bit	Value	Description	Comment
D7	0	Top to Bottom (When MADCTL B7='0').	---
	1	Bottom to Top (When MADCTL B7='1').	---
D6	0	Left to Right (When MADCTL B6='0')	---
	1	Right to Left (When MADCTL B6='1')	---
D5	0	Normal Mode (When MADCTL B5='0').	---
	1	Reverse Mode (When MADCTL B5='1')	---
D4	0	LCD Refresh Top to Bottom (When MADCTL B4='0')	---
	1	LCD Refresh Bottom to Top (When MADCTL B4='1').	---
D3	0	RGB (When MADCTL B3='0')	---
	1	BGR (When MADCTL B3='1').	---
D2	0	LCD Refresh Left to Right (When MADCTL B2='0').	---
	1	LCD Refresh Right to Left (When MADCTL B2='1').	---
D1	--	Switching between Segment outputs and RAM	Set to '0'
D0	--	Switching between Segment outputs and RAM	Set to '0'

X = Don't care

Restriction

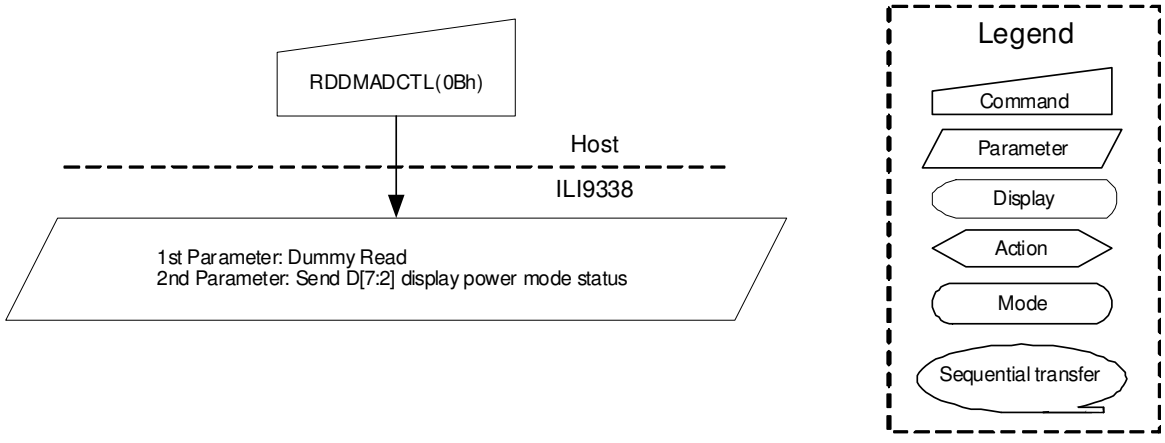
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	No Change
HW Reset	00h

Flow Chart



8.2.7. Read Display Pixel Format (0Ch)

0Ch	RDDCOLMOD (Read Display Pixel Format)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	0	1	1	0	0	0Ch
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XXXXXXXX	DPI [3:0]				0	DBI [2:0]			XX

Description

This command indicates the current status of the display as described in the table below:

DPI [3:0]				RGB Interface Format
0	0	0	0	Reserved
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	16 bits / pixel
0	1	1	0	18 bits / pixel
0	1	1	1	Reserved
1	1	1	0	18 bits / pixel (3 times data transfer)

DBI [2:0]			MCU Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

X = Don't care

Restriction

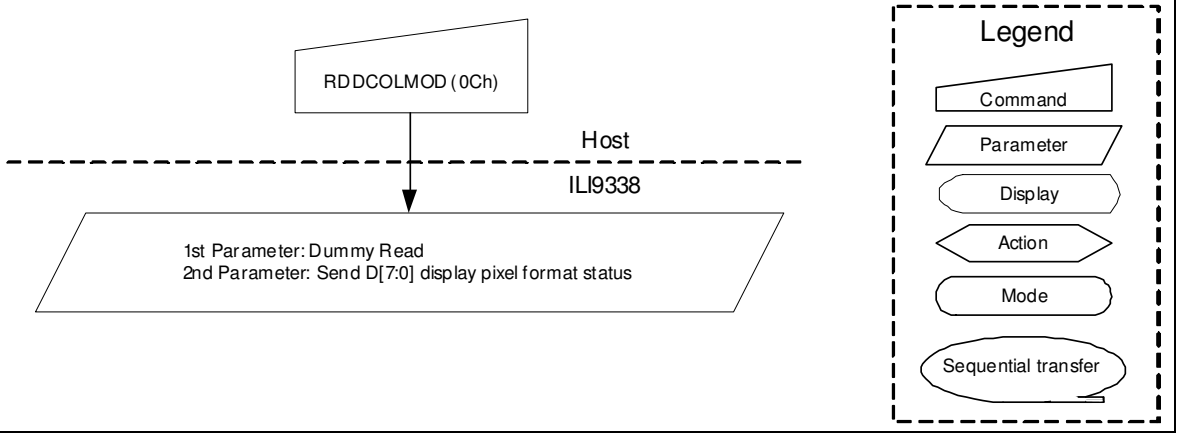
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000 0110b
SW Reset	No Chang
HW Reset	0000 0110b

Flow Chart



8.2.8. Read Display Image Format (0Dh)

0Dh	RDDIM (Read Display Image Mode)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	0	1	1	0	1	0Dh
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XXXXXXXX	0	0	0	0	0	D [2:0]			XX

Description

This command indicates the current status of the display as described in the table below:

D [2:0]	Description
000	Gamma curve 1
001	Gamma curve 2
010	Gamma curve 3
011	Gamma curve 4
Other	Not defined

X = Don't care

Restriction

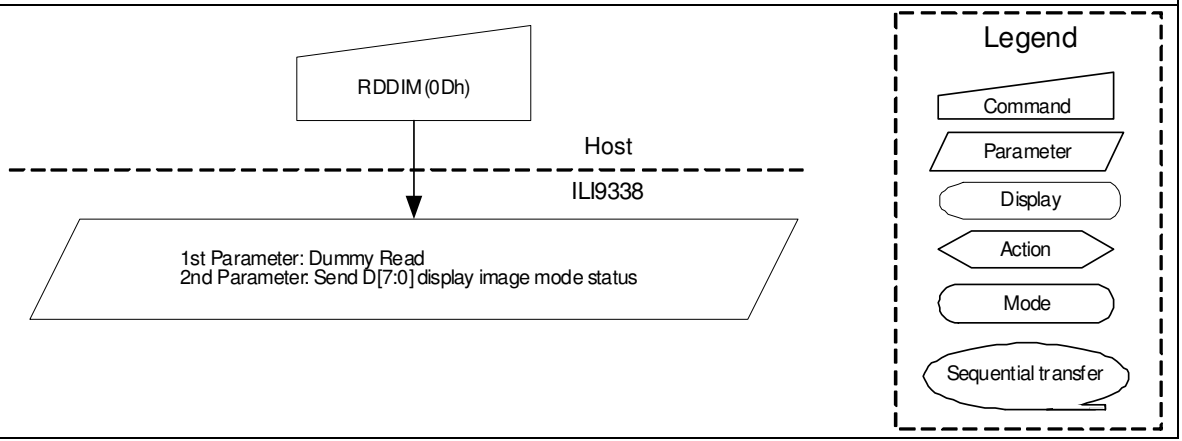
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



8.2.9. Read Display Signal Mode (0Eh)

0Eh	RDDSM (Read Display Signal Mode)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	0	1	1	1	0	0Eh
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XXXXXXXX	D7	D6	D5	D4	D3	D2	D1	D0	XX

Description

This command indicates the current status of the display as described in the table below:

Bit	Value	Description
D7	0	Tearing effect line OFF
	1	Tearing effect line ON
D6	0	Tearing effect line mode 1
	1	Tearing effect line mode 2
D5	0	Horizontal sync. (RGB interface) OFF
	1	Horizontal sync. (RGB interface) ON
D4	0	Vertical sync. (RGB interface) OFF
	1	Vertical sync. (RGB interface) ON
D3	0	Pixel clock (DOTCLK, RGB interface) OFF
	1	Pixel clock (DOTCLK, RGB interface) ON
D2	0	Data enable (DE, RGB interface) OFF
	1	Data enable (DE, RGB interface) ON
D1	0	Reserved
D0	0	Reserved

X = Don't care

Restriction

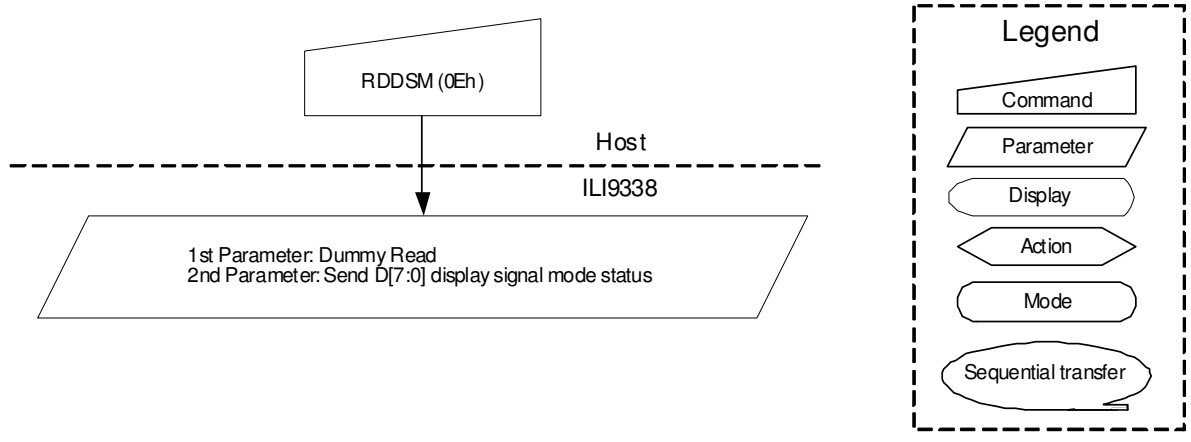
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



8.2.10. Read Display Self-Diagnostic Result (0Fh)

0Fh	RDDSDR (Read Display Self-Diagnostic Result)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	0	1	1	1	1	0Fh
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XXXXXXXX	D7	D6	0	0	0	0	0	0	XX

Description

Bit	Description	Action
D7	Register Loading Detection	Invert the D7 bit if register values loading work properly.
D6	Functionality Detection	Invert the D6 bit if the display is functionality
D5	Not Used	'0'
D4	Not Used	'0'
D3	Not Used	'0'
D2	Not Used	'0'
D1	Not Used	'0'
D0	Not Used	'0'

Restriction

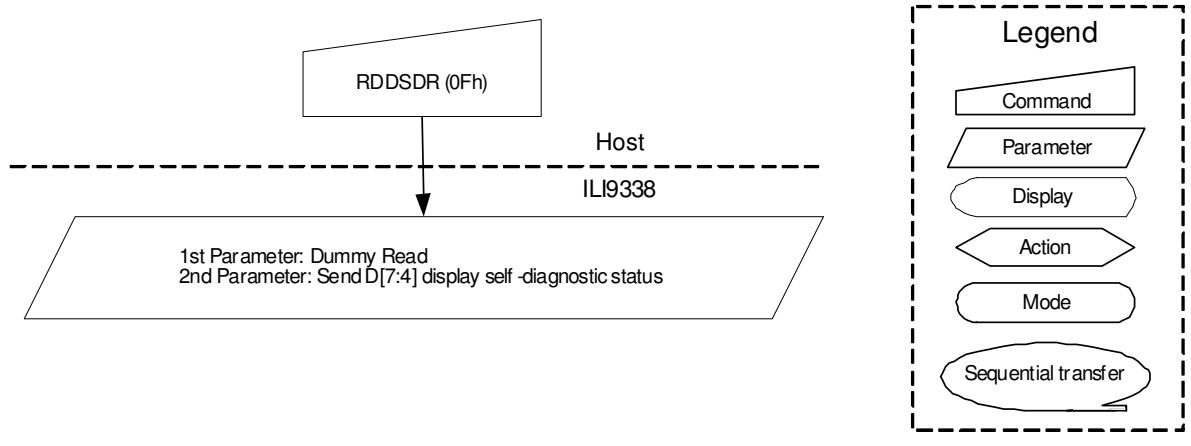
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



8.2.11. Enter Sleep Mode (10h)

10h	SPLIN (Enter Sleep Mode)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	1	0	0	0	0	10h
Parameter	No Parameter												
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped. Out → Blank → STOP MCU interface and memory are still working and the memory keeps its contents. X = Don't care												
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.												

Register Availability

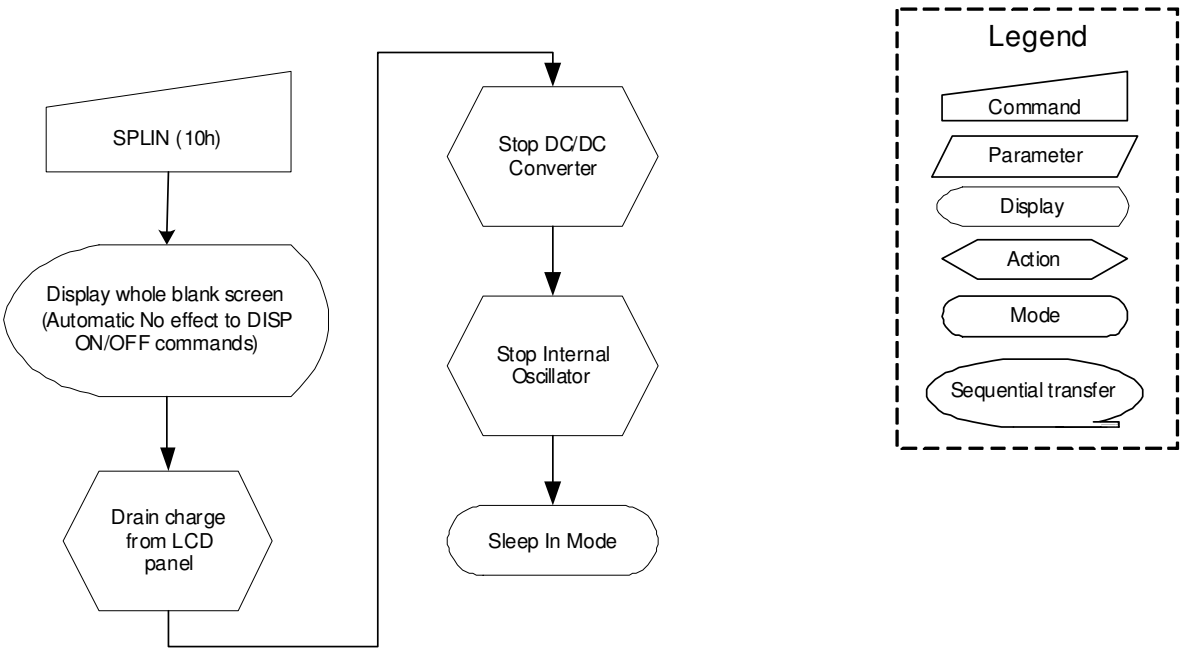
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

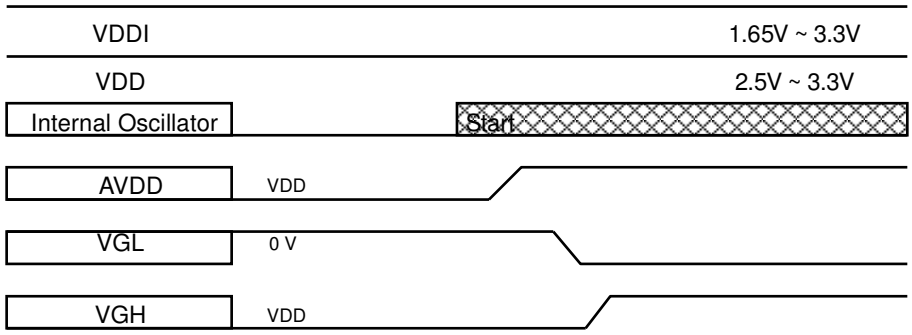
Status	Default Value
Power On Sequence	Sleep IN Mode
SW Reset	Sleep IN Mode
HW Reset	Sleep IN Mode

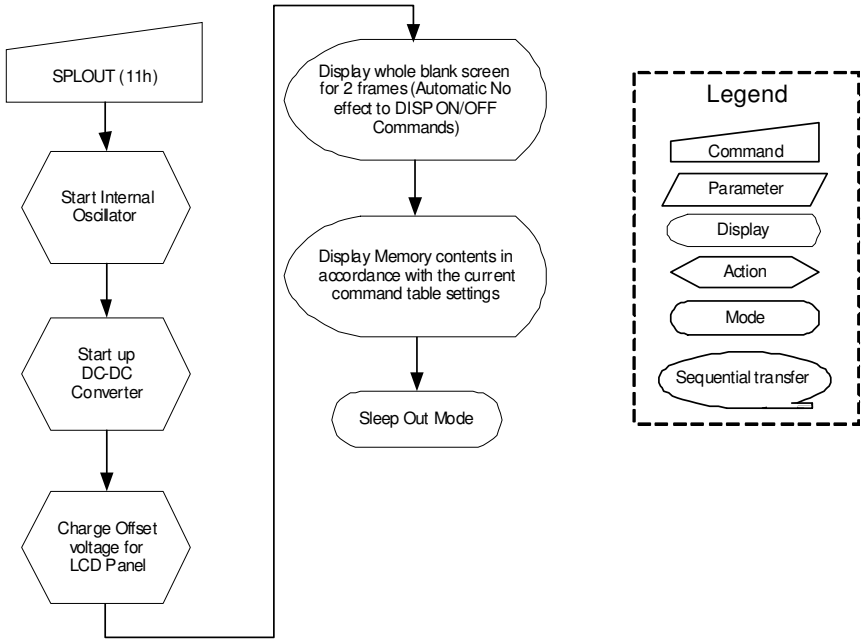
Flow Chart

It takes 120msec to get into Sleep In mode after SLPIN command issued.



8.2.12. Sleep Out (11h)

11h	SLPOUT (Sleep Out)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	1	0	0	0	1	11h
Parameter	No Parameter												
Description	This command turns off sleep mode. In this mode e.g. the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.  X = Don't care												
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.												
Register Availability	Status / Availability: Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes												
Default	Status / Default Value: Power On Sequence: Sleep IN Mode SW Reset: Sleep IN Mode HW Reset: Sleep IN Mode												
Flow Chart	It takes 120msec to become Sleep Out mode after SLPOUT command issued.												



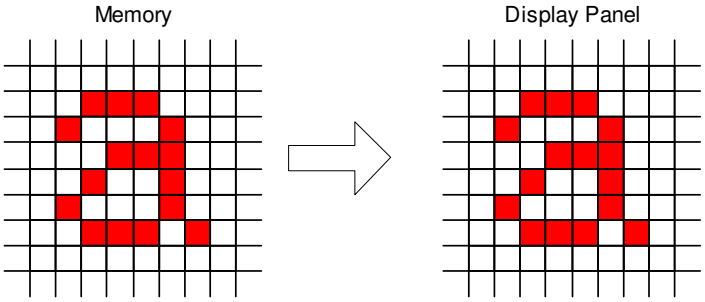
8.2.13. Partial Mode ON (12h)

<table>
<tr><th>12h</th><th colspan="12">PTLON (Partial Mode On)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D [15:8]</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XXXXXXXX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode ON</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

8.2.14. Normal Display Mode ON (13h)

<table>
<tr><th>13h</th><th colspan="12">NORON (Normal Display Mode On)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D [15:8]</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XXXXXXXX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command returns the display to normal mode.
Normal display mode on means Partial mode off.
Exit from NORON by the Partial mode On command (12h)
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode ON</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

8.2.15. Display Inversion OFF (20h)

20h	DINVOFF (Display Inversion OFF)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	0	0	0	0	0	20h
Parameter	No Parameter												
Description	This command is used to recover from display inversion mode. This command makes no change of the content of frame memory. This command doesn't change any other status.  X = Don't care												
Restriction	This command has no effect when module already is inversion OFF mode.												

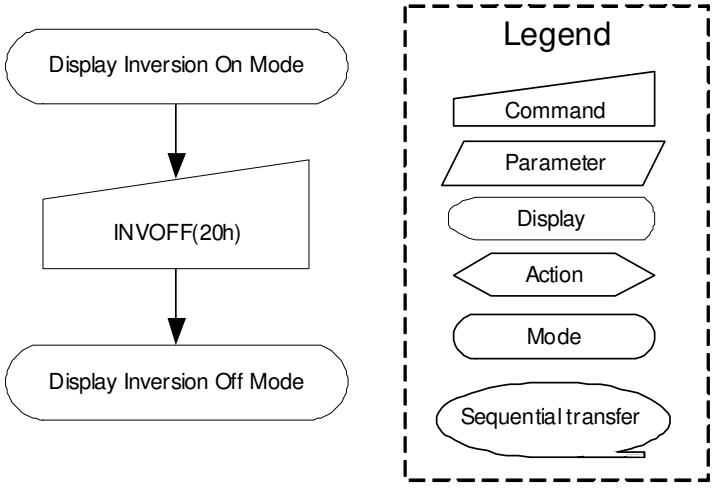
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart



8.2.16. Display Inversion ON (21h)

21h	DINVON (Display Inversion ON)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	0	0	0	0	1	21h
Parameter	No Parameter												

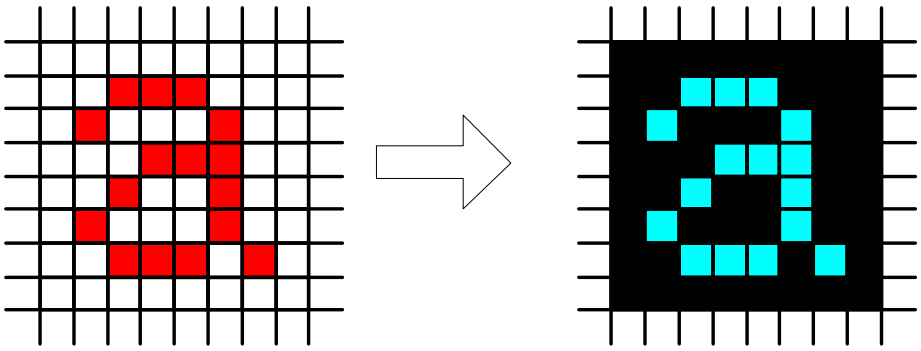
Description

This command is used to enter into display inversion mode.

This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display.

This command doesn't change any other status.

To exit Display inversion mode, the Display inversion OFF command (20h) should be written.



X = Don't care

Restriction

This command has no effect when module already is inversion ON mode.

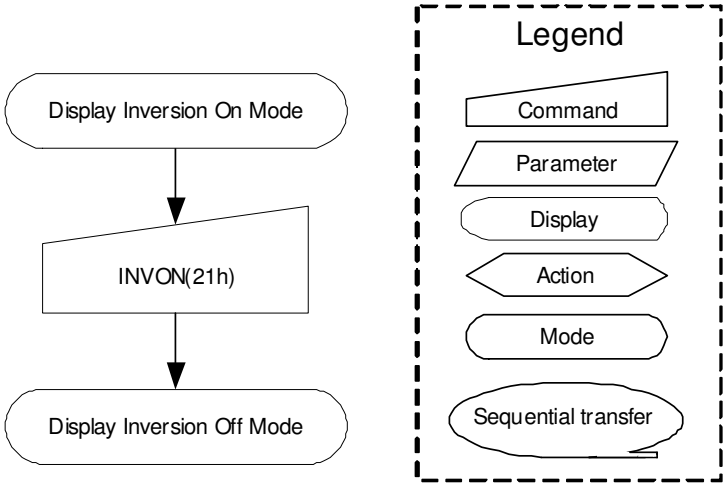
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

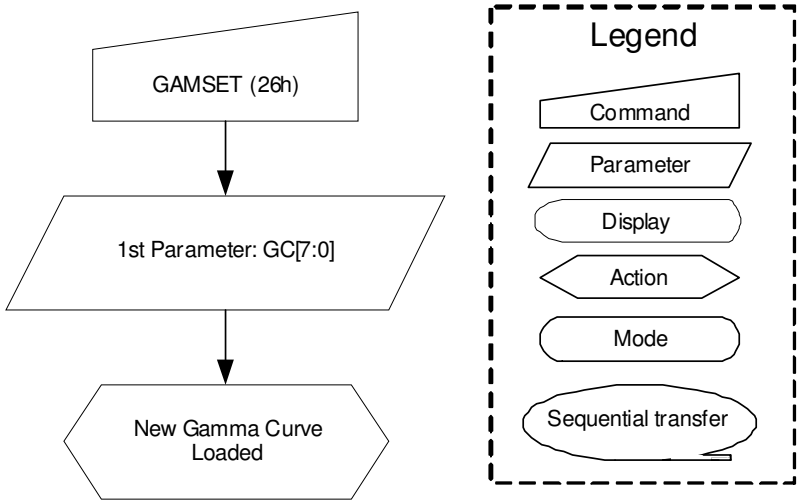
Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

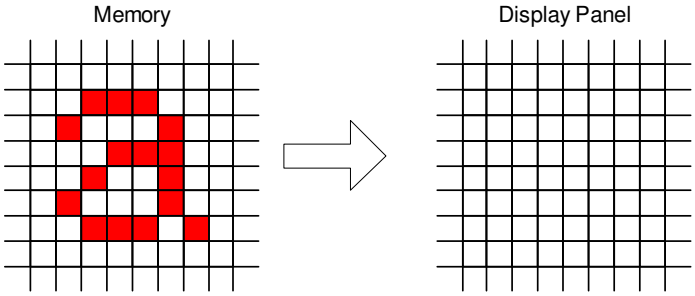
Flow Chart



8.2.17. Gamma Set (26h)

<table>
<tr><th>26h</th><th colspan="12">GAMSET (Gamma Set)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D [15:8]</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XXXXXXXX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>26h</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XXXXXXXX</td><td colspan="8">GC[7:0]</td><td>XX</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table:
<table>
<tr><th>GC[7:0]</th><th>Parameter</th><th>Curve Selected</th></tr>
<tr><td>01h</td><td>GC0</td><td>Gamma curve 1 (G2.2)</td></tr>
<tr><td>02h</td><td>GC1</td><td>Gamma curve 2 (G1.8)</td></tr>
<tr><td>04h</td><td>GC2</td><td>Gamma curve 3 (G2.5)</td></tr>
<tr><td>08h</td><td>GC3</td><td>Gamma curve 4 (G1.0)</td></tr>
</table>
Note: All other values are undefined.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">Values of GC [7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>01h</td></tr>
<tr><td>SW Reset</td><td>01h</td></tr>
<tr><td>HW Reset</td><td>01h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

8.2.18. Display OFF (28h)

28h	DISPOFF (Display OFF)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	0	1	0	0	0	28h
Parameter	No Parameter												
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display.  X = Don't care.												
Restriction	This command has no effect when module is already in display off mode.												

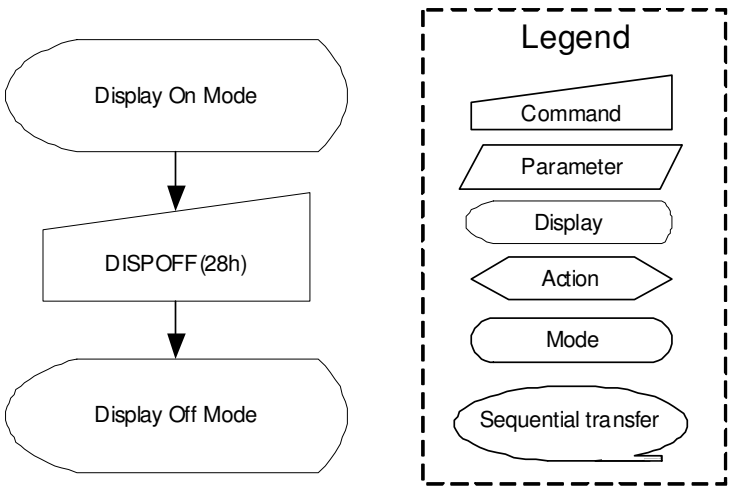
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

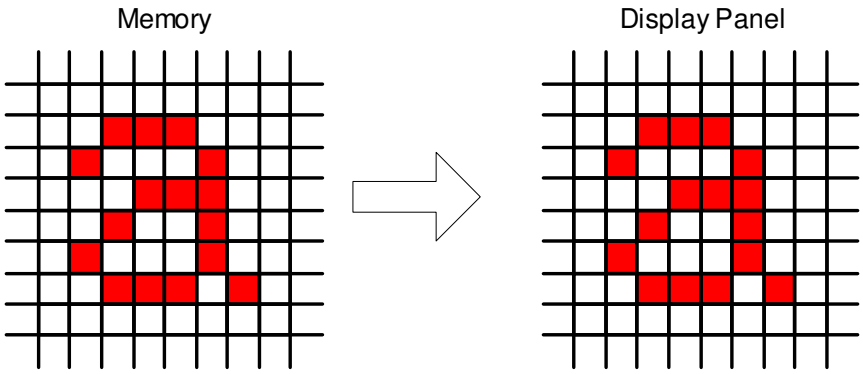
Default

Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart



8.2.19. Display ON (29h)

29h	DISPON (Display ON)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	0	1	0	0	1	29h
Parameter	No Parameter												
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status  X = Don't care.												
Restriction	This command has no effect when module is already in display on mode.												

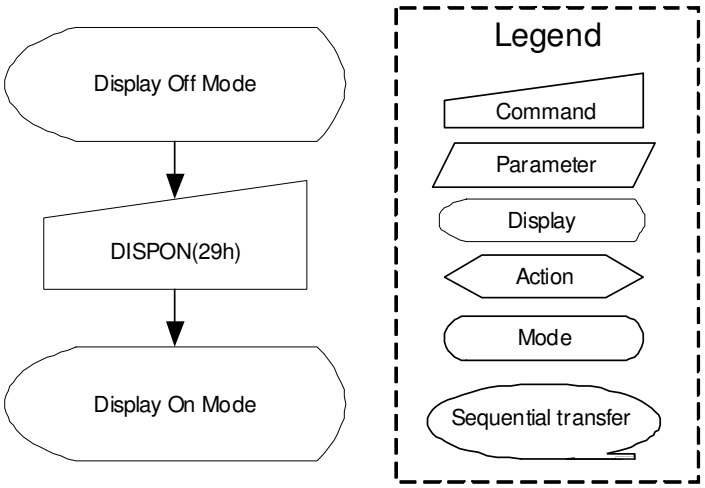
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart

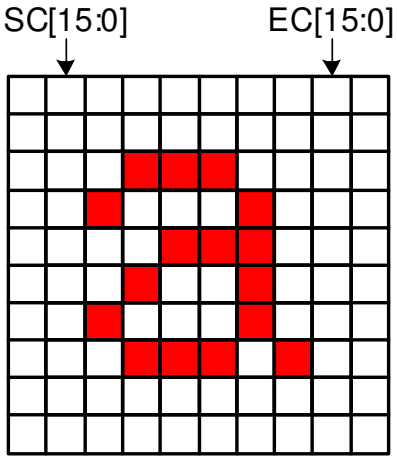


8.2.20. Column Address Set (2Ah)

2Ah	CASET (Column Address Set)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	0	1	0	1	0	2Ah
1st Parameter	1	1	↑	XXXXXXXX	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Note1
2ndParameter	1	1	↑	XXXXXXXX	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	
3rd Parameter	1	1	↑	XXXXXXXX	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	Note1
4th Parameter	1	1	↑	XXXXXXXX	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	

Description

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC [15:0] and EC [15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.



X = Don't care

Restriction

SC [15:0] always must be equal to or less than EC [15:0].

Note 1: When SC[15:0] or EC[15:0] is greater than 00EFh (When MADCTL's B5 = 0) or 013Fh (When MADCTL's B5 = 1), data of out of range will be ignored

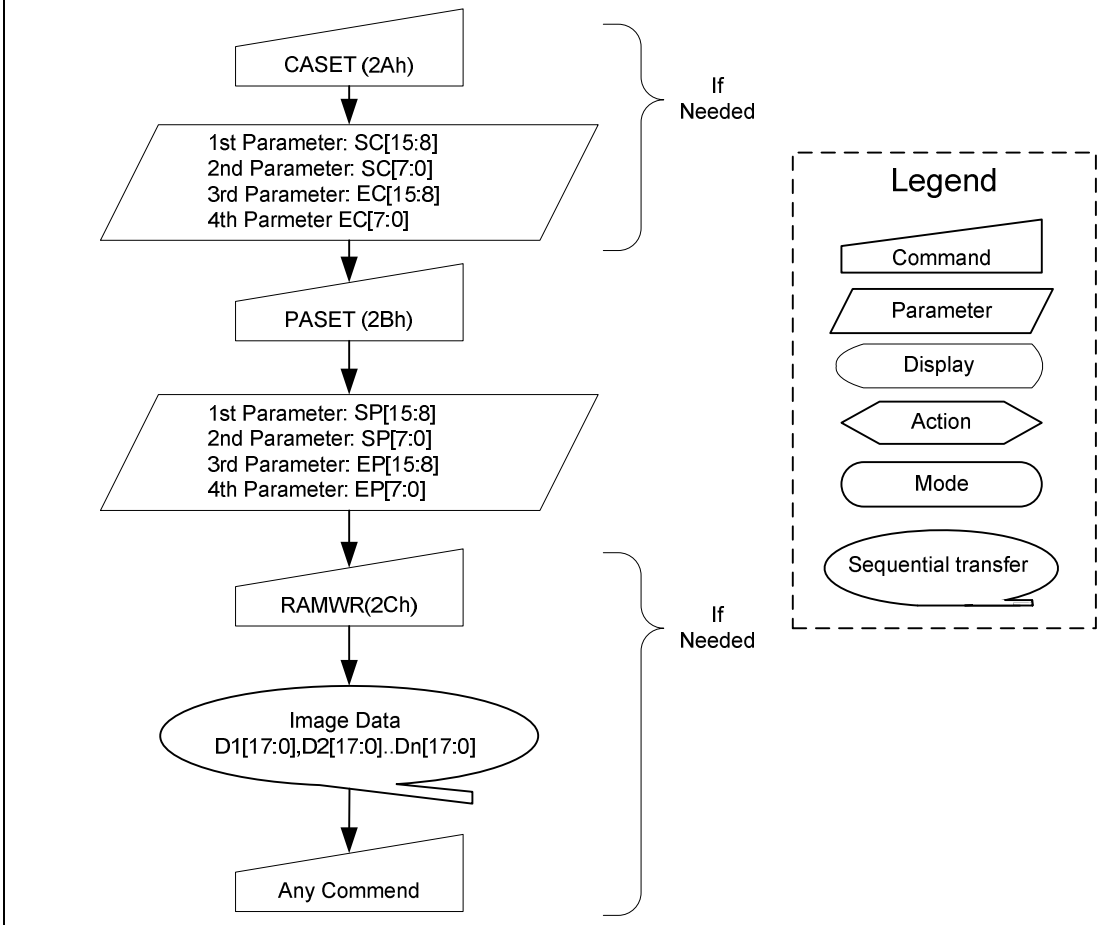
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SC[15:0]=0000h	EC[15:0]=00EFh
SW Reset	SC[15:0]=0000h	If MADCTL's B5 = 0: EC[15:0]=00EFh If MADCTL's B5 = 1: EC[15:0]=013Fh
HW Reset	SC[15:0]=0000h	EC[15:0]=00EFh

Flow Chart

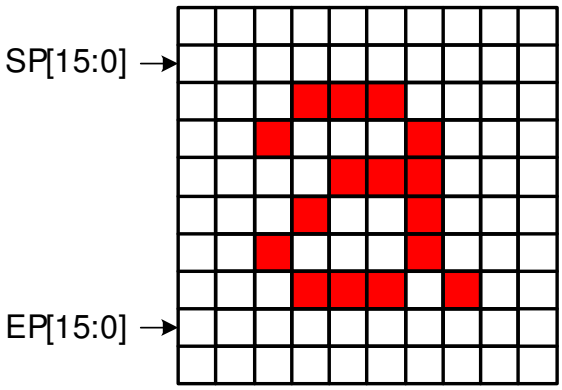


8.2.21. Page Address Set (2Bh)

2Bh	PASET (Page Address Set)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	0	1	0	1	1	2Bh
1st Parameter	1	1	↑	XXXXXXXX	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	Note1
2ndParameter	1	1	↑	XXXXXXXX	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
3rdParameter	1	1	↑	XXXXXXXX	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	Note1
4th Parameter	1	1	↑	XXXXXXXX	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	

Description

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.



X = Don't care

Restriction

SP[15:0] always must be equal to or less than EP[15:0]

When SP [15:0] or EP[15:0] is greater than 013Fh (When MADCTL's B5 = 0) or 00EFh (When MADCTL's B5 = 1), data of out of range will be ignored.

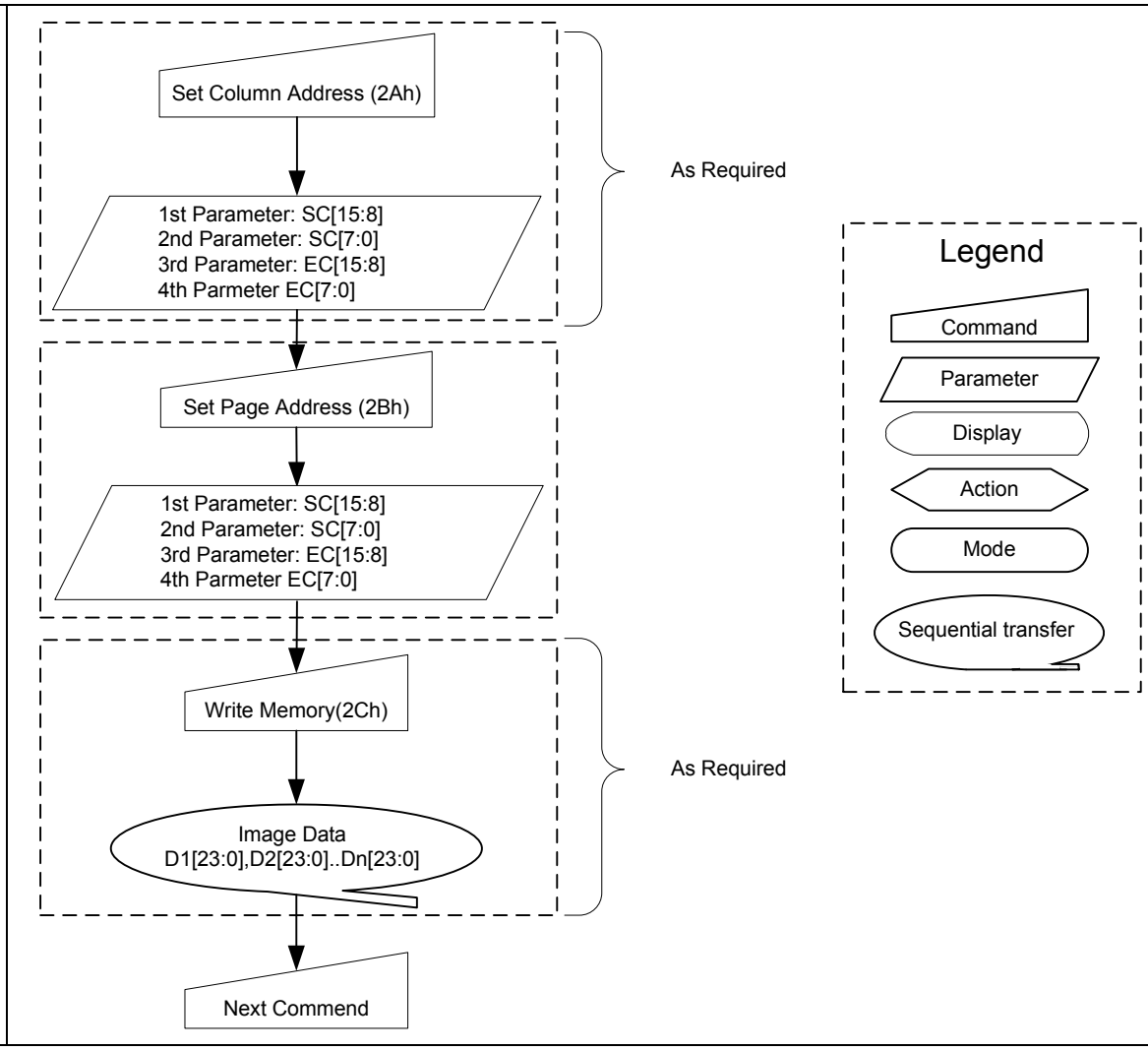
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SP[15:0]=0000h	EP[15:0]=013Fh
SW Reset	SP[15:0]=0000h	If MADCTL's B5 = 0: EP[15:0]=013Fh If MADCTL's B5 = 1: EP[15:0]=00EFh
HW Reset	SP[15:0]=0000h	EP[15:0]=013Fh

Flow Chart



8.2.22. Memory Write (2Ch)

2Ch	RAMWR (Memory Write)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	0	1	1	0	0	2Ch
1st Parameter	1	1	↑	D1[15:0]									XXXX
:	1	1	↑	Dx[15:0]									XXXX
Nth Parameter	1	1	↑	Dn[15:0]									XXXX
Description	This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting.) Then D [17:0] is stored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write. X = Don't care.												
Restriction	In all color modes, there is no restriction on length of parameters.												

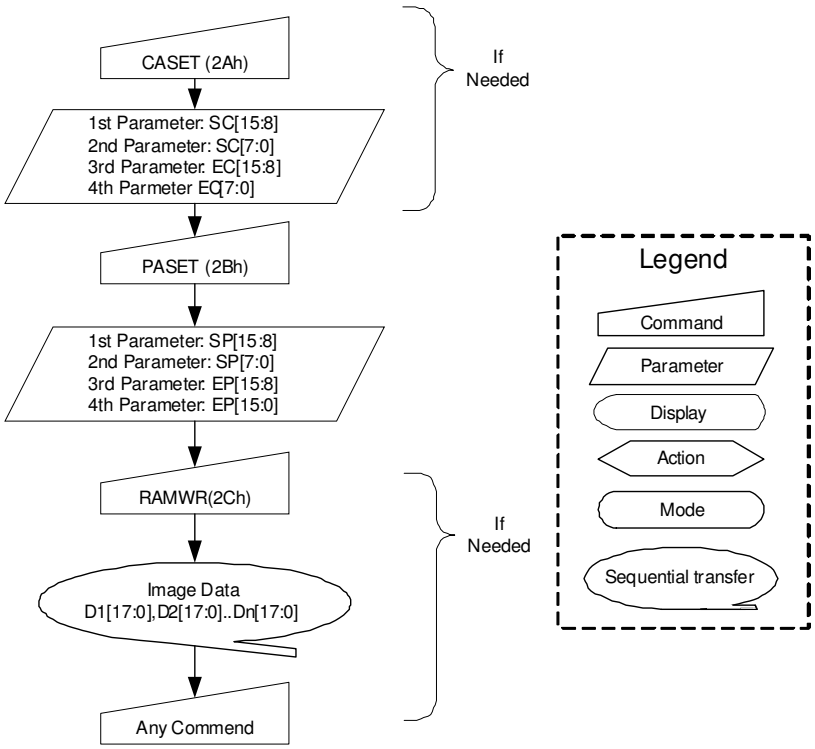
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow Chart



8.2.23. Color Set (2Dh)

2Dh	RGBSET (Color Set)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	0	1	1	0	1	2Dh
1st Parameter	1	1	↑	XXXXXXXX	R00[5:0]								XX
nth Parameter	1	1	↑	XXXXXXXX	Rnn[5:0]								XX
32ndParameter	1	1	↑	XXXXXXXX	R31[5:0]								XX
33rdParameter	1	1	↑	XXXXXXXX	G00[5:0]								XX
nth Parameter	1	1	↑	XXXXXXXX	Gnn[5:0]								XX
96thParameter	1	1	↑	XXXXXXXX	G63[5:0]								XX
97thParameter	1	1	↑	XXXXXXXX	B00[5:0]								XX
nth Parameter	1	1	↑	XXXXXXXX	Bnn[5:0]								XX
128thParameter	1	1	↑	XXXXXXXX	B31[5:0]								XX

Description

This command is used to define the LUT for 16-bit to 18-bit color depth conversion.

128 bytes must be written to the LUT regardless of the color mode. Only the values in Section 7.3 are referred.

This command has no effect on other commands, parameter and contents of frame memory. Visible change takes effect next time the frame memory is written to.

Restriction

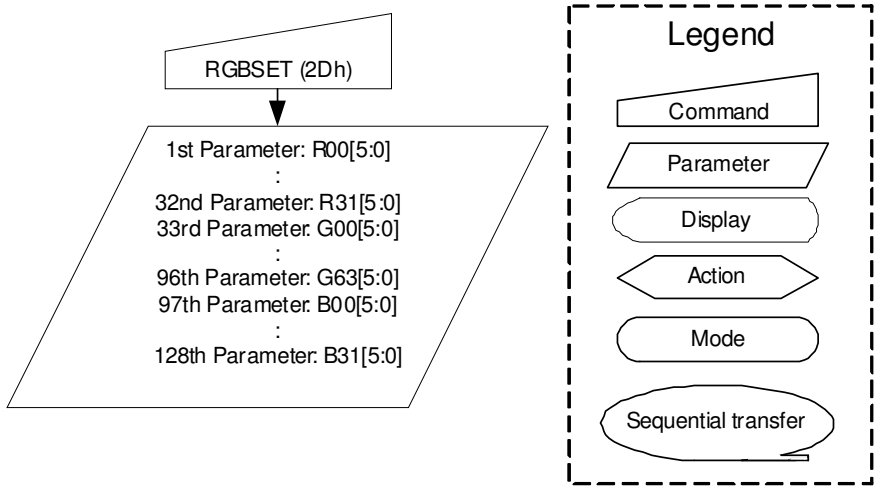
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Random values
SW Reset	Contents of LUT protected
HW Reset	Random values

Flow Chart



8.2.24. Memory Read (2Eh)

2Eh	RAMRD (Memory Read)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	0	1	1	1	0	2Eh
1st Parameter	1	1	↑	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	1	↑	D1[15:0]									XX
:	1	1	↑	Dx[15:0]									XX
(N+1)th Parameter	1	1	↑	Dn[15:0]									XX

Description

This command transfers image data from ILI9339's frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands.

If Memory Access control B5 = 0:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.

If Memory Access Control B5 = 1:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.

Restriction

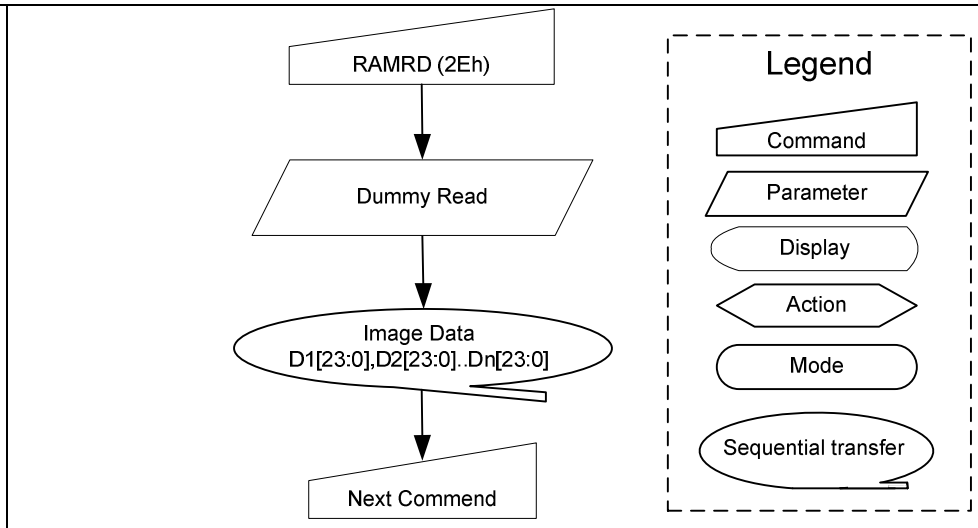
There is no restriction on length of parameters.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is set randomly
HW Reset	Contents of memory is set randomly

Flow Chart	

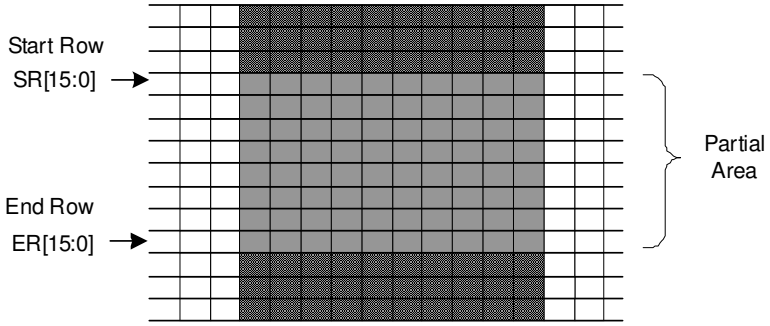
8.2.25. Partial Area (30h)

30h	PLTAR (Partial Area)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	1	0	0	0	0	30h
1st Parameter	1	1	↑	XXXXXXXX	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	XXXX
2nd Parameter	1	1	↑	XXXXXXXX	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	
3rd Parameter	1	1	↑	XXXXXXXX	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	XXXX
4th Parameter	1	1	↑	XXXXXXXX	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	

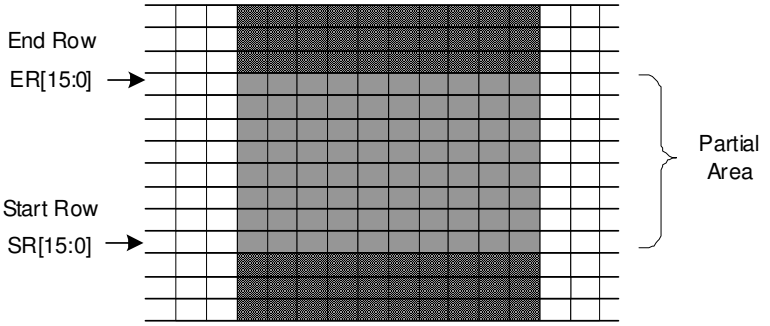
Description

This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.

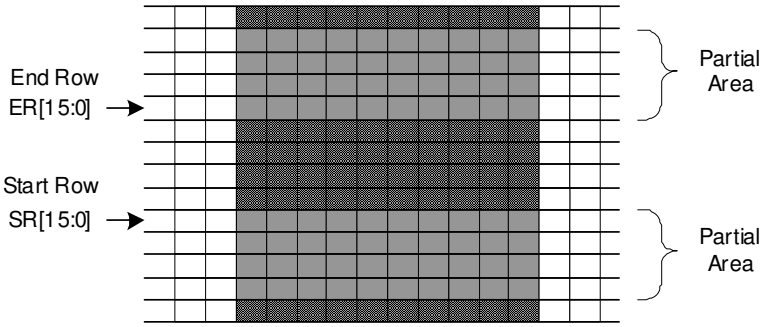
If End Row>Start Row when MADCTL B4=0:-



If End Row>Start Row when MADCTL B4=1:-



If End Row<Start Row when MADCTL B4=0:-



If End Row = Start Row then the Partial Area will be one row deep.

X = Don't care.

Restriction	SR [15…0] and ER [15…0] cannot be 0000h nor exceed 013Fh.

Register Availability

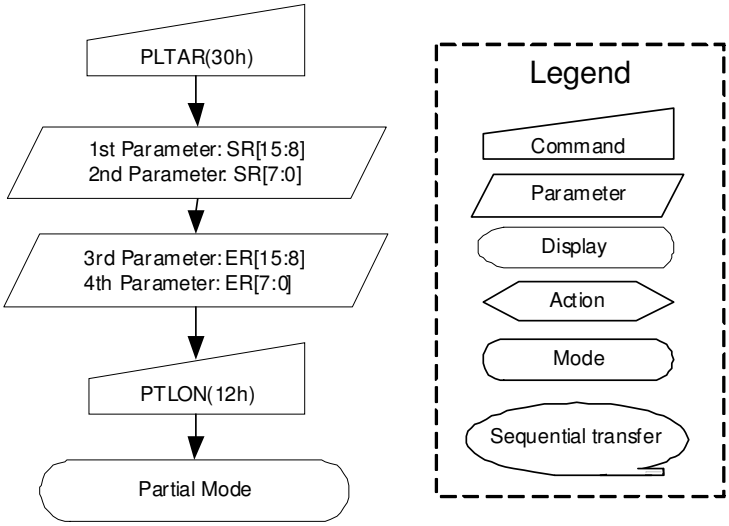
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

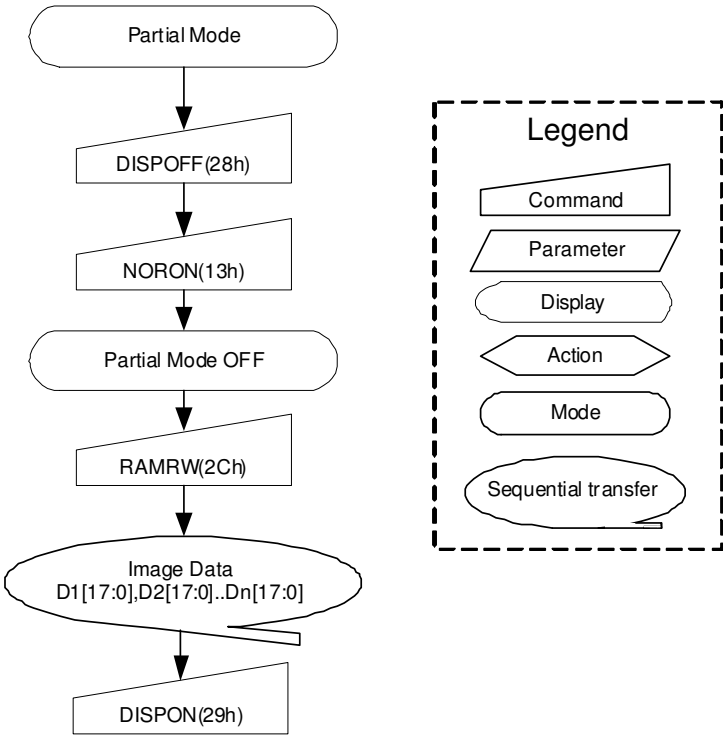
Status	Default Value	
Power On Sequence	SR[15:0]=0000h	ER[15:0]=013Fh
SW Reset	SR[15:0]=0000h	ER[15:0]=013Fh
HW Reset	SR[15:0]=0000h	ER[15:0]=013Fh

Flow Chart

1. To Enter Partial Mode



2. To Leave Partial Mode



8.2.26. Vertical Scrolling Definition (33h)

33h	VSCRDEF (Vertical Scrolling Definition)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	1	0	0	1	1	33h
1st Parameter	1	↑	1	XXXXXXXX	TFA [15:8]								XX
2nd Parameter	1	↑	1	XXXXXXXX	TFA [7:0]								XX
3rd Parameter	1	↑	1	XXXXXXXX	VSA [15:8]								XX
4th Parameter	1	↑	1	XXXXXXXX	VSA [7:0]								XX
5th Parameter	1	↑	1	XXXXXXXX	BFA [15:8]								XX
6th Parameter	1	↑	1	XXXXXXXX	BFA [7:0]								XX

Description

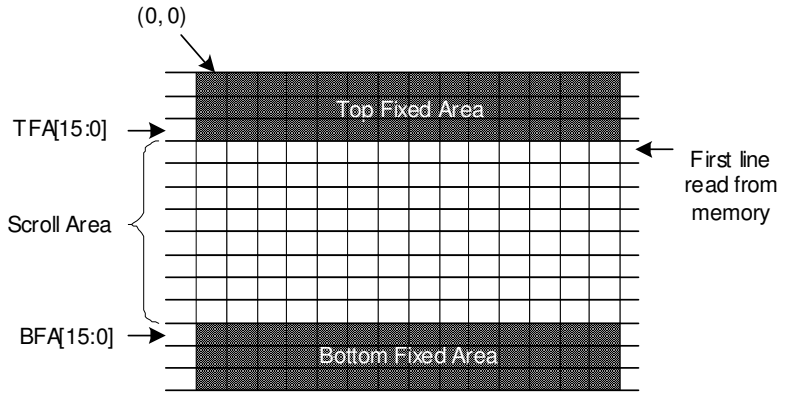
This command defines the Vertical Scrolling Area of the display.

When MADCTL B4=0

The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

The 5th & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.

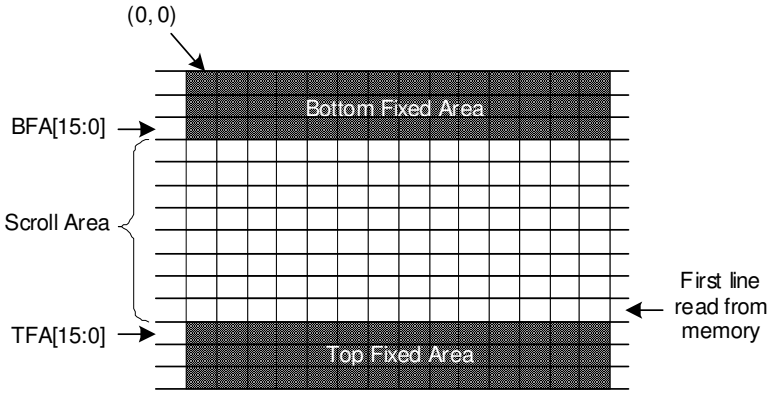


When MADCTL B4=1

The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

The 5th & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



X = Don't care

Restriction

Register Availability

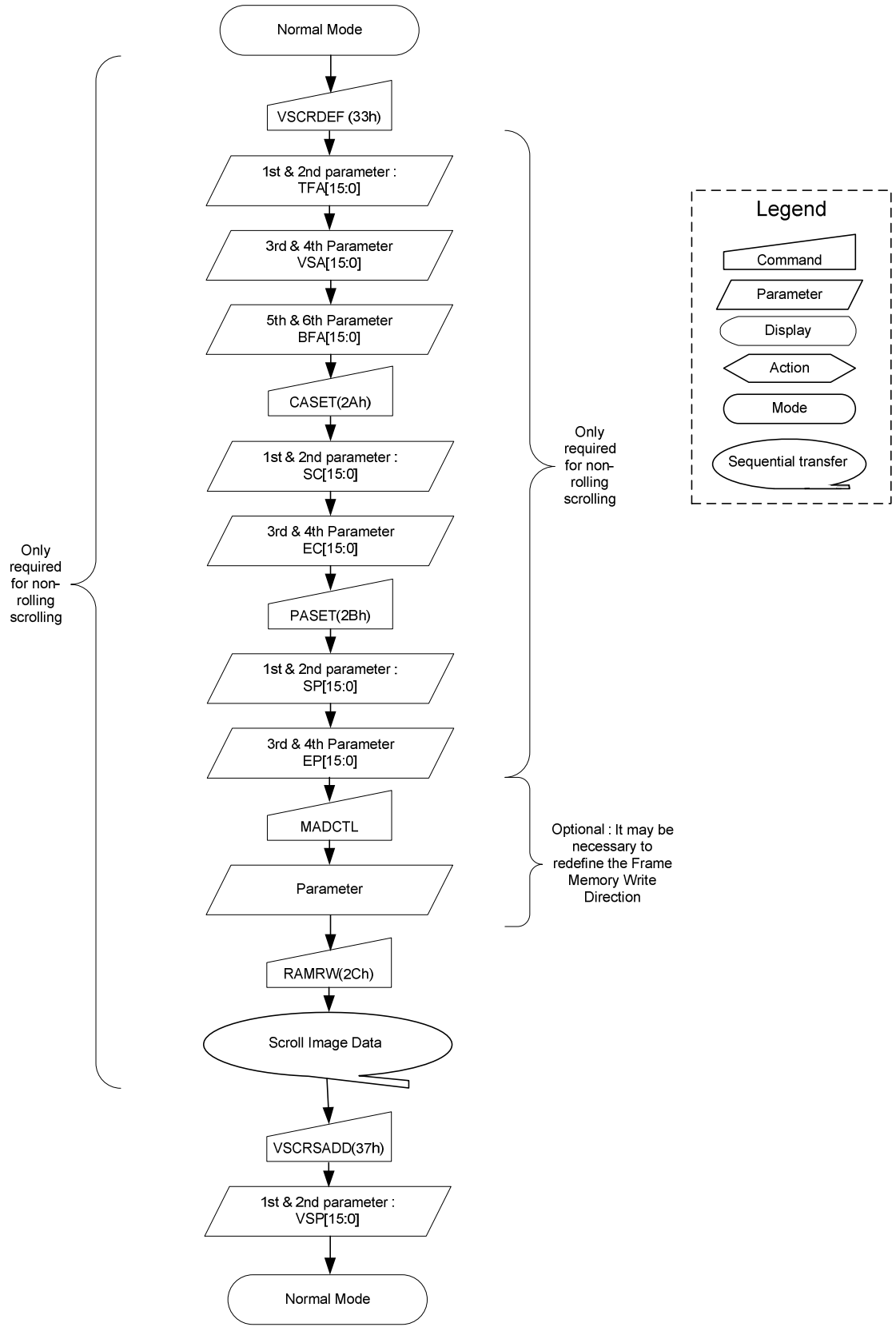
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
Power On Sequence	TFA[15:0]=0000h	VSA[15:0]=0140h	BFA[15:0]=0000h
SW Reset	TFA[15:0]=0000h	VSA[15:0]=0140h	BFA[15:0]=0000h
HW Reset	TFA[15:0]=0000h	VSA[15:0]=0140h	BFA[15:0]=0000h

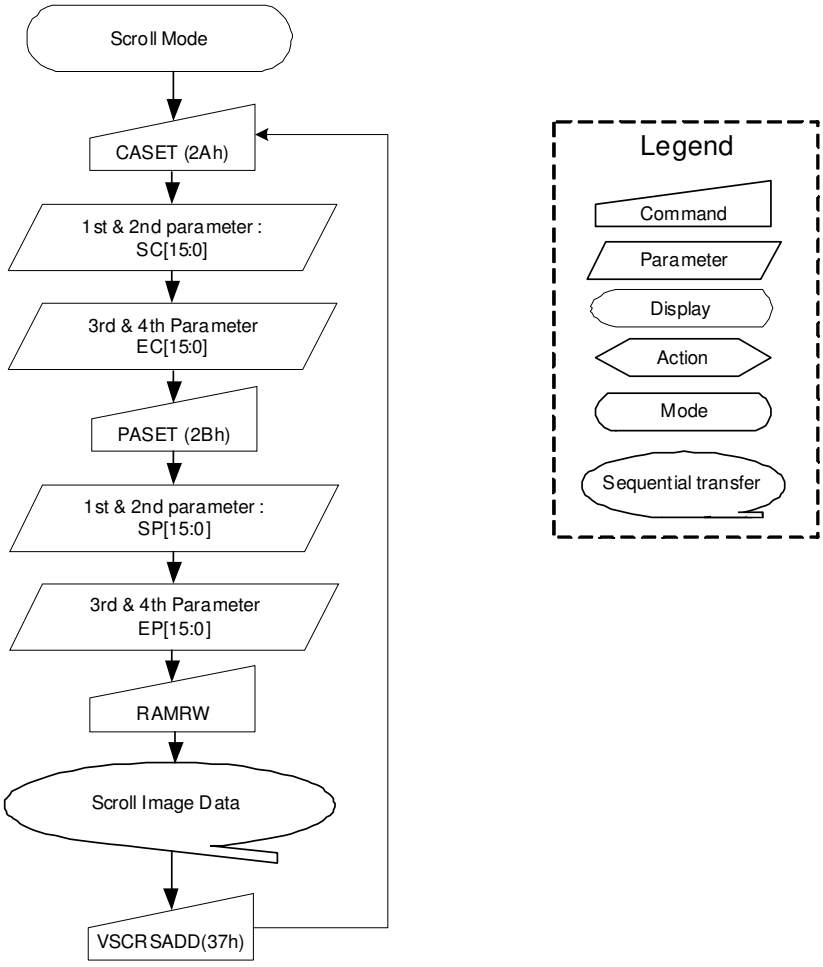
Flow Chart

1. To enter Vertical Scroll Mode :

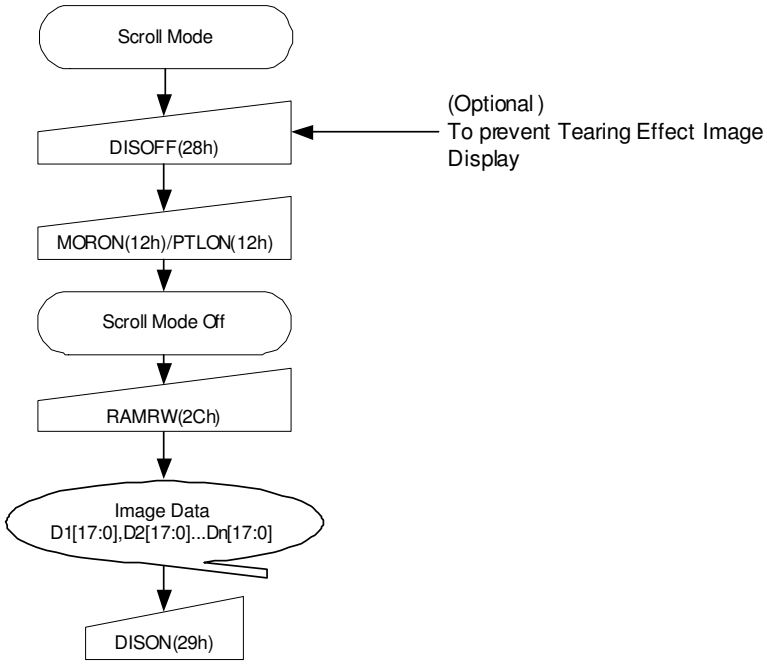


Note : The Frame Memory Window size ,must be defined correctly otherwise undesirable image will be displayed.

2. Continuous Scroll :

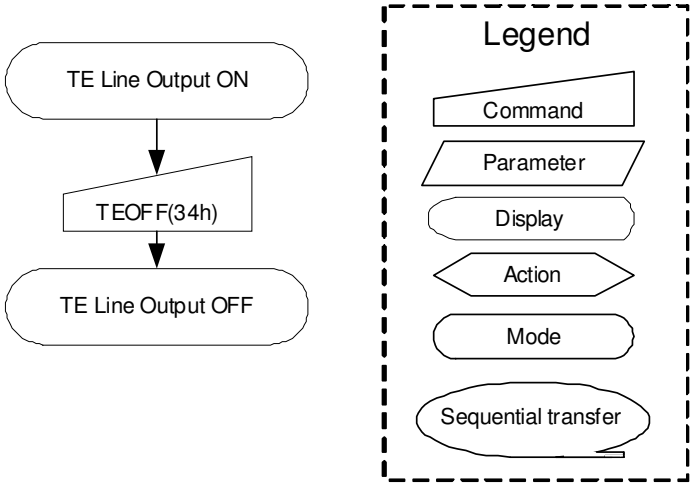


3.To Leave Vertical Scroll Mode:



Note: Scroll Mode can be left by both the Normal Display Mode ON (13h) and Partial Mode ON (12h) commands.

8.2.27. Tearing Effect Line OFF (34h)

<table>
<tr><th>34h</th><th colspan="13">TEOFF (Tearing Effect Line OFF)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D [15:8]</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XXXXXXXX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>34h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already OFF.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

8.2.28. Tearing Effect Line ON (35h)

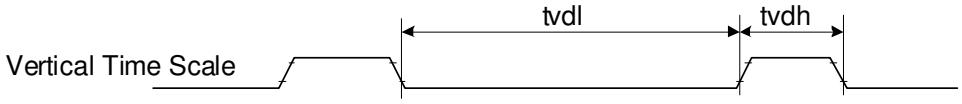
35h	TEON (Tearing Effect Line ON)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	1	0	1	0	1	35h
Parameter	1	1	↑	XXXXXXXX	X	X	X	X	X	X	X	M	XX

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

When **M=0**:

The Tearing Effect Output line consists of V-Blanking information only:



When **M=1**:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

X = Don't care.

Restriction

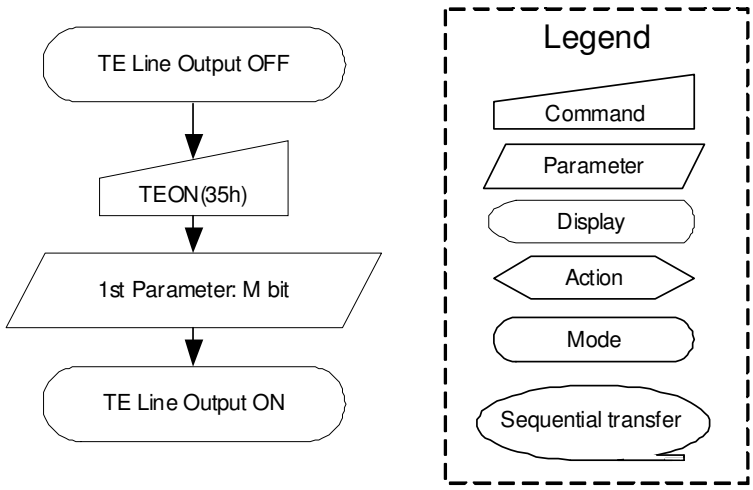
This command has no effect when Tearing Effect output is already ON

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart	

8.2.29. Memory Access Control (36h)

36h	MADCTL (Memory Access Control)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	1	0	1	1	0	36h
Parameter	1	1	↑	XXXXXXXX	MY	MX	MV	ML	BGR	MH	X	X	XX

Description

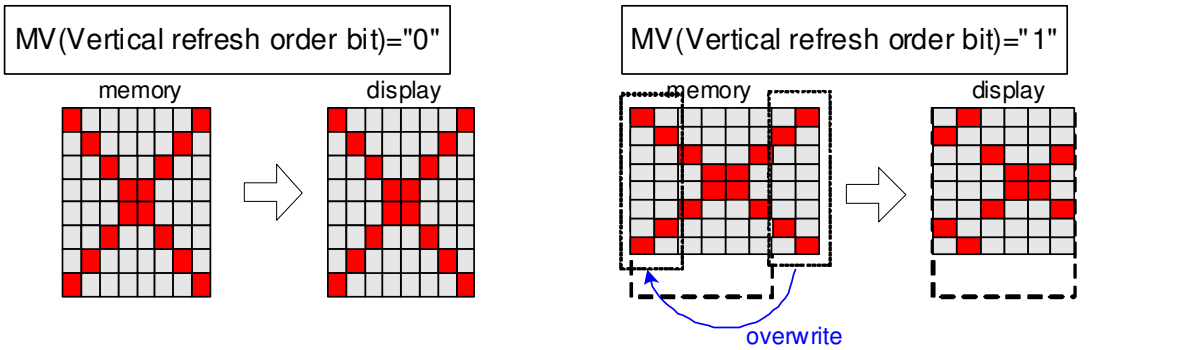
This command defines read/write scanning direction of frame memory.

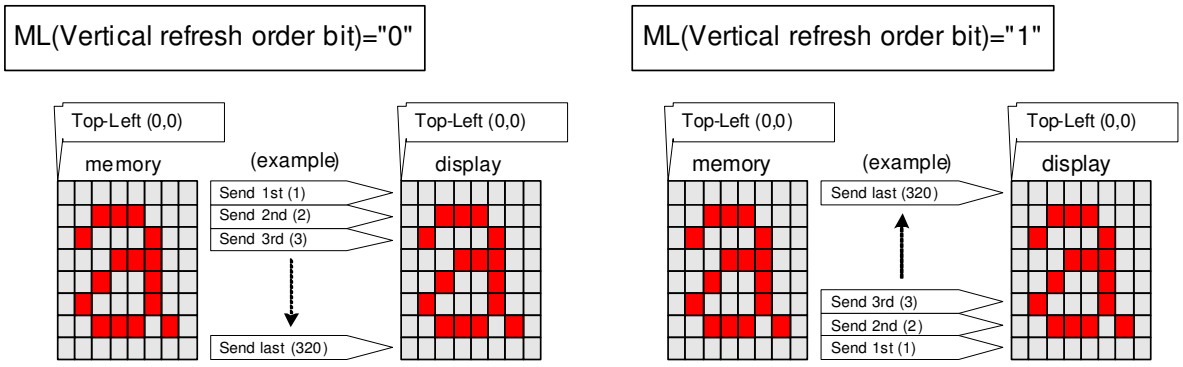
This command makes no change on the other driver status.

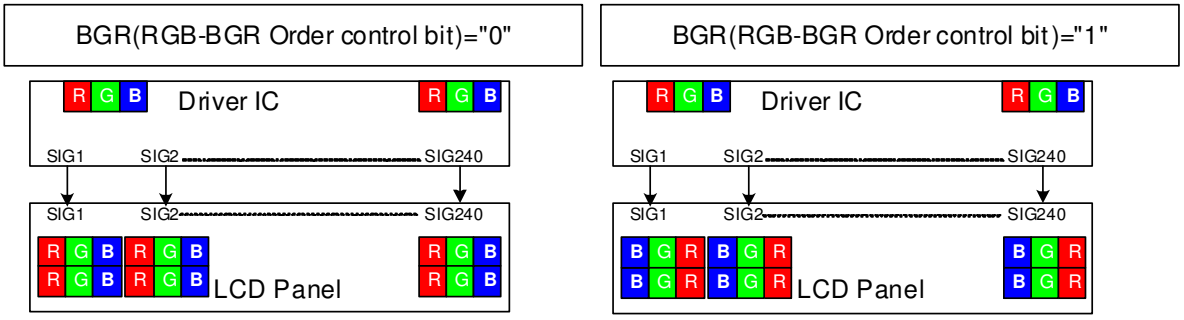
Bit	Name	Description
MY	Row Address Order	These 3 bits control MPU to memory write/read direction.
MX	Column Address Order	
MV	Row / Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control.
BGR	RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
MH	Horizontal Refresh ORDER	LCD horizontal refreshing direction control.

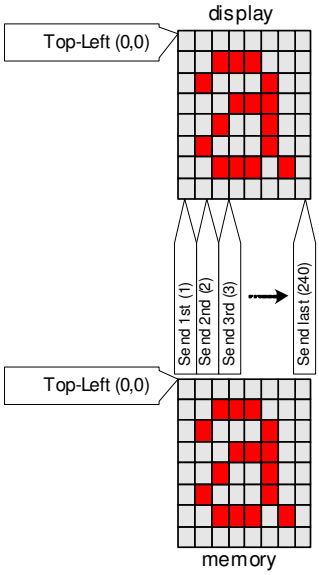
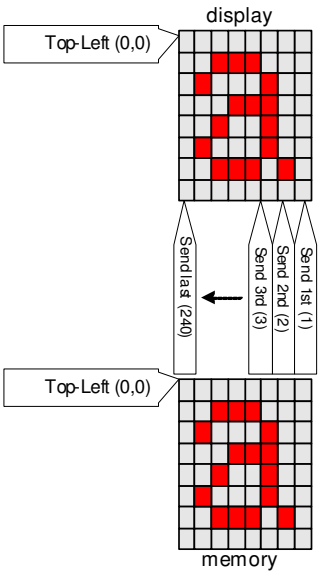
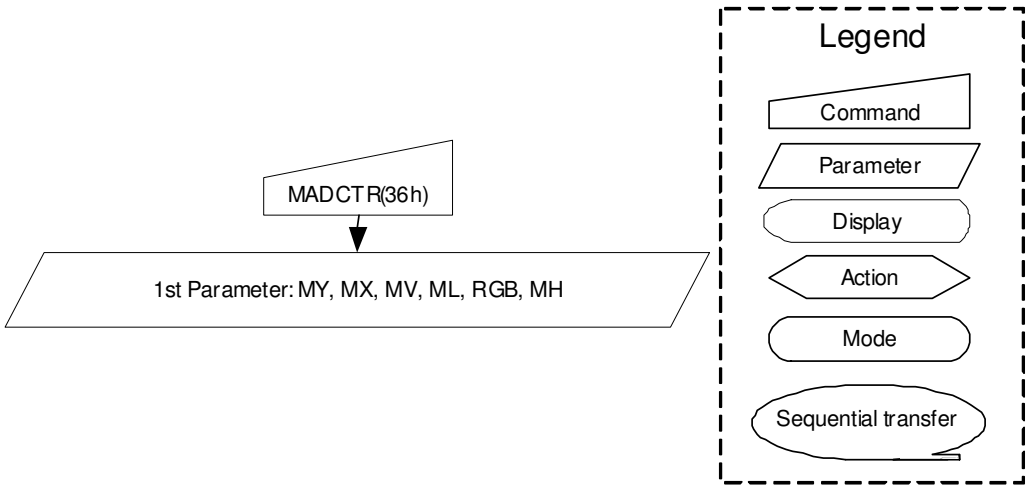
Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.

X = Don't care.







<table>
<tr><td></td><td>
<table>
<tr><td>MH(Horizontal refresh order control bit)="0"</td><td>MH(Horizontal refresh order control bit)="1"</td></tr>
<tr><td> 
</td><td> 
</td></tr>
</table>
Note: Top-Left (0,0) means a physical memory location.
</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>SW Reset</td><td>No change</td></tr>
<tr><td>HW Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

8.2.30. Vertical Scrolling Start Address (37h)

37h	VSCRSADD (Vertical Scrolling Start Address)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	1	0	1	1	1	37h
1st Parameter	1	↑	1	XXXXXXXX	VSP [15:8]								XX
2nd Parameter	1	↑	1	XXXXXXXX	VSP [7:0]								XX

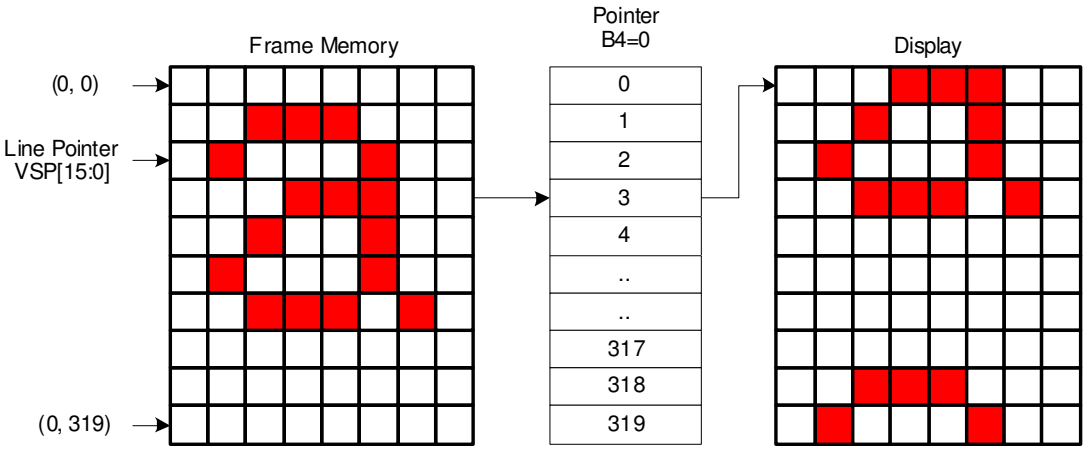
Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-

When MADCTL B4=0

Example:

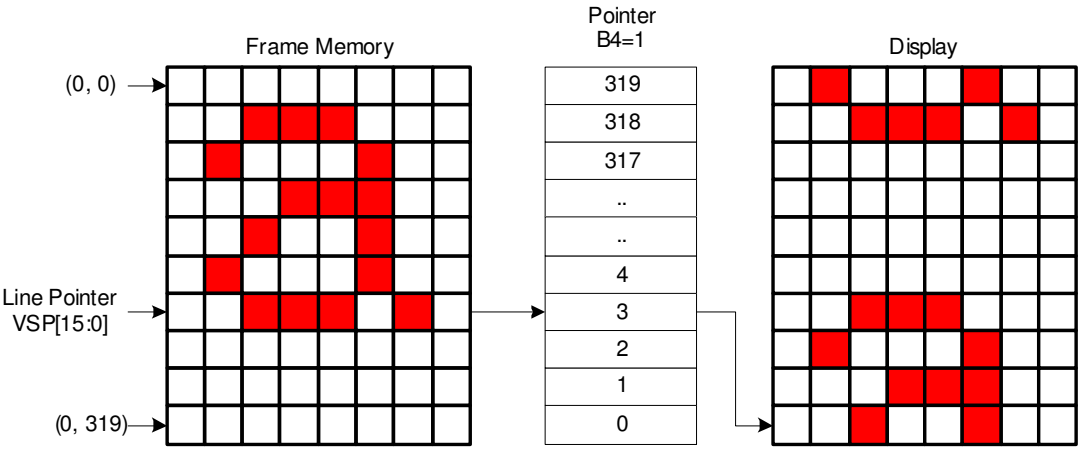
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.



When MADCTL B4=1

Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.



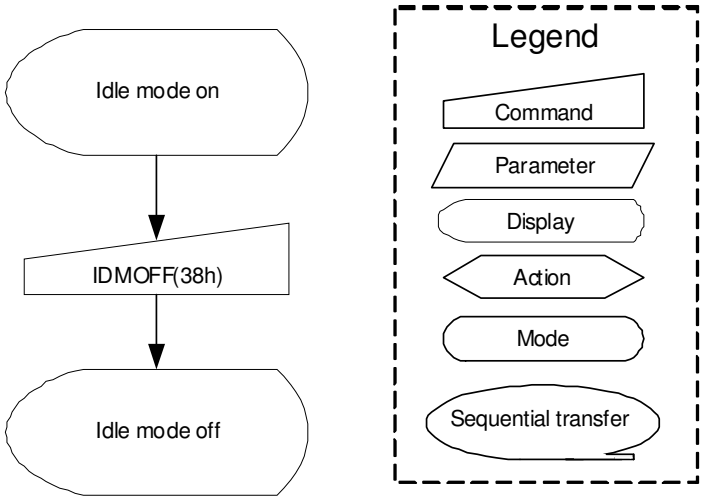
Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

(2) This command is ignored when the ILI9338B enters Partial mode.

X = Don't care

<table>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0000h</td></tr>
<tr><td>SW Reset</td><td>0000h</td></tr>
<tr><td>HW Reset</td><td>0000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

8.2.31. Idle Mode OFF (38h)

<table>
<tr><th>38h</th><th colspan="13">IDMOFF (Idle Mode OFF)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D [15:8]</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XXXXXXXX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>38h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to recover from Idle mode on.
In the idle off mode, LCD can display maximum 262,144 colors.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle mode OFF</td></tr><tr><td>SW Reset</td><td>Idle mode OFF</td></tr><tr><td>HW Reset</td><td>Idle mode OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

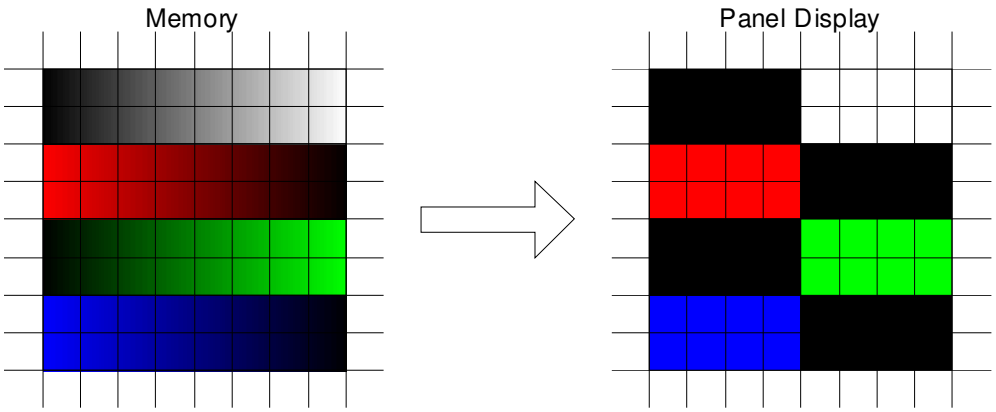
8.2.32. Idle Mode ON (39h)

39H	IDMON (Idle Mode ON)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	1	1	0	0	1	39h
Parameter	No Parameter												

Description

This command is used to enter into Idle mode on.

In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.



Memory Contents vs. Display Color			
	R_5 R_4 R_3 R_2 R_1 R_0	G_5 G_4 G_3 G_2 G_1 G_0	B_5 B_4 B_3 B_2 B_1 B_0
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

X = Don't care.

Restriction

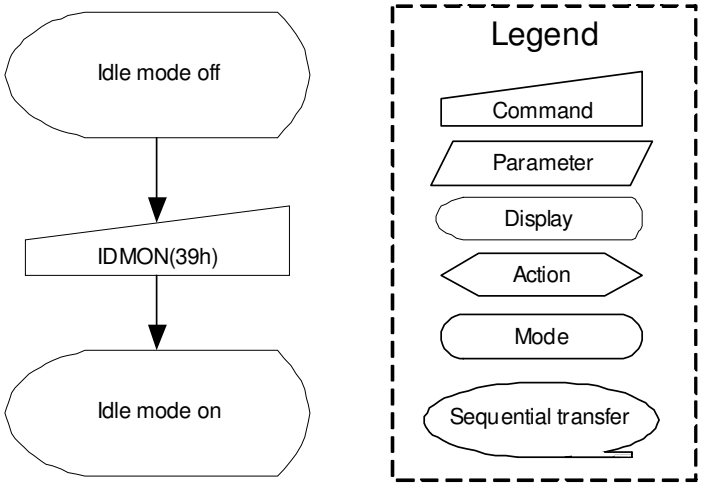
This command has no effect when module is already in idle off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode OFF
SW Reset	Idle mode OFF
HW Reset	Idle mode OFF

Flow Chart	

8.2.33. Pixel Format Set (3Ah)

3Ah	PIXSET (Pixel Format Set)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	0	0	1	1	0	26h
Parameter	1	1	↑	XXXXXXXX	DPI [3:0]				X	DBI [2:0]			XX

Description

This command sets the pixel format for the RGB image data used by the interface. DPI [3:0] is the pixel format select of RGB interface and DBI [2:0] is the pixel format of MCU interface. If a particular interface, either RGB interface or MCU interface, is not used then the corresponding bits in the parameter are ignored. The pixel format is shown in the table below.

DPI [3:0]				RGB Interface Format
0	0	0	0	Reserved
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	16 bits / pixel
0	1	1	0	18 bits / pixel
0	1	1	1	Reserved
1	1	1	0	18 bits / pixel (3 times data transfer)

DBI [2:0]			MCU Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

X = Don't care

Restriction: There is no visible until the image data is written to.

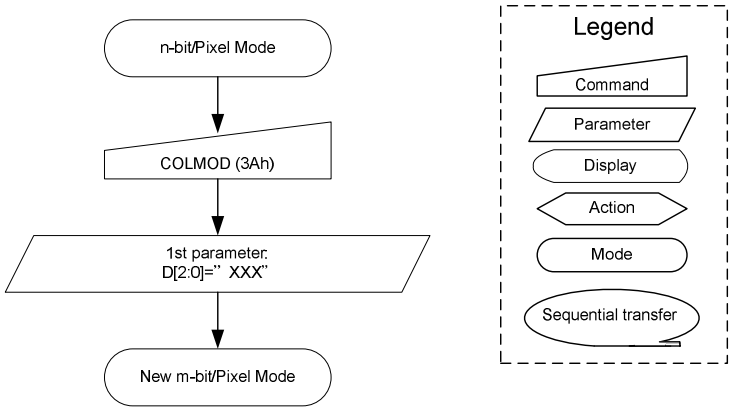
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	18 bits/pixel
SW Reset	No Change
HW Reset	18 bits/pixel

Flow Chart



8.2.34. Read ID1 (DAh)

DAh	RDID1 (Read ID1)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	1	1	0	1	0	DAh
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2ndParameter	1	↑	1	XXXXXXXX	ID1 [7:0]								XX
Description	This read byte identifies the LCD module's manufacturer ID and it is specified by User The 1st parameter is dummy data. The 2nd parameter is LCD module's manufacturer ID. X = Don't care												
Restriction													

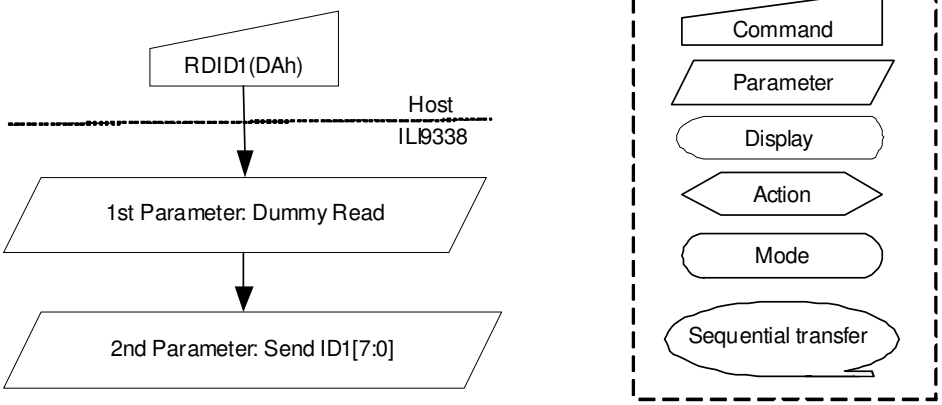
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	54h
SW Reset	54h
HW Reset	54h

Flow Chart



8.2.35. Read ID2 (DBh)

DBh	RDID2 (Read ID2)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	1	1	0	1	1	DBh
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XXXXXXXX	1	ID2 [6:0]							XX

Description

This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications.

The 1st parameter is dummy data.

The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh.

The ID2 can be programmed by OTP function.

X = Don't care

Restriction

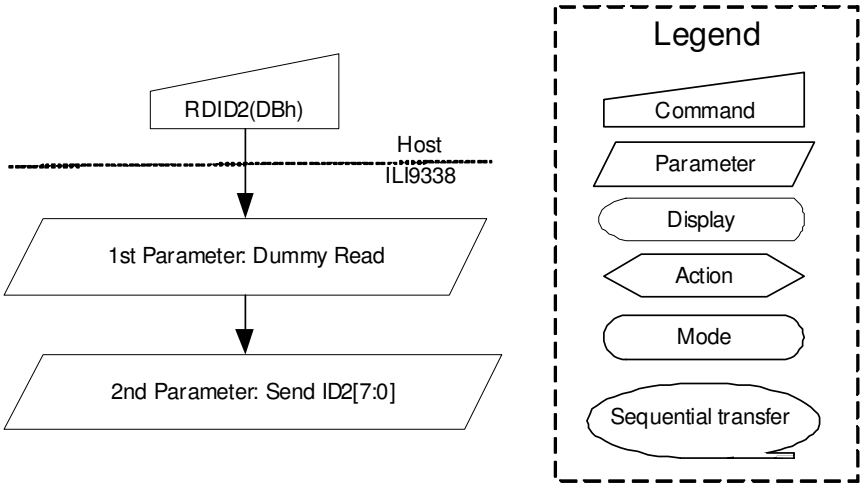
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before OTP program)	Default Value (After OTP program)
Power On Sequence	80h	OTP value
SW Reset	80h	OTP value
HW Reset	80h	OTP value

Flow Chart



8.2.36. Read ID3 (DCh)

DCh	RDID3 (Read ID3)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	1	1	1	0	0	DCh
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2ndParameter	1	↑	1	XXXXXXXX	ID3 [7:0]								XX
Description	This read byte identifies the LCD module/driver and It is specified by User. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver ID. The ID3 can be programmed by OTP function. X = Don't care												
Restriction													

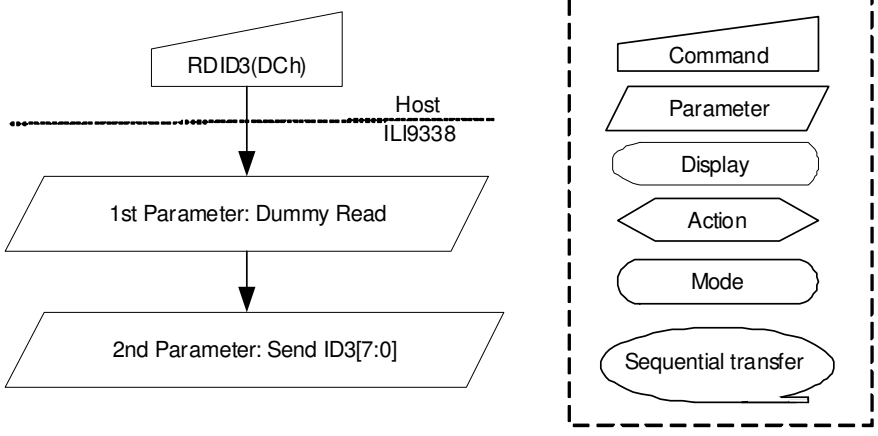
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before OTP program)	Default Value (After OTP program)
Power On Sequence	66h	OTP value
SW Reset	66h	OTP value
HW Reset	66h	OTP value

Flow Chart



8.2.37. Interface Mode Control (B0h)

<table>
<tr><th>B0h</th><th colspan="13">IFMODE (Interface Mode Control)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D [15:8]</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XXXXXXXX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B0h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XXXXXXXX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>VSPL</td><td>HSPL</td><td>DPL</td><td>EPL</td><td>XX</td></tr>
<tr><td>Description</td><td colspan="13">Sets the operation status of the display interface. The setting becomes effective as soon as the command is received.
EPL: DE polarity (“0”= High enable for RGB interface, “1”=Low enable for RGB interface)
DPL: DOTCLK polarity set (“0”=data fetched at the rising time, “1”=data fetched at the falling time)
HSPL: HSYNC polarity (“0”=Low level sync clock, “1”=High level sync clock)
VSPL: VSYNC polarity (“0”= Low level sync clock, “1”= High level sync clock)</td></tr>
<tr><td>Restriction</td><td colspan="13">Dummy_EXTC should be high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr><tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr><tr><td>Sleep IN</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="4">Default Value</th></tr><tr><th>DPL</th><th>EPL</th><th>HSPL</th><th>VSPL</th></tr><tr><td>Power ON Sequence</td><td>0b</td><td>0b</td><td>0b</td><td>0b</td></tr><tr><td>S/W Reset</td><td>0b</td><td>0b</td><td>0b</td><td>0b</td></tr></table></td></tr>
</table>

8.2.38. Frame Rate Control (In Normal Mode/Full Colors) (B1h)

B1h	FRMCTR1 (Frame Rate Control (In Normal Mode / Full colors))												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	0	0	1	B1h
1st Parameter	1	1	↑	XXXXXXXX	0	0	0	0	0	0	DIVA [1:0]		XX
2nd Parameter	1	1	↑	XXXXXXXX	0	0	0	RTNA [4:0]					XX

Description

Sets the division ratio for internal clocks of Normal mode at MCU interface.

DIVA [1:0] : division ratio for internal clocks when Normal mode.

DIVA[1:0]		Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

RTNA [4:0] : RTNA[4:0] is used to set 1H (line) period of Normal mode at MCU interface.

RTNA[4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

RTNA[4:0]					Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

RTNA[4:0]					Clock per Line
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	1	1	1	27 clocks
1	1	0	0	0	28 clocks
1	1	0	0	1	29 clocks
1	1	0	1	0	30 clocks
1	1	1	1	1	31 clocks

Restriction

Dummy_EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DIVA[1:0]	RTNA[4:0]
Power ON Sequence	2'b00	5'b10001
S/W Reset	2'b00	5'b10001
H/W Reset	2'b00	5'b10001

8.2.39. Frame Rate Control (In Idle Mode/8 colors) (B2h)

B2h	FRMCTR2 (Frame Rate Control (In Idle Mode / 8I colors))												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	0	1	0	B2h
1st Parameter	1	1	↑	XXXXXXXX	0	0	0	0	0	0	DIVB [1:0]		XX
2nd Parameter	1	1	↑	XXXXXXXX	0	0	0	RTNB [4:0]					XX

Description

Sets the division ratio for internal clocks of Idle mode at MCU interface.

DIVB [1:0]: division ratio for internal clocks when Idle mode.

DIVB[1:0]		Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

RTNB [4:0]: RTNB[4:0] is used to set 1H (line) period of Idle mode at MCU interface.

RTNB[4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

RTNB[4:0]					Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

RTNB[4:0]					Clock per Line
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	1	1	1	27 clocks
1	1	0	0	0	28 clocks
1	1	0	0	1	29 clocks
1	1	0	1	0	30 clocks
1	1	1	1	1	31 clocks

Restriction

Dummy_EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DIVB[1:0]	RTNB[4:0]
Power ON Sequence	2'b00	5'b10001
S/W Reset	2'b00	5'b10001
H/W Reset	2'b00	5'b10001

8.2.40. Frame Rate control (In Partial Mode/Full Colors) (B3h)

_B3h	FRMCTR3 (Frame Rate Control (In Partial Mode / Full colors))												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	0	1	1	B3h
1st Parameter	1	1	↑	XXXXXXXX	0	0	0	0	0	0	DIVC [1:0]		XX
2ndParameter	1	1	↑	XXXXXXXX	0	0	0	RTNC [4:0]					XX

Description

Sets the division ratio for internal clocks of Partial mode (Idle mode off) at MCU interface.

DIVC [1:0]: division ratio for internal clocks when Partial mode.

DIVC[1:0]		Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

RTNC [4:0]: RTNC [4:0] is used to set 1H (line) period of Partial mode at MCU interface.

RTNC[4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

RTNC[4:0]					Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

RTNC[4:0]					Clock per Line
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	1	1	1	27 clocks
1	1	0	0	0	28 clocks
1	1	0	0	1	29 clocks
1	1	0	1	0	30 clocks
1	1	1	1	1	31 clocks

Restriction

Dummy_EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DIVC[1:0]	RTNC[4:0]
Power ON Sequence	2'b00	5'b10001
S/W Reset	2'b00	5'b10001
H/W Reset	2'b00	5'b10001

8.2.41. Display Inversion Control (B4h)

B4h	INVTR (Display Inversion Control)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	1	0	0	B4h
1st Parameter	1	1	↑	XXXXXXXX	0	0	0	0	0	NLA	NLB	NLC	XX
2nd Parameter	1	1	↑	XXXXXXXX	0	0	NW [5:0]						XX

Description

Display inversion mode set

NLA: Inversion setting in full colors normal mode (Normal mode on)

NLB: Inversion setting in Idle mode (Idle mode on)

NLC: Inversion setting in full colors partial mode (Partial mode on / Idle mode off)

NLA / NLB / NLC	Inversion
0	Line inversion
1	Frame inversion

NW [5:0]: N-line inversion setting in NLA=0, NLB=0 and NLC=0.

NW[5:0]						N-line Inversion
0	0	0	0	0	0	1 lines
0	0	0	0	0	1	2 lines
0	0	0	0	1	0	3 lines
0	0	0	0	1	1	4 lines
0	0	0	1	0	0	5 lines
0	0	0	1	0	1	6 lines
0	0	0	1	1	0	7 lines
0	0	0	1	1	1	8 lines
0	0	1	0	0	0	9 lines
0	0	1	0	0	1	10 lines
0	0	1	0	1	0	11 lines
0	0	1	0	1	1	12 lines
0	0	1	1	0	0	13 lines
0	0	1	1	0	1	14 lines
0	0	1	1	1	0	15 lines
0	0	1	1	1	1	16 lines
0	1	0	0	0	0	17 lines
0	1	0	0	0	1	18 lines
0	1	0	0	1	0	19 lines
0	1	0	0	1	1	20 lines
0	1	0	1	0	0	21 lines
0	1	0	1	0	1	22 lines
0	1	0	1	1	0	23 lines
0	1	0	1	1	1	24 lines
0	1	1	0	0	0	25 lines
0	1	1	0	0	1	26 lines
0	1	1	0	1	0	27 lines
0	1	1	0	1	1	28 lines
0	1	1	1	0	0	29 lines
0	1	1	1	0	1	30 lines
0	1	1	1	1	0	31 lines
0	1	1	1	1	1	32 lines

NW[5:0]						N-line Inversion
1	0	0	0	0	0	33 lines
1	0	0	0	0	1	34 lines
1	0	0	0	1	0	35 lines
1	0	0	0	1	1	36 lines
1	0	0	1	0	0	37 lines
1	0	0	1	0	1	38 lines
1	0	0	1	1	0	39 lines
1	0	0	1	1	1	40 lines
1	0	1	0	0	0	41 lines
1	0	1	0	0	1	42 lines
1	0	1	0	1	0	43 lines
1	0	1	0	1	1	44 lines
1	0	1	1	0	0	45 lines
1	0	1	1	0	1	46 lines
1	0	1	1	1	0	47 lines
1	0	1	1	1	1	48 lines
1	1	0	0	0	0	49 lines
1	1	0	0	0	1	50 lines
1	1	0	0	1	0	51 lines
1	1	0	0	1	1	52 lines
1	1	0	1	0	0	53 lines
1	1	0	1	0	1	54 lines
1	1	0	1	1	0	55 lines
1	1	0	1	1	1	56 lines
1	1	1	0	0	0	57 lines
1	1	1	0	0	1	58 lines
1	1	1	0	1	0	59 lines
1	1	1	0	1	1	60 lines
1	1	1	1	0	0	61 lines
1	1	1	1	0	1	62 lines
1	1	1	1	1	0	63 lines
1	1	1	1	1	1	64 lines

Restriction	Dummy_EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value			
	NLA	NLB	NLC	NW[5:0]
Power ON Sequence	1'b0	1'b1	1'b0	6'b000000
S/W Reset	1'b0	1'b1	1'b0	6'b000000
H/W Reset	1'b0	1'b1	1'b0	6'b000000

8.2.42. Blanking Porch Control (B5h)

B5h	PRCTR (Blanking Porch)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	1	0	1	B5h
1st Parameter	1	1	↑	XXXXXXXX	0	VFP [6:0]							XX
2nd Parameter	1	1	↑	XXXXXXXX	0	VBP [6:0]							XX
3rd Parameter	1	1	↑	XXXXXXXX	0	0	0	HFP [4:0]					XX
4th Parameter	1	1	↑	XXXXXXXX	0	0	0	HBP [4:0]					XX

Description

VFP [6:0] / **VBP [6:0]:** The VFP [6:0] and VBP [6:0] bits specify the line number of vertical front and back porch period respectively.

VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch	VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch
0000000	Setting inhibited	1000000	64
0000001	Setting inhibited	1000001	65
0000010	2	1000010	66
0000011	3	1000011	67
0000100	4	1000100	68
0000101	5	1000101	69
0000110	6	1000110	70
0000111	7	1000111	71
0001000	8	1001000	72
0001001	9	1001001	73
0001010	10	1001010	74
0001011	11	1001011	75
0001100	12	1001100	76
0001101	13	1001101	77
: :	: :	: :	: :
0111101	61	1111101	125
0111110	62	1111110	126
0111111	63	1111111	127

Note: VFP + VBP ≦ 254 HSYNC signals

HFP [4:0] / **HBP [4:0]:** The HFP [4:0] and HBP [4:0] bits specify the line number of horizontal front and back porch period respectively.

HFP[4:0] HBP[4:0]	Number of DOTCLK of the front/back porch	HFP[4:0] HBP[4:0]	Number of DOTCLK of front/back porch
00000	Setting prohibited	10000	16
00001	Setting prohibited	10001	17
00010	2	10010	18
00011	3	10011	19
00100	4	10100	20
00101	5	10101	21
00110	6	10110	22
00111	7	10111	23
01000	8	11000	24
01001	9	11001	25
01010	10	11010	26
01011	11	11011	27
01100	12	11100	28
01101	13	11101	29
01110	14	11110	30
01111	15	11111	31

<table>
<tr><td>Restriction</td><td>Dummy_EXTC should be high to enable this command</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="4">Default Value</th></tr>
<tr><th>VFP[6:0]</th><th>VBP[6:0]</th><th>HFP[4:0]</th><th>HBP[4:0]</th></tr>
<tr><td>Power ON Sequence</td><td>7’b0000010</td><td>7’b0000010</td><td>5’b01010</td><td>5’b10100</td></tr>
<tr><td>S/W Reset</td><td>7’b0000010</td><td>7’b0000010</td><td>5’b01010</td><td>5’b10100</td></tr>
</table>
</td></tr>
</table>

8.2.43. Display Function Control (B6h)

B6h	DISCTRL (Display Function Control)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	1	1	0	B6h
1st Parameter	1	1	↑	XXXXXXXX	0	0	0	0	PTG [1:0]		PT [1:0]		XX
2nd Parameter	1	1	↑	XXXXXXXX	0	GS	SS	SM	ISC [3:0]				XX
3rd Parameter	1	1	↑	XXXXXXXX	0	0	NL [5:0]						XX

Description

PTG [1:0]: Set the scan mode in non-display area.

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	VCOM output
0	0	Normal scan	Set with the PT[2:0] bits	VCOMH/VCOML
0	1	Setting prohibited	---	---
1	0	Interval scan	Set with the PT[2:0] bits	
1	1	Setting prohibited	---	---

PT [1:0]: Determine source/VCOM output in a non-display area in the partial display mode.

PT[1:0]		Source output on non-display area		VCOM output on non-display area	
		Positive polarity	Negative polarity	Positive polarity	Negative polarity
0	0	V63	V0	VCOML	VCOMH
0	1	V0	V63	VCOML	VCOMH
1	0	AGND	AGND	AGND	AGND
1	1	Hi-Z	Hi-Z	AGND	AGND

SS: This bit controls MPU to memory write/read direction by column address order.

ISC [3:0]: Specify the scan cycle interval of gate driver in non-display area when PTG [1:0] ="10" to select interval scan.

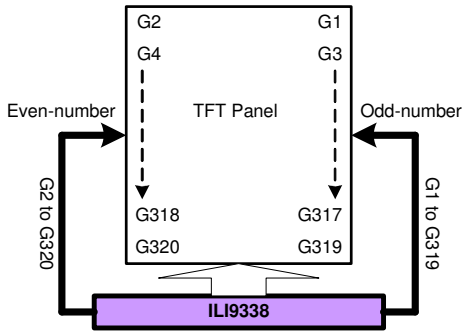
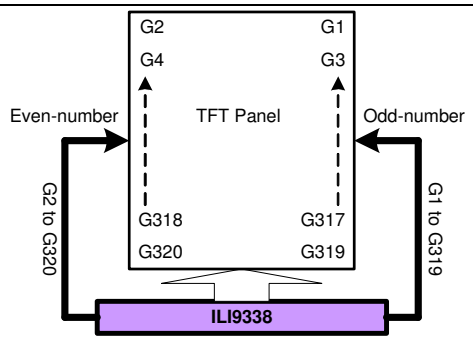
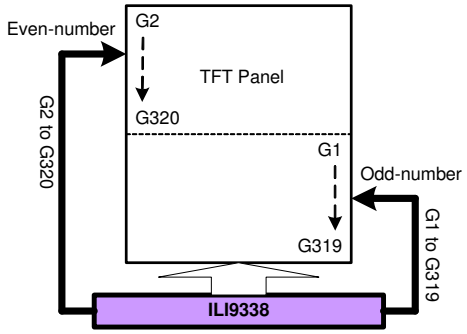
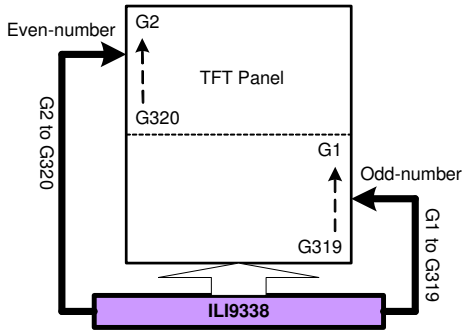
Then scan cycle is set as odd number from 0~29 frame periods. The polarity is inverted every scan cycle.

ISC[3:0]	Scan Cycle	f_{FLM} = 60Hz
0000	1 frame	17ms
0001	3 frames	51ms
0010	5 frames	85ms
0011	7 frames	119ms
0100	9 frames	153ms
0101	11 frames	187ms
0110	13 frames	221ms
0111	15 frames	255ms
1000	17 frames	289ms
1001	19 frames	323ms
1010	21 frames	357ms
1011	23 frames	391ms
1100	25 frames	425ms
1101	27 frames	459ms
1110	29 frames	493ms
1111	31 frames	527ms

GS: Sets the direction of scan by the gate driver in the range determined by SCN [4:0] and NL [4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

GS	Gate Output Scan Direction
0	G1 → G320
1	G320 → G1

SM: Sets the gate driver pin arrangement in combination with the GS bit (R60h) to select the optimal scan mode for the module.

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1→G2→G3→G4→ …… ….→G317→G318→G319→G320
0	1		G320→G319->G318→G317→…… …. →G4→G3→G2→G1
1	0		G1→G3→…….....→G317→G319→ G2→G4→……→G318→G320
1	1		G320, G318, G316, …, G10, G8, G6, G4, G2 G319, G317, G315, …, G9, G78, G5, G3, G1 G320→G318→…….....→G4→G2→ G319→G317→……→G3→G1

NL [5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL [5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[5:0]						LCD Drive Line
0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	1	16 lines
0	0	0	0	1	0	24 lines
0	0	0	0	1	1	32 lines
0	0	0	1	0	0	40 lines
0	0	0	1	0	1	48 lines
0	0	0	1	1	0	56 lines
0	0	0	1	1	1	64 lines

NL[5:0]						LCD Driver Line
0	1	0	1	0	1	176 lines
0	1	0	1	1	0	184 lines
0	1	0	1	1	1	192 lines
0	1	1	0	0	0	200 lines
0	1	1	0	0	1	208 lines
0	1	1	0	1	0	216 lines
0	1	1	0	1	1	224 lines
0	1	1	1	0	0	232 lines

0	0	1	0	0	0	72 lines
0	0	1	0	0	1	80 lines
0	0	1	0	1	0	88 lines
0	0	1	0	1	1	96 lines
0	0	1	1	0	0	104 lines
0	0	1	1	0	1	112 lines
0	0	1	1	1	0	120 lines
0	0	1	1	1	1	128 lines
0	1	0	0	0	0	136 lines
0	1	0	0	0	1	144 lines
0	1	0	0	1	0	152 lines
0	1	0	0	1	1	160 lines
0	1	0	1	0	0	168 lines

0	1	1	1	0	1	240 lines
0	1	1	1	1	0	248 lines
0	1	1	1	1	1	256 lines
1	0	0	0	0	0	264 lines
1	0	0	0	0	1	272 lines
1	0	0	0	1	0	280 lines
1	0	0	0	1	1	288 lines
1	0	0	1	0	0	296 lines
1	0	0	1	0	1	304 lines
1	0	0	1	1	0	312 lines
1	0	0	1	1	1	320 lines
Others						Setting inhibited

Restriction

Dummy_EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value						
	PTG[1:0]	PT[1:0]	GS	SS	SM	ISC[3:0]	NL[5:0]
Power ON Sequence	2'b10	2'b10	1'b0	1'b0	1'b0	4'b0010	6'b100111
S/W Reset	2'b10	2'b10	1'b0	1'b0	1'b0	4'b0010	6'b100111

8.2.44. Entry Mode Set (B7h)

B7h	ETMOD (Entry Mode Set)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	1	1	1	B7h
Parameter	1	1	↑	XXXXXXXX	0	0	0	0	DSTB	GON	DTE	GAS	XX

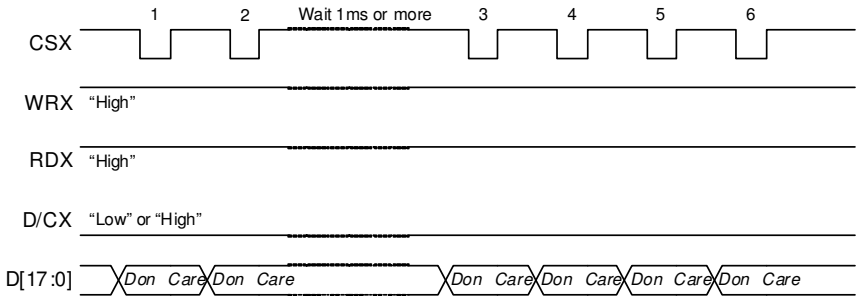
Description

DSTB: The ILI9338B driver enters the Deep Standby Mode when DSTB is set to high ("1"). In Deep Standby mode, both internal logic power and SRAM power are turn off, the display data stored in the Frame Memory and the instructions are not saved. Rewrite Frame Memory content and instructions after the Deep Standby Mode is exited.

Note: ILI9338B provides two ways to exit the Deep Standby Mode:

(1) Exit Deep Standby Mode by pull down CSX to low ("0") 6 times.

(2) Input a RESX pulse with effective low level duration to start up the inside logic regulator and makes a transition to the initial state.



GAS: Low voltage detection control.

GAS	Low voltage detection
0	Enable
1	Disable

GON/DTE: Set the output level of gate driver G1 ~ G320 as follows

GON	DTE	G1~G320 Gate Output
0	0	VGH
0	1	VGH
1	0	VGL
1	1	Normal display

Restriction: Dummy_EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value			
	DSTB	GON	DTE	GAS
Power ON Sequence	1'b0	1'b1	1'b1	1'b1
S/W Reset	1'b0	1'b1	1'b1	1'b1

8.2.45. Power Control 1 (C0h)

C0h	PWCTRL 1 (Power Control 1)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	0	0	0	0	C0h
1st Parameter	1	1	↑	XXXXXXXX	0	0	VRH [5:0]						XX
2nd Parameter	1	1	↑	XXXXXXXX	0	0	0	0	0	VC [2:0]			XX

Description

VRH [5:0]: Set the VREG1OUT level, which is a reference level for the VCOM level and the grayscale voltage level.

VRH[5:0]						VREG1OUT
0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	1	Setting prohibited
0	0	0	0	1	0	Setting prohibited
0	0	0	0	1	1	3.00 V
0	0	0	1	0	0	3.05 V
0	0	0	1	0	1	3.10 V
0	0	0	1	1	0	3.15 V
0	0	0	1	1	1	3.20 V
0	0	1	0	0	0	3.25 V
0	0	1	0	0	1	3.30 V
0	0	1	0	1	0	3.35 V
0	0	1	0	1	1	3.40 V
0	0	1	1	0	0	3.45 V
0	0	1	1	0	1	3.50 V
0	0	1	1	1	0	3.55 V
0	0	1	1	1	1	3.60 V
0	1	0	0	0	0	3.65 V
0	1	0	0	0	1	3.70 V
0	1	0	0	1	0	3.75 V
0	1	0	0	1	1	3.80 V
0	1	0	1	0	0	3.85 V
0	1	0	1	0	1	3.90 V
0	1	0	1	1	0	3.95 V
0	1	0	1	1	1	4.00 V
0	1	1	0	0	0	4.05 V
0	1	1	0	0	1	4.10 V
0	1	1	0	1	0	4.15 V
0	1	1	0	1	1	4.20 V
0	1	1	1	0	0	4.25 V
0	1	1	1	0	1	4.30 V
0	1	1	1	1	0	4.35 V
0	1	1	1	1	1	4.40 V

VRH[5:0]						VREG1OUT
1	0	0	0	0	0	4.45 V
1	0	0	0	0	1	4.50 V
1	0	0	0	1	0	4.55 V
1	0	0	0	1	1	4.60 V
1	0	0	1	0	0	4.65 V
1	0	0	1	0	1	4.70 V
1	0	0	1	1	0	4.75 V
1	0	0	1	1	1	4.80 V
1	0	1	0	0	0	4.85 V
1	0	1	0	0	1	4.90 V
1	0	1	0	1	0	4.95 V
1	0	1	0	1	1	5.00 V
1	0	1	1	0	0	5.05 V
1	0	1	1	0	1	5.10 V
1	0	1	1	1	0	5.15 V
1	0	1	1	1	1	5.20 V
1	1	0	0	0	0	5.25 V
1	1	0	0	0	1	5.30 V
1	1	0	0	1	0	5.35 V
1	1	0	0	1	1	5.40 V
1	1	0	1	0	0	5.45 V
1	1	0	1	0	1	5.50 V
1	1	0	1	1	0	5.55 V
1	1	0	1	1	1	5.60 V
1	1	1	0	0	0	5.65 V
1	1	1	0	0	1	5.70 V
1	1	1	0	1	0	5.75 V
1	1	1	0	1	1	5.80 V
1	1	1	1	0	0	5.85 V
1	1	1	1	0	1	5.90 V
1	1	1	1	1	0	5.95 V
1	1	1	1	1	1	6.00 V

Note1: Make sure that VC and VRH setting restriction: VREG1OUT ≦ (DDVDH - 0.5) V.

VC [2:0]: Sets VCI1 regulator voltage.

VC[2:0]			VCI1 Voltage
0	0	0	2.75V
0	0	1	2.70V
0	1	0	2.65V
0	1	1	2.60V
1	0	0	2.55V
1	0	1	2.50V
1	1	0	2.45V
1	1	1	External VDD

Note2: When VDD<2.8V, Internal reference voltage VCI1 will refer to VDD gone down.

Restriction	Dummy_EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	VC[2:0]	VRH[5:0]
Power ON Sequence	3'b001	6'b100110
S/W Reset	3'b001	6'b100110

8.2.46. Power Control 2 (C1h)

<table>
<tr><th>C1h</th><th colspan="13">PWCTRL 2 (Power Control 2)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D [15:8]</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XXXXXXXX</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>C1h</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XXXXXXXX</td><td>0</td><td colspan="3">SAP [2:0]</td><td colspan="4">BT [3:0]</td><td>XX</td></tr>
<tr><td>Description</td><td colspan="13">
BT [3:0]: Sets the factor used in the step-up circuits.
Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.
<table>
<tr><th colspan="4">BT[3:0]</th><th>DDVDH</th><th>VGH</th><th>VGL</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="11">VCI1 x 2</td><td rowspan="3">VCI1 x 6</td><td>-VCI1 x 5</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>-VCI1 x 4</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>-VCI1 x 3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td rowspan="3">VCI1 x 5</td><td>-VCI1 x 5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>-VCI1 x 4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>-VCI1 x 3</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td rowspan="2">VCI1 x 4</td><td>-VCI1 x 4</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>-VCI1 x 3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td rowspan="11">VCI1 x 3</td><td rowspan="3">VCI1 x 9</td><td>-VCI1 x 7</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>-VCI1 x 6</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>-VCI1 x 4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td rowspan="3">VCI1 x 7</td><td>-VCI1 x 7</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>-VCI1 x 6</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>-VCI1 x 4</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td rowspan="2">VCI1 x 6</td><td>-VCI1 x 6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>-VCI1 x 4</td></tr>
</table>
Note1: Make sure that DDVDH setting restriction: DDVDH ≦ 6.0 V.
2: Make sure that VGH and VGL setting restriction: VGH -VGL≦ 32 V.

SAP [2:0]: It is used to adjust the constant current in the operational amplifier circuit in the LCD power supply circuit. Larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off between the display quality and the current consumption into account.
<table>
<tr><th colspan="3">SAP[2:0]</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Halt</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Small</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Small</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Small</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Medium</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Medium to Large</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Large</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Large</td></tr>
</table>
When starting the charge-pump of LCD in the Power ON stage, make sure that SAP=0, and set the SAP=1, after starting up the LCD power supply circuit.
</td></tr>
<tr><td>Restriction</td><td colspan="13">Dummy_EXTC should be high to enable this command</td></tr>
</table>

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	BT[3:0]	SAP[2:0]
Power ON Sequence	4'b0000	3'b001
S/W Reset	4'b0000	3'b001

8.2.47. Power Control 3 (For Normal Mode) (C2h)

C2h	PWCTRL 3 (Power Control 3)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	0	0	1	0	C2h
1st Parameter	1	1	↑	XXXXXXXX	0	DCA1 [2:0]			0	DCA0 [2:0]			XX

Description

DCA0 [2:0]: Selects the operating frequency of the step-up circuit 1 for Normal mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCA1 [2:0]: Selects the operating frequency of the step-up circuit 2/3/4 for Normal mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCA0[2:0]			Step-up cycle for step-up circuit 1
0	0	0	DCCK / 1
0	0	1	DCCK / 2
0	1	0	DCCK / 4
0	1	1	DCCK / 8
1	0	0	DCCK / 16
1	0	1	DCCK / 32
1	1	0	DCCK / 64
1	1	1	Setting prohibited

DCA1[2:0]			Step-up cycle for step-up circuit 2/3/4
0	0	0	DCCK / 2
0	0	1	DCCK / 4
0	1	0	DCCK / 8
0	1	1	DCCK / 16
1	0	0	DCCK / 32
1	0	1	DCCK / 64
1	1	0	DCCK / 128
1	1	1	Setting prohibited

Restriction: Dummy_EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DCA0[2:0]	DCA1[2:0]
Power ON Sequence	3'b010	3'b011
S/W Reset	3'b010	3'b011

8.2.48. Power Control 4 (For Idle Mode) (C3h)

C3h	PWCTRL 4 (Power Control 4)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	0	0	1	1	C3h
1st Parameter	1	1	↑	XXXXXXXX	0	DCB1 [2:0]			0	DCB0 [2:0]			XX

Description

DCB0 [2:0]: Selects the operating frequency of the step-up circuit 1 for Idle mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCB1 [2:0]: Selects the operating frequency of the step-up circuit 2/3/4 for Idle mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCB0[2:0]			Step-up cycle for step-up circuit 1
0	0	0	DCCK / 1
0	0	1	DCCK / 2
0	1	0	DCCK / 4
0	1	1	DCCK / 8
1	0	0	DCCK / 16
1	0	1	DCCK / 32
1	1	0	DCCK / 64
1	1	1	Setting prohibited

DCB1[2:0]			Step-up cycle for step-up circuit 2/3/4
0	0	0	DCCK / 2
0	0	1	DCCK / 4
0	1	0	DCCK / 8
0	1	1	DCCK / 16
1	0	0	DCCK / 32
1	0	1	DCCK / 64
1	1	0	DCCK / 128
1	1	1	Setting prohibited

Restriction

Dummy_EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DCB0[2:0]	DCB1[2:0]
Power ON Sequence	3'b010	3'b011
S/W Reset	3'b010	3'b011

8.2.49. Power Control 5 (For Partial Mode) (C4h)

C4h	PWCTRL 5 (Power Control 5)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	0	1	0	0	C4h
1st Parameter	1	1	↑	XXXXXXXX	0	DCC1 [2:0]			0	DCC0 [2:0]			XX

Description

DCC0 [2:0]: Selects the operating frequency of the step-up circuit 1 for Partial mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCC1 [2:0]: Selects the operating frequency of the step-up circuit 2/3/4 for Partial mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCC0[2:0]			Step-up cycle for step-up circuit 1
0	0	0	DCCK / 1
0	0	1	DCCK / 2
0	1	0	DCCK / 4
0	1	1	DCCK / 8
1	0	0	DCCK / 16
1	0	1	DCCK / 32
1	1	0	DCCK / 64
1	1	1	Setting prohibited

DCC1[2:0]			Step-up cycle for step-up circuit 2/3/4
0	0	0	DCCK / 2
0	0	1	DCCK / 4
0	1	0	DCCK / 8
0	1	1	DCCK / 16
1	0	0	DCCK / 32
1	0	1	DCCK / 64
1	1	0	DCCK / 128
1	1	1	Setting prohibited

Restriction: Dummy_EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DCC0[2:0]	DCC1[2:0]
Power ON Sequence	3'b010	3'b011
S/W Reset	3'b010	3'b011

8.2.50. VCOM Control 1(C5h)

C5h	VMCTRL1 (VCOM Control 1)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	0	1	0	1	C5h
1st Parameter	1	1	↑	XXXXXXXX	0	VMH [6:0]							XX
2nd Parameter	1	1	↑	XXXXXXXX	0	VML [6:0]							XX

Description

VMH [6:0] : Set the VCOMH voltage.

VMH[6:0]	VCOMH(V)	VMH[6:0]	VCOMH(V)	VMH[6:0]	VCOMH(V)	VMH[6:0]	VCOMH(V)
0000000	2.700	0100000	3.500	1000000	4.300	1100000	5.100
0000001	2.725	0100001	3.525	1000001	4.325	1100001	5.125
0000010	2.750	0100010	3.550	1000010	4.350	1100010	5.150
0000011	2.775	0100011	3.575	1000011	4.375	1100011	5.175
0000100	2.800	0100100	3.600	1000100	4.400	1100100	5.200
0000101	2.825	0100101	3.625	1000101	4.425	1100101	5.225
0000110	2.850	0100110	3.650	1000110	4.450	1100110	5.250
0000111	2.875	0100111	3.675	1000111	4.475	1100111	5.275
0001000	2.900	0101000	3.700	1001000	4.500	1101000	5.300
0001001	2.925	0101001	3.725	1001001	4.525	1101001	5.325
0001010	2.950	0101010	3.750	1001010	4.550	1101010	5.350
0001011	2.975	0101011	3.775	1001011	4.575	1101011	5.375
0001100	3.000	0101100	3.800	1001100	4.600	1101100	5.400
0001101	3.025	0101101	3.825	1001101	4.625	1101101	5.425
0001110	3.050	0101110	3.850	1001110	4.650	1101110	5.450
0001111	3.075	0101111	3.875	1001111	4.675	1101111	5.475
0010000	3.100	0110000	3.900	1010000	4.700	1110000	5.500
0010001	3.125	0110001	3.925	1010001	4.725	1110001	5.525
0010010	3.150	0110010	3.950	1010010	4.750	1110010	5.550
0010011	3.175	0110011	3.975	1010011	4.775	1110011	5.575
0010100	3.200	0110100	4.000	1010100	4.800	1110100	5.600
0010101	3.225	0110101	4.025	1010101	4.825	1110101	5.625
0010110	3.250	0110110	4.050	1010110	4.850	1110110	5.650
0010111	3.275	0110111	4.075	1010111	4.875	1110111	5.675
0011000	3.300	0111000	4.100	1011000	4.900	1111000	5.700
0011001	3.325	0111001	4.125	1011001	4.925	1111001	5.725
0011010	3.350	0111010	4.150	1011010	4.950	1111010	5.750
0011011	3.375	0111011	4.175	1011011	4.975	1111011	5.775
0011100	3.400	0111100	4.200	1011100	5.000	1111100	5.800
0011101	3.425	0111101	4.225	1011101	5.025	1111101	5.825
0011110	3.450	0111110	4.250	1011110	5.050	1111110	5.850
0011111	3.475	0111111	4.275	1011111	5.075	1111111	5.875

VMF [6:0] : Set the VCOML voltage

VML[6:0]	VCOML(V)	VML[6:0]	VCOML(V)	VML[6:0]	VCOML(V)	VML[6:0]	VCOML(V)
0000000	-2.500	0100000	-1.700	1000000	-0.900	1100000	-0.100
0000001	-2.475	0100001	-1.675	1000001	-0.875	1100001	-0.075
0000010	-2.450	0100010	-1.650	1000010	-0.850	1100010	-0.050
0000011	-2.425	0100011	-1.625	1000011	-0.825	1100011	-0.025
0000100	-2.400	0100100	-1.600	1000100	-0.800	1100100	0
0000101	-2.375	0100101	-1.575	1000101	-0.775	1100101	Reserved
0000110	-2.350	0100110	-1.550	1000110	-0.750	1100110	Reserved
0000111	-2.325	0100111	-1.525	1000111	-0.725	1100111	Reserved
0001000	-2.300	0101000	-1.500	1001000	-0.700	1101000	Reserved
0001001	-2.275	0101001	-1.475	1001001	-0.675	1101001	Reserved
0001010	-2.250	0101010	-1.450	1001010	-0.650	1101010	Reserved
0001011	-2.225	0101011	-1.425	1001011	-0.625	1101011	Reserved
0001100	-2.200	0101100	-1.400	1001100	-0.600	1101100	Reserved
0001101	-2.175	0101101	-1.375	1001101	-0.575	1101101	Reserved
0001110	-2.150	0101110	-1.350	1001110	-0.550	1101110	Reserved
0001111	-2.125	0101111	-1.325	1001111	-0.525	1101111	Reserved
0010000	-2.100	0110000	-1.300	1010000	-0.500	1110000	Reserved
0010001	-2.075	0110001	-1.275	1010001	-0.475	1110001	Reserved
0010010	-2.050	0110010	-1.250	1010010	-0.450	1110010	Reserved
0010011	-2.025	0110011	-1.225	1010011	-0.425	1110011	Reserved

0010100	-2.000	0110100	-1.200	1010100	-0.400	1110100	Reserved
0010101	-1.975	0110101	-1.175	1010101	-0.375	1110101	Reserved
0010110	-1.950	0110110	-1.150	1010110	-0.350	1110110	Reserved
0010111	-1.925	0110111	-1.125	1010111	-0.325	1110111	Reserved
0011000	-1.900	0111000	-1.100	1011000	-0.300	1111000	Reserved
0011001	-1.875	0111001	-1.075	1011001	-0.275	1111001	Reserved
0011010	-1.850	0111010	-1.050	1011010	-0.250	1111010	Reserved
0011011	-1.825	0111011	-1.025	1011011	-0.225	1111011	Reserved
0011100	-1.800	0111100	-1.000	1011100	-0.200	1111100	Reserved
0011101	-1.775	0111101	-0.975	1011101	-0.175	1111101	Reserved
0011110	-1.750	0111110	-0.950	1011110	-0.150	1111110	Reserved
0011111	-1.725	0111111	-0.925	1011111	-0.125	1111111	Reserved

Restriction: Dummy_EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	VMH[6:0]	VML[6:0]
Power ON Sequence	7'b0110001	7'b0111100
S/W Reset	7'b0110001	7'b0111100

8.2.51. VCOM Control 2(C7h)

C7h	VMCTRL1 (VCOM Control 1)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	0	1	1	1	C7h
1st Parameter	1	1	↑	XXXXXXXX	nVM	VMF [6:0]							XX

Description

nVM: nVM equals to "0" after power on reset and VCOM offset equals to program OTP value. When nVM set to "1", setting of VMF6-0 becomes valid and VCOMH/VCOML can be adjusted.

VMF [6:0]: Set the VCOM offset voltage.

VMF[6:0]	VCOMH	VCOML	VMF[6:0]	VCOMH	VCOML
0000000	VMH	VML	1000000	VMH	VML
0000001	VMH – 63	VML – 63	1000001	VMH + 1	VML + 1
0000010	VMH – 62	VML – 62	1000010	VMH + 2	VML + 2
0000011	VMH – 61	VML – 61	1000011	VMH + 3	VML + 3
0000100	VMH – 60	VML – 60	1000100	VMH + 4	VML + 4
0000101	VMH – 58	VML – 58	1000101	VMH + 5	VML + 5
0000110	VMH – 58	VML – 58	1000110	VMH + 6	VML + 6
0000111	VMH – 57	VML – 57	1000111	VMH + 7	VML + 7
0001000	VMH – 56	VML – 56	1001000	VMH + 8	VML + 8
0001001	VMH – 55	VML – 55	1001001	VMH + 9	VML + 9
0001010	VMH – 54	VML – 54	1001010	VMH + 10	VML + 10
0001011	VMH – 53	VML – 53	1001011	VMH + 11	VML + 11
0001100	VMH – 52	VML – 52	1001100	VMH + 12	VML + 12
0001101	VMH – 51	VML -51	1001101	VMH + 13	VML + 13
0001110	VMH – 50	VML – 50	1001110	VMH + 14	VML + 14
0001111	VMH – 49	VML – 49	1001111	VMH + 15	VML + 15
0010000	VMH – 48	VML – 48	1010000	VMH + 16	VML + 16
0010001	VMH – 47	VML – 47	1010001	VMH + 17	VML + 17
0010010	VMH – 46	VML – 46	1010010	VMH + 18	VML + 18
0010011	VMH – 45	VML – 45	1010011	VMH + 19	VML + 19
0010100	VMH – 44	VML – 44	1010100	VMH + 20	VML + 20
0010101	VMH – 43	VML – 43	1010101	VMH + 21	VML + 21
0010110	VMH – 42	VML – 42	1010110	VMH + 22	VML + 22
0010111	VMH – 41	VML – 41	1010111	VMH + 23	VML + 23
0011000	VMH – 40	VML – 40	1011000	VMH + 24	VML + 24
0011001	VMH – 39	VML – 39	1011001	VMH + 25	VML + 25
0011010	VMH – 38	VML – 38	1011010	VMH + 26	VML + 26
0011011	VMH – 37	VML – 37	1011011	VMH + 27	VML + 27
0011100	VMH – 36	VML – 36	1011100	VMH + 28	VML + 28
0011101	VMH – 35	VML – 35	1011101	VMH + 29	VML + 29
0011110	VMH – 34	VML – 34	1011110	VMH + 30	VML + 30
0011111	VMH – 33	VML – 33	1011111	VMH + 31	VML + 31
0100000	VMH – 32	VML – 32	1100000	VMH + 32	VML + 32
0100001	VMH – 31	VML – 31	1100001	VMH + 33	VML + 33
0100010	VMH – 30	VML – 30	1100010	VMH + 34	VML + 34
0100011	VMH – 29	VML – 29	1100011	VMH + 35	VML + 35
0100100	VMH – 28	VML – 28	1100100	VMH + 36	VML + 36
0100101	VMH – 27	VML – 27	1100101	VMH + 37	VML + 37
0100110	VMH – 26	VML – 26	1100110	VMH + 38	VML + 38
0100111	VMH – 25	VML – 25	1100111	VMH + 39	VML + 39
0101000	VMH – 24	VML – 24	1101000	VMH + 40	VML + 40
0101001	VMH – 23	VML – 23	1101001	VMH + 41	VML + 41
0101010	VMH – 22	VML – 22	1101010	VMH + 42	VML + 42
0101011	VMH – 21	VML – 21	1101011	VMH + 43	VML + 43
0101100	VMH – 20	VML – 20	1101100	VMH + 44	VML + 44
0101101	VMH – 19	VML – 19	1101101	VMH + 45	VML + 45
0101110	VMH – 18	VML – 18	1101110	VMH + 46	VML + 46
0101111	VMH – 17	VML – 17	1101111	VMH + 47	VML + 47
0110000	VMH – 16	VML – 16	1110000	VMH + 48	VML + 48
0110001	VMH – 15	VML – 15	1110001	VMH + 49	VML + 49
0110010	VMH – 14	VML – 14	1110010	VMH + 50	VML + 50
0110011	VMH – 13	VML – 13	1110011	VMH + 51	VML + 51
0110100	VMH – 12	VML – 12	1110100	VMH + 52	VML + 52
0110101	VMH – 11	VML – 11	1110101	VMH + 53	VML + 53

0110110	VMH – 10	VML – 10		1110110	VMH + 54	VML + 54
0110111	VMH – 9	VML – 9		1110111	VMH + 55	VML + 55
0111000	VMH – 8	VML – 8		1111000	VMH + 56	VML + 56
0111001	VMH – 7	VML – 7		1111001	VMH + 57	VML + 57
0111010	VMH – 6	VML – 6		1111010	VMH + 58	VML + 58
0111011	VMH – 5	VML – 5		1111011	VMH + 59	VML + 59
0111100	VMH – 4	VML – 4		1111100	VMH + 60	VML + 60
0111101	VMH – 3	VML – 3		1111101	VMH + 61	VML + 61
0111110	VMH – 2	VML – 2		1111110	VMH + 62	VML + 62
0111111	VMH – 1	VML – 1		1111111	VMH + 63	VML + 63

Restriction: Dummy_EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	nVM	VMF[6:0]
Power ON Sequence	1'b1	7'b1000000
S/W Reset	1'b1	7'b1000000

8.2.52. NV Memory Write (D0h)

D0h	NVMWR (NV Memory Write)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	1	0	0	0	0	D0h
1st Parameter	1	1	↑	XXXXXXXX	0	0	0	0	0	PGM_ADR [2:0]			XX
2nd Parameter	1	1	↑	XXXXXXXX	PGM_DATA [7:0]								XX

Description

This command is used to program the NV memory data. After a successful OTP operation, the information of PGM_DATA [7:0] will programmed to NV memory.

PGM_ADR [2:0]: The select bits of ID2, ID3 and VMF [6:0] programming.

PGM_ADR[2:0]			Programmed NV Memory Selection
0	0	0	ID2 programming
0	0	1	ID3 programming
0	1	0	VMF[6:0] programming
Others			Reserved

PGM_DATA [7:0]: The programmed data.

Restriction

Dummy_EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	PGM_ADR[2:0]	PGM_DATA[7:0]
Power ON Sequence	3'b000	8'bXXXXXXXX
S/W Reset	3'b000	8'bXXXXXXXX

8.2.53. NV Memory Protection Key (D1h)

D1h	NVMPKEY (NV Memory Protection Key)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	1	0	0	0	1	D1h
1st Parameter	1	1	↑	XXXXXXXX	KEY [23:16]								00h
2nd Parameter	1	1	↑	XXXXXXXX	KEY [15:8]								00h
3rd Parameter	1	1	↑	XXXXXXXX	KEY [7:0]								00h
Description	**KEY [23:0]:** NV memory programming protection key. When writing OTP data to D0h, this register must be set to 0x55AA66h to enable OTP programming. If D1h register is not written with 0x55AA66h, then NV memory programming will be aborted.												
Restriction	Dummy_EXTC should be high to enable this command												

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	24'h000000h
S/W Reset	24'h000000h

8.2.54. NV Memory Status Read (D2h)

D2h	RDNVM (NV Memory Status Read)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	1	0	0	1	0	D2h
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XXXXXXXX	ID3_CNT [3:0]				ID2_CNT [3:0]				XX
3rd Parameter	1	↑	1	XXXXXXXX	BUSY	X	X	X	VMF_CNT [3:0]				XX
4th Parameter	1	↑	1	XXXXXXXX	OTP_DATA[7:0]								XX

Description

PGM_CNT [1:0]: NV memory program record. The bits will increase "+1" automatically after writing the NV_VMF [5:0] to NV memory.

ID2_CNT[3:0] / ID3_CNT[3:0] / VMF_CNT[3:0]				Description
0	0	0	0	No Programmed
0	0	0	1	Programmed 1 time
0	0	1	1	Programmed 2 times
0	1	1	1	Programmed 3 times
1	1	1	1	Programmed 4 times

BUSY: The status bit of NV memory programming.

BUSY	The Status of NV Memory
0	Idle
1	Busy

OTP_DATA [7:0]: The programmed value of VMF parameter in NV memory. This function is only for read operation.

Restriction

Dummy_EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value				
	ID3_CNT	ID2_CNT	VMF_CNT	BUSY	OTP_DATA
Power ON Sequence	X	X	X	X	X
S/W Reset	X	X	X	X	X

8.2.55. Read ID4 (D3h)

D4h	RDID4 (Read ID4)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	1	0	0	1	1	D3h
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2ndParameter	1	↑	1	XXXXXXXX	0	0	0	0	0	0	0	0	00h
3rdParameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
4th Parameter	1	↑	1	XXXXXXXX	0	0	1	1	1	0	0	0	38h
Description	Read IC device code. The 1st parameter is dummy read period. The 2nd parameter means the IC version. The 3rd and 4th parameter mean the IC model name.												
Restriction	Dummy_EXTC should be high to enable this command												
Register Availability													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	ID4=24'h00XX38h
S/W Reset	ID4=24'h00XX38h

8.2.56. Positive Gamma Correction (E0h)

E0h	PGAMCTRL (Positive Gamma Control)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	1	0	0	0	0	0	E0h
1st Parameter	1	1	↑	XXXXXXXX	0	0	0	0	VP63 [3:0]				XX
2ndParameter	1	1	↑	XXXXXXXX	0	0	VP62 [5:0]						XX
3rdParameter	1	1	↑	XXXXXXXX	0	0	VP61 [5:0]						XX
4th Parameter	1	1	↑	XXXXXXXX	0	0	0	0	VP59 [3:0]				XX
5th Parameter	1	1	↑	XXXXXXXX	0	0	0	VP57 [4:0]					XX
6th Parameter	1	1	↑	XXXXXXXX	0	0	0	0	VP50 [3:0]				XX
7th Parameter	1	1	↑	XXXXXXXX	0	VP43 [6:0]							XX
8th Parameter	1	1	↑	XXXXXXXX	VP36 [3:0]				VP27 [3:0]				XX
9th Parameter	1	1	↑	XXXXXXXX	0	VP20 [6:0]							XX
10thParameter	1	1	↑	XXXXXXXX	0	0	0	0	VP13 [3:0]				XX
11thParameter	1	1	↑	XXXXXXXX	0	0	0	VP6 [4:0]					XX
12thParameter	1	1	↑	XXXXXXXX	0	0	0	0	VP4 [3:0]				XX
13thParameter	1	1	↑	XXXXXXXX	0	0	VP2 [5:0]						XX
14thParameter	1	1	↑	XXXXXXXX	0	0	VP1 [5:0]						XX
15thParameter	1	1	↑	XXXXXXXX	0	0	0	0	VP0 [3:0]				XX
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.												
Restriction	Dummy_EXTC should be high to enable this command												
Register Availability													
Default													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

8.2.57. Negative Gamma Correction (E1h)

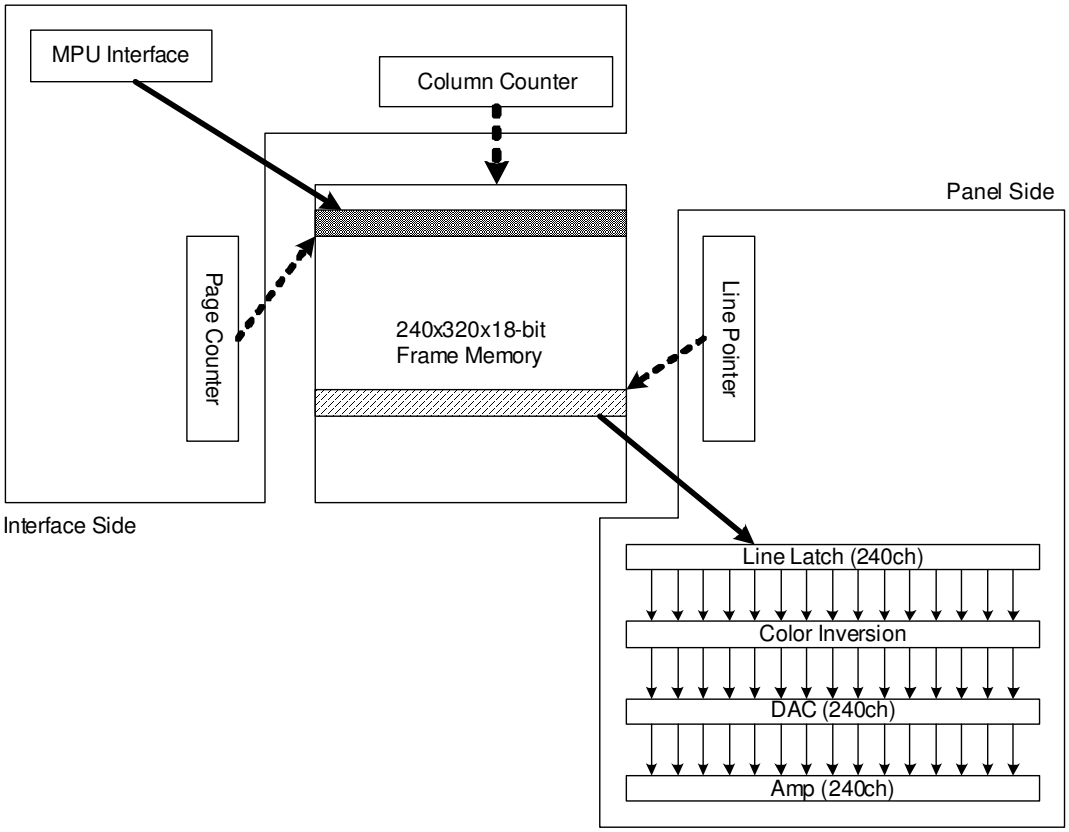
E1h	NGAMCTRL (Negative Gamma Correction)												
	D/CX	RDX	WRX	D [15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	1	0	0	0	0	1	E1h
1st Parameter	1	1	↑	XXXXXXXX	0	0	0	0	VN63 [3:0]				XX
2ndParameter	1	1	↑	XXXXXXXX	0	0	VN62 [5:0]						XX
3rdParameter	1	1	↑	XXXXXXXX	0	0	VN61 [5:0]						XX
4th Parameter	1	1	↑	XXXXXXXX	0	0	0	0	VN59 [3:0]				XX
5th Parameter	1	1	↑	XXXXXXXX	0	0	0	VN57 [4:0]					XX
6th Parameter	1	1	↑	XXXXXXXX	0	0	0	0	VN50 [3:0]				XX
7th Parameter	1	1	↑	XXXXXXXX	0	VN43 [6:0]							XX
8th Parameter	1	1	↑	XXXXXXXX	VN36 [3:0]				VN27 [3:0]				XX
9th Parameter	1	1	↑	XXXXXXXX	0	VN20 [6:0]							XX
10thParameter	1	1	↑	XXXXXXXX	0	0	0	0	VN13 [3:0]				XX
11thParameter	1	1	↑	XXXXXXXX	0	0	0	VN6 [4:0]					XX
12thParameter	1	1	↑	XXXXXXXX	0	0	0	0	VN4 [3:0]				XX
13thParameter	1	1	↑	XXXXXXXX	0	0	VN2 [5:0]						XX
14thParameter	1	1	↑	XXXXXXXX	0	0	VN1 [5:0]						XX
15thParameter	1	1	↑	XXXXXXXX	0	0	0	0	VN0 [3:0]				XX
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.												
Restriction	Dummy_EXTC should be high to enable this command												
Register Availability													
Default													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

9. Display Data RAM

9.1. Configuration

The display data RAM stores display dots and consists of 1,382,400 bits (240x18x320 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous panel read and interface read or write display data to the same location of the frame memory.

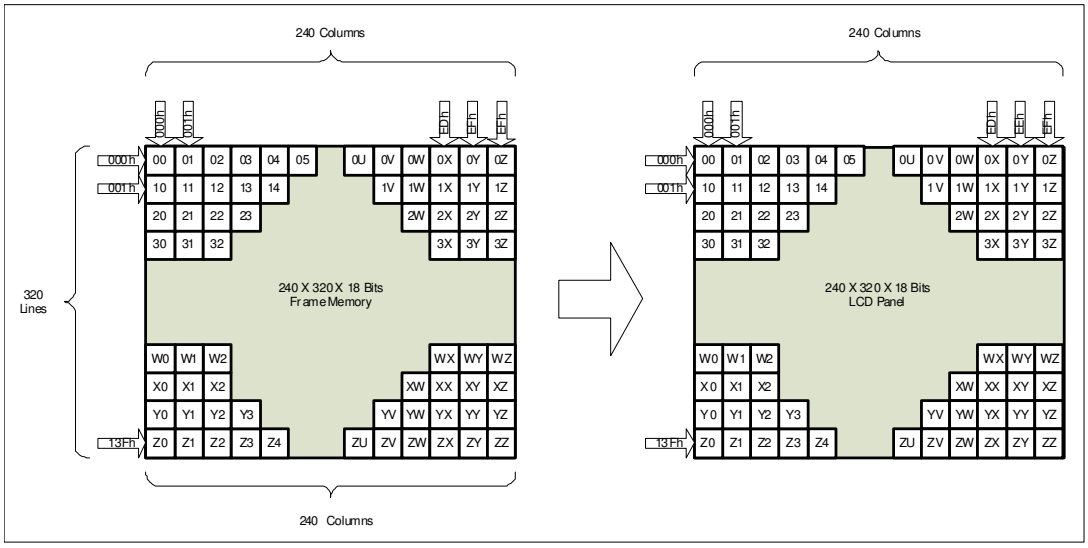


9.2. Memory to Display Address Mapping

9.2.1. Normal Display ON or Partial Mode ON, Vertical Scroll Mode OFF

In this mode, the content of frame memory within an area where column pointer is 0000h to 00EFh and page pointer is 0000h to 013Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0)

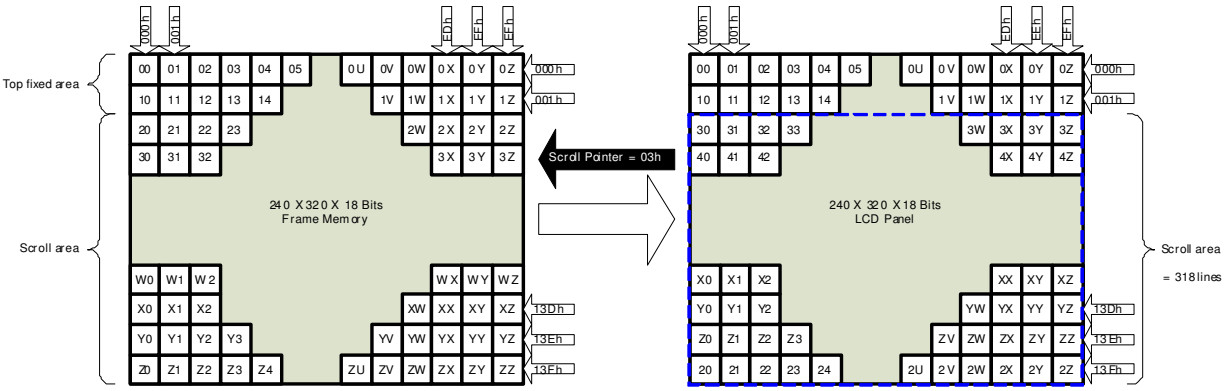


9.2.2. Vertical Scroll Mode

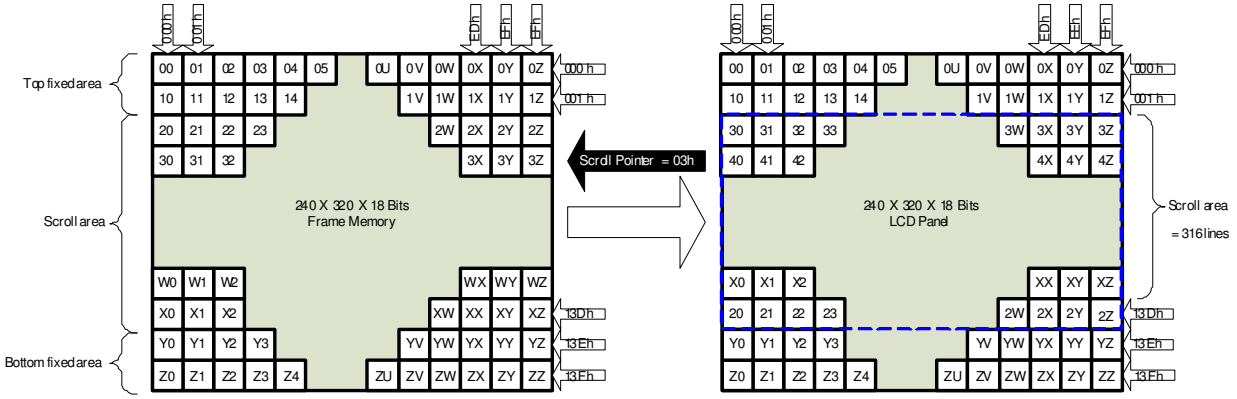
There is a vertical scrolling mode, which is determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

The Vertical Scroll Mode function is explained by these examples in the following.

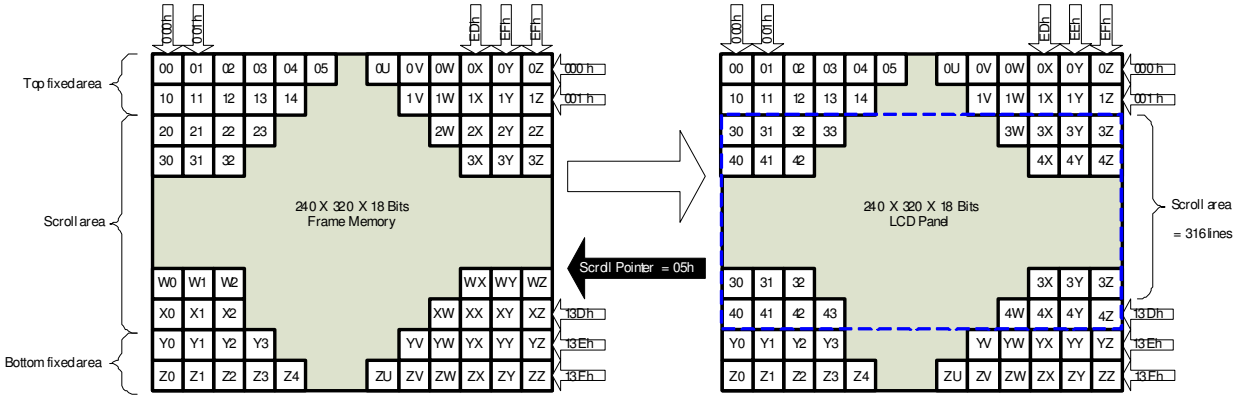
TFA=2, VSA=318, BFA=0 when MADCTL ML bit = 0



TFA=2, VSA=316, BFA=2 when MADCTL ML bit = 0



TFA=2, VSA=316, BFA=4 when MADCTL ML bit = 0



Note: When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) ≠ 320, Scrolling Mode is undefined.

9.2.3. Vertical Scroll Example

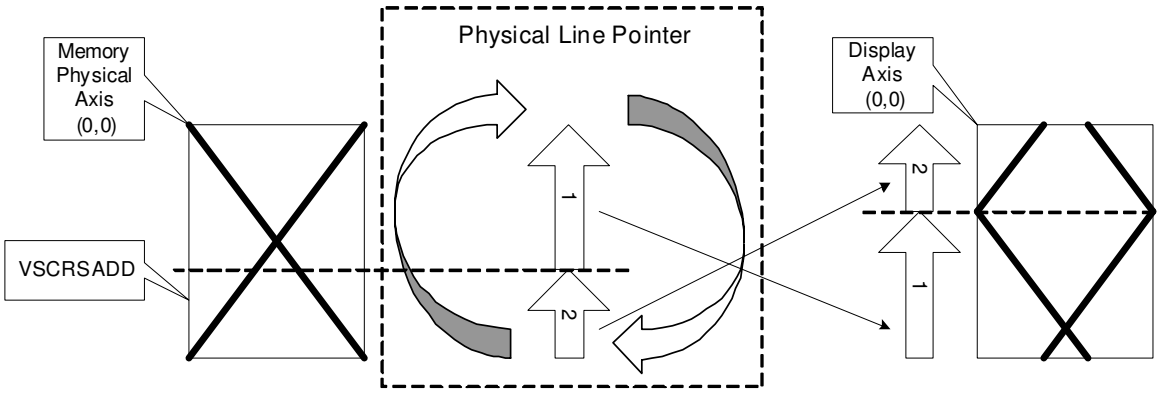
9.2.4. Case1: TFA+VSA+BFA < 320

This setting is prohibited, unless unexpected picture will be shown.

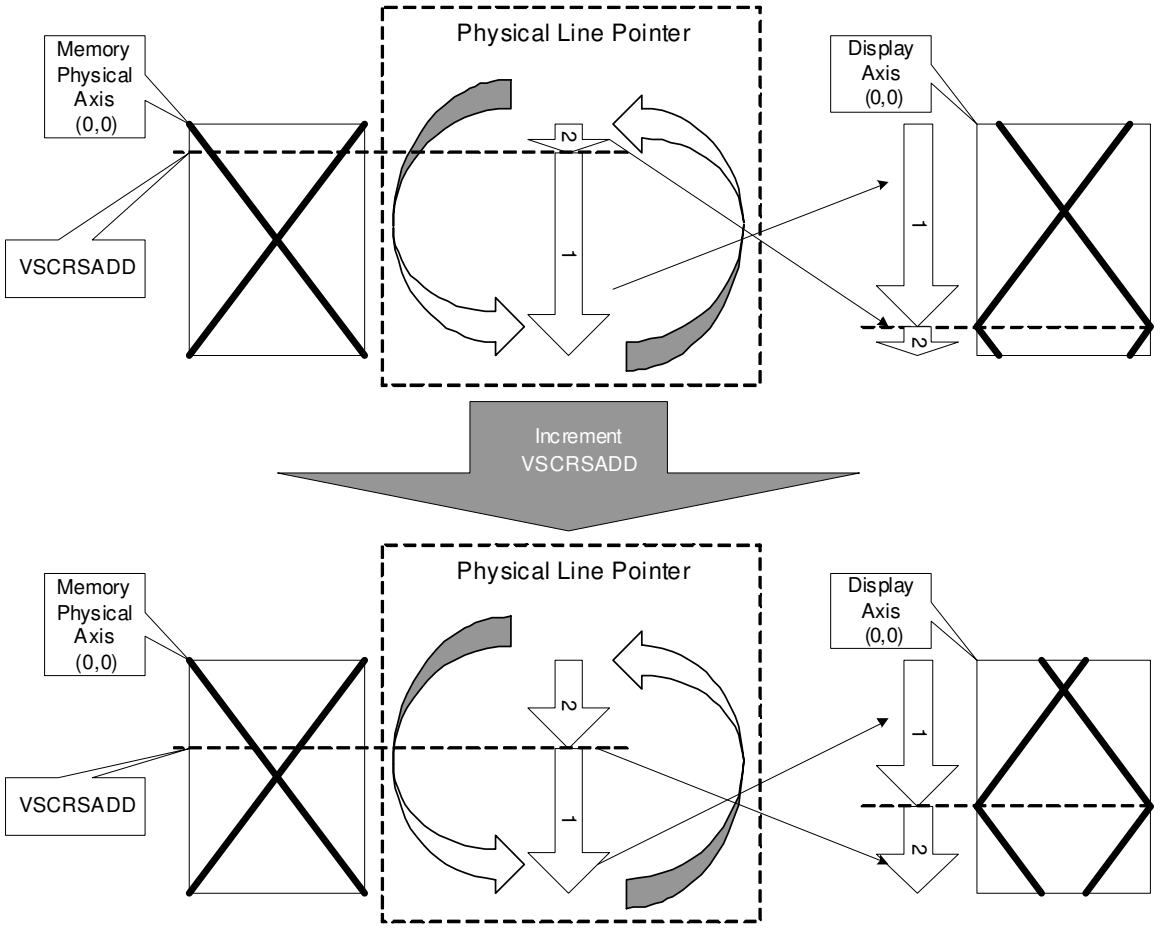
9.2.5. Case2: TFA+VSA+BFA = 320 (Rolling Scrolling)

The operation of Rolling Scrolling is explained by these examples in the following.

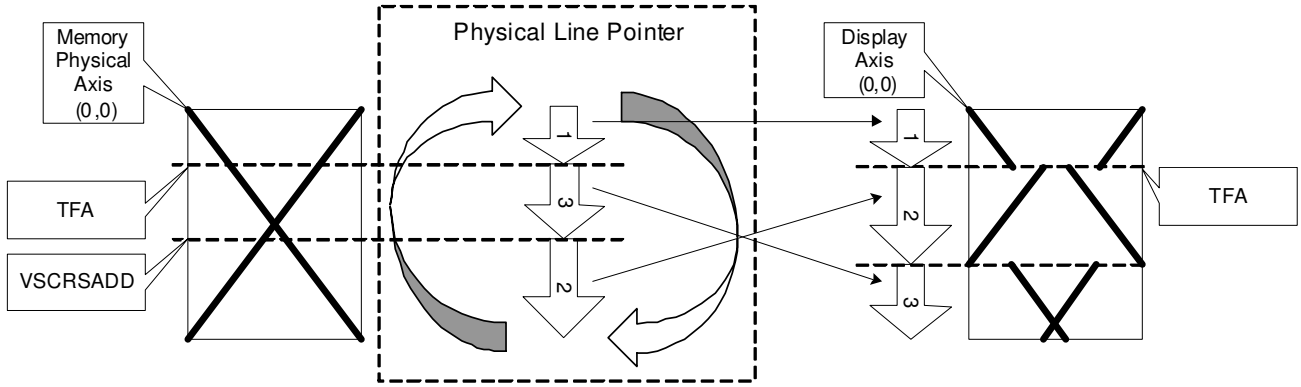
When TFA=0, VSA=320, BFA=0, VSCRSADD=40 and MADCTL ML bit = 1



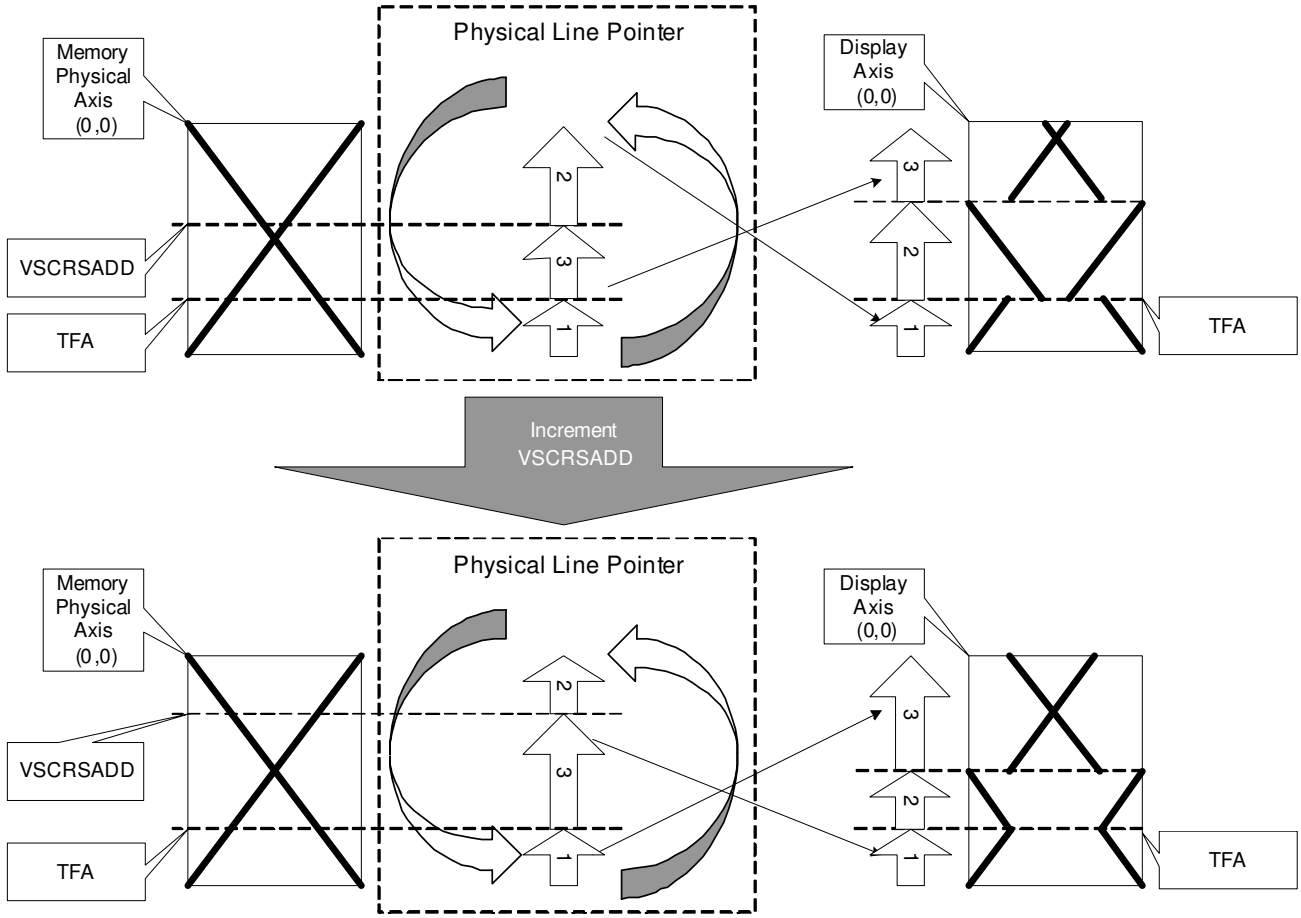
When TFA=0, VSA=320, BFA=0, VSCRSADD=40 and MADCTL ML bit = 0



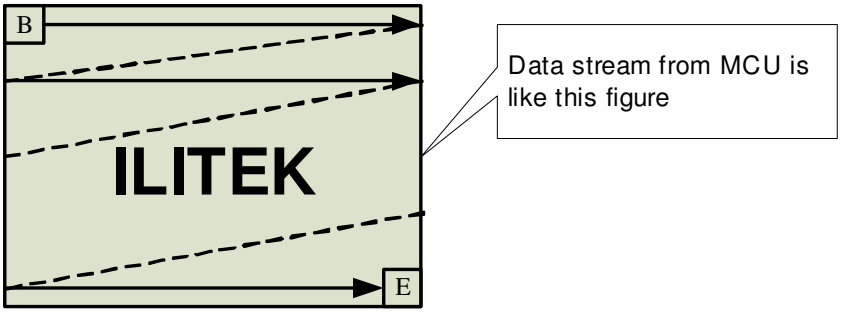
When TFA=30, VSA=290, BFA=0, VSCRSADD=80 and MADCTL ML bit = 0



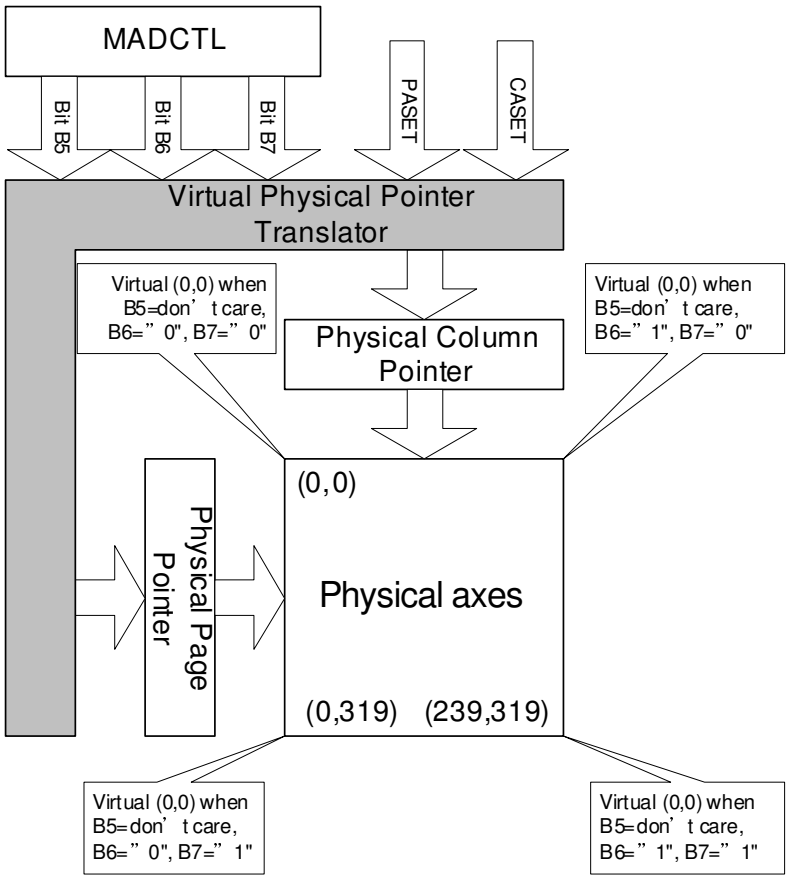
When TFA=30, VSA=290, BFA=0, VSCRSADD=80 and MADCTL ML bit = 1



9.3. MCU to memory write/read direction



The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, Bits B5, B6, and B7 as described below.



B5	B6	B7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319-Physical Page Pointer)
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (239-Physical Column Pointer)	Direct to (319-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (319-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (319-Physical Page Pointer)	Direct to (239-Physical Column Pointer)

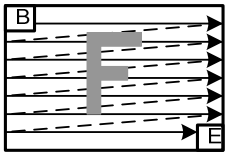
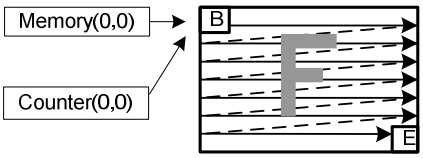
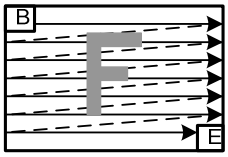
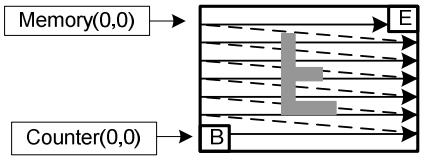
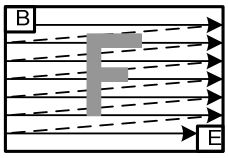
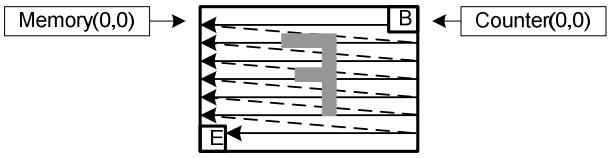
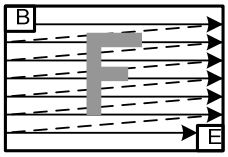
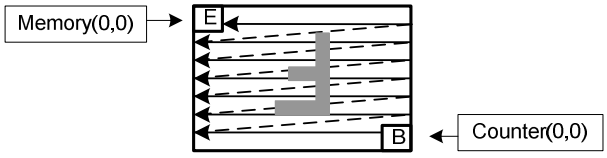
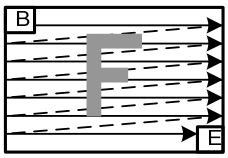
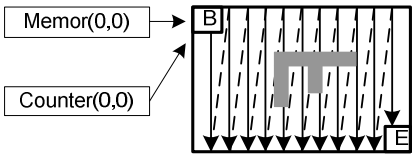
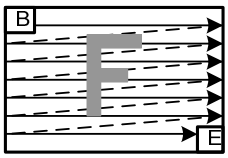
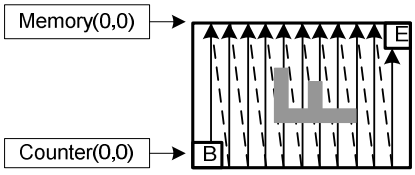
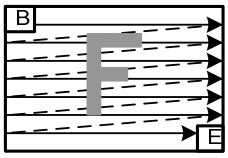
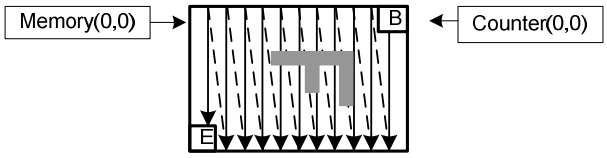
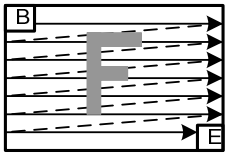
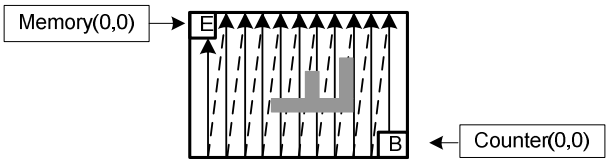
Condition	Column Counter	Page counter
When RAMWR/RAMRD command is accepted	Return to “Start column”	Return to “Start Page”
Complete Pixel Read/Write action	Increment by 1	No change
The Column values is large than “End Column”	Return to “Start column”	Increment by 1
The Page counter is large than “End Page”	Return to “Start column”	Return to “Start Page”

Note:

Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7, B6 and B5. The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

Display Data Direction	MADCTR Parameter			Image in the Memory (MPU)	Image in the Driver (Frame Memory)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Y Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
XY Exchange X-Mirror	1	1	0		
XY Exchange X-Y Mirror	1	1	1		

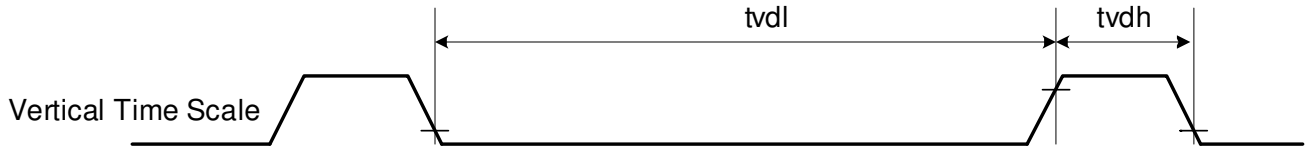
10. Tearing Effect Output

The Tearing Effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the parameter of the Tearing Effect Line Off & On commands.

The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

10.1. Tearing Effect Line Modes

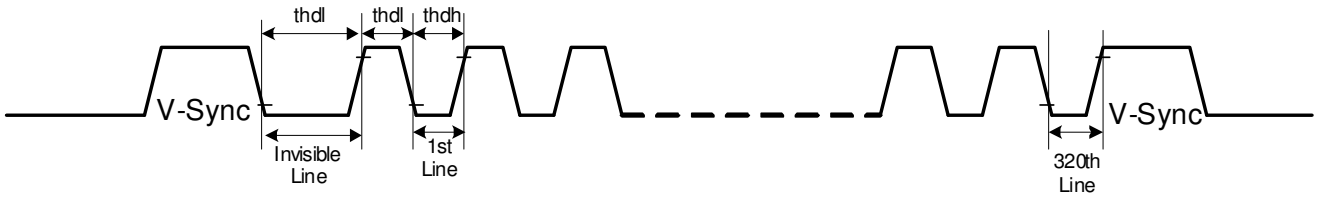
Mode 1, the Tearing Effect Output signal consists of V-Sync information only:



tvdh = The LCD display is not updated from the Frame Memory.

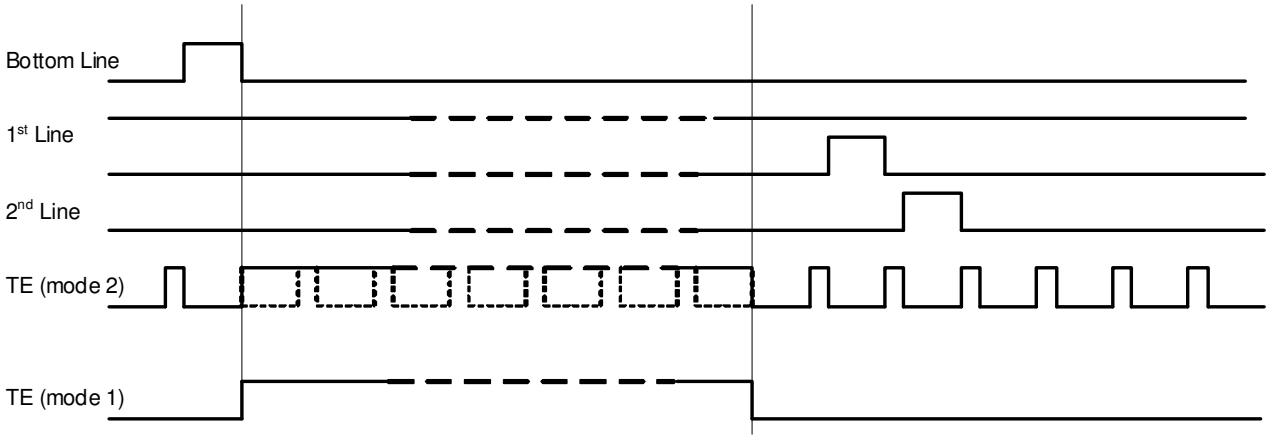
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

Mode 2, the tearing effect output signal consists of V-Sync and H-Sync information; there is one V-sync and 320 H-sync pulses per field:



thdh = The LCD display is not updated from the Frame Memory.

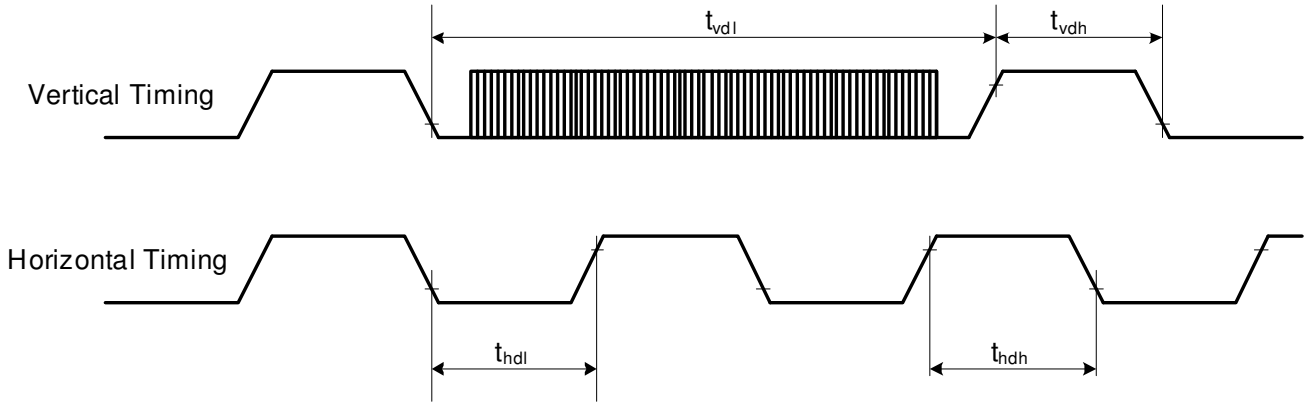
thdl = The LCD display is updated from the Frame Memory (except Invisible Line – see above).



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

10.2. Tearing Effect Line Timings

The tearing effect signal is described below:

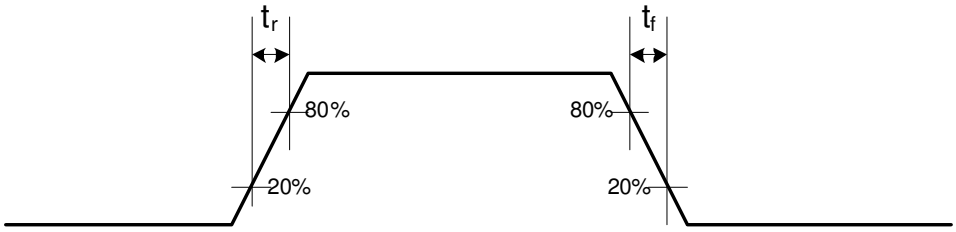


AC characteristics of Tearing Effect Signal (Frame Rate = 60Hz)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
t_{vdl}	Vertical timing low duration	--	--	--	ms	
t_{vdh}	Vertical timing high duration	1000	--	--	us	
t_{hdl}	Horizontal timing low duration	--	--	--	us	
t_{hdh}	Horizontal timing high duration	--	--	500	us	

Note:

1. The timings in Table as above apply when MADCTL B4=0 and B4=1
2. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

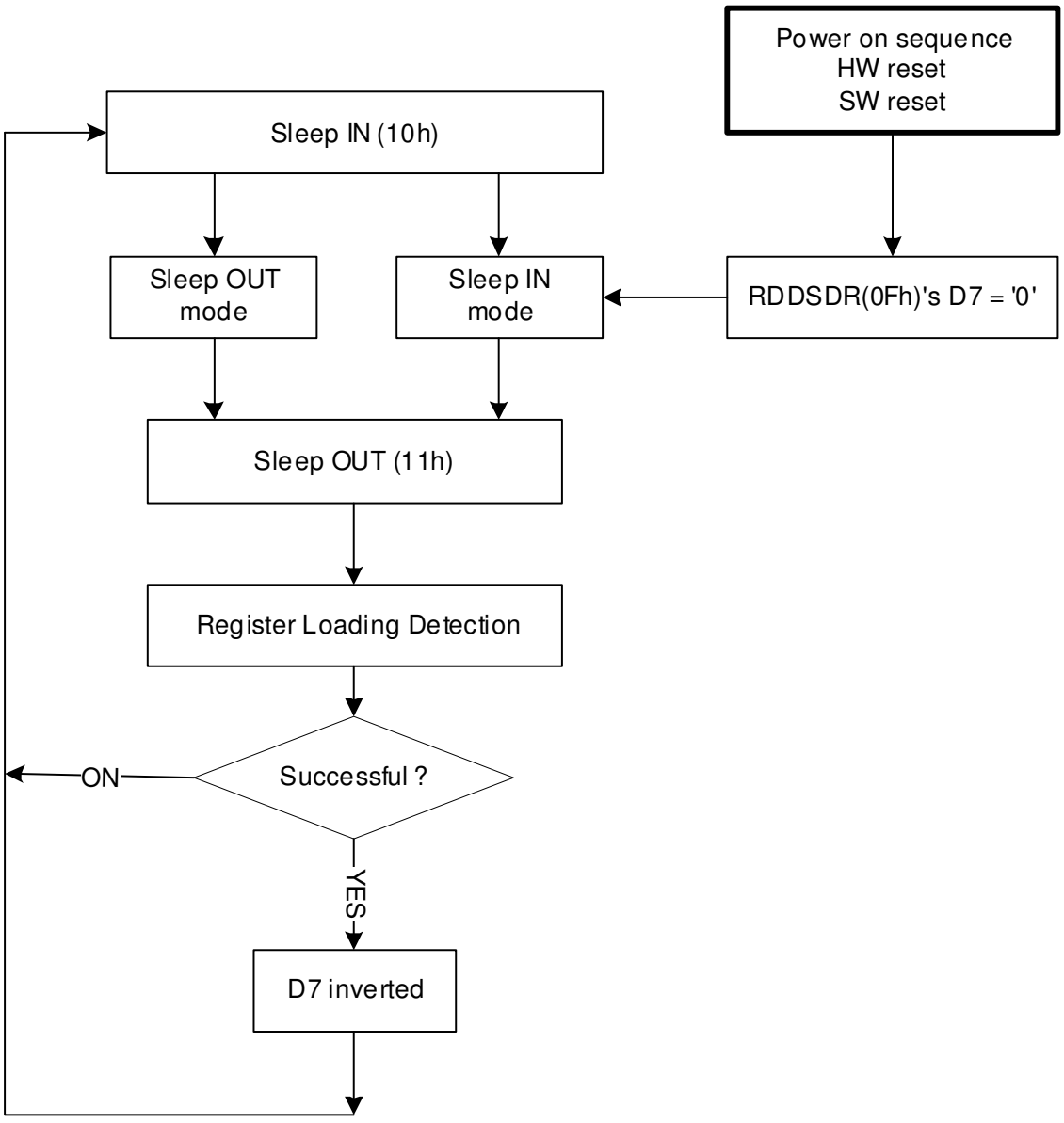
11. Sleep Out – Command and Self-Diagnostic Functions of the Display Module

11.1. Register loading Detection

Sleep Out-command (Command “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EV Memory(or similar device) to registers of the display controller is working properly.

If the register loading detection is successfully, there is inverted (= increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D7). If it is failure, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following:

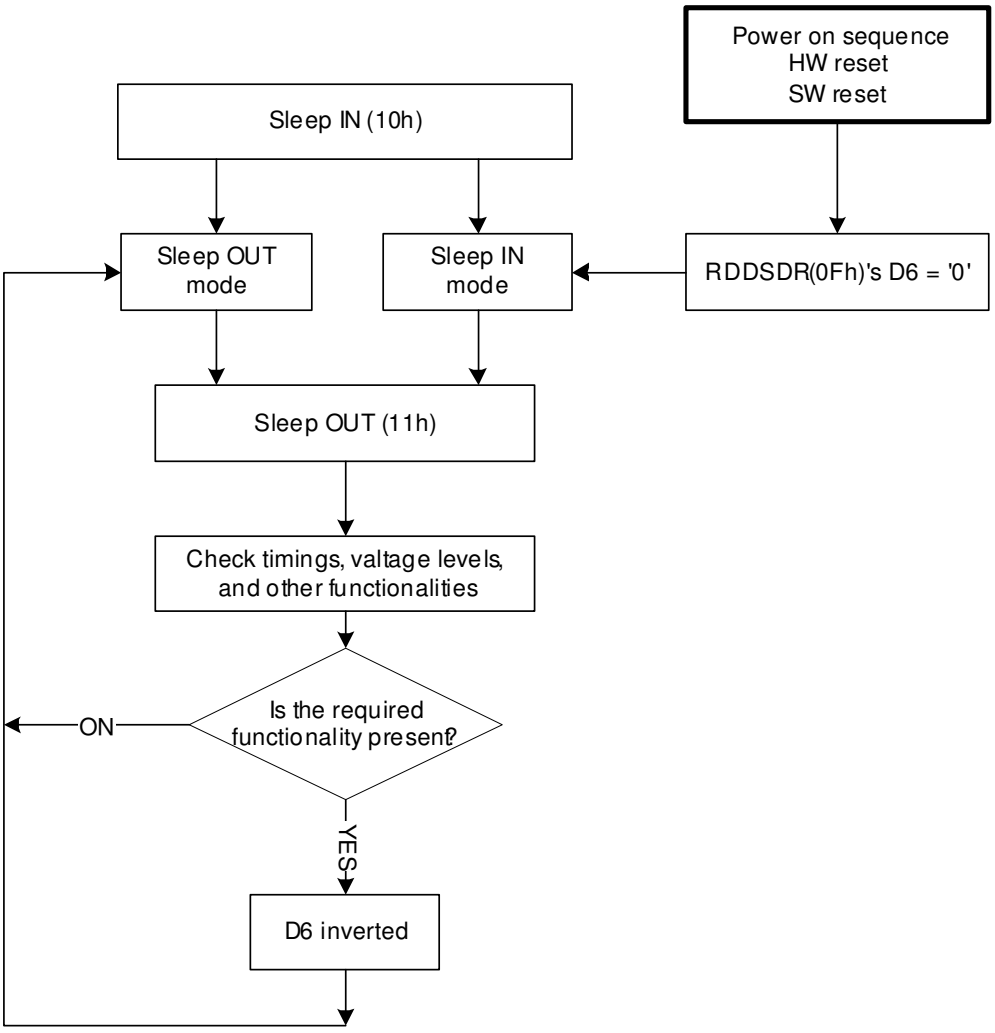


11.2. Functionality Detection

Sleep Out-command (Command “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.) If functionality requirement is met, there is an inverted (= increased by 1) bit, which defined in command “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.

The flow chart for this internal function is following:



Note 1: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if User’s functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.

12. Power ON/OFF Sequence

VDDI and VDD can be applied in any order.

VDD and VDDI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.

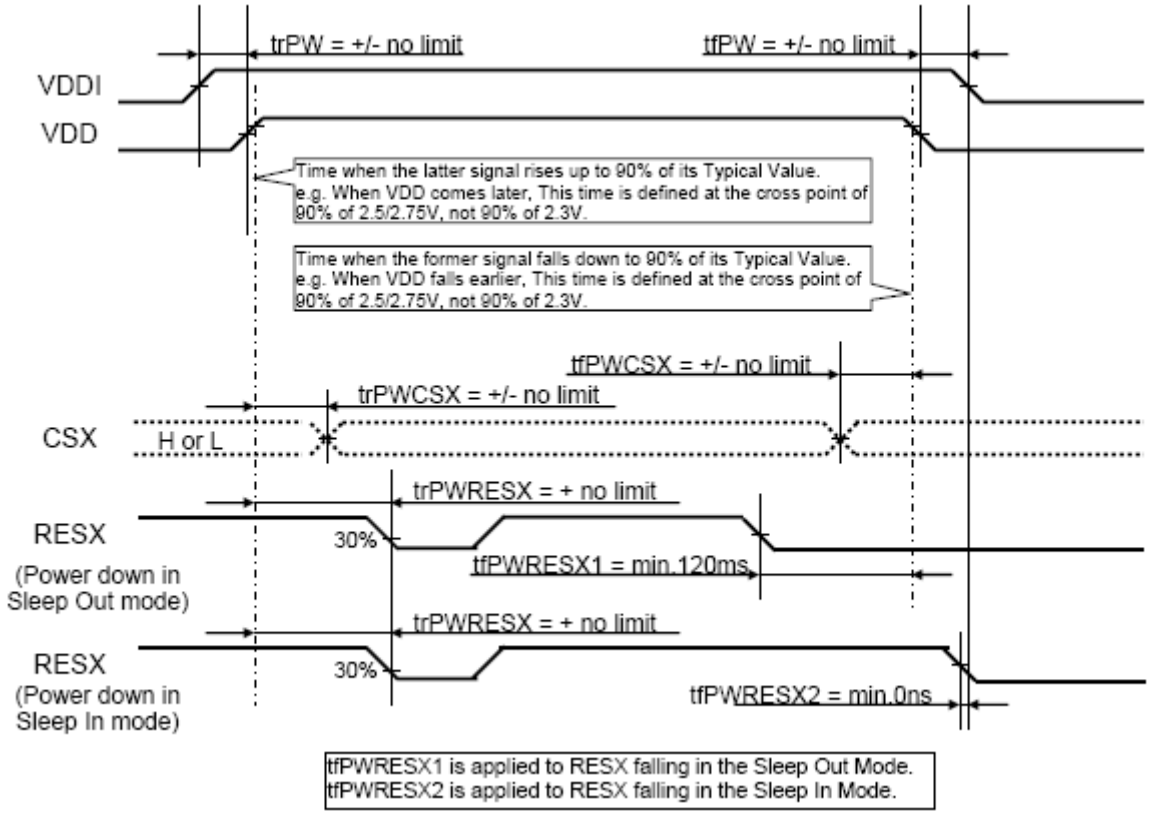
Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in Sections 12.1 and 12.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

12.1. Case 1 – RESX line is held High or Unstable by Host at Power ON

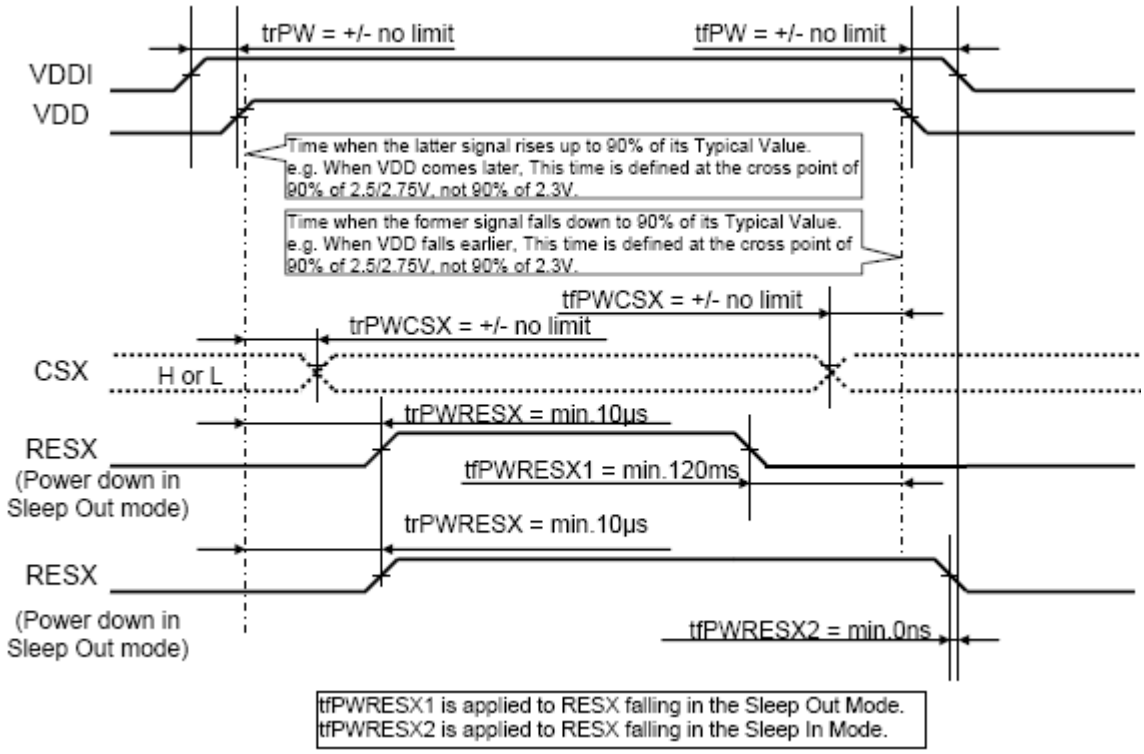
If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.

12.2. Case 2 – RESX line is held Low by Host at Power ON

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VDD and VDDI have been applied.



Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.

12.3. Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off event, ILI9338B will force the display to blank and will not be any abnormal visible effects with in 1 second on the display and remains blank until “Power On Sequence” actives.

13. Power Level Definition

13.1. Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

   In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.

   In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

   In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.

   In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode.

   In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.

6. Deep Standby Mode.

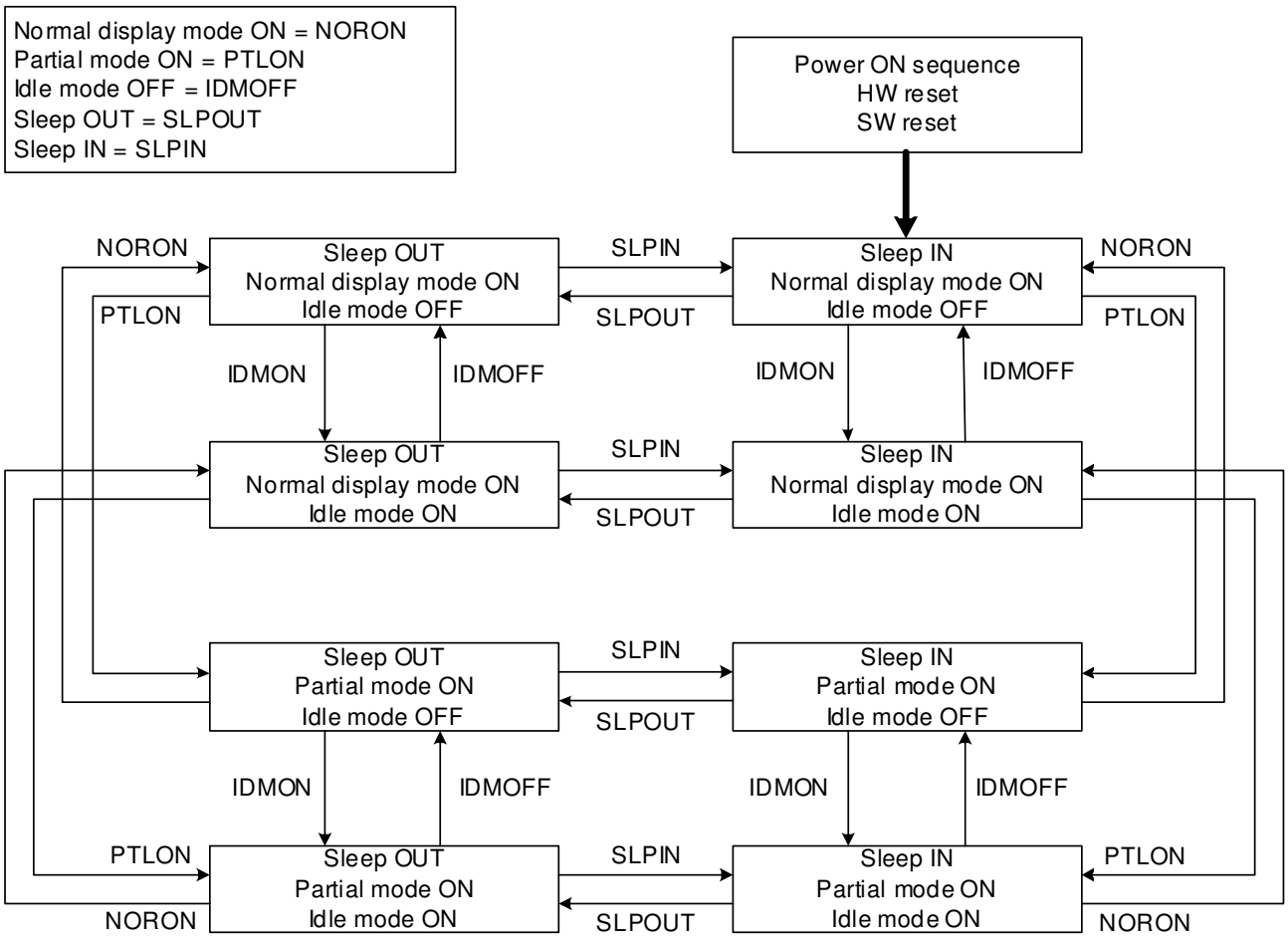
   In Deep Standby mode, both internal logic power and SRAM power are turn off, the display data stored in the Frame Memory and the instructions are not saved. Rewrite Frame Memory content and instructions after the Deep Standby Mode is exited.

7. Power Off Mode.

   In this mode, both VDD and VDDI are removed.

Note1: Transition between modes 1-6 is controllable by MCU commands. Mode 7 is entered only when both Power supplies are removed.

13.2. Power Flow Chart



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

14. Gamma Curves Selection

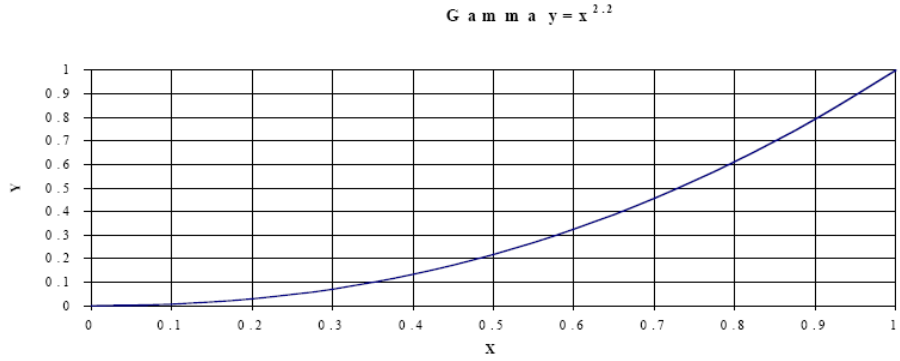
ILI9338B provide four gamma curves (Gamma1.0, Gamma1.8, Gamma2.2 and Gamma2.5). The gamma curve can be selected by the GC0 to GC3 settings.

14.1. Gamma Default Values (for NW type LC)

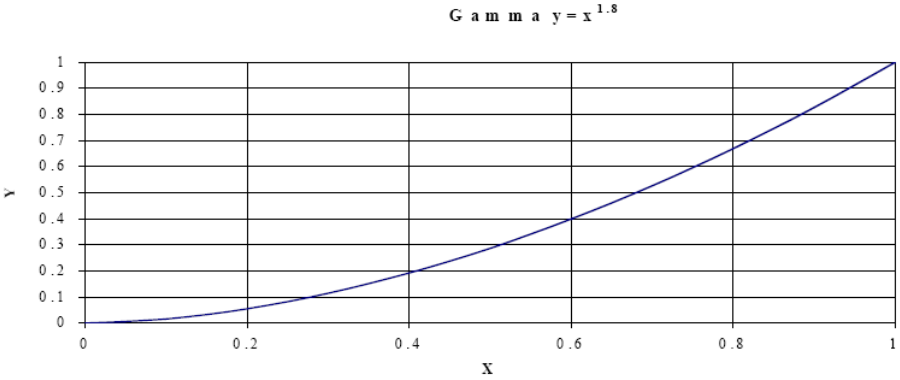
Data	Output Voltage									
	VCOM = Low					VCOM = High				
	Gamma	1.0	1.8	2.2	2.5	Gamma	1.0	1.8	2.2	2.5
0	V0P	4.082	4.083	4.084	4.084	V0N	0.279	0.278	0.277	0.276
1	V1P	2.944	3.842	4.015	4.049	V1N	1.278	0.519	0.346	0.310
2	V2P	2.736	3.566	3.843	3.981	V2N	1.623	0.793	0.482	0.345
3	V3P	2.617	3.384	3.681	3.863	V3N	1.728	0.952	0.629	0.465
4	V4P	2.498	3.202	3.518	3.745	V4N	1.834	1.111	0.776	0.585
5	V5P	2.439	3.090	3.445	3.612	V5N	1.891	1.217	0.924	0.736
6	V6P	2.380	2.978	3.371	3.480	V6N	1.948	1.324	1.071	0.887
7	V7P	2.330	2.901	3.285	3.389	V7N	1.995	1.401	1.157	0.980
8	V8P	2.281	2.825	3.199	3.298	V8N	2.042	1.478	1.242	1.073
9	V9P	2.240	2.761	3.128	3.223	V9N	2.081	1.542	1.314	1.150
10	V10P	2.199	2.697	3.056	3.147	V10N	2.120	1.606	1.385	1.228
11	V11P	2.158	2.633	2.985	3.071	V11N	2.159	1.670	1.456	1.305
12	V12P	2.125	2.582	2.928	3.011	V12N	2.191	1.722	1.513	1.367
13	V13P	2.092	2.531	2.871	2.950	V13N	2.222	1.773	1.570	1.429
14	V14P	2.067	2.484	2.802	2.891	V14N	2.249	1.817	1.619	1.484
15	V15P	2.041	2.437	2.733	2.832	V15N	2.276	1.861	1.668	1.540
16	V16P	2.019	2.397	2.674	2.782	V16N	2.299	1.899	1.710	1.587
17	V17P	1.998	2.357	2.615	2.731	V17N	2.322	1.937	1.753	1.634
18	V18P	1.976	2.317	2.557	2.681	V18N	2.345	1.975	1.795	1.682
19	V19P	1.958	2.284	2.508	2.639	V19N	2.365	2.006	1.830	1.721
20	V20P	1.940	2.251	2.458	2.597	V20N	2.384	2.038	1.865	1.761
21	V21P	1.918	2.224	2.425	2.560	V21N	2.404	2.064	1.899	1.798
22	V22P	1.897	2.197	2.391	2.522	V22N	2.424	2.091	1.932	1.836
23	V23P	1.876	2.171	2.357	2.485	V23N	2.444	2.117	1.966	1.873
24	V24P	1.854	2.144	2.323	2.447	V24N	2.464	2.144	2.000	1.911
25	V25P	1.833	2.117	2.289	2.410	V25N	2.484	2.170	2.034	1.948
26	V26P	1.812	2.090	2.256	2.373	V26N	2.504	2.197	2.068	1.986
27	V27P	1.790	2.064	2.222	2.335	V27N	2.524	2.224	2.102	2.023
28	V28P	1.772	2.041	2.193	2.304	V28N	2.540	2.246	2.129	2.052
29	V29P	1.754	2.019	2.165	2.273	V29N	2.557	2.269	2.155	2.082
30	V30P	1.736	1.996	2.136	2.241	V30N	2.574	2.291	2.182	2.111
31	V31P	1.726	1.974	2.108	2.210	V31N	2.591	2.313	2.208	2.141
32	V32P	1.699	1.951	2.080	2.178	V32N	2.609	2.336	2.235	2.170
33	V33P	1.681	1.928	2.051	2.147	V33N	2.625	2.358	2.262	2.199
34	V34P	1.663	1.906	2.023	2.116	V34N	2.642	2.381	2.288	2.229
35	V35P	1.645	1.883	1.994	2.084	V35N	2.659	2.403	2.315	2.258
36	V36P	1.627	1.861	1.966	2.053	V36N	2.676	2.426	2.342	2.287
37	V37P	1.611	1.842	1.942	2.026	V37N	2.694	2.450	2.368	2.317
38	V38P	1.596	1.822	1.917	1.999	V38N	2.713	2.475	2.395	2.346
39	V39P	1.580	1.803	1.893	1.973	V39N	2.731	2.499	2.421	2.376
40	V40P	1.565	1.784	1.869	1.946	V40N	2.749	2.524	2.448	2.405
41	V41P	1.550	1.765	1.845	1.919	V41N	2.768	2.548	2.475	2.434
42	V42P	1.534	1.746	1.820	1.892	V42N	2.786	2.573	2.501	2.464
43	V43P	1.519	1.727	1.796	1.866	V43N	2.805	2.597	2.528	2.493
44	V44P	1.504	1.706	1.776	1.845	V44N	2.819	2.614	2.549	2.513
45	V45P	1.489	1.685	1.755	1.825	V45N	2.834	2.632	2.571	2.533
46	V46P	1.472	1.660	1.730	1.801	V46N	2.852	2.652	2.597	2.557
47	V47P	1.454	1.635	1.706	1.777	V47N	2.869	2.673	2.623	2.581
48	V48P	1.436	1.610	1.681	1.753	V48N	2.887	2.694	2.649	2.605
49	V49P	1.415	1.581	1.653	1.725	V49N	2.908	2.718	2.679	2.633
50	V50P	1.395	1.552	1.624	1.697	V50N	2.928	2.743	2.710	2.661
51	V51P	1.376	1.529	1.598	1.672	V51N	2.947	2.768	2.735	2.688
52	V52P	1.358	1.506	1.573	1.647	V52N	2.966	2.794	2.761	2.715
53	V53P	1.335	1.478	1.541	1.615	V53N	2.990	2.826	2.793	2.749
54	V54P	1.311	1.449	1.508	1.583	V54N	3.013	2.859	2.825	2.783
55	V55P	1.288	1.421	1.476	1.551	V55N	3.037	2.891	2.857	2.817
56	V56P	1.261	1.386	1.438	1.513	V56N	3.065	2.929	2.895	2.858
57	V57P	1.233	1.352	1.400	1.475	V57N	3.093	2.968	2.933	2.899
58	V58P	1.204	1.321	1.359	1.418	V58N	3.145	3.034	2.982	2.955
59	V59P	1.175	1.289	1.319	1.362	V59N	3.196	3.101	3.031	3.011
60	V60P	1.122	1.214	1.246	1.285	V60N	3.243	3.161	3.109	3.081
61	V61P	1.069	1.139	1.173	1.208	V61N	3.290	3.220	3.186	3.151
62	V62P	0.897	1.036	1.070	1.070	V62N	3.428	3.324	3.289	3.255
63	V63P	0.279	0.279	0.279	0.279	V63N	4.083	4.083	4.083	4.083

14.2. Gamma Curves

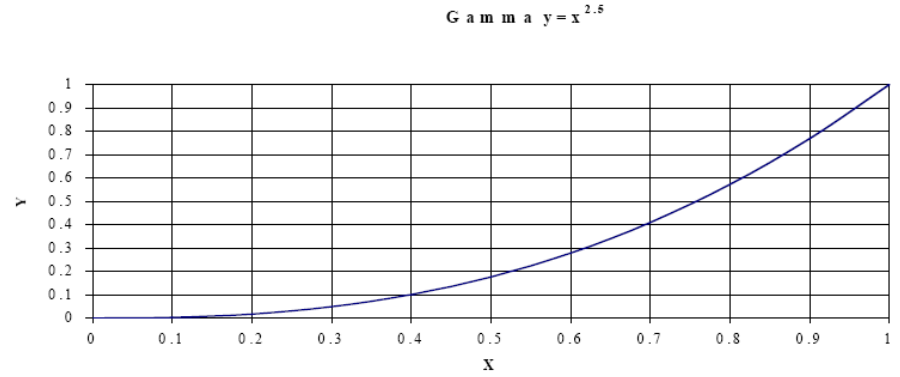
14.2.1. Gamma Curve 1 (GC0), applies the function $y=x^{2.2}$



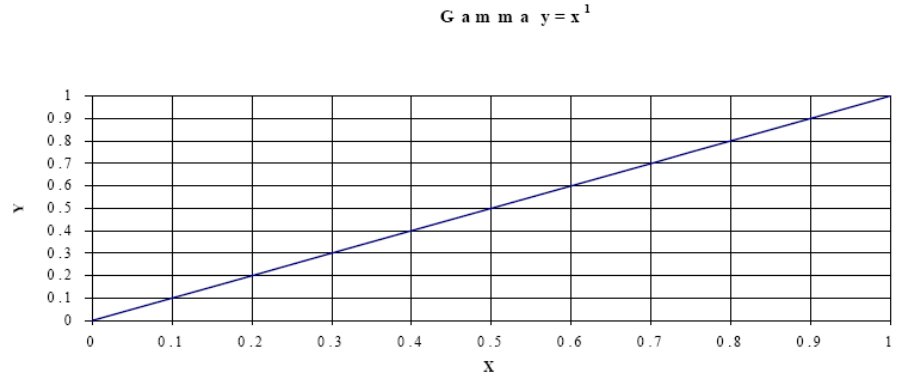
14.2.2. Gamma Curve 2 (GC1), applies the function $y=x^{1.8}$



14.2.3. Gamma Curve 3 (GC2), applies the function $y=x^{2.5}$



14.2.4. Gamma Curve 4 (GC3), applies the function $y=x^{1.0}$



15. Reset

15.1. Registers

The registers that are initialized are listed as below:

	After Powered ON	After Hardware Reset	After Software Reset
Frame Memory	Random	After Repair Values	No Change
Sleep	In	In	In
Display Mode	Normal	Normal	Normal
Display	Off	Off	Off
Idle	Off	Off	Off
Column Start Address	0000 h	0000 h	0000 h
Column End Address	00EF h	00EF h	If MADCTL's B5=0:00EF h If MADCTL's B5=1:013F h
Page Start Address	0000 h	0000 h	0000 h
Page End Address	013F h	013F h	If MADCTL's B5 = 0:013F h If MADCTL's B5=1:00EF h
Gamma Setting	GC0	GC0	GC0
Partial Area Start	0000 h	0000 h	0000 h
Partial Area End	013F h	013F h	013F h
Memory Data Access Control	00 h	00 h	No Change
RDDPM	08 h	08 h	08 h
RDDMADCTL	00 h	00 h	No Change
RDDCOLMOD	06 h	06 h	06 h
RDDIM	00 h	00 h	00 h
RDDSM	00 h	00 h	00 h
RDDSDR	00 h	00 h	00 h
TE Output Line	Off	Off	Off
TE Line Mode	Mode 1 (Note 3)	Mode 1 (Note 3)	Mode 1 (Note 3)

Note 1: There will be no abnormal visible effects on the display when S/W or H/W Resets are applied.

Note 2: After Powered-On Reset finishes within 10µs after both VDD & VDDI are applied.

Note 3: Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

Note 4: When a RESX input is entered into the ILI9338B while it is in deep standby mode, the ILI9338B starts up the inside logic regulator and makes a transition to the initial state. During this period, the state of the interface pins may become unstable.

15.2. Output Pins, I/O Pins

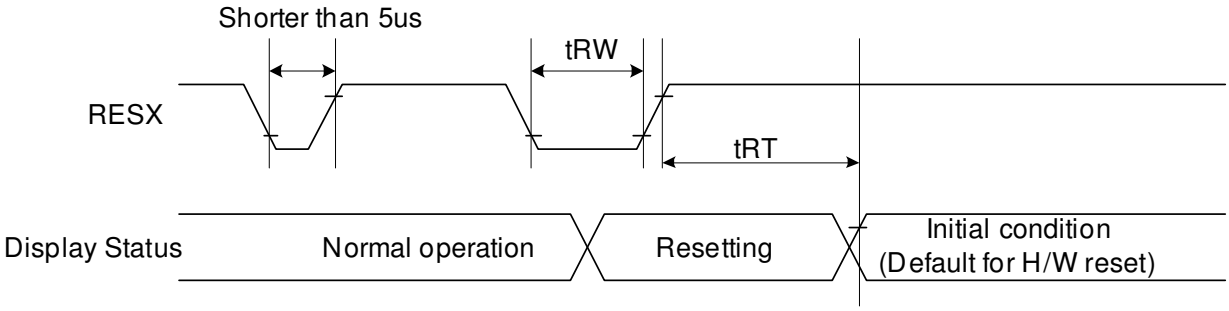
	After Power ON	After Hardware Reset	After Software Reset
TE line	Low	Low	Low
D[17:0] (output driver)	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)

Note 1: There will be no output from D [17:0] during Power ON/OFF sequence, hardware reset and software reset.

15.3. Input Pins

	During Power ON Process	After Power ON	After Hardware Reset	After Software Reset	During Power OFF Process
RESX	See Chapter 12	Input valid	Input valid	Input valid	See Chapter 12
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D[17:0] (input driver)	Input invalid	Input valid	Input valid	Input valid	Input invalid

15.4. Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

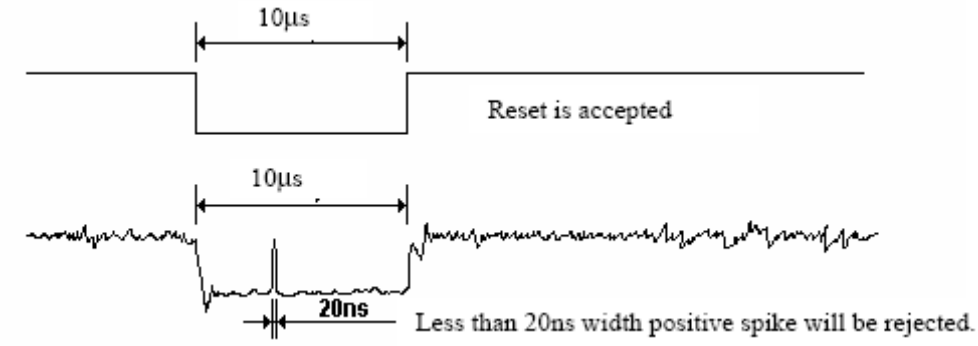
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 9us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:

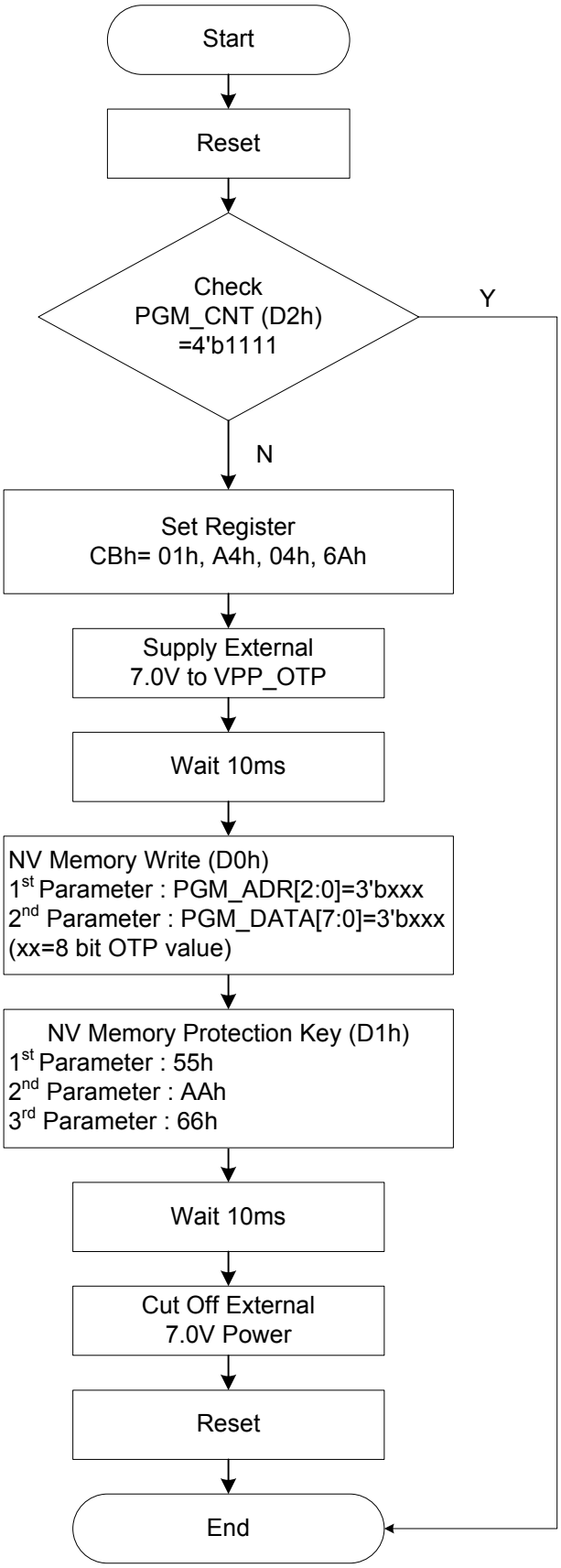


Note 5: When Reset applied during Sleep In Mode.

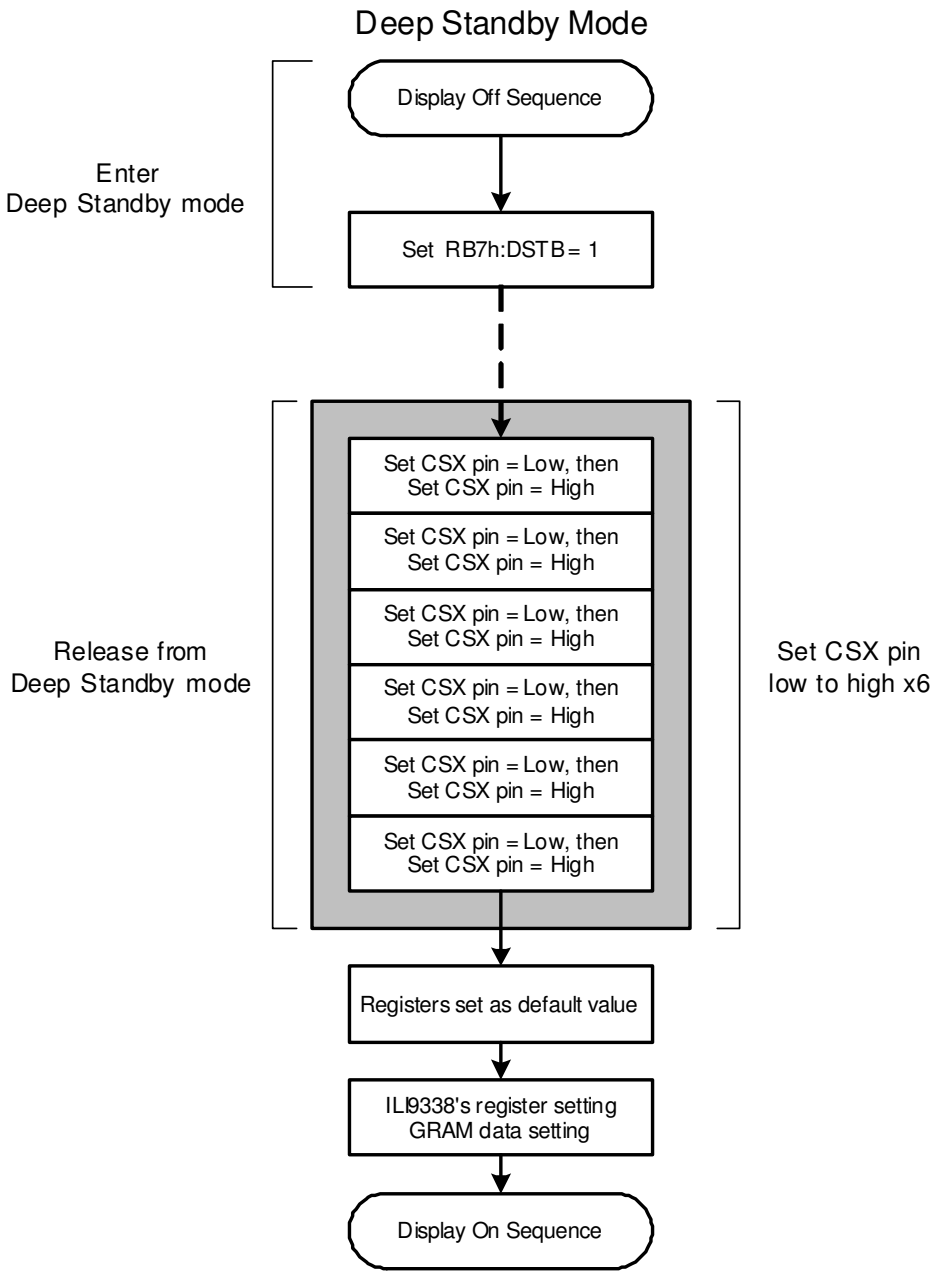
Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

16. NV Memory Programming Flow



17. Deep Standby Mode Setting



Note: (1) To Return display mode according to normal display ON sequence when ILI9338B exits Deep standby mode to Sleep mode.

(2) Leave at lease 1ms between the 2nd and 3rd inputs of CSX=Low.

(3) This sequence must be completed before writing data to GRAM.

(4) ILI9338B exits deep standby mode and enters to sleep mode when an effective RESX pulse is inputted during Deep Standby mode.

18. Electrical Characteristics

18.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9338B is used out of the absolute maximum ratings, ILI9338B may be permanently damaged. To use ILI9338B within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, ILI9338B will malfunction and cause poor reliability.

Item	Symbol	Unit	Value
Supply voltage	VDD	V	-0.3 ~ +4.6
Supply voltage (Logic)	VDDI	V	-0.3 ~ +4.6
Supply voltage (Digital)	VCORE	V	-0.3 ~ +2.4
Driver supply voltage	VGH-VGL	V	-0.3 ~ +32.0
Logic input voltage range	VIN	V	-0.3 ~ VDDI + 0.3
Logic output voltage range	VO	V	-0.3 ~ VDDI + 0.3
Operating temperature	Topr	℃	-40 ~ +80
Storage temperature	Tstg	℃	-55 ~ +110
Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.			

18.2. DC Characteristics

18.2.1. General DC Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VDD	V	Operating voltage	2.5	2.8	3.3	Note2
Logic Operating Voltage	VDDI	V	I/O supply voltage	1.65	2.8	3.3	Note2
Digital Operating voltage	VCORE	V	Digital supply voltage	-	1.8	-	Note2
Gate Driver High Voltage	VGH	V	-	10.0	-	16.0	Note3
Gate Driver Low Voltage	VGL	V	-	-16.0	-	-9.0	Note3
Driver Supply Voltage	-	V	|VGH-VGL|	19	-	32	Note3
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.8VDDI	-	VDDI	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	DGND	-	0.2VDDI	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8VDDI	-	VDDI	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	DGND	-	0.2VDDI	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=VDDI or DGND	-0.1	-	+0.1	Note1,2,3
VCOM Operation							
VCOM High Voltage	VCOMH	V	Ccom=12nF	2.5	-	5.0	Note3
VCOM Low Voltage	VCOML	V	Ccom=12nF	-2.5	-	0.0	Note3
VCOM Amplitude Voltage	VCOMA	V	|VCOMH-VCOML|	4.0	-	5.5	Note3
Source Driver							
Source Output Range	Vsout	V	-	0.1	-	DDVDH-0.1	Note4
Gamma Reference Voltage	VREG1OUT	V	-	3.0	-	5.0	Note3

Note 1: VDDI=1.65 to 3.3V, VDD=2.5 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 (to +80 no damage) ℃.

Note2: Please supply digital VDDI voltage equal or less than analog VDD voltage.

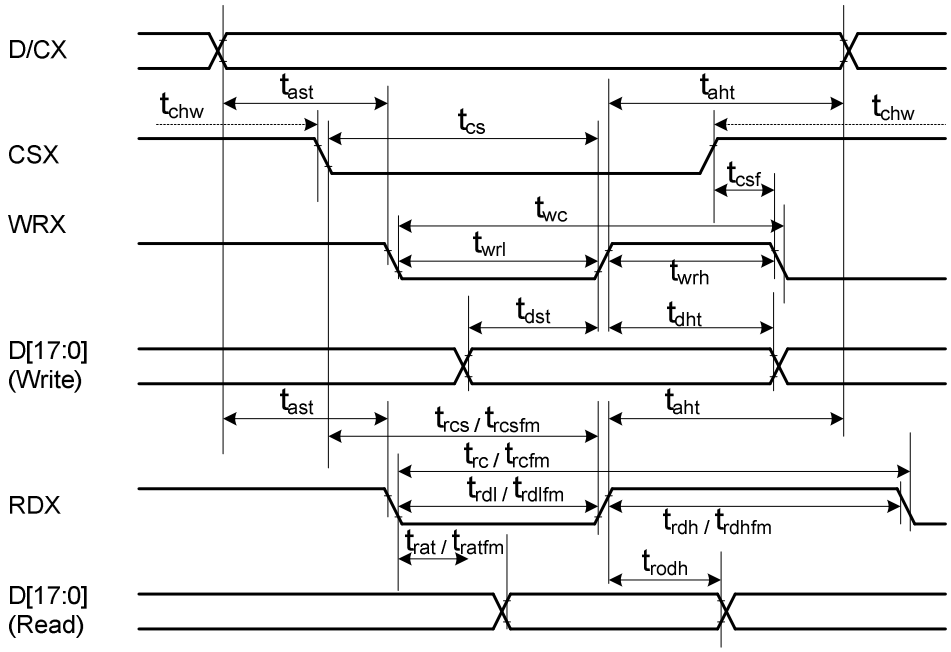
Note3: CSX, RDX, WRX, D[17:0], D/CX, RESX, TE, DOTCLK, VSYNC, HSYNC, DE, SDA, SCL, RCM1, RCM0, IM3, IM2, IM1, IM0, SRGB, REV, SMX, SMY, and Test pins.

Note4: When the measurements are performed with LCD module. Measurement Points are like Note3.

Note5: Source channel loading = 10pF/channel, Gate channel loading = 50pF/channel

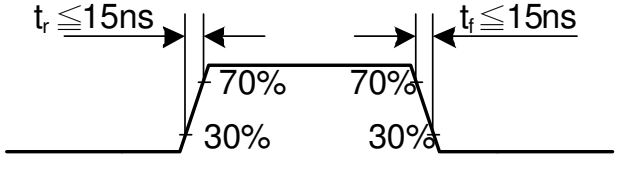
18.3. AC Characteristics

18.3.1. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-system)

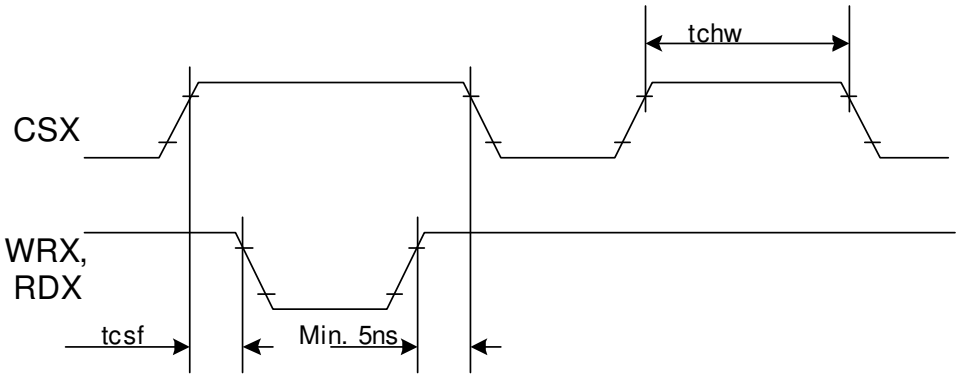


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	33	-	ns	
	twrl	Write Control pulse L duration	33	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45			
D[17:0], D[15:0], D[8:0], D[7:0]	tdst	Write data setup time	20			
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	60	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read Control pulse L duration	45	-	ns	
		Write data setup time	20	-	ns	For maximum CL=30pF For minimum CL=8pF

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VDD=2.5V to 3.3V, DGND=0V

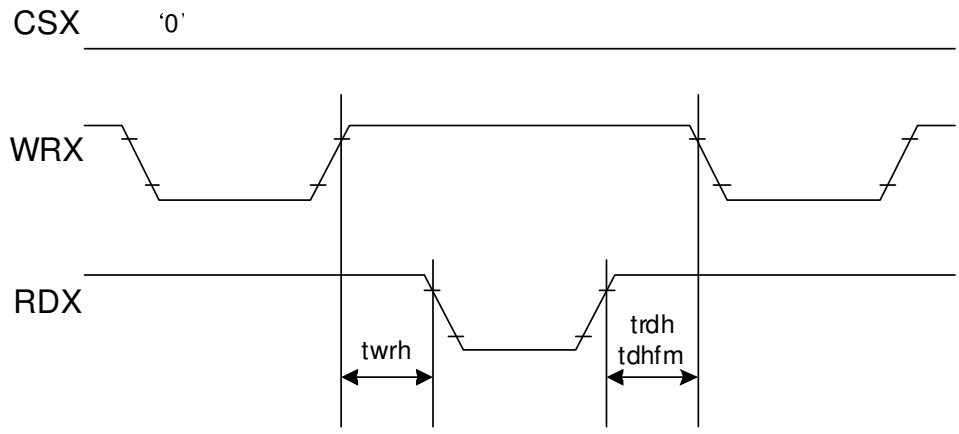


CSX timings :



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:

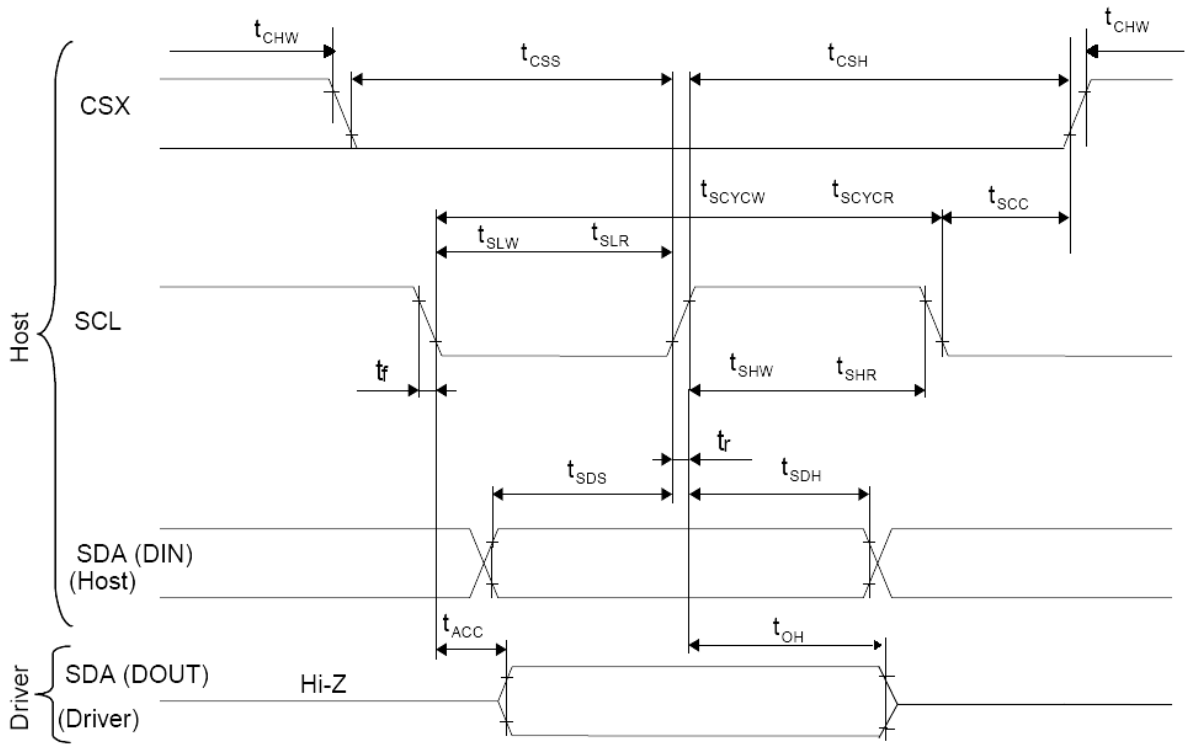


Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

18.3.2.

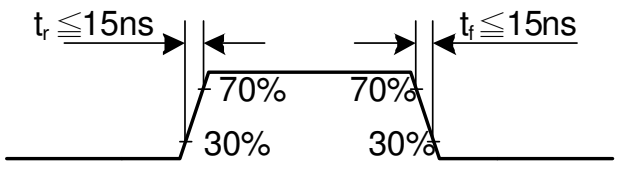
18.3.3.

18.3.4. Display Serial Interface Timing Characteristics (3-line SPI system)

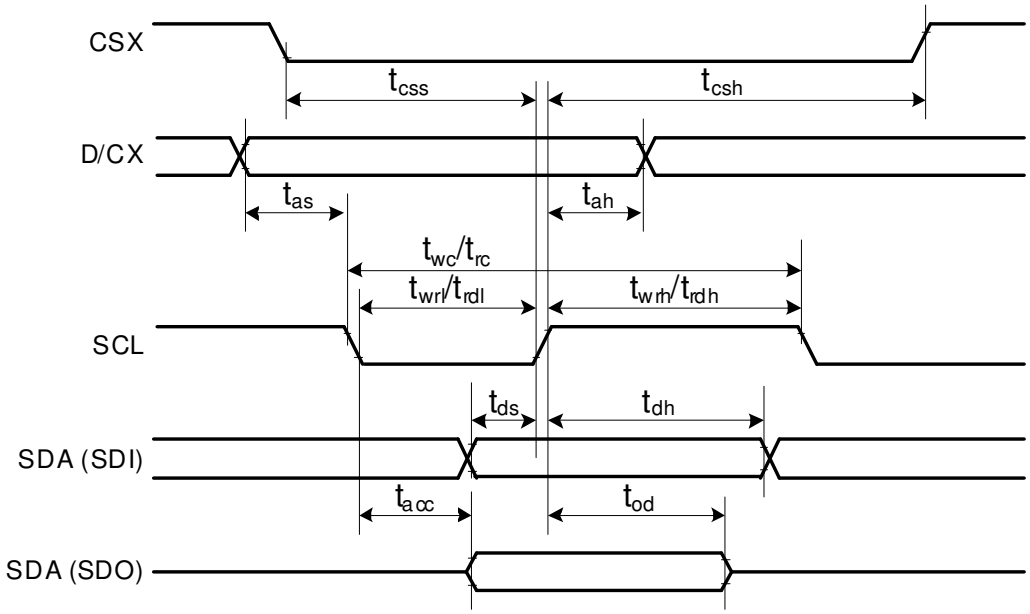


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	80	-	ns	
	tshw	SCL “H” Pulse Width (Write)	40	-	ns	
	tslw	SCL “L” Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL “H” Pulse Width (Read)	75	-	ns	
	tslr	SCL “L” Pulse Width (Read)	75	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	10	-	ns	
	tsdh	Data hold time (Write)	10	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	60	ns	
	toh	Output disable time (Read)	15	-	ns	
CSX	tscc	SCL-CSX	30	-	ns	
	tchw	CSX “H” Pulse Width	60	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VDD=2.5V to 3.3V, AGND=DGND=0V

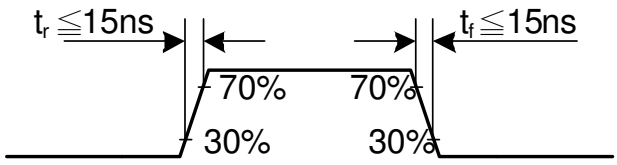


18.3.5. Display Serial Interface Timing Characteristics (4-line SPI system)

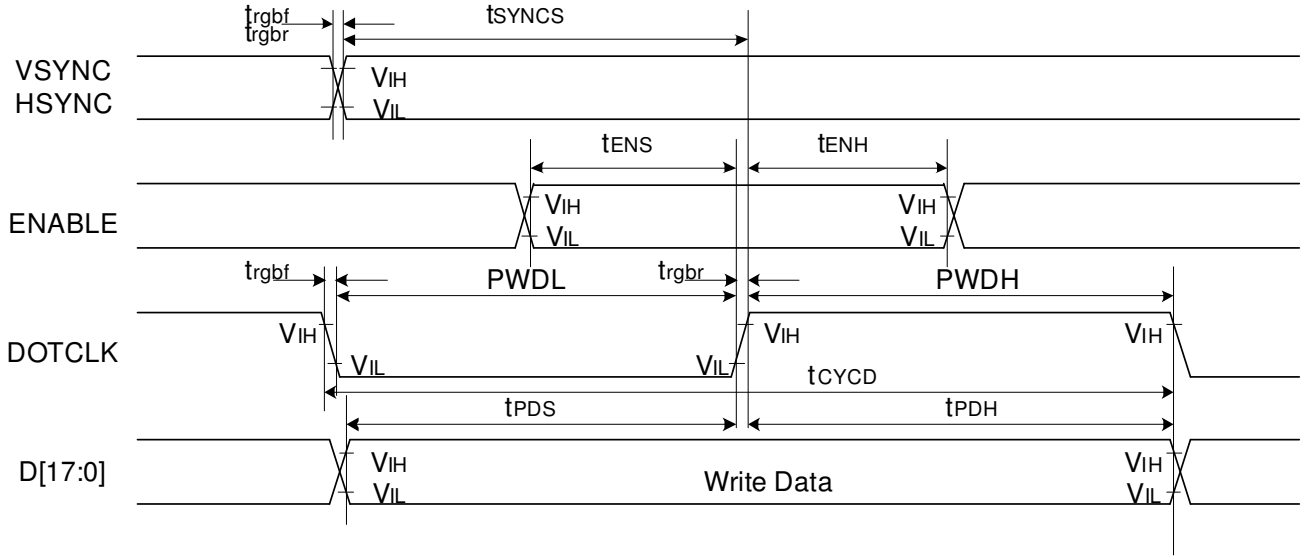


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	30	-	ns	
	tcsh	Chip select hold time (Read)	30	-	ns	
SCL	twc	Serial clock cycle (Write)	80	-	ns	
	twrh	SCL “H” pulse width (Write)	40	-	ns	
	twrl	SCL “L” pulse width (Write)	40	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL “H” pulse width (Read)	75	-	ns	
	trdl	SCL “L” pulse width (Read)	75	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write / Read)	10	-	ns	
SDA / SDI (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	60	ns	For maximum CL=30pF
	tod	Output disable time (Read)	15		ns	For minimum CL=8pF

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VDD=2.5V to 3.3V, AGND=DGND=0V

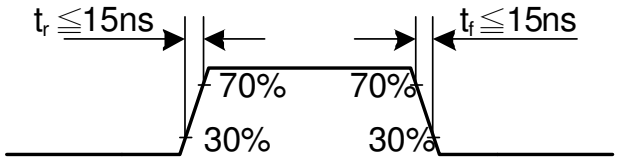


18.3.6. Parallel 18/16-bit RGB Interface Timing Characteristics

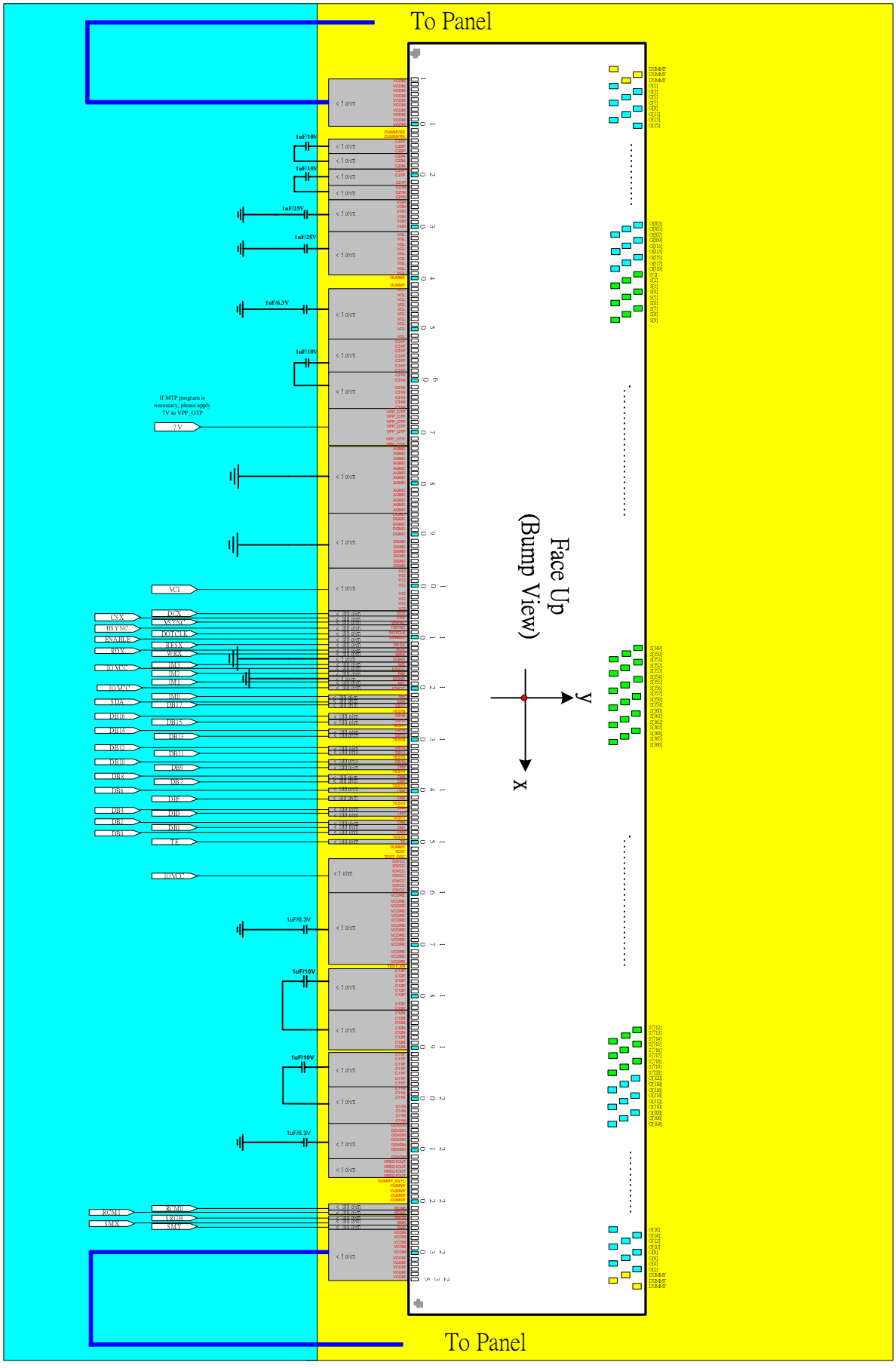


Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	50	-	ns	
	PWDL	DOTCLK low-level period	50	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VDD=2.5V to 3.3V, AGND=DGND=0V



19. Configuration of Power Supply Circuit



The Following tables shows specifications of external elements connected to the ILI9338B's power supply circuit.

Items	Recommended Specification	Pin connection
Capacity 1 F (B characteristics)	6.3V	VCORE,VCL,C11 A/B, C13A/B
	10V	DDVDD, C21 A/B,C22 A/B
	25V	VGH, VGL

20. Revision History

Version No.	Date	Page	Description
V0.01	2009/04/27	All	New Created
V0.02	2009/07/08	All	V0.01modify default register
V0.03	2009/08/10	-	Modify the IM pin interface definition
V0.04	2009/12/21	p184	Add Configuration of Power Supply Circuit
V0.05	2010/1/12	p150	Correct E0h/E1h VP63/VP0/VN63/VN0 5-bit to 4-bit
		P11 P184	Remove VREG1OUT cap
V0.06	2010/3/24	179~183	Timing adjustment
		131	B6h description