Document Number: MMA6231Q
Rev 2, 10/2006

±10g Dual Axis Micromachined Accelerometer

MMA6231Q
MMA6233Q

The MMA6200 series of low cost capacitive micromachined accelerometers feature signal conditioning, a 1-pole low pass filter and temperature compensation. Zero-g offset full scale span and filter cut-off are factory set and require no external devices. A full system self-test capability verifies system functionality.

MMA6230Q Series: X-Y AXIS SENSITIVITY MICROMACHINED ACCELEROMETER ±10 g

Features

- Low Noise
- Low Cost
- Low Power
- 2.7 V to 3.6 V Operation
- 6mm x 6mm x 1.98 mm QFN
- Integral Signal Conditioning with Low Pass Filter
- Linear Output
- Ratiometric Performance
- Self-Test
- Robust Design, High Shocks Survivability

Typical Applications

- Pedometer
- Appliance Control
- Impact Monitoring
- Vibration Monitoring and Recording
- Position & Motion Sensing
- Freefall Detection
- Smart Portable Electronics

Bottom View

16-LEAD QFN CASE 1477-02

Top View

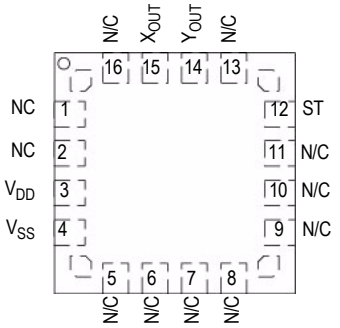

Figure 1. Pin Connections

ORDERING INFORMATION				
Device Name	**Bandwidth Response**	**I_{DD}**	**Case No.**	**Package**
MMA6231Q	300 Hz	1.2 mA	1477-02	QFN-16, Tube
MMA6231QR2	300 Hz	1.2 mA	1477-02	QFN-16,Tape & Reel
MMA6233Q	900 Hz	2.2 mA	1477-02	QFN-16, Tube
MMA6233QR2	900 Hz	2.2 mA	1477-02	QFN-16,Tape & Reel

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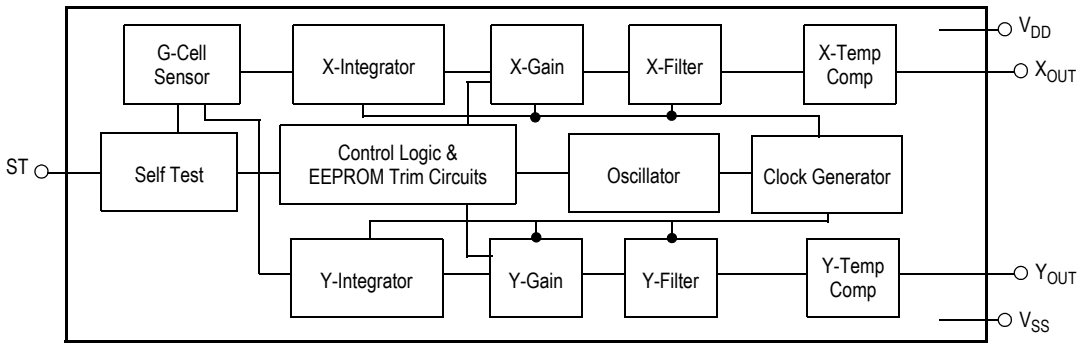


Figure 2. Simplified Accelerometer Functional Block Diagram

Table 1. Maximum Ratings

(Maximum ratings are the limits to which the device can be exposed without causing permanent damage.)

Rating	Symbol	Value	Unit
Maximum Acceleration (all axis)	g_{max}	±2000	g
Supply Voltage	V_{DD}	–0.3 to +3.6	V
Drop Test(1)	D_{drop}	1.2	m
Storage Temperature Range	T_{stg}	–40 to +125	°C

1. Dropped onto concrete surface from any axis.

ELECTRO STATIC DISCHARGE (ESD)

WARNING: This device is sensitive to electrostatic discharge.

Although the Freescale accelerometers contain internal 2 kV ESD protection circuitry, extra precaution must be taken by the user to protect the chip from ESD. A charge of over 2000 volts can accumulate on the human body or associated test equipment. A charge of this magnitude can alter the performance or cause failure of the chip. When handling the accelerometer, proper ESD precautions should be followed to avoid exposing the device to discharges which may be detrimental to its performance.

Table 2. Operating Characteristics

Unless otherwise noted: -20°C ≤ T_A ≤ 85°C, 3.0 V ≤ V_{DD} ≤ 3.6 V, Acceleration = 0g, Loaded output (1)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Range(2)					
Supply Voltage(3)	V_{DD}	2.7	3.3	3.6	V
Supply Current					
MMA6231Q	I_{DD}	—	1.2	1.5	mA
MMA6233Q	I_{DD}	—	2.2	3.0	mA
Operating Temperature Range	T_A	–20	—	+85	°C
Acceleration Range	g_{FS}	—	10	—	g
Output Signal					
Zero g (T_A = 25°C, V_{DD} = 3.3 V)(4)	V_{OFF}	1.485	1.65	1.815	V
Zero g	V_{OFF}, T_A	—	2.0	—	mg/°C
Sensitivity (T_A = 25°C, V_{DD} = 3.3 V)	S	111	120	129	mV/g
Sensitivity	S, T_A	—	0.015	—	%/°C
Bandwidth Response					
MMA6231Q	f_{-3dB}	—	300	—	Hz
MMA6233Q	f_{-3dB}	—	900	—	Hz
Nonlinearity	NL_{OUT}	–1.0	—	+1.0	% FSO
Noise					
MMA6231Q RMS (0.1 Hz – 1 kHz)	n_{RMS}	—	0.7	—	mVrms
MMA6233Q RMS (0.1 Hz – 1 kHz)	n_{RMS}	—	0.6	—	
Power Spectral Density RMS (0.1 Hz – 1 kHz)					
MMA6231Q	n_{PSD}	—	50	—	ug/$\sqrt{Hz}$
MMA6233Q	n_{PSD}	—	30	—	
Self-Test					
Output Response	g_{ST}	2.0	—	—	g
Input Low	V_{IL}	—	—	0.3 V_{DD}	V
Input High	V_{IH}	0.7 V_{DD}	—	V_{DD}	V
Pull-Down Resistance(5)	R_{PO}	43	57	71	kΩ
Response Time(6)	t_{ST}	—	2.0	—	ms
Output Stage Performance					
Full-Scale Output Range (I_{OUT} = 200 µA)	V_{FSO}	V_{SS} +0.25	—	V_{DD} –0.25	V
Capacitive Load Drive(7)	C_L	—	—	100	pF
Output Impedance	Z_O	—	50	300	Ω
Power-Up Response Time					
MMA6231Q	$t_{RESPONSE}$	—	2.0	—	ms
MMA6233Q	$t_{RESPONSE}$	—	0.7	—	ms
Mechanical Characteristics					
Transverse Sensitivity(8)	$V_{ZX, YX, ZY}$	–5.0	—	+5.0	% FSO

1. For a loaded output, the measurements are observed after an RC filter consisting of a 1.0 kΩ resistor and a 0.1 µF capacitor to ground.
2. These limits define the range of operation for which the part will meet specification.
3. Within the supply range of 2.7 and 3.6 V, the device operates as a fully calibrated linear accelerometer. Beyond these supply limits the device may operate as a linear device but is not guaranteed to be in calibration.
4. The device can measure both + and – acceleration. With no input acceleration the output is at midsupply. For positive acceleration the output will increase above V_{DD}/2. For negative acceleration, the output will decrease below V_{DD}/2.
5. The digital input pin has an internal pull-down resistance to prevent inadvertent self-test initiation due to external board level leakages.
6. Time for the output to reach 90% of its final value after a self-test is initiated.
7. Preserves phase margin (60°) to guarantee output amplifier stability.
8. A measure of the device's ability to reject an acceleration applied 90° from the true axis of sensitivity.

PRINCIPLE OF OPERATION

The Freescale accelerometer is a surface-micromachined integrated-circuit accelerometer.

The device consists of a surface micromachined capacitive sensing cell (g-cell) and a signal conditioning ASIC contained in a single integrated circuit package. The sensing element is sealed hermetically at the wafer level using a bulk micromachined *cap* wafer.

The g-cell is a mechanical structure formed from semiconductor materials (polysilicon) using semiconductor processes (masking and etching). It can be modeled as a set of beams attached to a movable central mass that moves between fixed beams. The movable beams can be deflected from their rest position by subjecting the system to an acceleration (Figure 3).

As the beams attached to the central mass move, the distance from them to the fixed beams on one side will increase by the same amount that the distance to the fixed beams on the other side decreases. The change in distance is a measure of acceleration.

The g-cell plates form two back-to-back capacitors (Figure 4). As the center plate moves with acceleration, the distance between the plates changes and each capacitor's value will change, ($C = A\varepsilon/D$). Where A is the area of the plate, ε is the dielectric constant, and D is the distance between the plates.

The ASIC uses switched capacitor techniques to measure the g-cell capacitors and extract the acceleration data from the difference between the two capacitors. The ASIC also signal conditions and filters (switched capacitor) the signal, providing a high level output voltage that is ratiometric and proportional to acceleration.

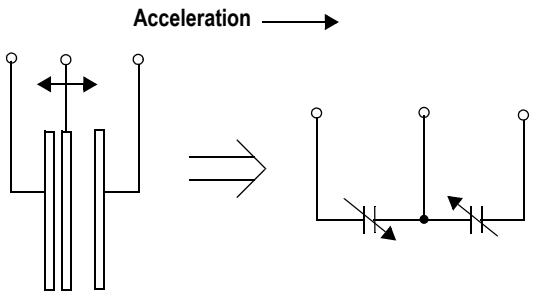


Figure 3. Transducer Physical Model

Figure 4. Equivalent Circuit Model

SPECIAL FEATURES

Filtering

These Freescale accelerometers contain an onboard single-pole switched capacitor filter. Because the filter is realized using switched capacitor techniques, there is no requirement for external passive components (resistors and capacitors) to set the cut-off frequency.

Self-Test

The sensor provides a self-test feature allowing the verification of the mechanical and electrical integrity of the accelerometer at any time before or after installation. A fourth *plate* is used in the g-cell as a self-test plate. When a logic high input to the self-test pin is applied, a calibrated potential is applied across the self-test plate and the moveable plate. The resulting electrostatic force ($Fe = {}^1/_2\ AV^2/d^2$) causes the center plate to deflect. The resultant deflection is measured by the accelerometer's ASIC and a proportional output voltage results. This procedure assures both the mechanical (g-cell) and electronic sections of the accelerometer are functioning.

Freescale accelerometers include fault detection circuitry and a fault latch. Parity of the EEPROM bits becomes odd in number.

Self-test is disabled when EEPROM parity error occurs.

Ratiometricity

Ratiometricity simply means the output offset voltage and sensitivity will scale linearly with applied supply voltage. That is, as supply voltage is increased, the sensitivity and offset increase linearly; as supply voltage decreases, offset and sensitivity decrease linearly. This is a key feature when interfacing to a microcontroller or an A/D converter because it provides system level cancellation of supply induced errors in the analog to digital conversion process.

BASIC CONNECTIONS

Pinout Description

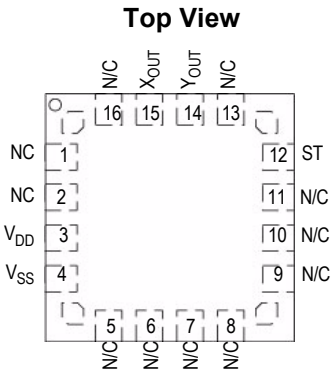


Figure 4. Pinout Description

Pin No.	Pin Name	Description
1, 5–7, 13, 16	N/C	No internal connection. Leave unconnected.
14	Y_{OUT}	Output voltage of the accelerometer. Y Direction.
15	X_{OUT}	Output voltage of the accelerometer. X Direction.
3	V_{DD}	Power supply input.
4	V_{SS}	The power supply ground.
2, 8–11	N/C	Used for factory trim. Leave unconnected.
12	ST	Logic input pin used to initiate self-test.

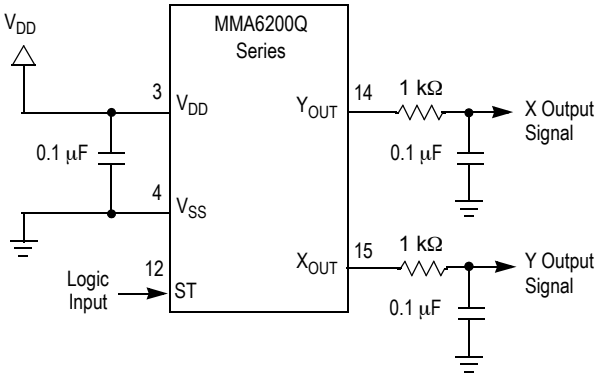


Figure 5. Accelerometer with Recommended Connection Diagram

PCB Layout

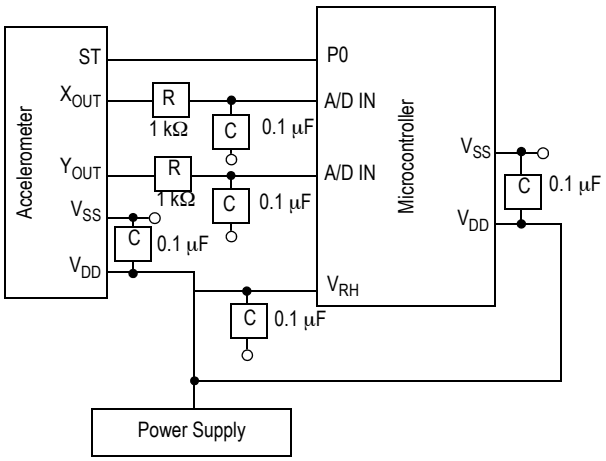


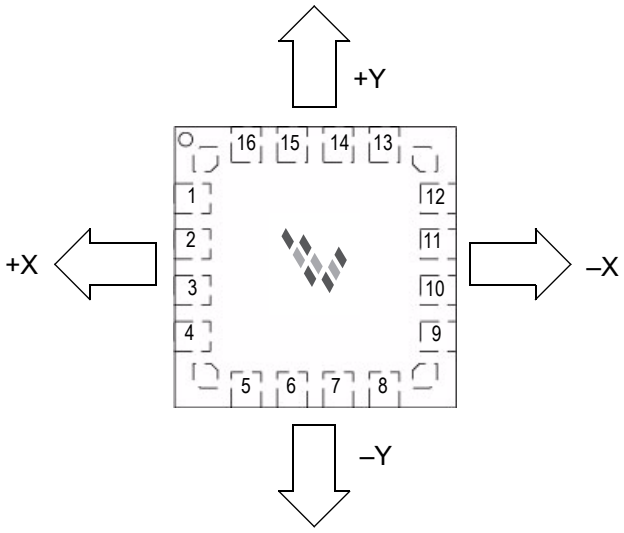
Figure 6. Recommend PCB Layout for Interfacing Accelerometer to Microcontroller

NOTES:

1. Use 0.1 µF capacitor on V_{DD} to decouple the power source.
2. Physical coupling distance of the accelerometer to the microcontroller should be minimal.
3. Flag underneath package is connected to ground.
4. Place a ground plane beneath the accelerometer to reduce noise, the ground plane should be attached to all of the open ended terminals shown in Figure 6.
5. Use an RC filter with 1.0 kΩ and 0.1 µF on the outputs of the accelerometer to minimize clock noise (from the switched capacitor filter circuit).
6. PCB layout of power and ground should not couple power supply noise.
7. Accelerometer and microcontroller should not be a high current path.
8. A/D sampling rate and any external power supply switching frequency should be selected such that they do not interfere with the internal accelerometer sampling frequency (16 kHz for Low I_{DD} and 52 kHz for Standard I_{DD} for the sampling frequency). This will prevent aliasing errors.
9. PCB layout should not run traces or vias under the QFN part. This could lead to ground shorting to the accelerometer flag.

DYNAMIC ACCELERATION

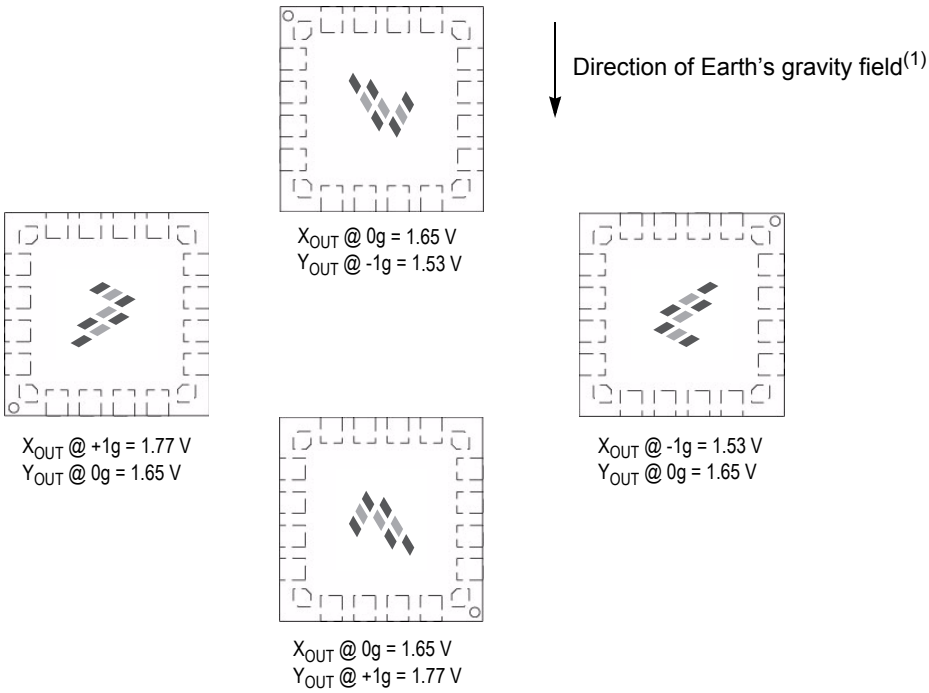
Top View



16-Pin QFN Package

STATIC ACCELERATION

Top View

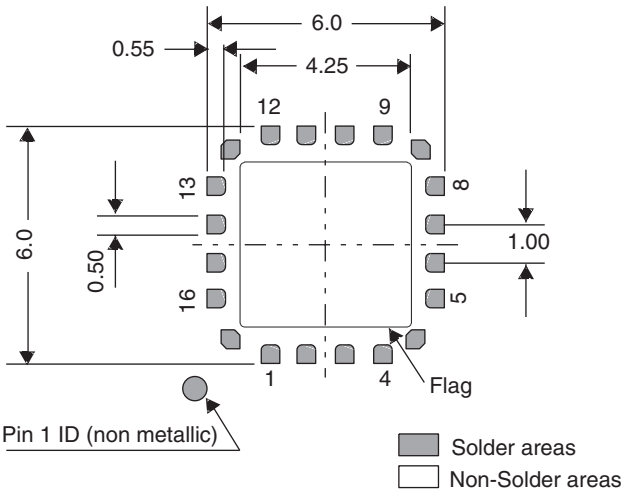


1. When positioned as shown, the Earth's gravity will result in a positive 1g output.

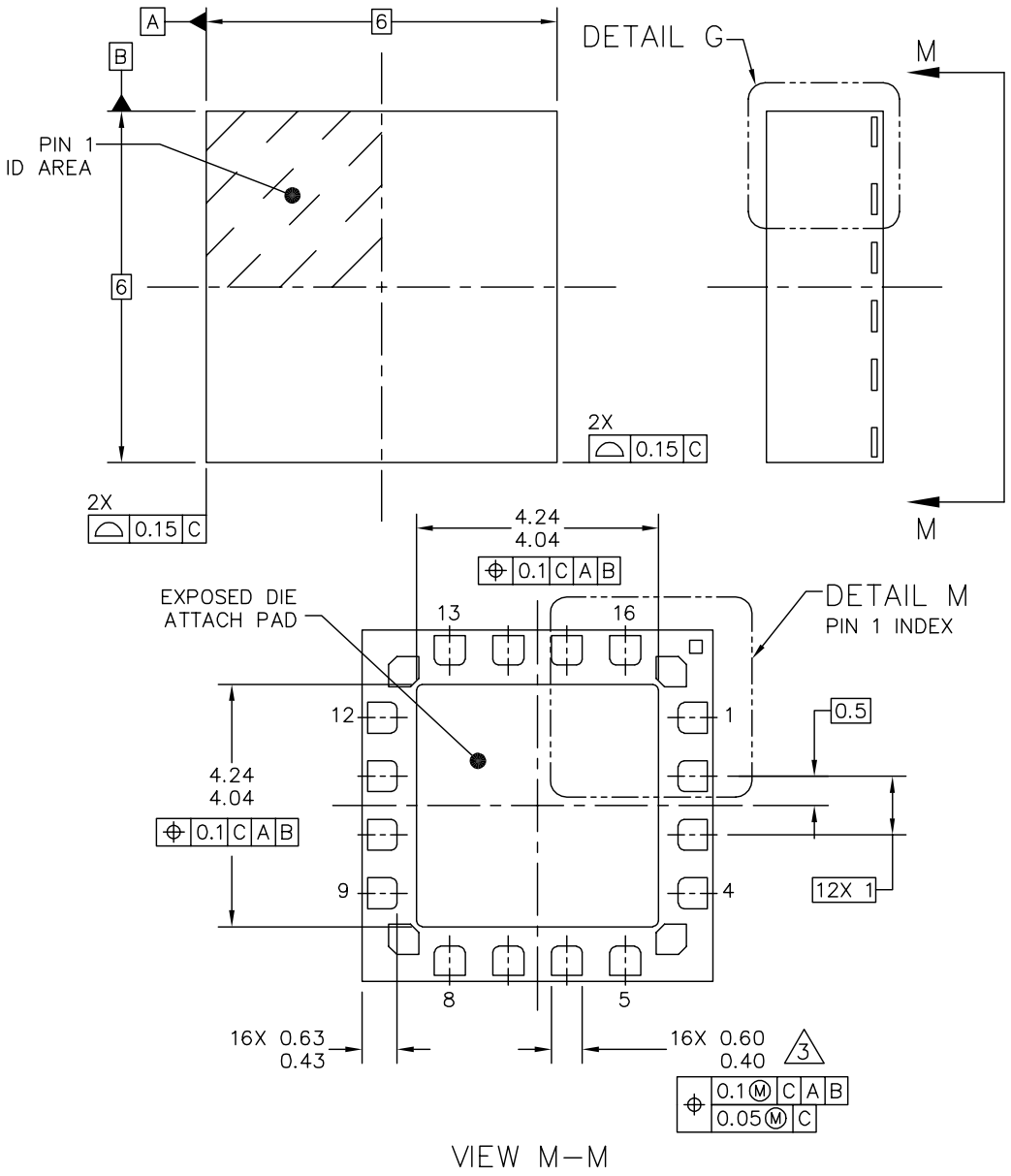
MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the board and the package.

With the correct footprint, the packages will self-align when subjected to a solder reflow process. It is always recommended to design boards with a solder mask layer to avoid bridging and shorting between solder pads.



PACKAGE DIMENSIONS



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CASE 1477-02
ISSUE B
16-LEAD QFN

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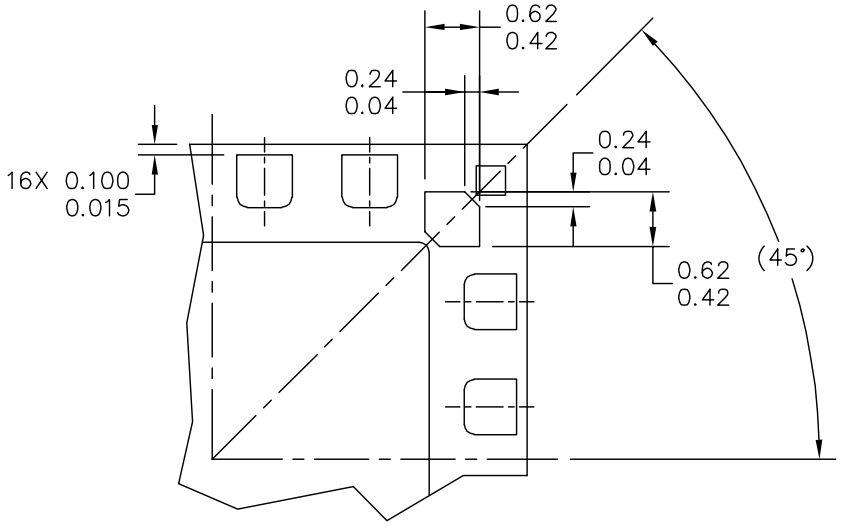

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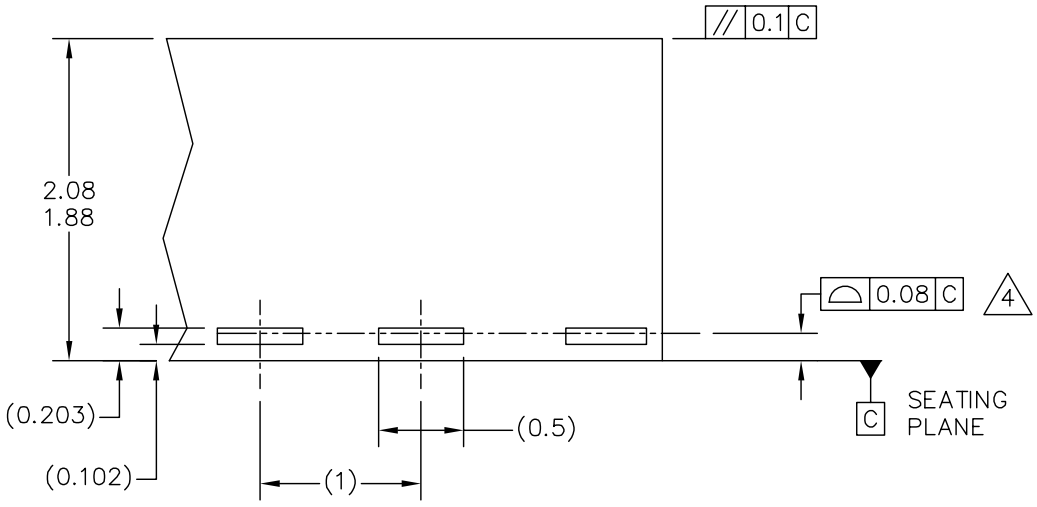

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VIEW ROTATED 90° CW

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PACKAGE DIMENSIONS

NOTES:

1. ALL DIMENSIONS ARE IN MILLMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THIS DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25MM AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG, TERMINALS AND CORNER PADS.
5. RADIUS ON TERMINAL IS OPTIONAL.
6. MINIMUM METAL GAP SHOULD BE 0.2MM EXCEPT GAP BETWEEN CORNER PADS AND THE EXPOSED HEAT SLUG.

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