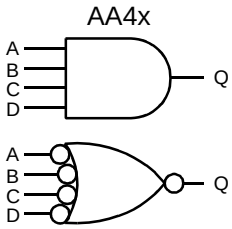
Description

AA4x is a family of 4-input gates which perform the logical AND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

HDL Syntax

Verilog ..... AA4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AA4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AA41	AA42	AA44	AA46
A	1.0	1.0	3.1	3.1
B	1.0	1.0	3.1	3.1
C	1.0	1.0	3.1	3.1
D	1.0	1.0	3.1	3.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQLpd (Eq-load)
AA41	3.0	TBD	4.1
AA42	3.0	TBD	5.2
AA44	8.0	TBD	11.3
AA46	9.0	TBD	15.7

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

AA41	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.45 0.26	0.56 0.37	0.70 0.50	0.86 0.64	0.98 0.75
AA42	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.50 0.28	0.66 0.42	0.78 0.53	0.88 0.64	1.00 0.75
AA44	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.35 0.20	0.49 0.33	0.61 0.43	0.72 0.52	0.81 0.62
AA46	**Number of Equivalent Loads**		**1**	**21**	**42**	**62**	**83 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.43 0.24	0.57 0.37	0.67 0.48	0.77 0.58	0.87 0.69

Delay will vary with input conditions. See page 2-17 for interconnect estimates.