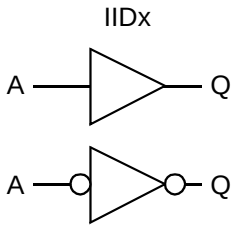
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

IIDx is a family of non-inverting clock drivers with a single output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

HDL Syntax

Verilog ..... IIDx *inst_name* (Q, A);

VHDL..... *inst_name*: IIDx port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads				
	IID1	IID2	IID3	IID4	IID6
A	1.0	1.0	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IID1	1.0	TBD	2.3
IID2	2.0	TBD	3.8
IID3	3.0	TBD	5.5
IID4	3.0	TBD	7.6
IID6	4.0	TBD	11.0

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

IID1	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.21 0.21	0.31 0.32	0.42 0.44	0.56 0.59	0.68 0.72
IID2	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.15 0.23	0.27 0.35	0.38 0.45	0.49 0.56	0.60 0.69
IID3	**Number of Equivalent Loads**		**1**	**11**	**22**	**32**	**43 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.15 0.18	0.28 0.31	0.38 0.41	0.47 0.50	0.57 0.61
IID4	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.20 0.21	0.29 0.34	0.39 0.44	0.48 0.54	0.57 0.65
IID6	**Number of Equivalent Loads**		**1**	**21**	**42**	**62**	**83 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.22 0.25	0.34 0.37	0.44 0.47	0.52 0.58	0.60 0.69

Delay will vary with input conditions. See page 2-17 for interconnect estimates.