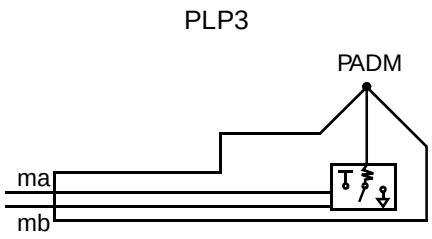
AMERICAN MICROSYSTEMS, INC.

## AMI5HG 0.5 micron CMOS Gate Array

### Description

PLP3 is a programmable pull-up/pull-down buffer piece.

**Logic Symbol**




**Truth Table**

| MA | MB | PADM Function |
|---|---|---|
| L | L | Pull-down |
| H | H | Pull-up |
| H | L | Tristate |
| L | H | Tristate |

**Pin Loading**

| | Load |
|---|---|
| MA | 2.1 eql |
| MB | 1.8 eql |



### HDL Syntax

Verilog ..... PLP3 *inst_name* (PADM, MA, MB);

VHDL..... *inst_name*: PLP3 port map (PADM, MA, MB);

### Power Characteristics

| Parameter | Value | Units |
|---|---|---|
| Static $I_{DD}$ ($T_J$ = 85°C) | TBD | nA |
| $EQL_{pd}$ | 146.8 | Eq-load |

See page 2-15 for power equation.