N- and P-Channel 30V (D-S) MOSFET

GENERAL DESCRIPTION

The ME3500 is the N- and P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq$ 35mΩ@V_{GS}=10V (N-Ch)
- $R_{DS(ON)} \leqq$ 52mΩ@V_{GS}=4.5V (N-Ch)
- $R_{DS(ON)} \leqq$ 70mΩ@V_{GS}=-10V (P-Ch)
- $R_{DS(ON)} \leqq$ 95mΩ@V_{GS}=-4.5V (P-Ch)
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

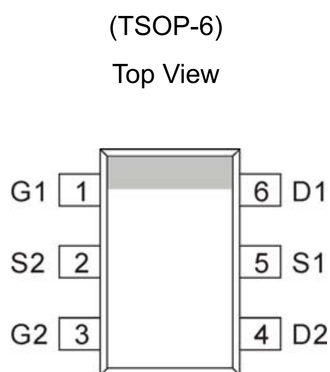
APPLICATIONS

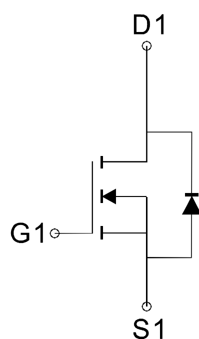
- Power Management in Note book
- Portable Equipment
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION

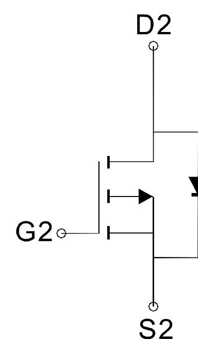
(TSOP-6)

Top View





N-Channel MOSFET



P-Channel MOSFET

Ordering Information: ME3500 (Pb-free)

ME3500-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current*	T_A=25℃	I_D	4.5	-3.3	A
	T_A=70℃		3.6	-2.7	
Pulsed Drain Current		I_{DM}	18	-13	A
Maximum Power Dissipation*	T_A=25℃	P_D	1.1	1.3	W
	T_A=70℃		0.7	0.8	
Operating Junction Temperature		T_J	-55 to 150		℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	110	100	℃/W

*The device mounted on 1in2 FR4 board with 2 oz copper

N- and P-Channel 30V (D-S) MOSFET

Electrical Characteristics (T_A =25℃ Unless Otherwise Specified)

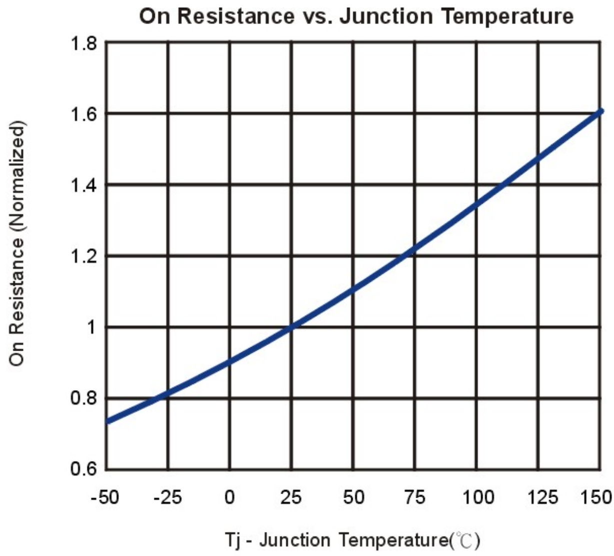
Symbol	Parameter	Limit		Min	Typ	Max	Unit
STATIC							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, I_D=250 μA $V_{DS}=V_{GS}$, I_D=-250 μA	N-Ch P-Ch	1.0 -1.0		3.0 -3.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V	N-Ch P-Ch			±100 ±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V V_{DS}=-30V, V_{GS}=0V	N-Ch P-Ch			1 -1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=10V, I_D= 5A V_{GS}=-10V, I_D= -5A	N-Ch P-Ch		22 55	35 70	mΩ
		V_{GS}=4.5V, I_D= 4A V_{GS}=-4.5V, I_D= -4A	N-Ch P-Ch		33 75	52 95	
V_{SD}	Diode Forward Voltage	I_S=1.7A, V_{GS}=0V I_S=-1.7A, V_{GS}=0V	N-Ch P-Ch		0.8 -0.8	1.2 -1.2	V
DYNAMIC							
Qg	Total Gate Charge	N-Channel V_{DS}=15V, V_{GS}=10V, I_D=5A P-Channel V_{DS}=-15V, V_{GS}=-10V, I_D=-5A	N-Ch P-Ch		12 14	15 17	nC
Qgs	Gate-Source Charge		N-Ch P-Ch		2 4		
Qgd	Gate-Drain Charge		N-Ch P-Ch		2.5 3		
Ciss	Input Capacitance	N-Channel V_{DS}=15V, V_{GS}=0V, f=1MHz P-Channel V_{DS}=-15V, V_{GS}=0V, f=1MHz	N-Ch P-Ch		360 450	420 490	pF
Coss	Output Capacitance		N-Ch P-Ch		70 70		
Crss	Reverse Transfer Capacitance		N-Ch P-Ch		17 20		
Rg	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz	N-Ch P-Ch		0.5 3.5		Ω
td(on)	Turn-On Delay Time	N-Channel V_{DD}=15V, R_L =15Ω I_D=1A, V_{GEN}=10V, R_G=6Ω P-Channel V_{DD}=-15V, R_L =15Ω I_D=-1A, V_{GEN}=-10V,R_G=6Ω	N-Ch P-Ch		9.3 27	13 33	ns
tr	Turn-On Rise Time		N-Ch P-Ch		14 11	18 15	
td(off)	Turn-Off Delay Time		N-Ch P-Ch		32 40	41 52	
tf	Turn-Off Fall Time		N-Ch P-Ch		3.2 4	5 6	

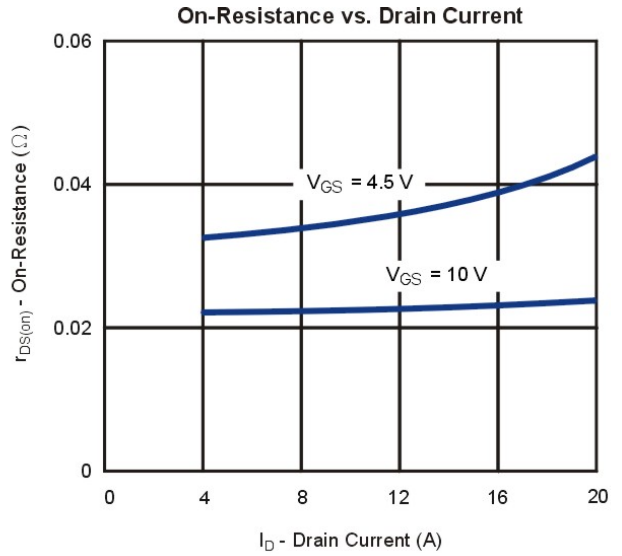
Note: a. Pulse test: pulse width<=300us, duty cycle<=2%

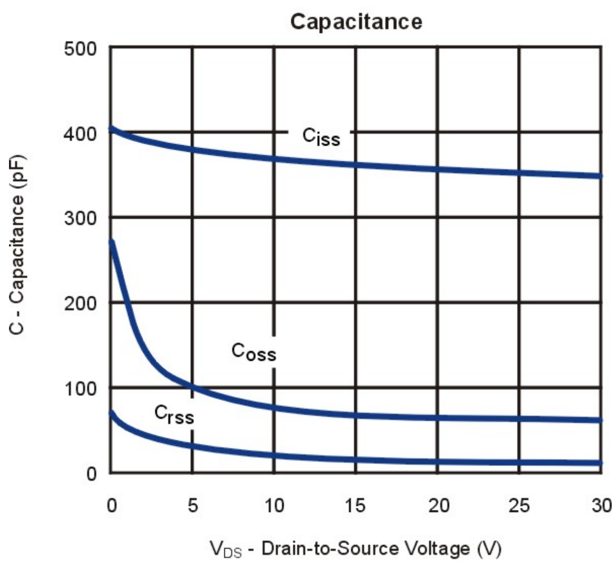
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

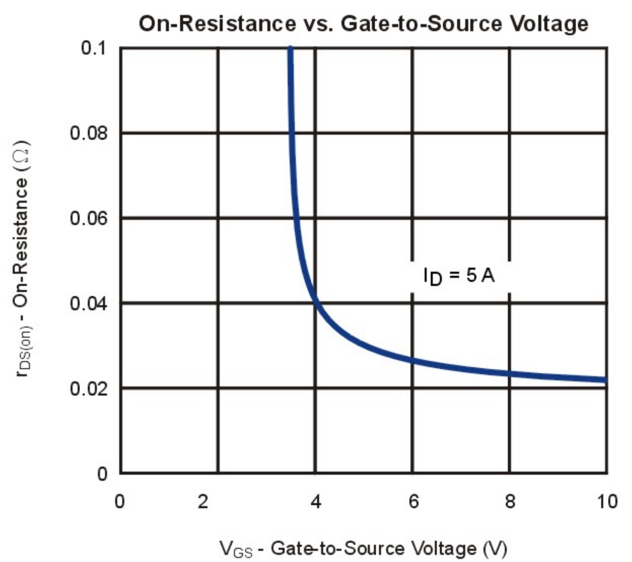
N- and P-Channel 30V (D-S) MOSFET

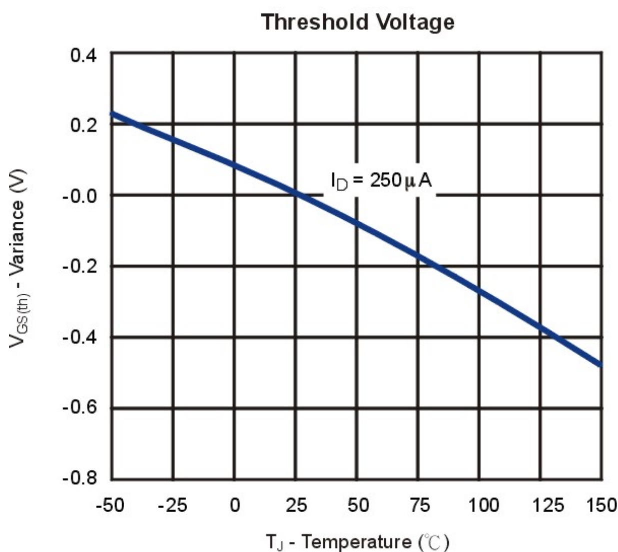
Typical Characteristics (T_J =25℃ Noted) N-CHANNEL

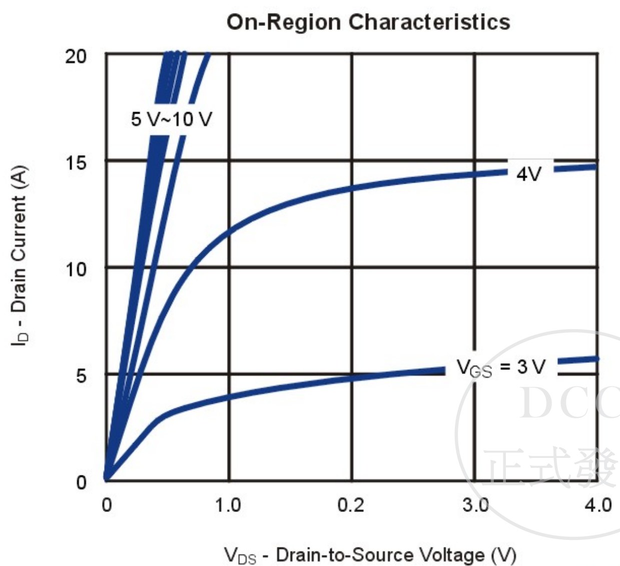






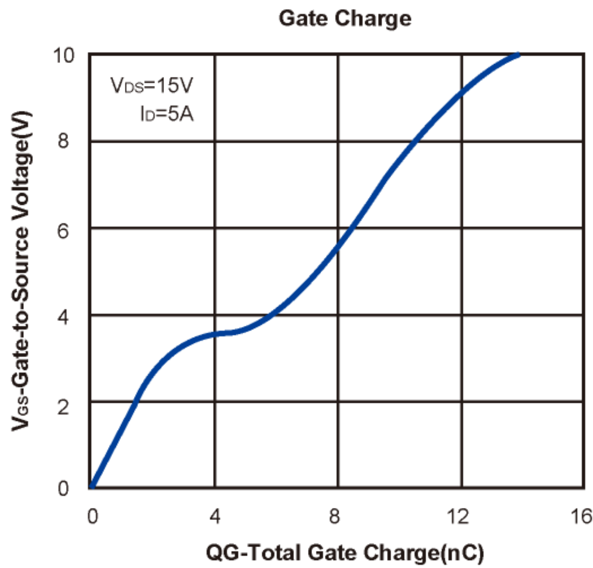


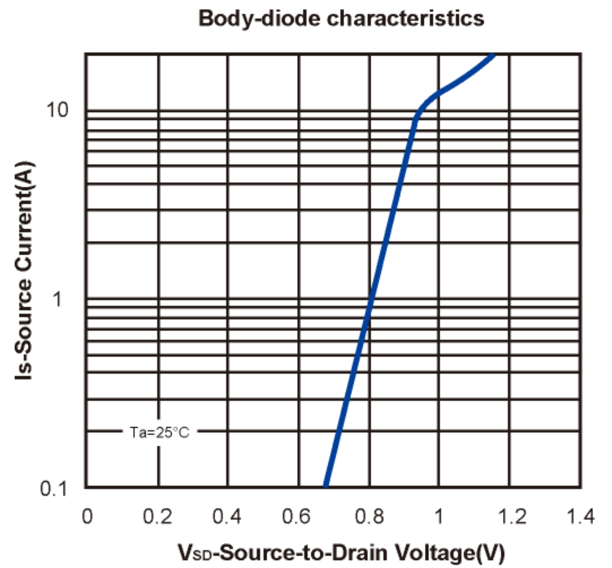


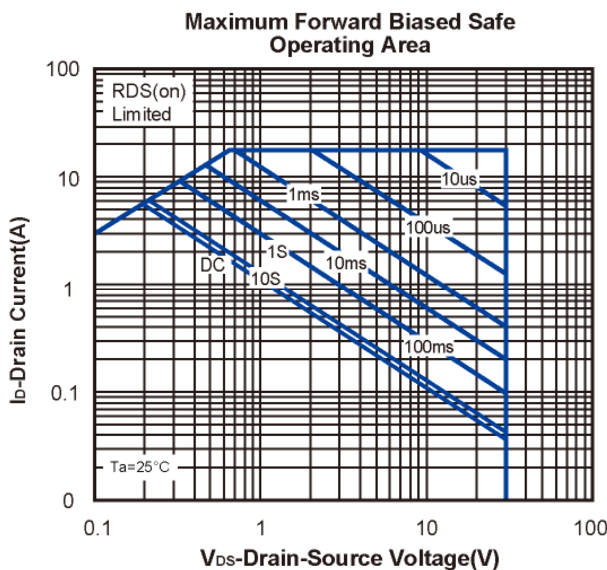


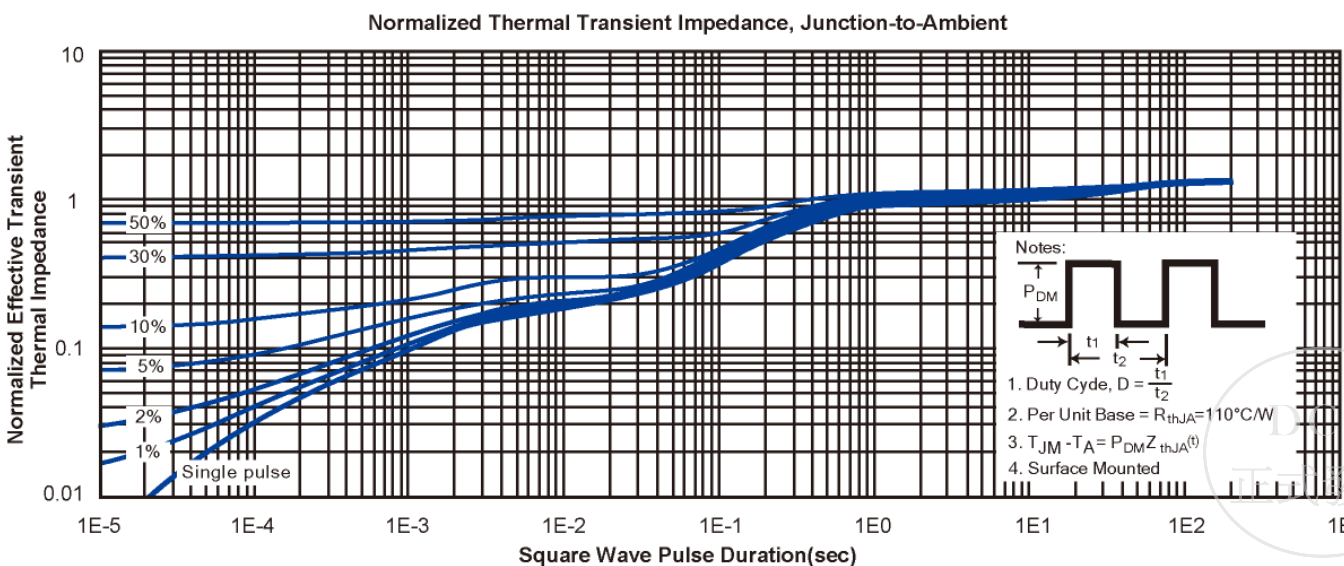
N- and P-Channel 30V (D-S) MOSFET

Typical Characteristics (TJ =25℃ Noted) N-CHANNEL



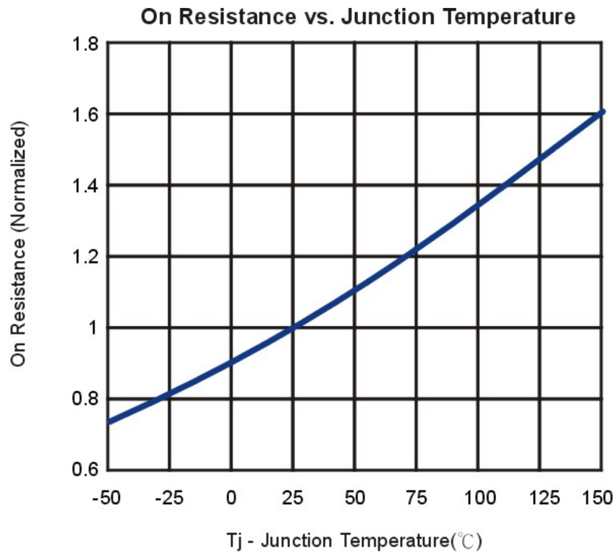


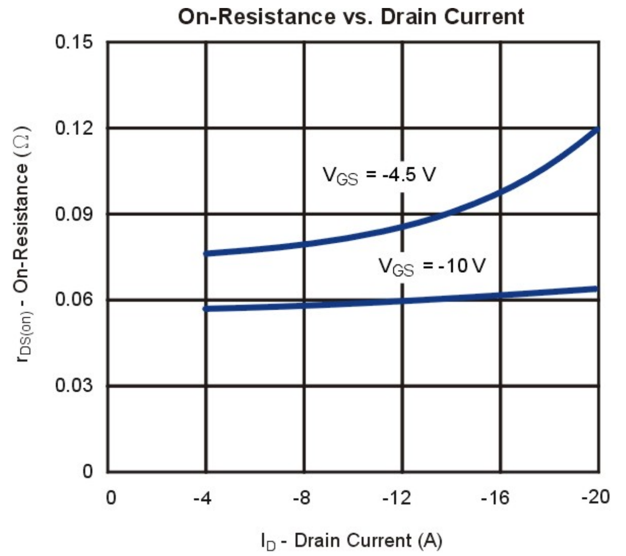


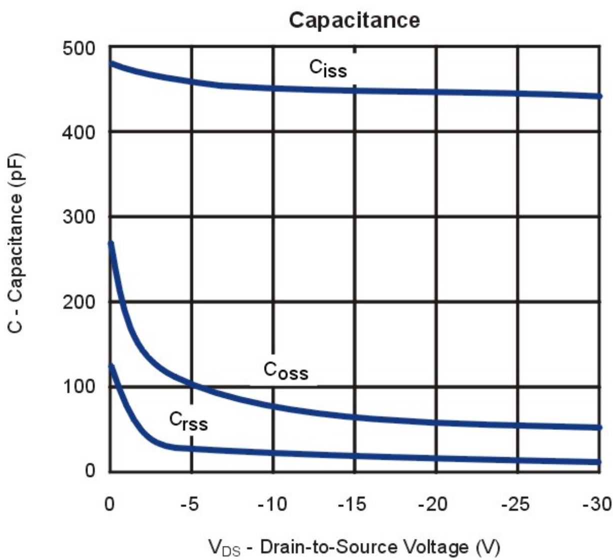


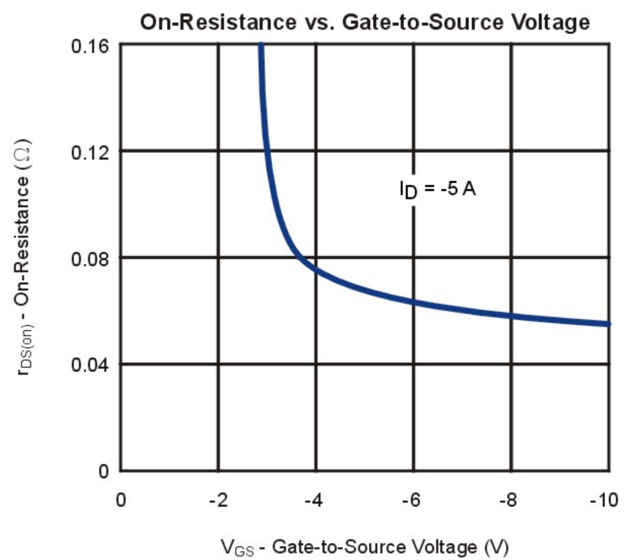
N- and P-Channel 30V (D-S) MOSFET

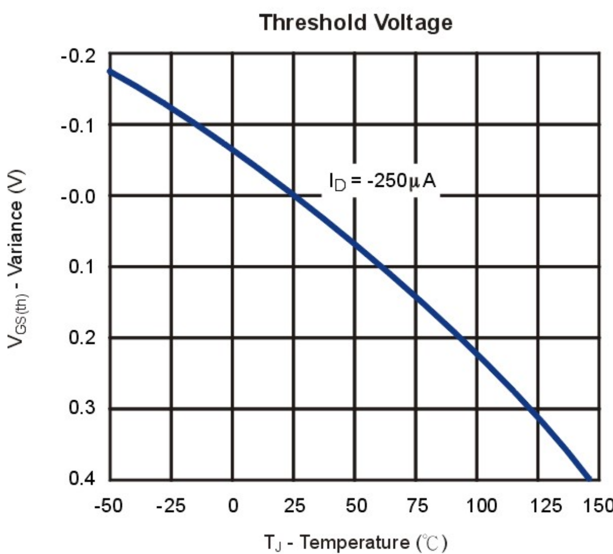
Typical Characteristics (T_J =25℃ Noted) P-CHANNEL

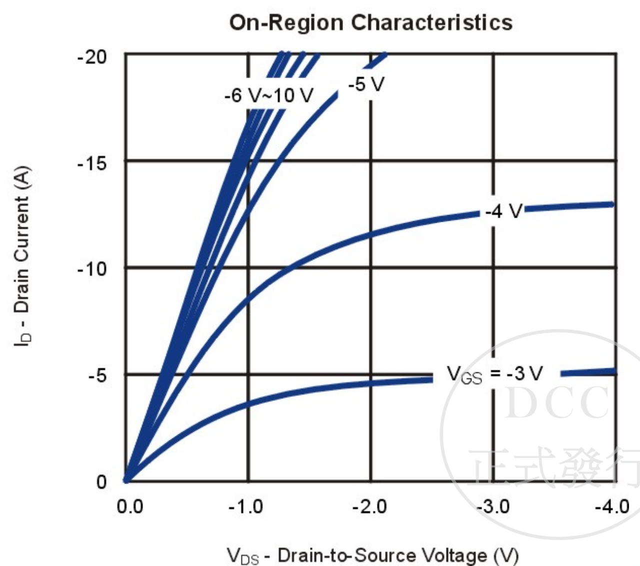






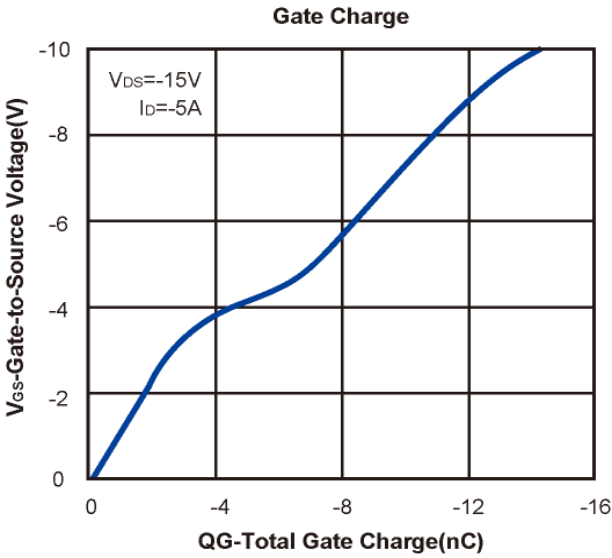


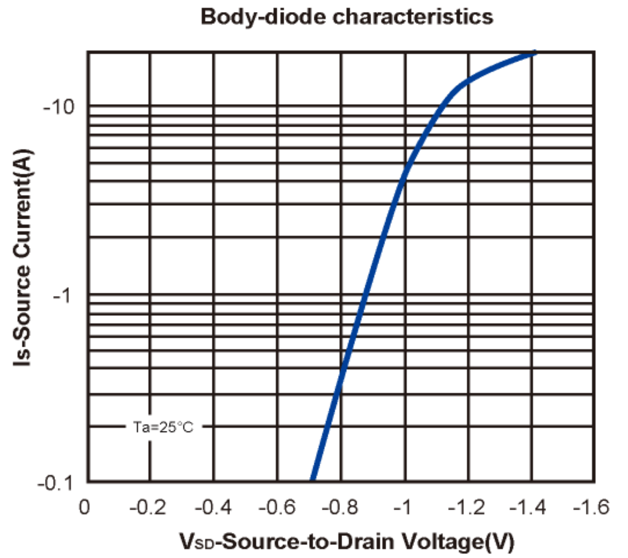


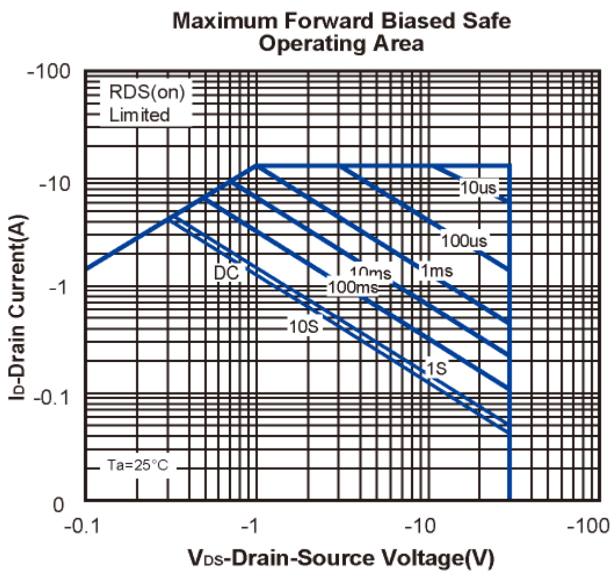


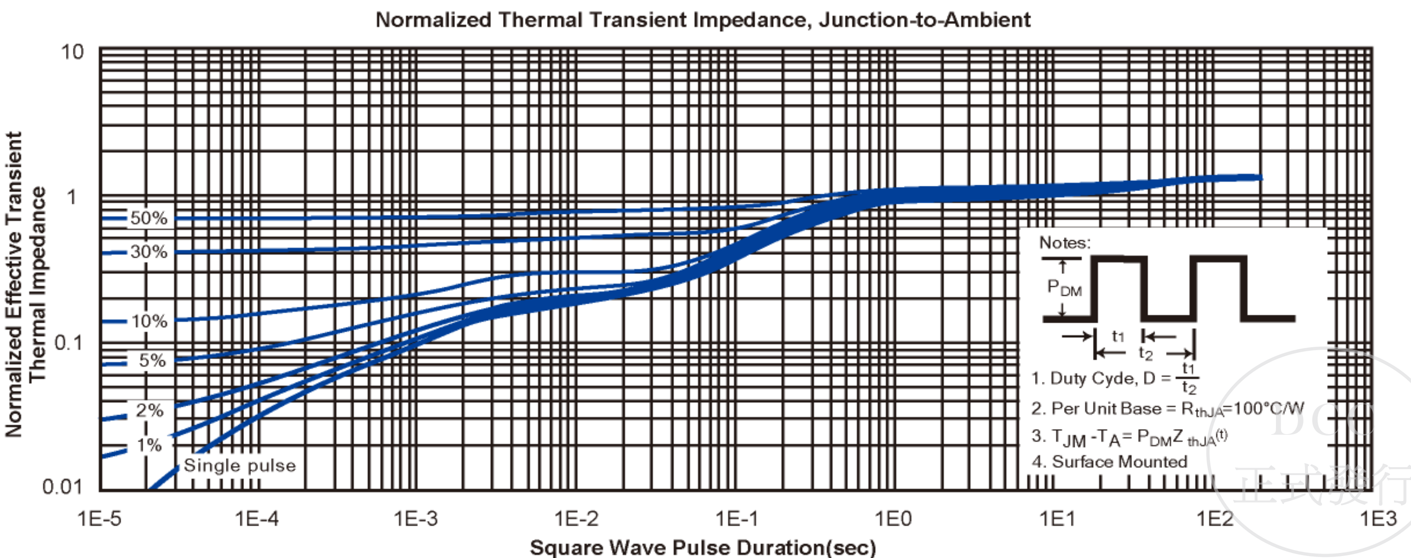
N- and P-Channel 30V (D-S) MOSFET

Typical Characteristics (TJ =25℃ Noted)   P-CHANNEL

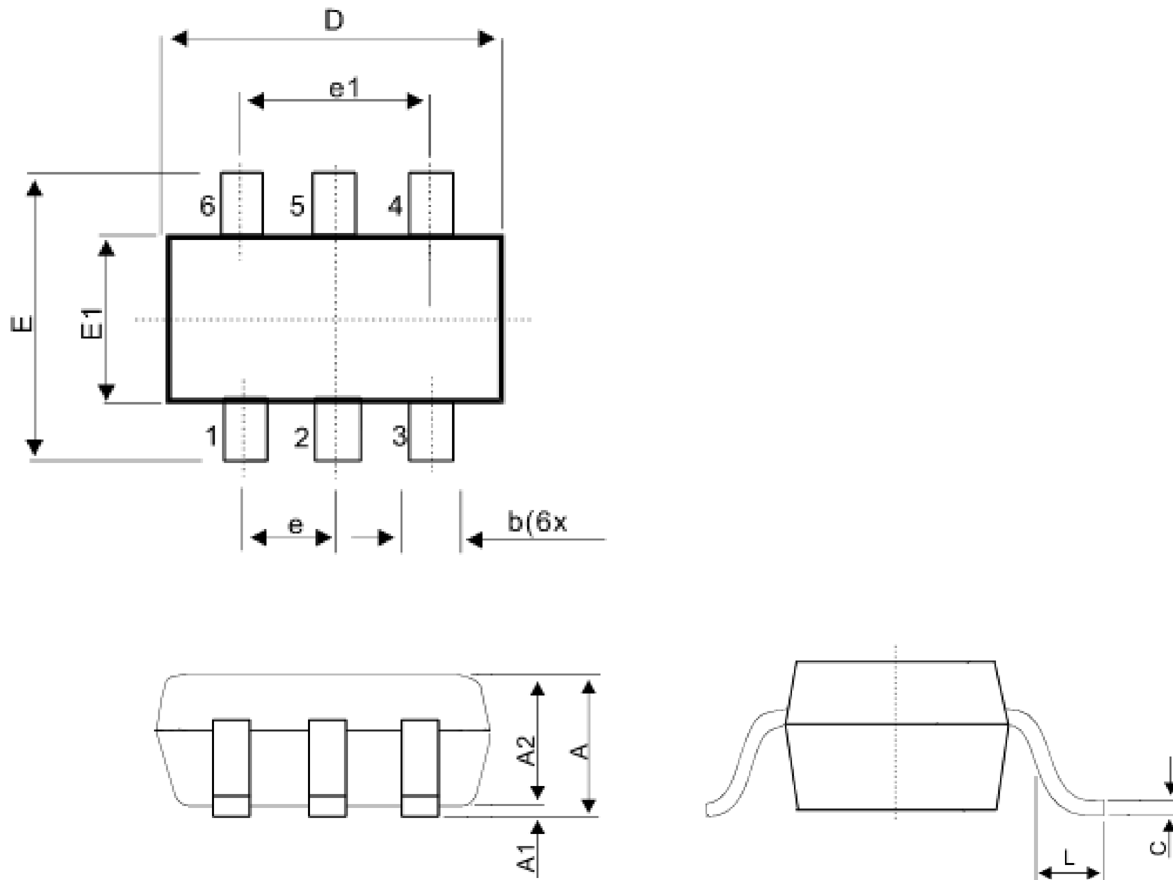








TSOP-6 Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	0.90	1.20
A1	0.01	0.10
A2	0.90	1.15
b	0.25	0.50
C	0.10	0.20
D	2.80	3.10
E	2.60	3.00
E1	1.50	1.70
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60