Dual N-Channel 30V(D-S) MOSFET

GENERAL DESCRIPTION

The ME3920-G is the Dual N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

FEATURES FEATURES

- $R_{DS(ON)} \leqq 24m\Omega @ V_{GS} = 10V$
- $R_{DS(ON)} \leqq 46m\Omega @ V_{GS} = 4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

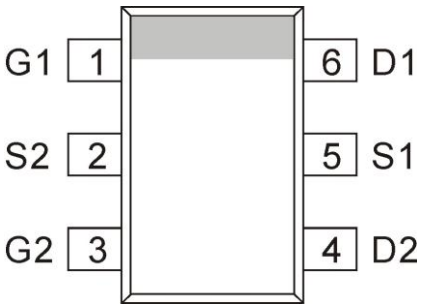
APPLICATIONS

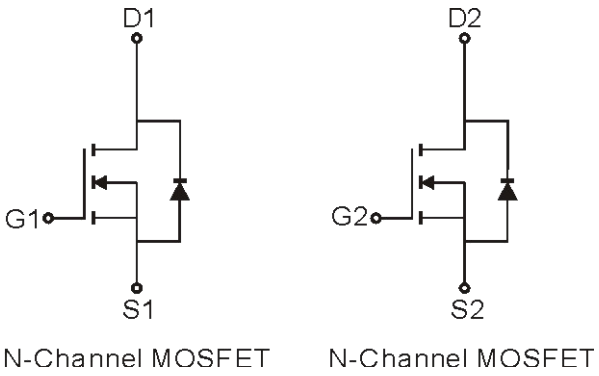
- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

TSOP-6

Top View





Ordering Information:ME3920-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DSS}	30	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(Tj=150℃)	T_A=25℃	I_D	6.6	A
	T_A=70℃		5.3	
Pulsed Drain Current		I_{DM}	27	
Maximum Power Dissipation	T_A=25℃	P_D	1.7	W
	T_A=70℃		1.1	
Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	74	℃/W

*The device mounted on 1in2 FR4 board with 2 oz copper

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Electrical Characteristics (T_J=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC PARAMETERS						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		3	V
I_{GSS}	Gate-Body Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance[a]	V_{GS}=10V, I_D=6.9A		20	24	mΩ
		V_{GS}=4.5V, I_D=5.8A		35	46	
V_{SD}	Diode Forward Voltage	I_S=1.7A, V_{GS}=0V		0.8	1.2	V
DYNAMIC PARAMETERS						
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=4A		10.9		nC
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=4.5V, I_D=4A		5.3		
Qgs	Gate-Source Charge			3.4		
Qgd	Gate-Drain Charge			2.4		
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz		375		pF
Coss	Output Capacitance			54		
Crss	Reverse Transfer Capacitance			37		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=15V, R_L=3.75Ω V_{GS}=10V, R_G=6Ω I_D=4A		8.1		ns
t_r	Rise Time			30.8		
$t_{d(off)}$	Turn-Off Delay Time			18.1		
t_f	Fall Time			11		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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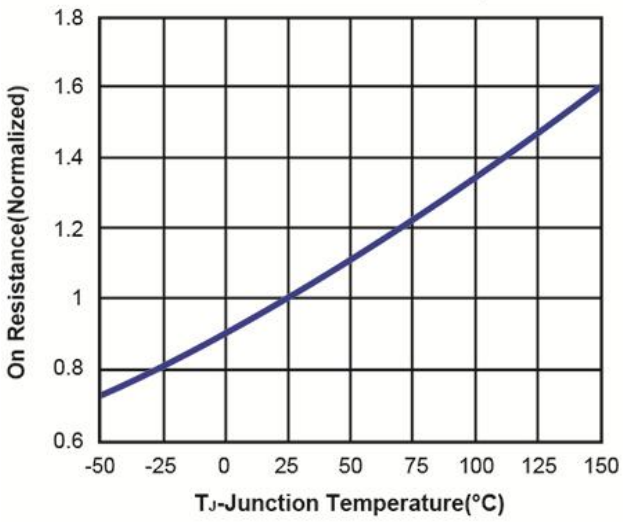
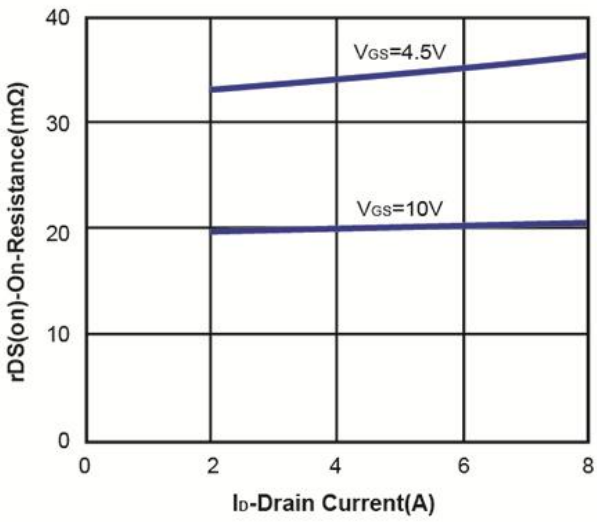
Typical Characteristics (T_J =25℃ Noted)

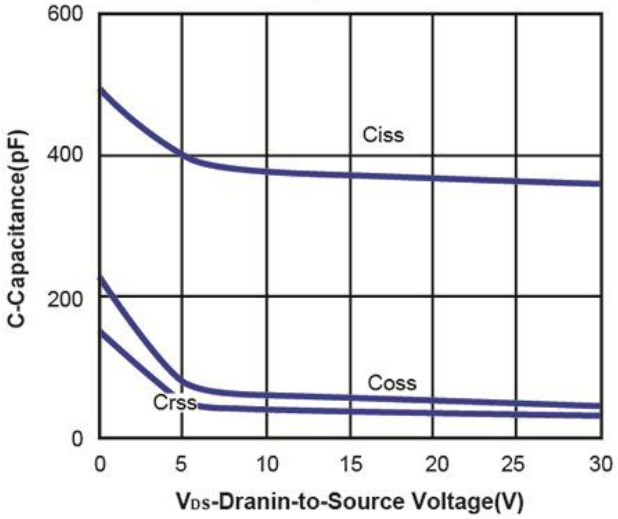
On Resistance vs. Junction Temperature



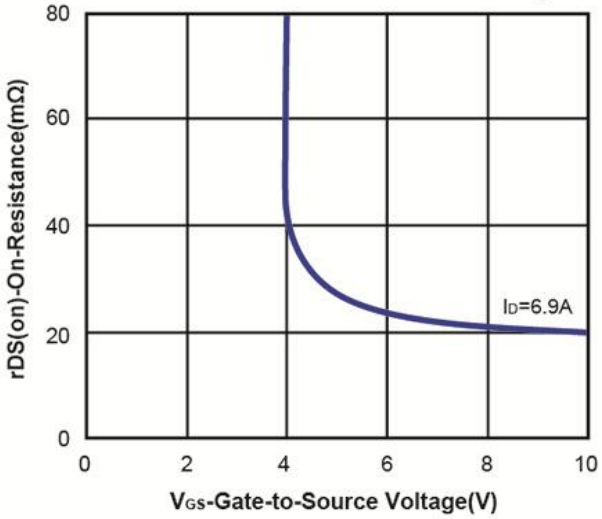
On Resistance vs. Drain Current



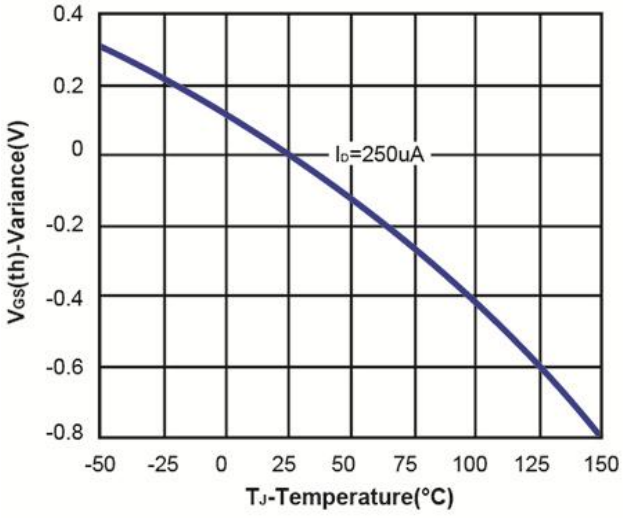
Capacitance



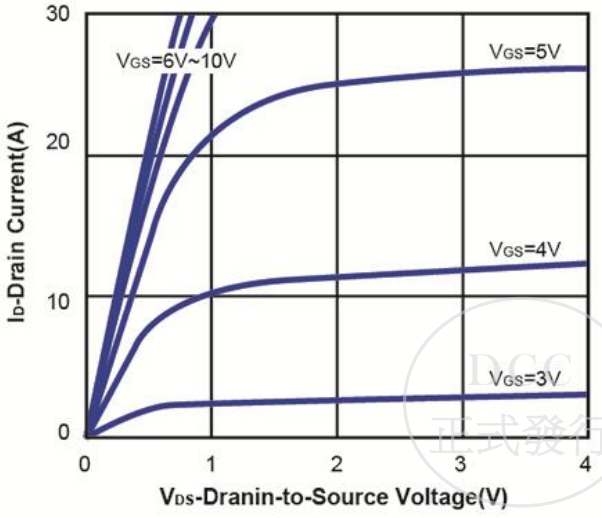
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



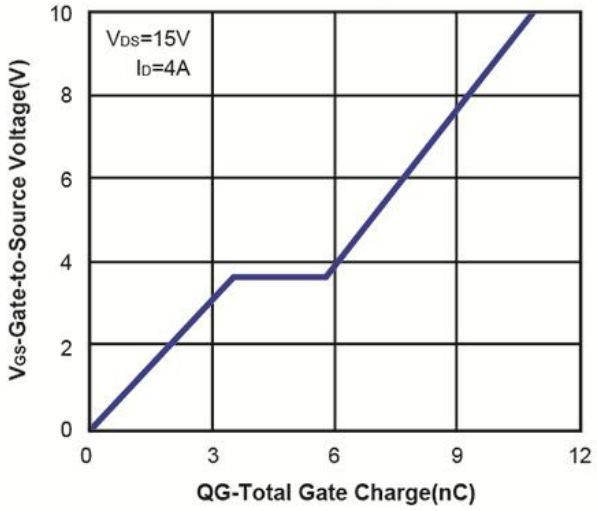
On-Region Characteristics



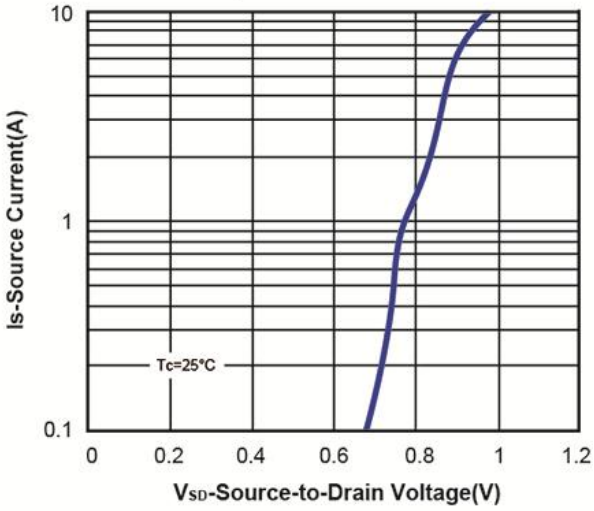
Dual N-Channel 30V(D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

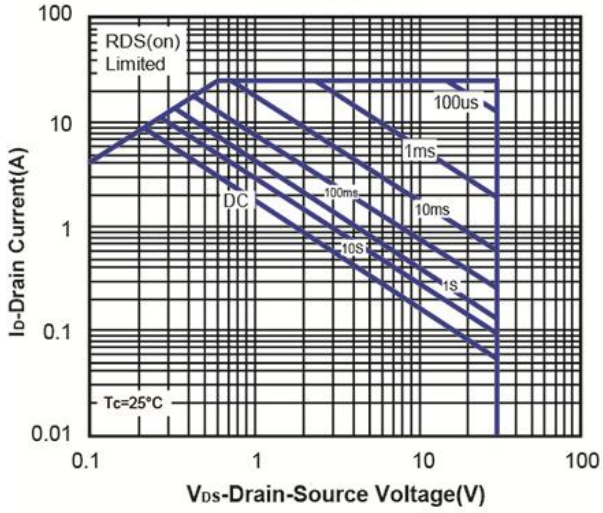
Gate Charge



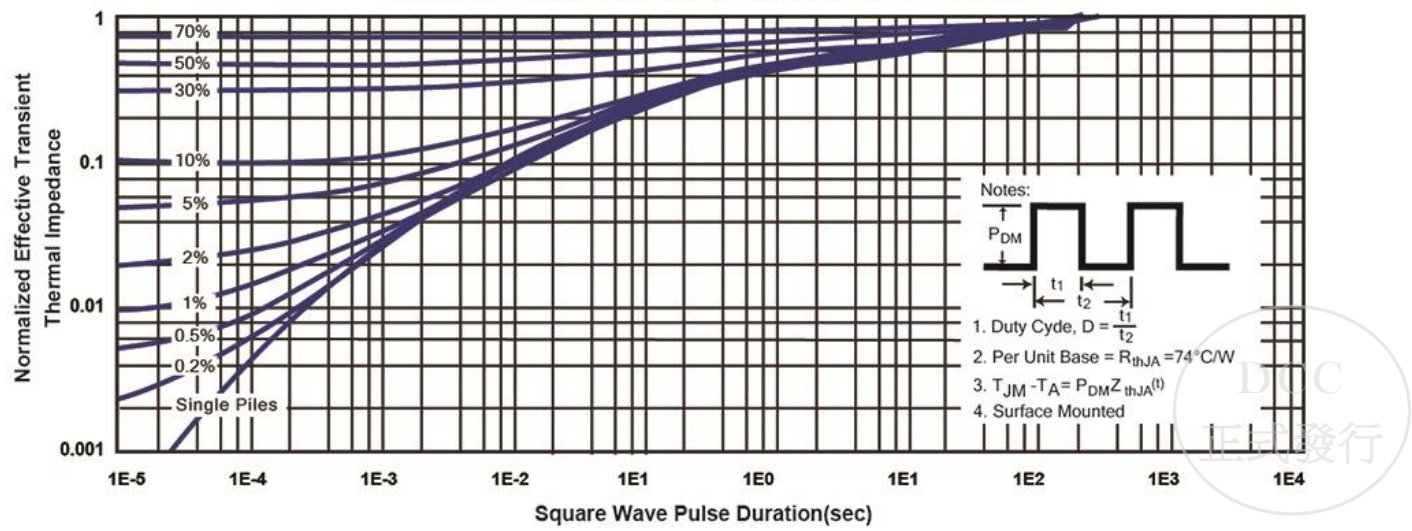
Body-diode characteristics



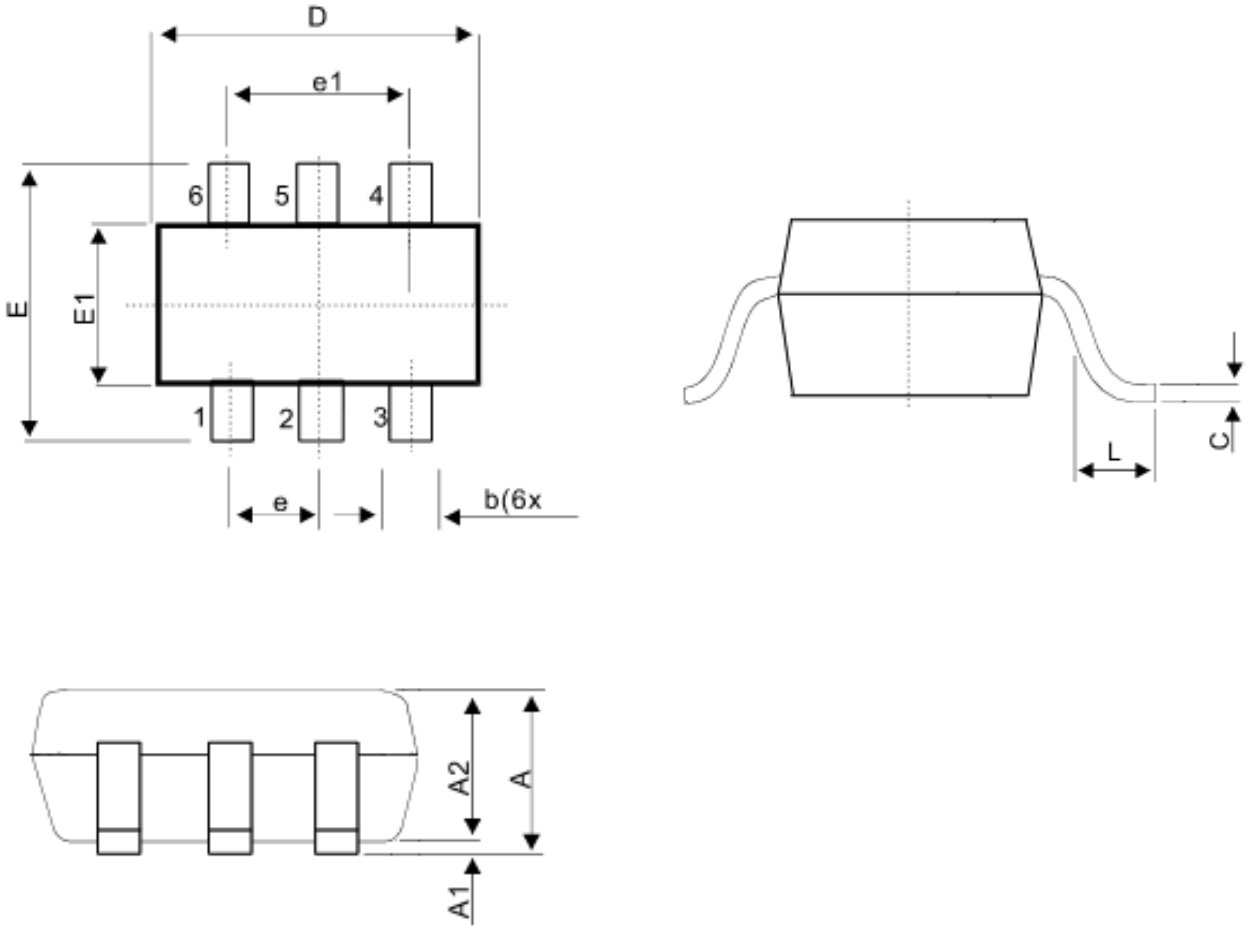
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



TSOP-6 Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	0.90	1.20
A1	0.01	0.10
A2	0.90	1.15
b	0.25	0.50
C	0.10	0.20
D	2.80	3.10
E	2.60	3.00
E1	1.50	1.70
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60