

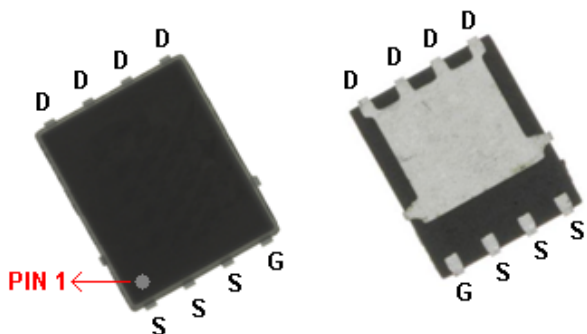
N-Channel 30V(D-S) Enhancement MOSFET

GENERAL DESCRIPTION

The ME7688 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as notebook computer power management and other battery powered circuits where Low-side switching , and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

PowerDFN 5x6

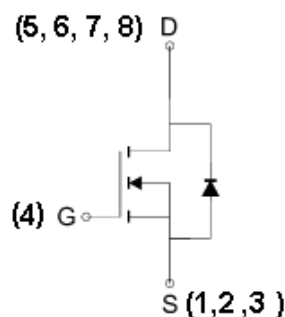


FEATURES

- $R_{DS(ON)} \leq 11m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 19.5m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- NB/MB Vcore Low side switching
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch



N-Channel MOSFET

Ordering Information: ME7688 (Pb-free)

ME7688-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain*	$T_C=25^\circ C$	I_D	46.4	A
	$T_C=70^\circ C$		37.1	
	$T_A=25^\circ C$		12.6	
	$T_A=70^\circ C$		10.1	
Pulsed Drain Current		I_{DM}	50	A
Maximum Power Dissipation*	$T_C=25^\circ C$	P_D	37.9	W
	$T_C=70^\circ C$		24.2	
	$T_A=25^\circ C$		2.8	
	$T_A=70^\circ C$		1.8	
Operating Junction Temperature		T_J	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	45	$^\circ C/W$
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	3.3	$^\circ C/W$

*The device mounted on 1in² FR4 board with 2 oz copper

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Electrical Characteristics (TA=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1		3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-State Resistance ^a	V _{GS} =10V, I _D =15A		9	11	mΩ
		V _{GS} =4.5V, I _D =12A		15	19.5	
V _{SD}	Diode Forward Voltage	I _S =15A, V _{GS} =0V		0.9	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =10V, I _D =15A		18		nC
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =4.5V, I _D =15A		9		
Q _{gs}	Gate-Source Charge			4.3		
Q _{gd}	Gate-Drain Charge			3.3		
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, F=1MHz		695		pF
C _{oss}	Output Capacitance			151		
C _{rss}	Reverse Transfer Capacitance			47		
R _g	Gate-Resistance	V _{DS} =0V, V _{GS} =0V, F=1MHz		1.5		Ω
t _{d(on)}	Turn-On Delay Time	V _{DD} =15V, R _L =15Ω I _D =1A, V _{GEN} =10V R _G =6Ω		14		ns
t _r	Turn-On Rise Time			13		
t _{d(off)}	Turn-Off Delay Time			42		
t _f	Turn-Off Fall Time			7		

Note: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

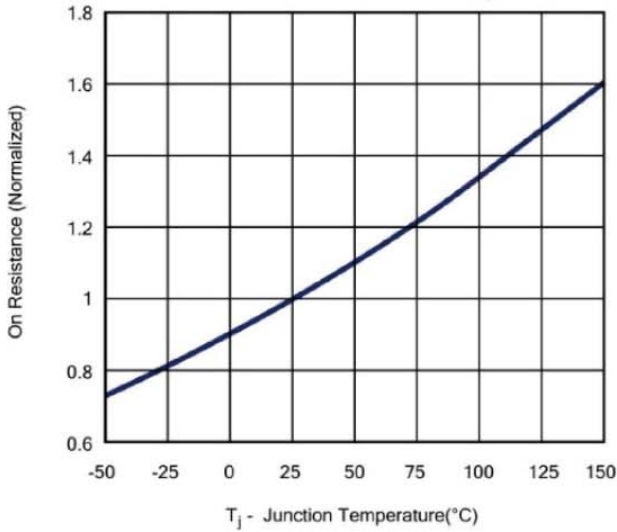
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



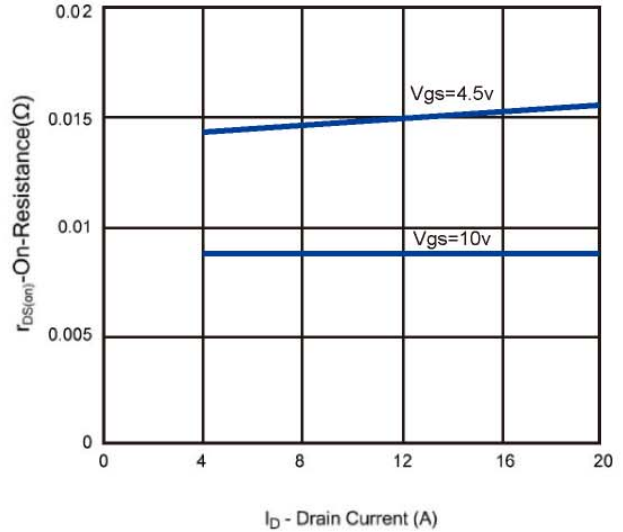
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Typical Characteristics (T_J =25°C Noted)

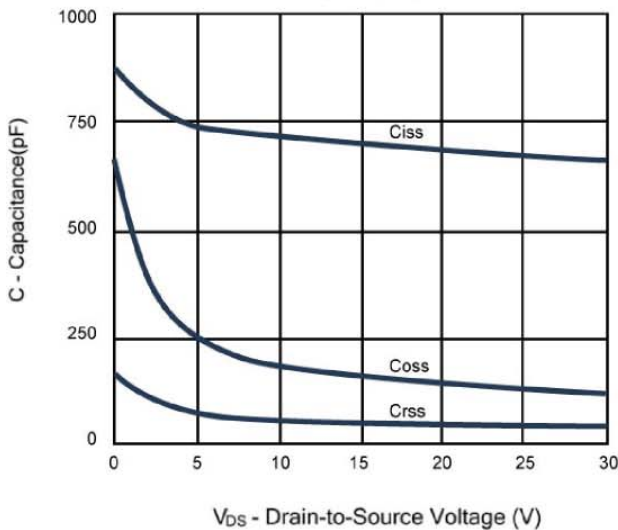
On Resistance vs. Junction Temperature



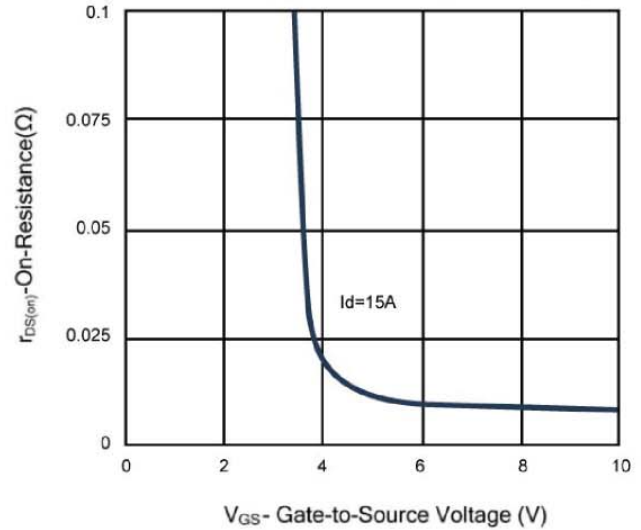
On-Resistance vs. Drain Current



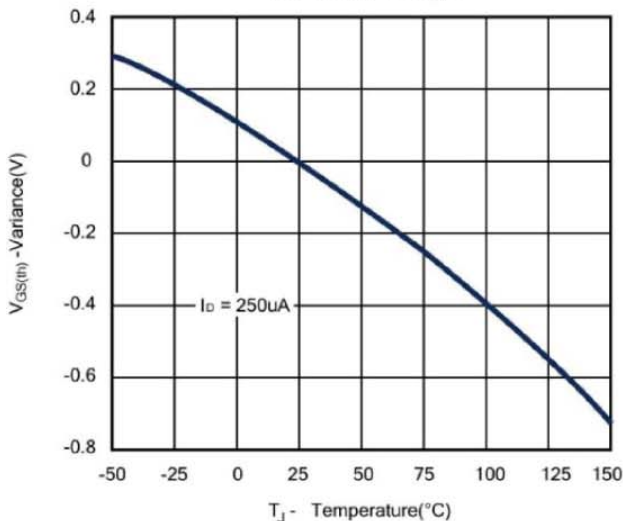
Capacitance



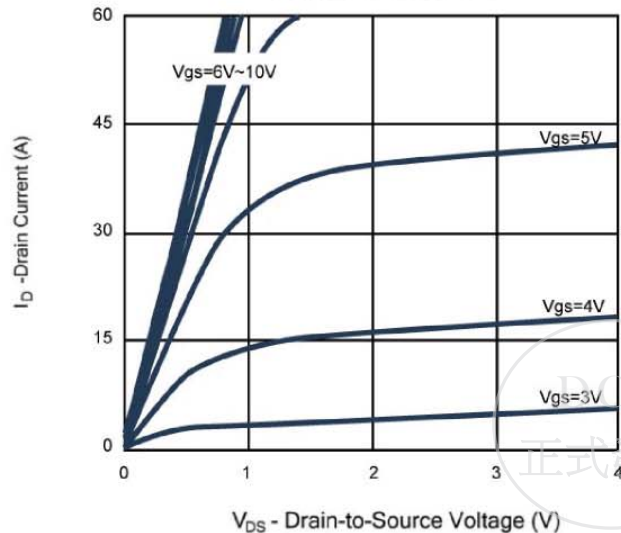
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

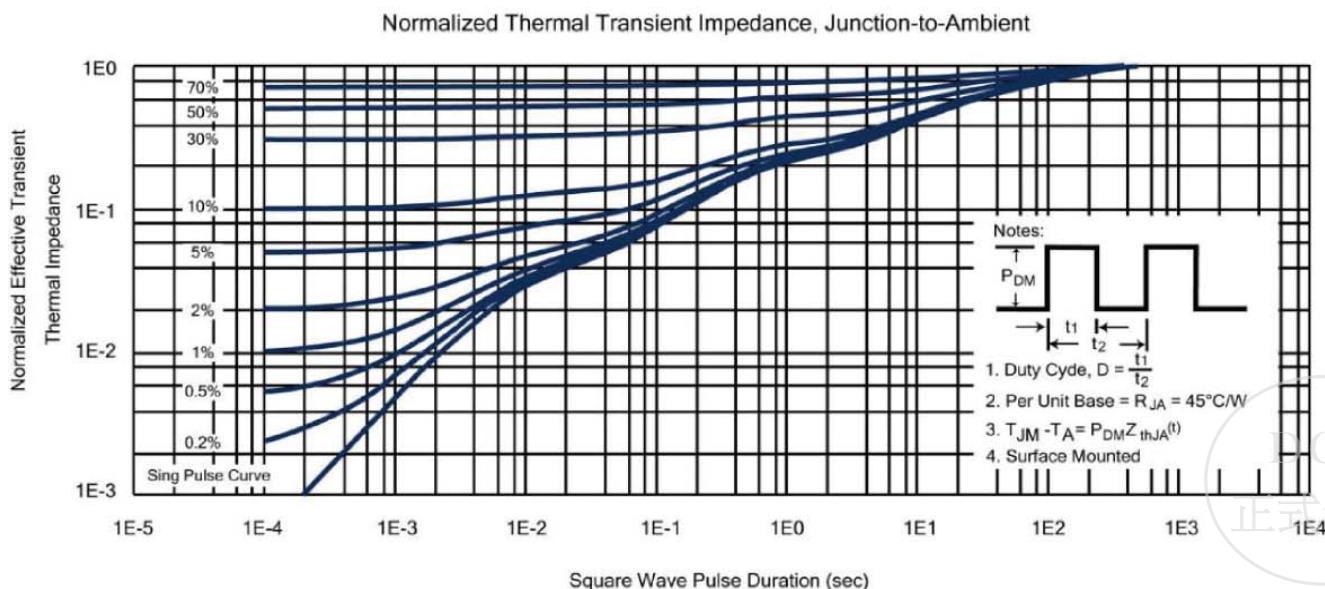
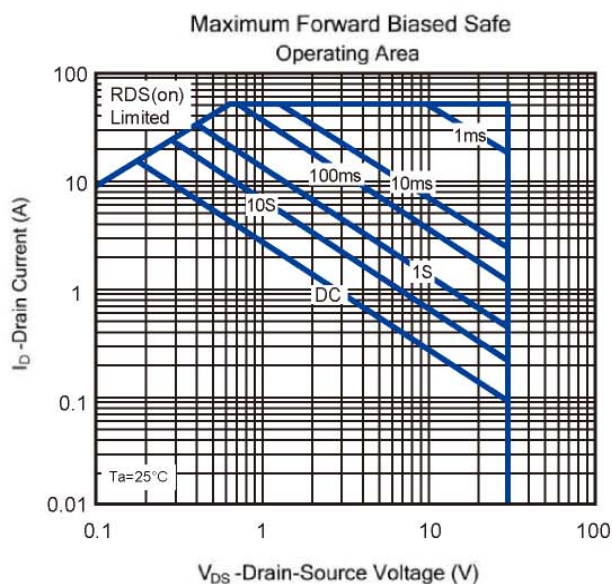
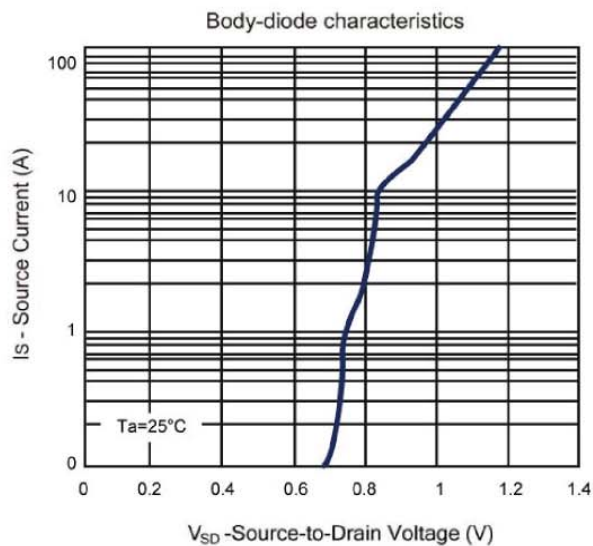
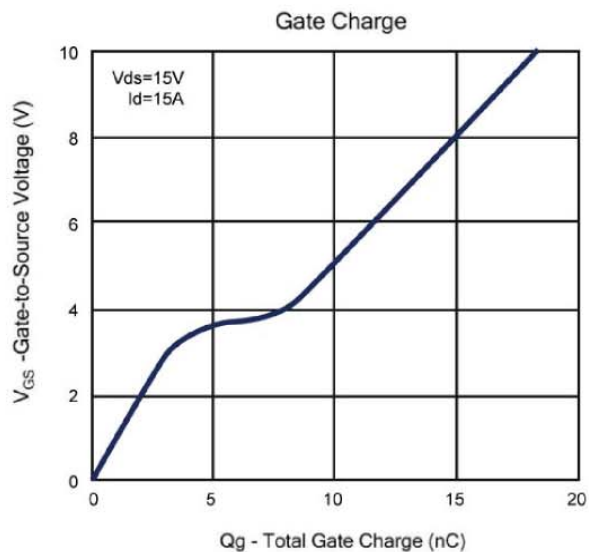


On-Region Characteristics

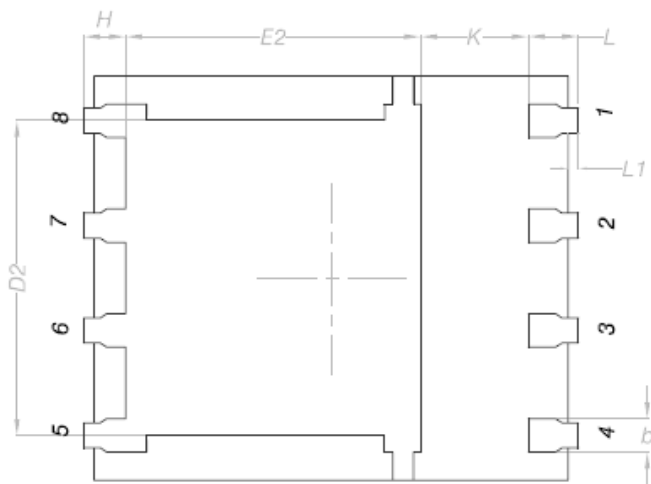


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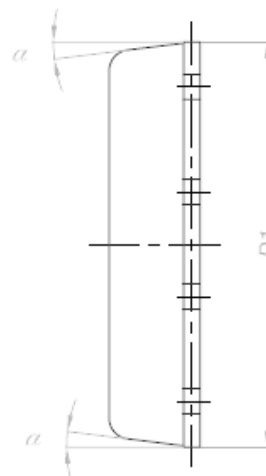
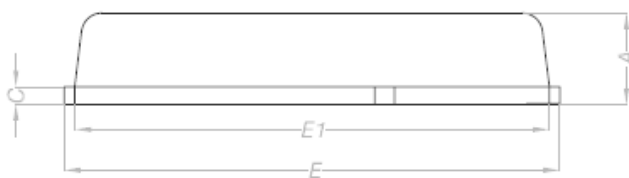
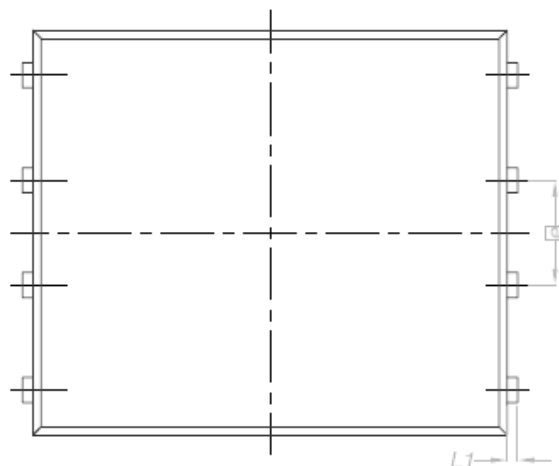
Typical Characteristics (T_J = 25°C Noted)



PowerDFN5x6 Package Outline



BACKSIDE VIEW



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	0.90	1.10
b	0.33	0.51
C	0.20	0.30
D1	4.80	5.00
D2	3.61	3.96
E	5.90	6.10
E1	5.70	5.80
E2	3.38	3.78
e	1.27 BSC	
H	0.41	0.61
K	1.10	-
L	0.51	0.71
L1	0.06	0.20
α	0°	12°

