N-Channel 40V(D-S) Enhancement MOSFET

GENERAL DESCRIPTION

The ME7642-G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as notebook computer power management and other battery powered circuits where Low-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

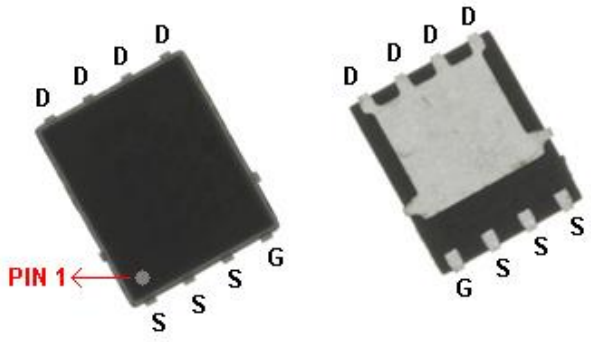
- $R_{DS(ON)} \leqq 4m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 5.5m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

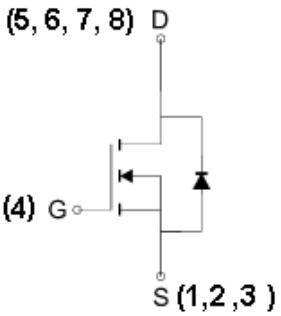
APPLICATIONS

- Power Management in Note book
- NB/MB Vcore Low side switching
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch

PIN CONFIGURATION

PowerDFN 5x6





N-Channel MOSFET

Ordering Information: ME7642/ ME7642-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current*	T_A=25℃	ID	20.8	A
	T_A=70℃		16.6	
Pulsed Drain Current		I_{DM}	83	A
Maximum Power Dissipation*	T_A=25℃	P_D	2.8	W
	T_A=70℃		1.8	
Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	45	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_J=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=10V, I_D=25A		3.3	4	mΩ
		V_{GS}=4.5V, I_D=19A		4.1	5.5	
V_{SD}	Diode Forward Voltage	I_S=25A, V_{GS}=0V		0.8	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=4.5V, I_D=20A		40.5		nC
Qgs	Gate-Source Charge			17.4		
Qgd	Gate-Drain Charge			17.9		
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V,F=1MHz		4622		pF
Coss	Output Capacitance			328		
Crss	Reverse Transfer Capacitance			283		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=15V, R_L=15Ω I_D=1A, V_{GEN}=10V R_G=6Ω		28.9		ns
t_r	Turn-On Rise Time			19.3		
$t_{d(off)}$	Turn-Off Delay Time			111		
t_f	Turn-Off Fall Time			18.9		

Note: a.Pulse test: pulse width≦300us, duty cycle≦2%

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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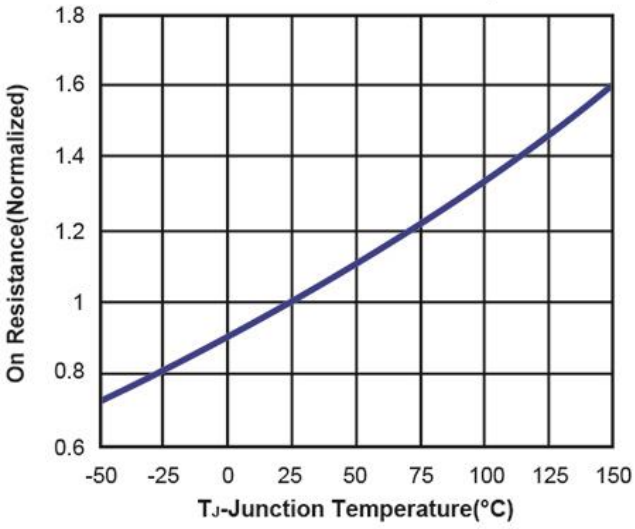
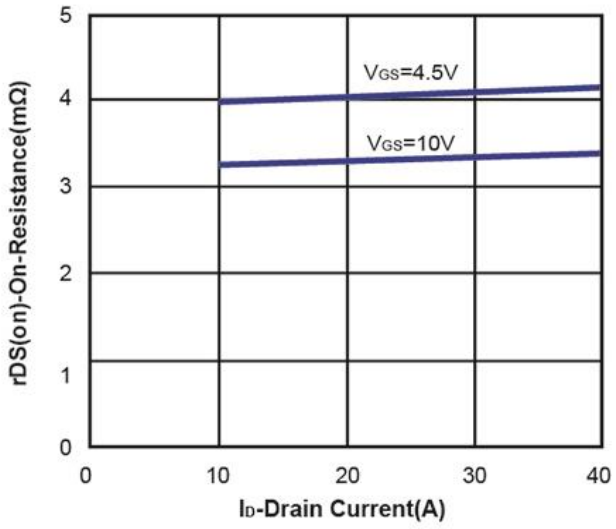
Typical Characteristics (T_J =25℃ Noted)

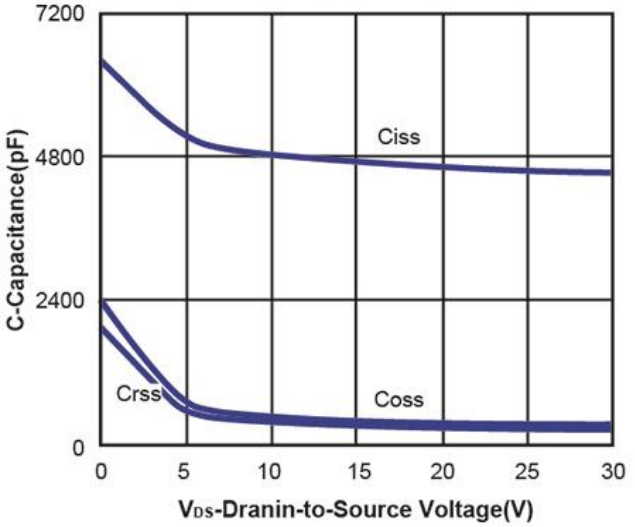
On Resistance vs. Junction Temperature



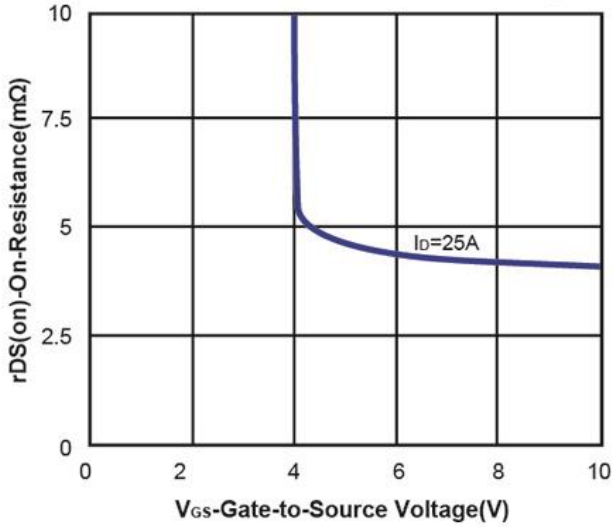
On Resistance vs. Drain Current



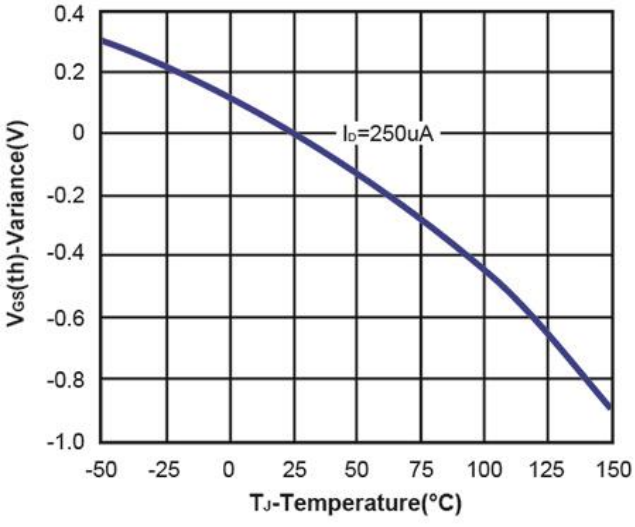
Capacitance



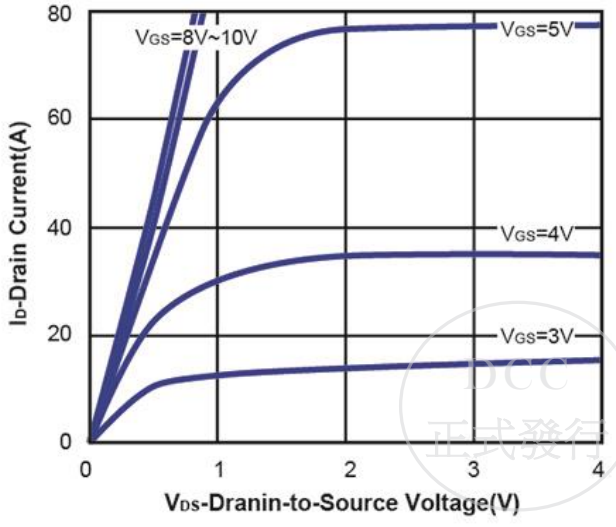
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



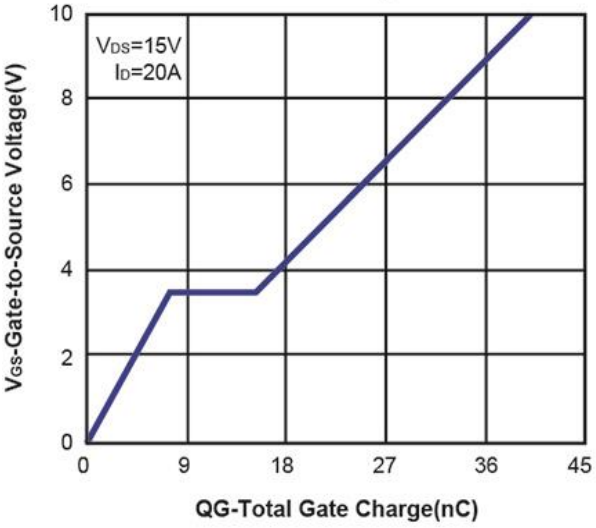
On-Region Characteristics



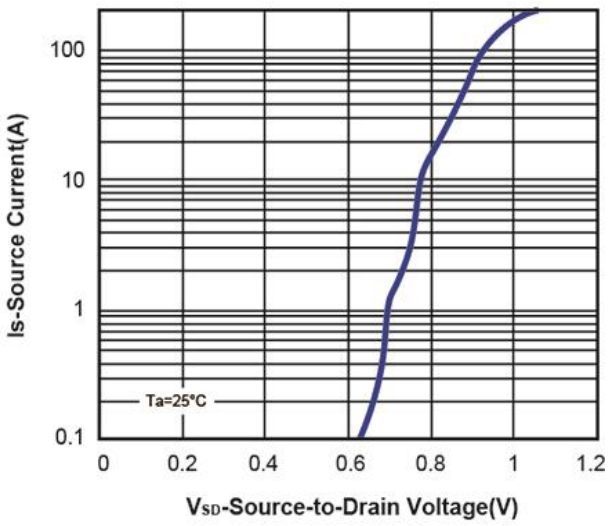
N-Channel 40V(D-S) Enhancement MOSFET

Typical Characteristics (T_J =25℃ Noted)

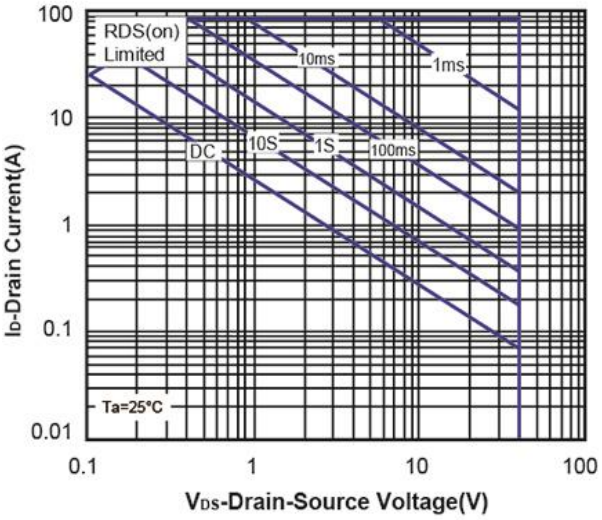
Gate Charge



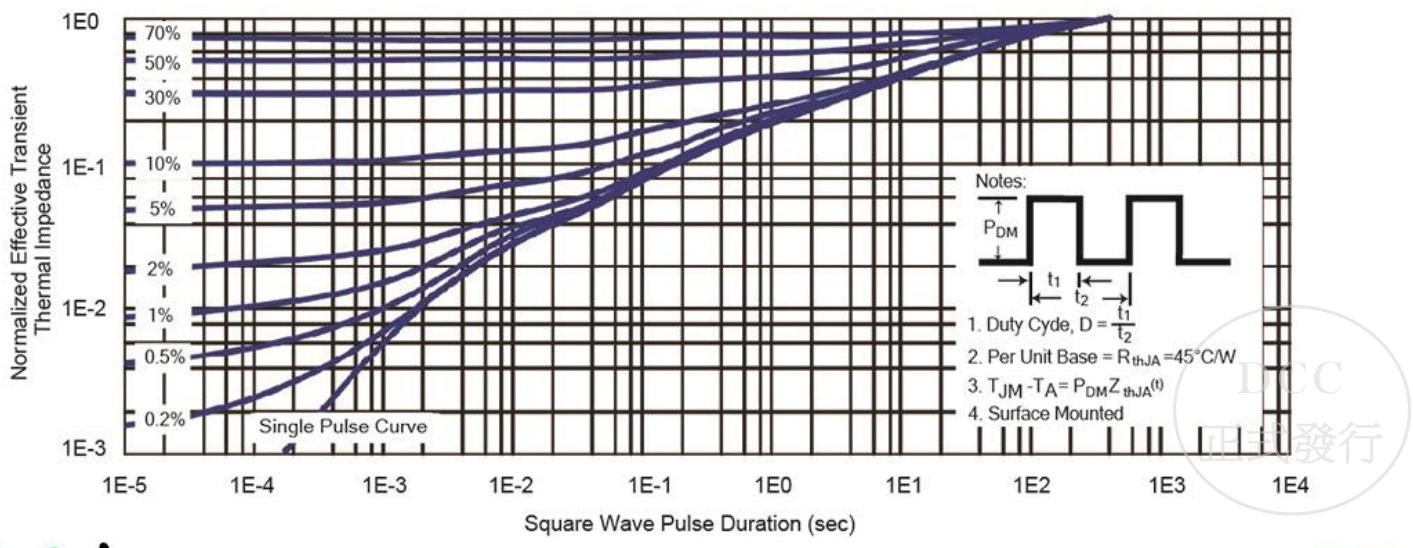
Body-diode characteristics



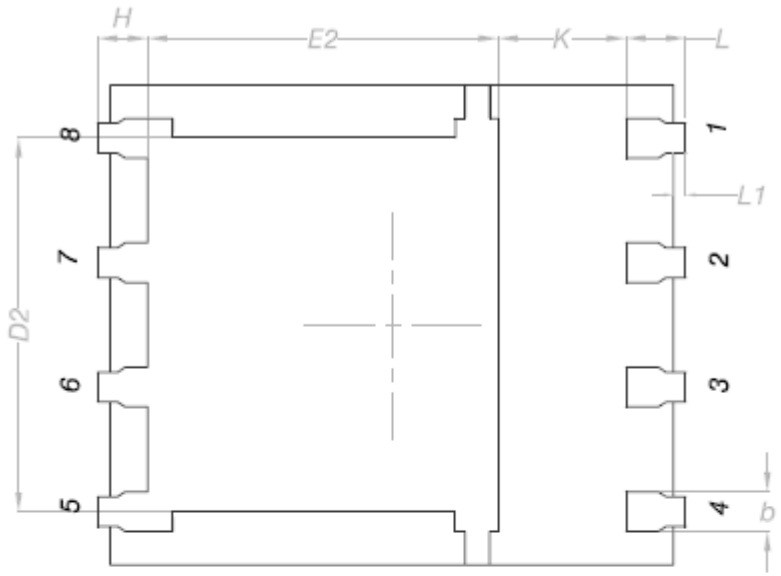
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



PowerDFN 5x6 Package Outline



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°