ME80N75AF / ME80N75AF-G

N- Channel 75-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME80N75AF is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as notebook computer power management and other battery powered circuits where Low-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 10m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

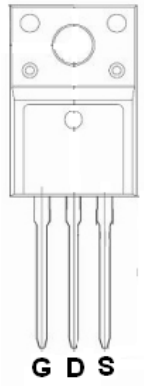
APPLICATIONS

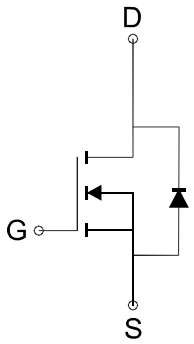
- Power Management
- DC/DC Converter
- Load Switch

PIN CONFIGURATION

(TO-220F)

Top View





N-Channel MOSFET

Ordering Information: ME80N75AF (Pb-free)

ME80N75AF-G (Green product-Halogen free)

Absolute Maximum Ratings (T_C=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	75	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current	T_C=25℃	I_D	55.7	A
	T_C=70℃		46.6	
Pulsed Drain Current		I_{DM}	223	A
Maximum Power Dissipation	T_C=25℃	P_D	61.9	W
	T_C=70℃		43.4	
Junction and Storage Temperature Range		TJ, Tstg	-55 to 175	℃
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	2.42	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper.

N- Channel 75-V (D-S) MOSFET

Electrical Characteristics (T_C =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	75			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2.0		4.0	V
I_{GSS}	Gate-Body Leakage	V_{DS}=0V, V_{GS}=±25V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=75V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance*	V_{GS}=10V, I_D=40A		8	10	mΩ
V_{SD}	Diode Forward Voltage *	I_S=40A, V_{GS}=0V		0.9	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DD}=60V, V_{GS}=10V, I_D=75A		132		nC
Qg	Total Gate Charge	V_{DD}=60V, V_{GS}=4.5V, I_D=75A		31		
Qgs	Gate-Source Charge			39.5		
Qgd	Gate-Drain Charge			43.9		
Ciss	Input Capacitance	V_{DS}=20V, V_{GS}=0V, f=1MHz		7440		pF
Coss	Output Capacitance			394		
Crss	Reverse Transfer Capacitance			337		
$t_{d(on)}$	Turn-On Delay Time	V_{GS} =10V, R_L=15Ω V_{DS}=30V, R_G=10Ω I_D=2A		60.6		ns
t_r	Turn-On Rise Time			38.7		
$t_{d(off)}$	Turn-Off Delay Time			170		
t_f	Turn-Off Fall Time			48		

Notes: a. pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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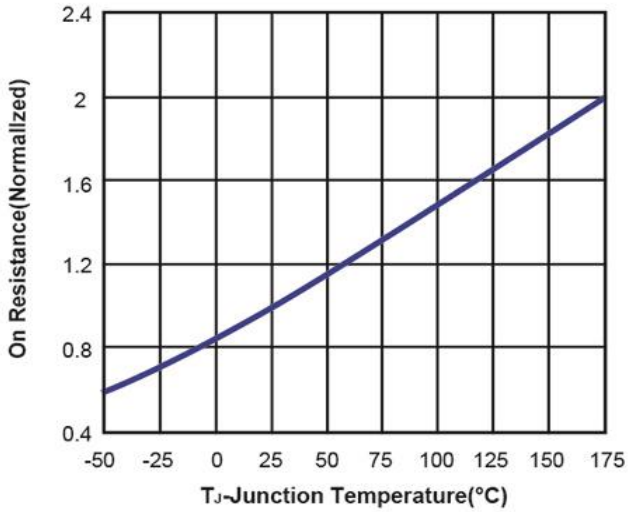
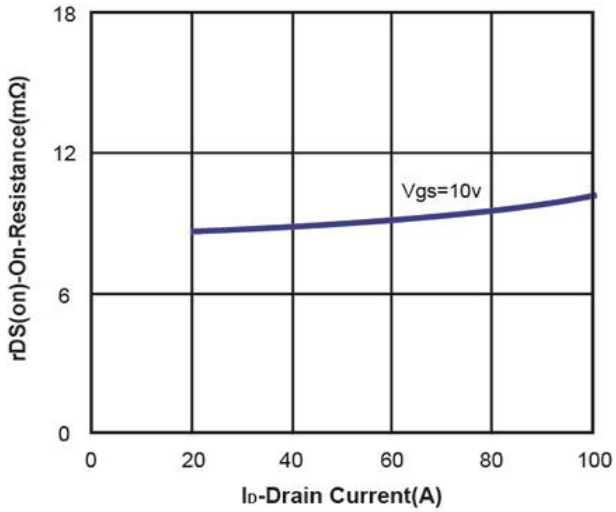
N- Channel 75-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

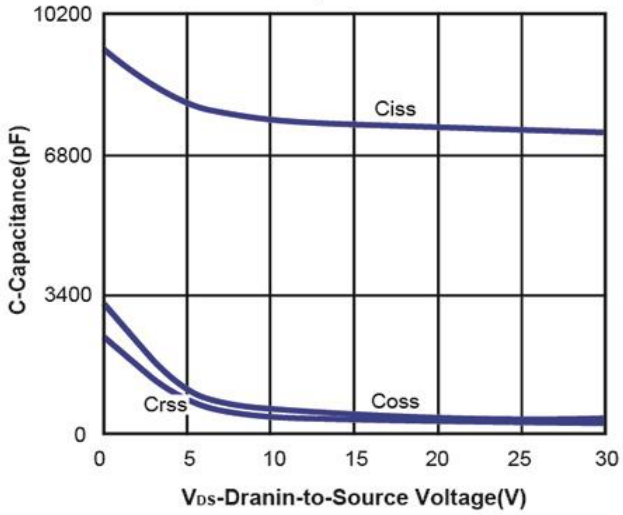
On Resistance vs. Junction Temperature



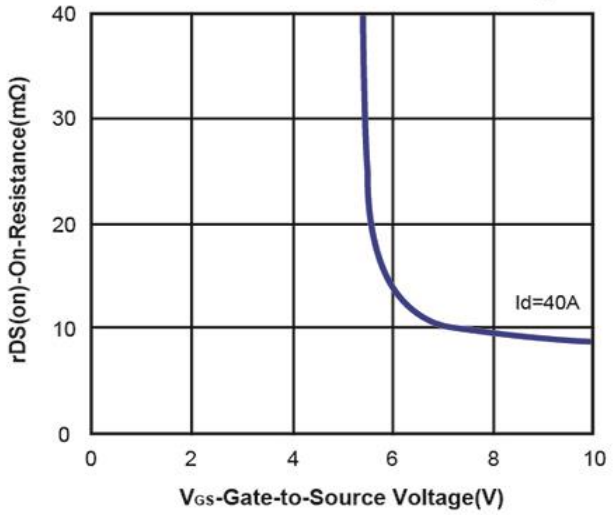
On Resistance vs. Drain Current



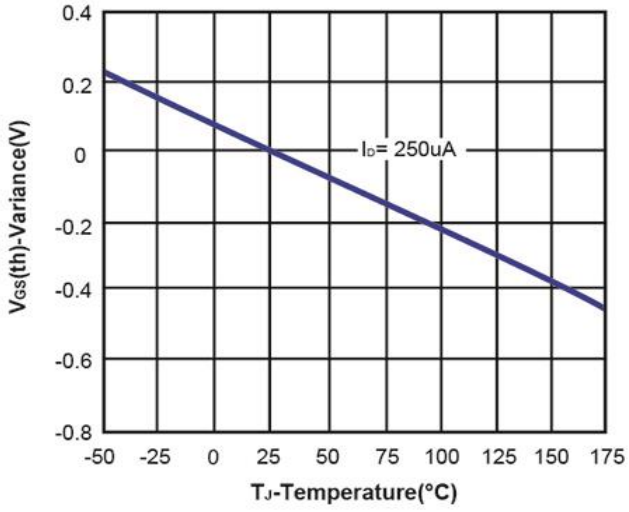
Capacitance



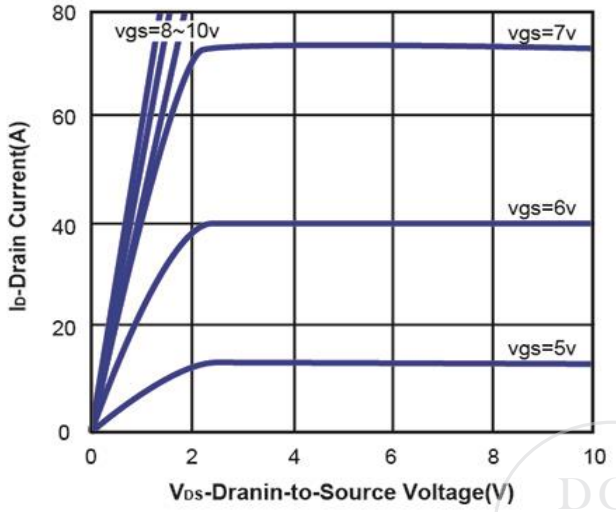
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



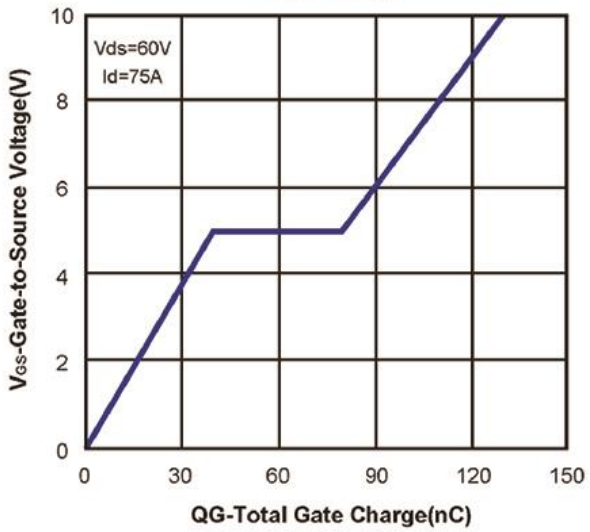
On-Region Characteristics



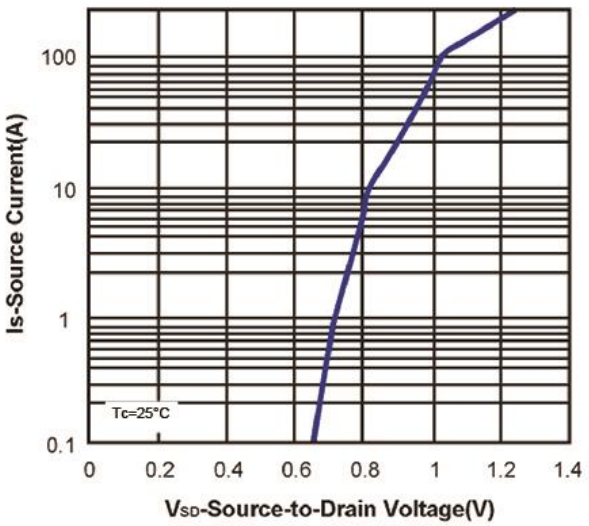
N- Channel 75-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

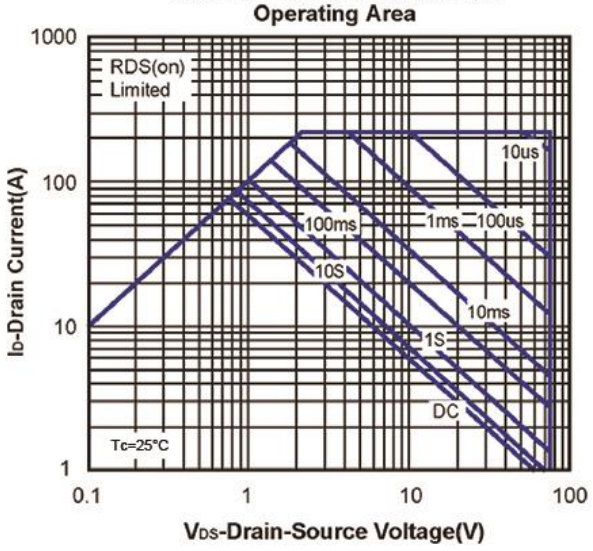
Gate Charge



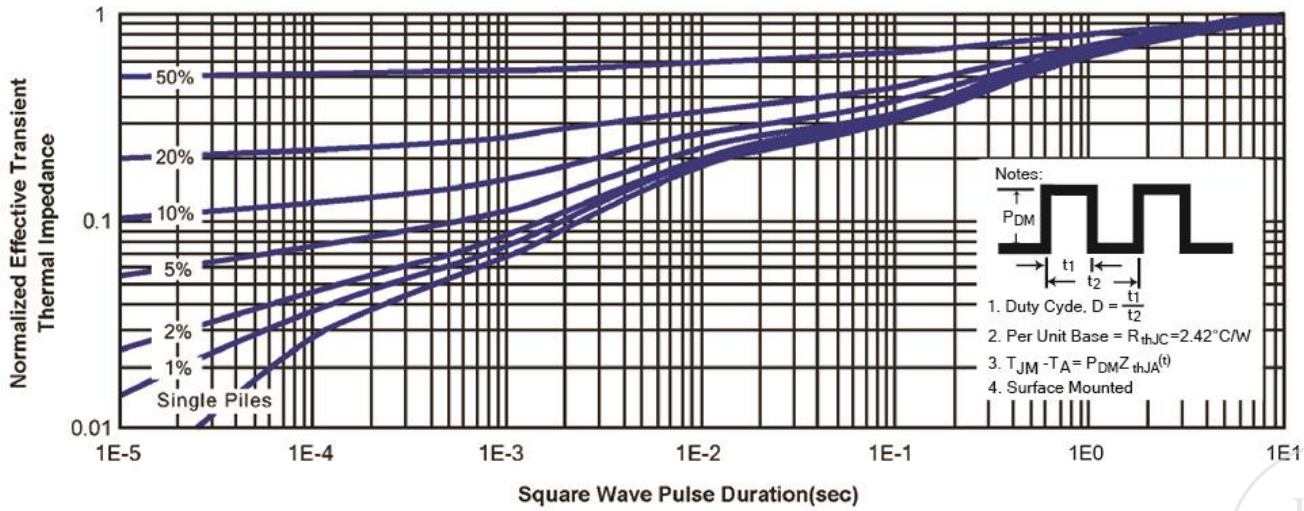
Body-diode characteristics



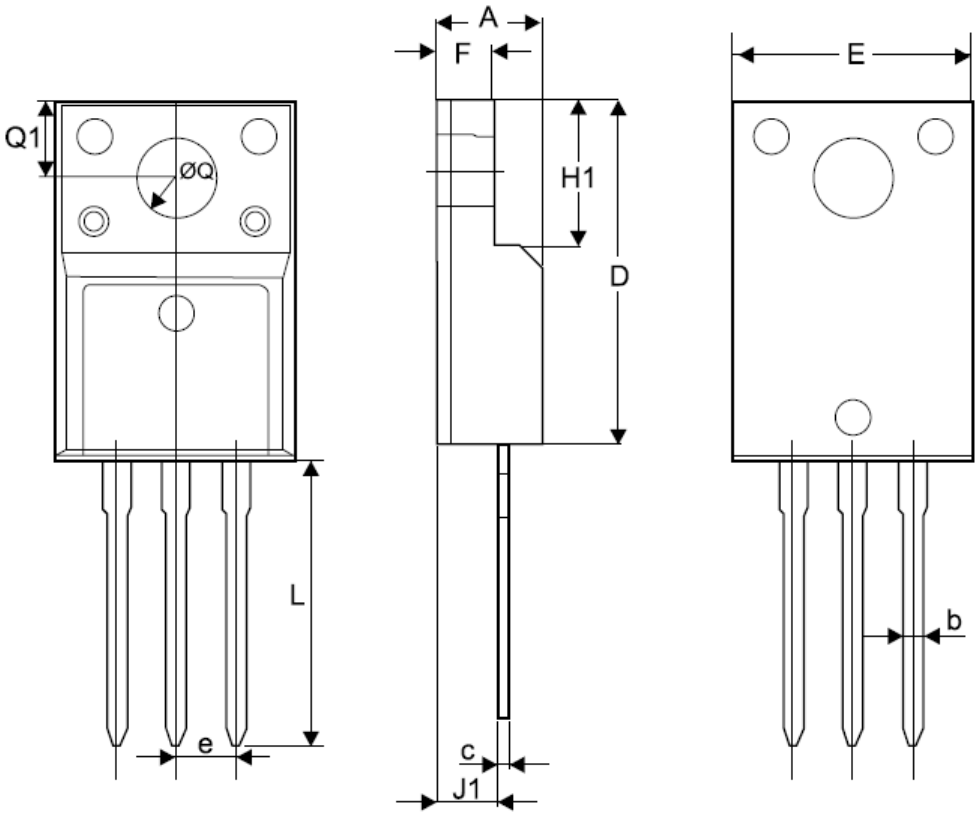
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



TO-220F Package Outline



Symbol	MILLIMETERS(mm)	
	MIN	MAX
A	4.40	5.00
b	0.60	1.00
C	0.30	0.70
D	15.40	16.40
E	6.96	10.46
F	2.30	2.80
e	2.54 TYP	
H1	6.40	7.00
J1	2.45	3.05
L	12.28	13.68
Ø Q	2.92	3.38
Q1	3.05	3.55