

N-Channel 80V(D-S) MOSFET

GENERAL DESCRIPTION

The ME80N08A is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

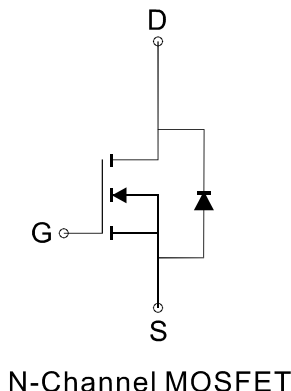
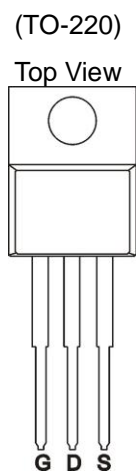
FEATURES

- $R_{DS(ON)} \leq 5m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION



Ordering Information: ME80N08A (Pb-free)
ME80N08A-G (Green product-Halogen free)

Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V _{DS}	80	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current*	I _D	T _c =25°C	194
		T _c =70°C	162
Pulsed Drain Current ^a	I _{DM}	776	A
Power Dissipation	P _D	T _c =25°C	300
		T _c =70°C	210
Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 175	°C
Thermal Resistance-Junction to Case**	R _{θJC}	0.5	°C/W

* Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 80A.

** The device mounted on 1in² FR4 board with 2 oz copper.

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Electrical Characteristics ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	80			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0		4.0	V
I_{GSS}	Gate-Body Leakage	$V_{GS}=\pm 20V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=80V, V_{GS}=0V$			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance*	$V_{GS}=10V, I_D=80A$		3.9	5	m Ω
V_{SD}	Diode Forward Voltage *	$I_S=40A, V_{GS}=0V$		0.8	1.2	V
DYNAMIC						
Q_g	Total Gate Charge	$V_{DD}=40V, V_{GS}=10V, I_D=80A$		221		nC
Q_g	Total Gate Charge	$V_{DD}=40V, V_{GS}=4.5V, I_D=80A$		56		
Q_{gs}	Gate-Source Charge			63		
Q_{gd}	Gate-Drain Charge			55		
C_{iss}	Input Capacitance	$V_{DS}=25V, V_{GS}=0V, f=1MHz$		12500		pF
C_{oss}	Output Capacitance			1150		
C_{rss}	Reverse Transfer Capacitance			375		
$t_{d(on)}$	Turn-On Delay Time	$V_{GS}=10V, R_L=20\Omega$		65		ns
t_r	Turn-On Rise Time			43		
$t_{d(off)}$	Turn-Off Delay Time	$V_{DD}=40V, R_G=3.3\Omega$		196		
t_f	Turn-Off Fall Time			53		

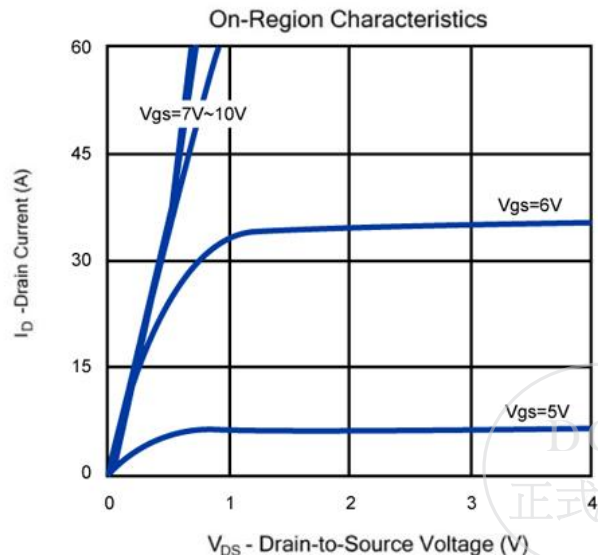
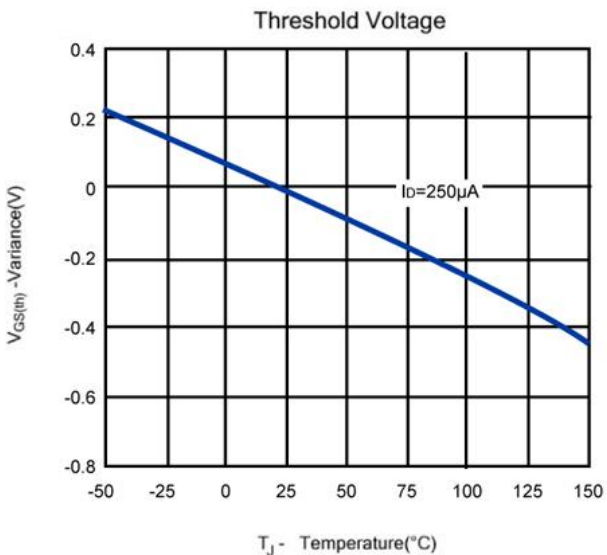
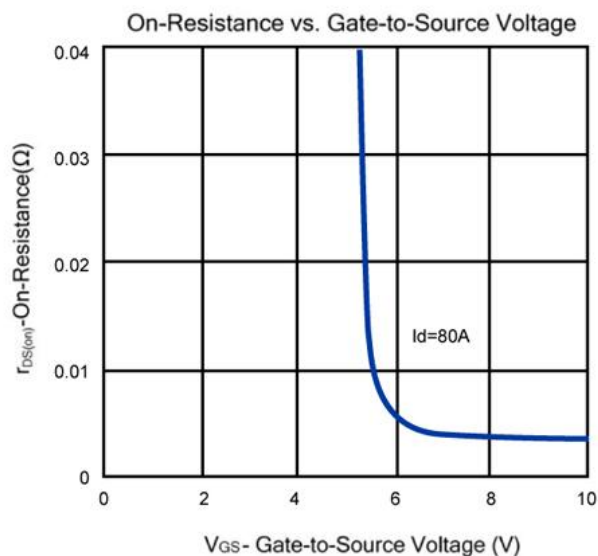
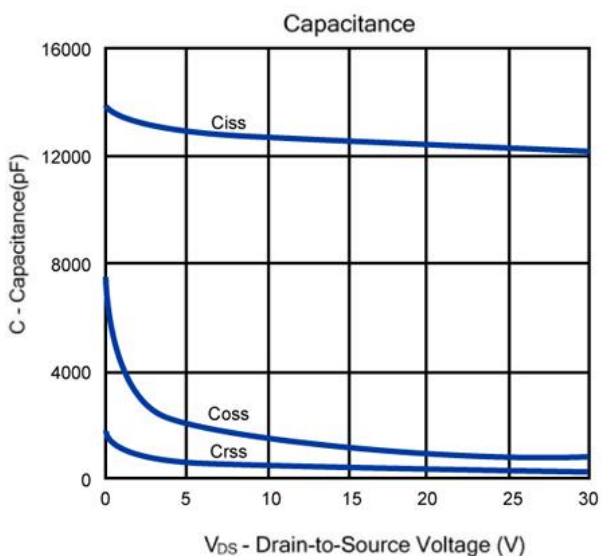
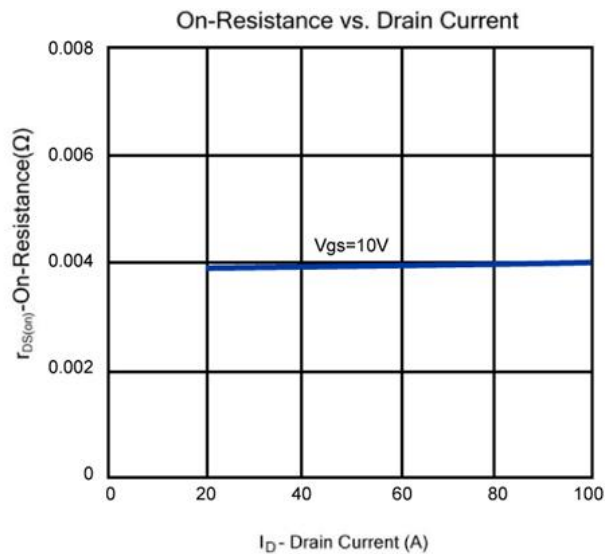
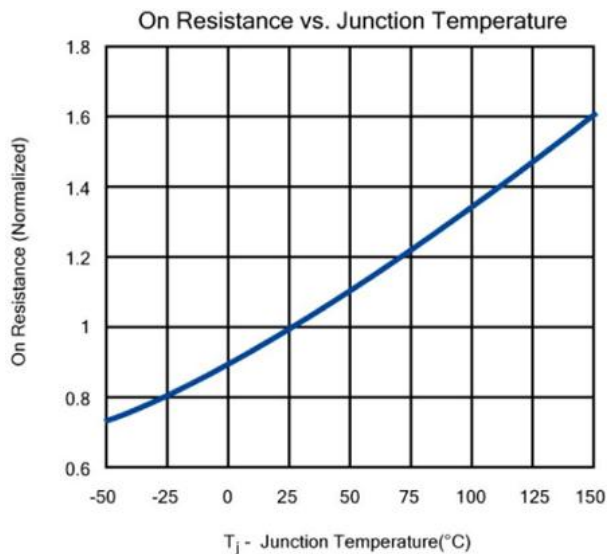
 Notes: a. pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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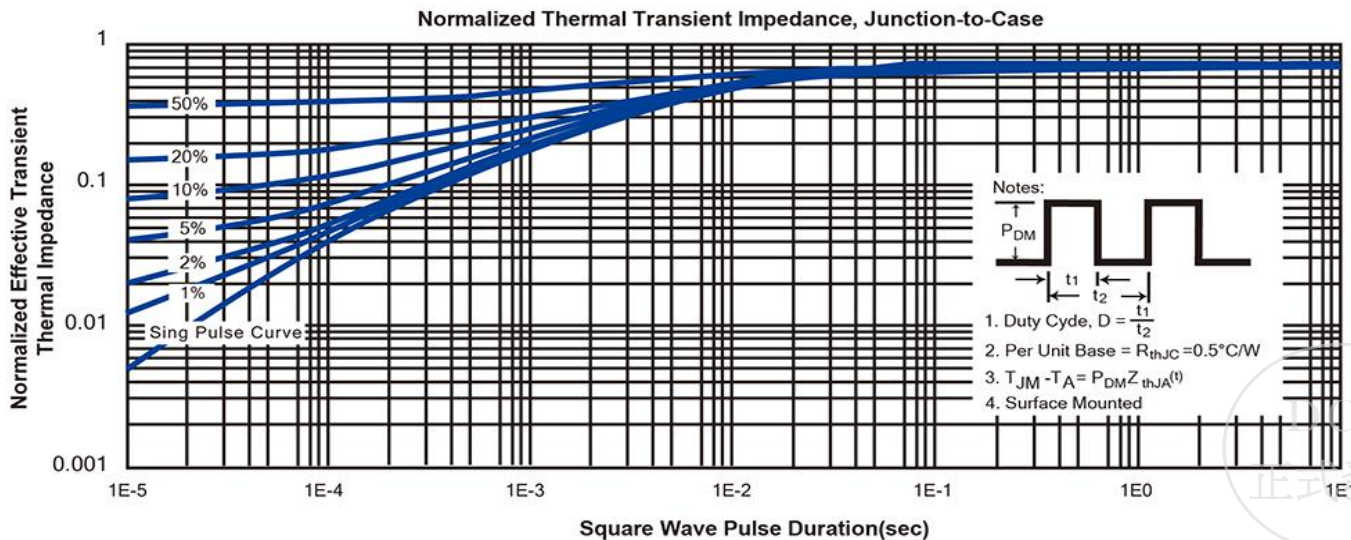
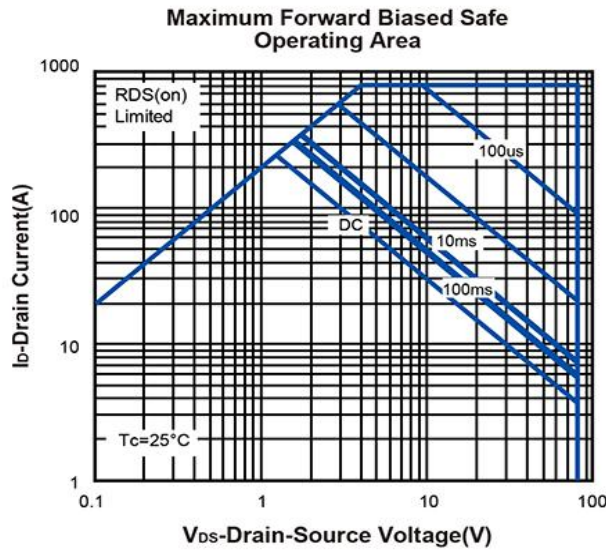
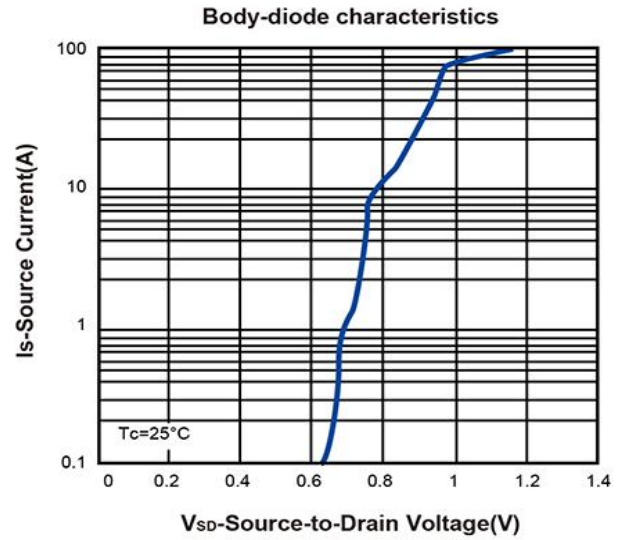
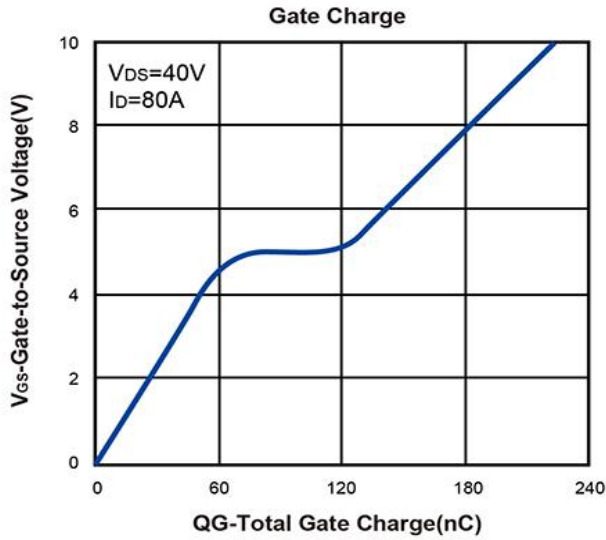
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Typical Characteristics (T_J =25°C Noted)

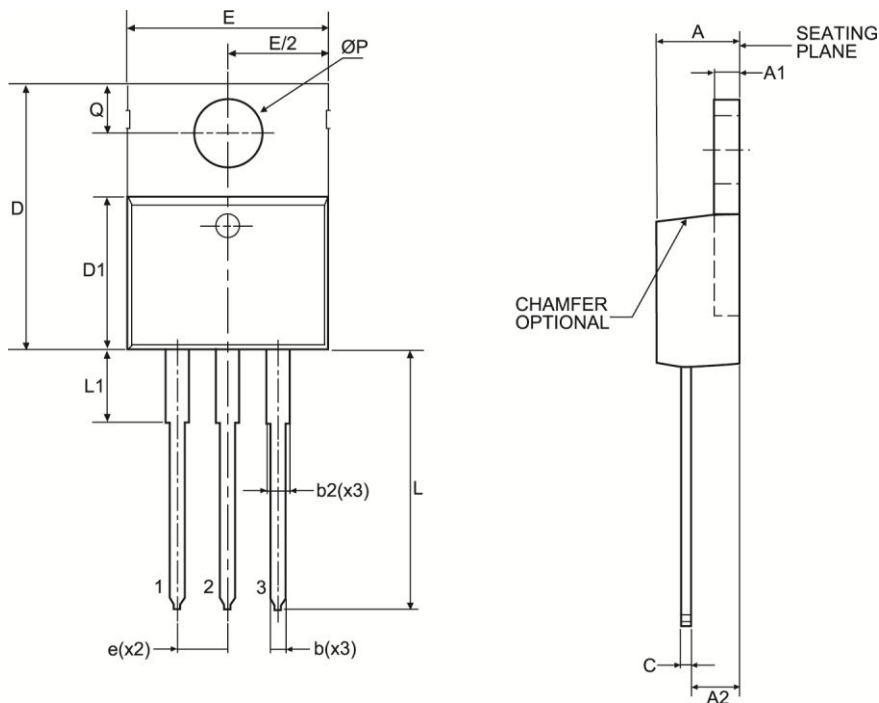


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TO-220 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	3.50	4.90
A1	1.00	1.40
A2	2.00	3.00
b	0.70	1.40
c	0.35	0.65
D	14.00	16.50
D1	8.30	9.50
E	9.60	10.70
e	2.54 BSC	
L	12.50	15.00
ØP	3.60 TYP	
Q	2.50	3.10
b2	1.10	1.80
L1	2.40	3.20

