PRELIMINARY
Notice: This is not a final specification. Some parametric limits are Subject to change.

M5M82C37AP,-4,-5

CMOS PROGRAMMABLE DMA CONTROLLER

DESCRIPTION

The M5M82C37AP is a programmable 4-channel DMA (Direct Memory Access) controller. This device is specially designed to simplify data transfer at high trasfer rate for microcomputer systems.

Fabricated using the silicon-gate CMOS technology, the M5M82C37AP operates using a single 5V power supply.

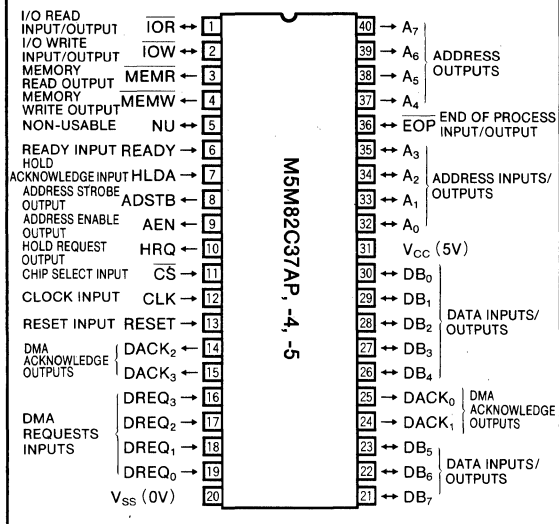
FEATURES

- 5V single supply, single TTL clock
- Four channel DMA controls with priority DMA request acknowledge functions
- DMA enable/disable, automatic initialization enable/disable, address increment/decrement programmability for each cannel
- Programmable DREQ input and DACK output logic polarity
- Direct connecting permits easy DMA channel expansion.
- Memory to memory data transfer
- EOP input/output permits DMA operation completion check as well as forcibly completing DMA operation.

APPLICATION

- DMA control of peripheral equipment such as floppy diskettes and CRT terminals that require high-speed data transfer.

PIN CONFIGURATION (TOP VIEW)



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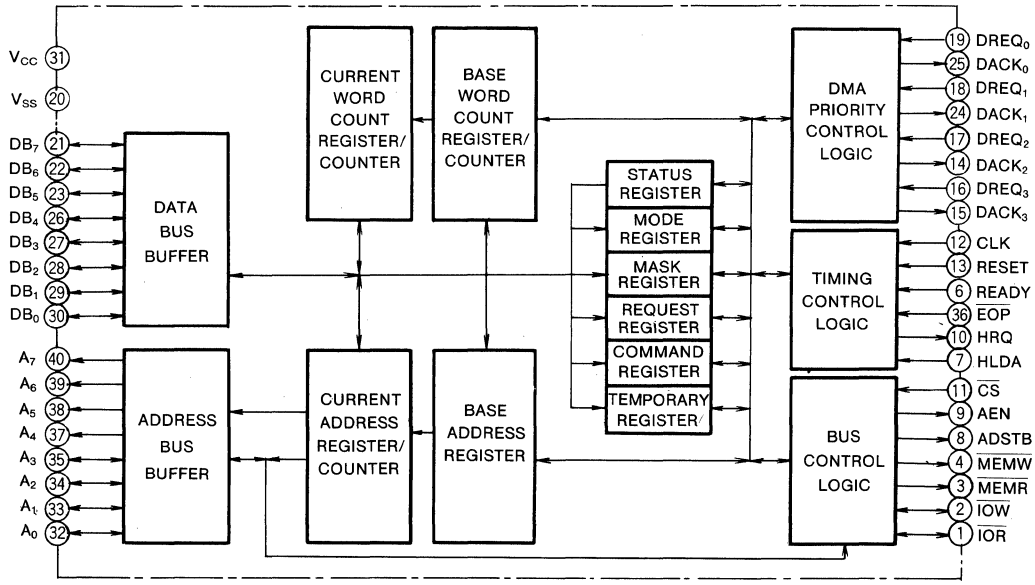
BLOCK DIAGRAM



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FUNCTION

M5M82C37AP is a programmable DMA controller LSI used in microprocessor systems.

This device basically consists of a DMA request control block for acknowledging DMA requests, a CPU interface for exchanging data and commands with the CPU, a timing control circuit for controlling each of the various types of timing, and a register for holding and counting DMA addresses and number of transfer words.

After setting the transfer mode, starting address, and byte number in each of the registers and when a DMA request is made to an unmasked channel, the M5M82C37AP requires use of the bus to the CPU. When the HLDA signal is received from the CPU, the DMA acknowledge signal is sent to DMA requesting channel with the highest priority and begins DMA operation.

During DMA operation, the contents of the low-byte of the transfer memory address are output through $A_7 \sim A_0$. Every time a change in the high-order 8-bit values is necessitated immediately after DMA operation has begun or due to borrowing or decrement during DMA operation, the change is output via pins $DB_7 \sim DB_0$ to the externally mounted latch circuit. After the address is transmitted, read and write signals are sent to the memories and peripherals activating DMA transfer.

PIN DESCRIPTION

$\overline{IOR}$ input/output (I/O read input/output)

The function of this pin differs depending on the state of the M5M82C37AP.

During DMA operation, the $\overline{IOR}$ outputs low-level pulses providing read timing to the peripheral devices.

In the cascade mode DMA, this pin becomes high impedance. In non-DMA mode, $\overline{IOR}$ is an input to read the contents of the registers in the M5M82C37AP.

$\overline{IOW}$ input/output (I/O write input/output)

The function of this pin deffers depending on the state of the M5M82C37AP. In DMA operation, $\overline{IOW}$ outputs a low-level pulse to denote the write timing to peripheral devices.

In cascade mode DMA, this pin becomes high impedance.

In non-DMA mode, $\overline{IOW}$ is input to write data to the registers of the M5M82C37AP.

$\overline{MEMR}$ output (Memory read output)

In DMA mode, this pin outputs a low-level pulse to denote the memory read timing.

In cascade mode DMA or in non-DMA operation this pin becomes high impedance.

$\overline{MEMW}$ output (memory write output)

In DAM mode, this pin outputs a low-level pulse to denote the memory write timing.

In cascade mode DMA or in non-DMA opration, this pin becomes high impedance.

NU pin (Non-usable)

Pin 5 is a non-usable pin. This pin should be tied to V_{CC}, or it should be left open.

READY input (ready input)

This input is used to extend the read or write pulse in the DMA operation. As long as low-level is input, the DMA transfer period is extended. If no timing extension is needed, this input should be tied to V_{CC}.

Note : The ready input level must be stable near the falling edge of the clock input. If the minimum READY setup time from clock or the minimum READY hold time after clock is violated, M5M82C37AP might go into illegal DMA operations.

HLDA input (hold acknowledge input)

This input means that the CPU acknowledges the use of the bus. If M5M82C37AP sets the HRQ output high-level and the HLDA input goes to high-level the M5M82C37AP begins DMA operation.

Note : (i) When HLDA is high-level, $\overline{CS}$ input is disabled and unexpected read or write operation to M5M82C37AP is prevented.
(ii) At least 1 clock period is required from HRQ rising edge to HLDA rising edge

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ADSTB output (address strobe output)
This pin outputs a high-level pulse when the higher 8 bits of the transfer address is output through data bus at the DMA operation. This pulse is used as the strobe pulse for the external address latch circuit.
In non-DMA mode or in cascade mode DMA this output remains low-level.

AEN output (address enable output)
AEN is an output which denotes that the bus control signal address output etc. from the M5M82C37AP are valid. When AEN output is high-level, they are valid output, so AEN is used as a control input for an external three-state bus buffer.

HRQ output (hold request output)
This output denotes that the M5M82C37AP requests the use of the bus to the CPU. The M5M82C37AP sets HRQ high in response to the DMA request.

$\overline{CS}$ input (chip select input)
This input is a chip select signal which is set to low-level when the CPU reads or writes data to the M5M82C37AP. When HLDA is high-level, this input is masked and the M5M82C37AP is not selected.

CLK input (clock input)
The master clock for the M5M82C37AP is input.

RESET input (reset input)
When a high-level pulse is input from RESET, the M5M82C37AP is set to the initial state.

DACK0, DACK1, DACK2, DACK3 output (DMA acknowledge output)
DMA acknowledge is the signals which shows a peripheral device whether DMA operaiton for its channel is under execution.
By resetting, they become active low outputs, but they can be mode into high-acive outputs by altering the contents of the command register.

DREQ0, DREQ1, DREQ2, DREQ3
DREQ is an input which shows that a peripheral device requests DMA service. By resetting, they become active high inputs but they can be made into active low inputs by altering the contents of the command regsiter. DREQ should keep in active until the DACK output returns.

V_{SS}
V_{SS} is connected to system ground.

$DB_7 \sim DB_0$ inputs/outputs (data bus inputs/outputs)
In non-DMA mode, the contents of the registers of the M5M82C37AP are read out or written through $DB_7 \sim DB_0$.
In DMA mode, the higher 8 bits of the transfer address are output through $DB_7 \sim DB_0$ in the S_1 state. In the memory to memory DMA mode, data to be transferred between memories via the temporary register are read and written by the M5M82C37AP through $DB_7 \sim DB_0$.

V_{CC}
The 5V power supply is connected through V_{CC}.

$A_7 \sim A_0$ input/output (address input/output)
In the DMA mode, the lower 8 bits of the transfer address are output through $A_7 \sim A_0$.
In cascade mode DMA, they become high impedance. In the non-DMA mode, $A_3 \sim A_0$ become register select address inputs, while $A_7 \sim A_4$ become high impedance.

$\overline{EOP}$ input/output (end of process input/output)
$\overline{EOP}$ is an N-channel open drain input/output. When the word count register reaches count-up, a low-level pulse is output from $\overline{EOP}$. (This is called internal $\overline{EOP}$.) $\overline{EOP}$ may be pulled down to low-level. If $\overline{EOP}$ is pulled down during DMA operation, the DMA operation is forcibly terminated. (This is called external $\overline{EOP}$.)

Note : In cascade mode DMA, the $\overline{EOP}$ pulse is not output, and external $\overline{EOP}$ cannot terminate cascade mode DMA operation.

OPERATION

The unit of operation of the M5M82C37AP is one clock period long and is called a 'state'. The M5M82C37AP has seven kinds of states.

The following is the description of the basic DMA operation. When the M5M82C37AP is DMA disabled or no DMA request comes for unmasked DMA channel, the M5M82C37AP is in stand-by condition. At this time the M5M82C37AP repeats S_I (Inactive state) until a valid DMA request comes. When the M5M82C37AP is enabled and a valid DMA request arrives, the M5M82C37AP sets HRQ output high and waits until the use of the bus is acknowledged. This state is called so state. The M5M82C37AP repeats S_0 state as long as the HLDA input is low. When HLDA goes to high, the M5M82C37AP begins DMA operation.

Care must be taken became the M5M82C37AP requires at least 1 clock period from the HRQ rising edge to the HLDA rising edge. (I.e. S_0 state must be repeated at least twice.)

In DMA operation, the M5M82C37AP normally executes four (or three) states per one word transfer.

These four states are called S_1, S_2, S_3 and S_4 state in sequence.

In S_1 state, AEN is set to high (if AEN is low), the lower 8 bits of data of the transfer address are output through $A_7 \sim A_0$ and the higher 8 bits of address data are output through $DB_7 \sim DB_0$. The higher address data are output only in the S_1 state, so the strobe pulse for the external address latch circuit is output from ADSTB. The S_1 state is not executed if the higher 8 bits of address data are not changed in demand mode DMA or block mode DMA.

In the S_2 state, $\overline{MEMR}$ or $\overline{IOR}$ output is set to low. If the S_1 state is not executed, address outputs $A_7 \sim A_0$ are changed at the S_2 state also.

In the S_3 state, $\overline{MEMW}$ or $\overline{IOW}$ output goes down to low. The S_4 state is the last state of a word transfer. $\overline{MEMR}$ (or $\overline{IOR}$) and $\overline{IOR}$ (or $\overline{MEMW}$) outputs rise up to high. And the contents of the current address register and the current word counter are updated.

If DMA continues in demand mode or block mode, the S_1 or S_2 state follows after the S_4 state.

If not the S_I state follows after S_4. (In single mode DMA, S_I always follows after S_4.)

When the M5M82C37AP returns to the S_I state, the HRQ and AEN outputs are reset, $A_7 \sim A_4$, $DB_7 \sim DB_0$, $\overline{MEMR}$, $\overline{MEMW}$ are set to high impedance and $A_3 \sim A_0$, $\overline{IOR}$, $\overline{IOW}$ are set to inputs.

If the read or write pulse width is not sufficient for the memories or the peripherals, the transfer time can be extended by setting the READY input to low. Until READY goes up to high, wait states (S_W) are inserted before S_4 and read , write, and address outputs are hold.

The M5M82C37AP has four type of DMA transfers.

- READ TRANSFER
  This is the transfer operation from memories to peripheral. Low-level pulses are output from $\overline{MEMR}$ and $\overline{IOW}$, while $\overline{MEMW}$, $\overline{IOR}$ remain high.
- WRITE TRANSFER
  This is the transfer operation from peripheral to memories. Low-level pulses are output from $\overline{MEMW}$ and $\overline{IOR}$, while $\overline{MEMR}$ and $\overline{IOW}$ remain high .
- VERIFY TRANSFER
  This is the dummy transfer, $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$ and $\overline{IOW}$ all remain high. (not high impedance). Low-level input to READY is ignored. AEN. ADSTB. DACK and address information are normally output.
- MEMORY-TO-MEMORY TRANSFER
  This is the transfer from the memory address designated by channel 0 to the memory address designated by channel 1. In this transfer, the channel 0 address and channel 1 address are alternately output. when the channel 0 address is active, the $\overline{MEMR}$ pulse is output at the same time and the memory data are read and written to the temporary register when the channel 1 address is active, the $\overline{MEMW}$ pulse is output and the contents of the temporary register are output from the data bus.
  Accordingly, ϕ1 byte memory transfer is executed by two operations a read operation which consists of S_{11}, S_{12}, S_{13} and S_{14} states and write operation which consists of S_{21}, S_{22}, S_{23} and S_{24} states).
  In memory to memory DMA, The transfer type assignment of ch 0, ch 1 mode register (read, write or verify) is ignored.

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Notes for memory-to-memory transfer

Observe the following points when programming memory-to-memory DMA.

- The contents of the word count register of channel 0 and 1 must be programmed identically.
- The transfer mode of channel 0 and 1 must be set to the block transfer mode.
- All the mask bits must be set to inhibit external DMA request input. (Memory-to-memory DMA is started by software DMA request to channel 0.)
- In memory-to-memory DMA operation, all the DACK outputs are inactive. (but AEN is set during transfer.)

PRIORITY

Two kinds of DMA priority can be programmed for the M5M82C37AP. (Command register bit 4) If plural channels request DMA at the same time, DMA is acknowledged for the channel which has the highest priority. (Table 1)

(1) Fixed Priority (bit 4=0)
The DMA channel which has the highest priority is channel 0. Channel 1 has the second, channel 2 has the third and channel 3 has the lowest priority.

(2) Rotating Priority (bit 4=1)
This priority mode is that the channel which has serviced the DMA request, has the lowest priority at the next DMA operation. (Just after reset the lowest priority channel is channel 3)
For example, just after channel 1 DMA is executed, channel 2 has the highest priority, channel 3 has the second highest, channel 0 has the third and channel 1 has the lowest priority.

Table 1 DMA priority for the M5M82C37AP

Priority type	DMA channel serviced	DMA priority for next transter			
		Highest	2nd	3rd	Lowest
Fixed priority	————	ch0	ch1	ch2	ch3
Rotating priority	ch0	ch1	ch2	ch3	ch0
	ch1	ch2	ch3	ch0	ch1
	ch2	ch3	ch0	ch1	ch2
	ch3	ch0	ch1	ch2	ch3

Description Of The Transfer Mode

The following is the description of the transfer mode of the M5M82C37AP

(1) Single mode DMA transfer

In single mode DMA, the M5M82C37AP executes only one word transfer when the bus control is acknowledged by the CPU, and when the S_4 state is ended, the M5M82C37AP reset HRQ output and releases the bus.

If the DMA request input continues at active level, at least one S_I state is executed since the HLDA input falls down to low, and HRQ is kept low. Accordingly, 8085 CPU etc. can execute at least one instruction between DMA transfer.

(2) Block mode DMA transfer

In the block mode, once the DMA request is acknowledged, the DMA is executed continuously until the terminal count (TC) occurs.

TC means that

(i)The contents of the current word count register are about to be counted down from 0000_{16} to $FFFF_{16}$

or that

(ii)an external $\overline{EOP}$ pulse is input before the S_2 state.

The DREQ input should be kept active until the DACK output is made active, but once DMA is acknowledged, DMA transfer continues until TC occurs even when DMA request becomes inactive.

When DMA is executed continuously, the S_1 or S_2 state follows directly after S_4. If the contents of the higher 8 bits of the address are not changed at the following word transfer, the S_1 state is skipped and the S_2 state is executed just after S_4.

(3) Demand mode DMA transfer

In the demand mode, DMA is executed continuously while the DMA request is active.

Once the DMA is acknowledged to the channel which is programmed for the demand mode, DMA operation is executed continuously until TC occurs or the DMA request becomes inactive.

If DMA stops due to an inactive DREQ before TC, the rest of the DMA will be resumed when DREQ becomes active and the DMA is acknowledged again.

The operation during DMA is almost the same as in the block mode DMA.

(4) Cascade mode DMA transfer

This mode is used for DMA channel expansion by cascade connction when more than 4 channels are required. (See fig. 1)

If the DMA request for the channel which is programmed in the cascade mode occurs and the request is acknowledged, only the DACK output becomes active. ($\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$, $\overline{MEMW}$, $DB_7 \sim DB_0$, $A_7 \sim A_0$ become floating. AEN, ADSTB outputs stay at low. $\overline{CS}$ and READY inputs are ignored.)

Accordingly the cascade mode DMA operation of the M5M82C37AP is only that it requests a bus hold request for the CPU instead of the low-level M5M82C37AP and transmits the bus acknowledgement signal by setting DACK active.

Note :

- The contents of the base and current address/word count regsiters of channels programmed in the cascade mode are invalid and change unpredictably.
- A software DMA request for the channel which is programmed in cascade mode may cause the system of hangup.
- When cascaded M5M82C37AP's are connected as shown in fig. 1, the high level M5M82C37AP should be initialized first and the DACK output set 'high active' in order to initialize the low level M5M82C37AP's because the registers of the M5M82C37AP cannot be read or written when HLDA input is high.
- An external $\overline{EOP}$ cannot terminate cascade mode DMA operation.

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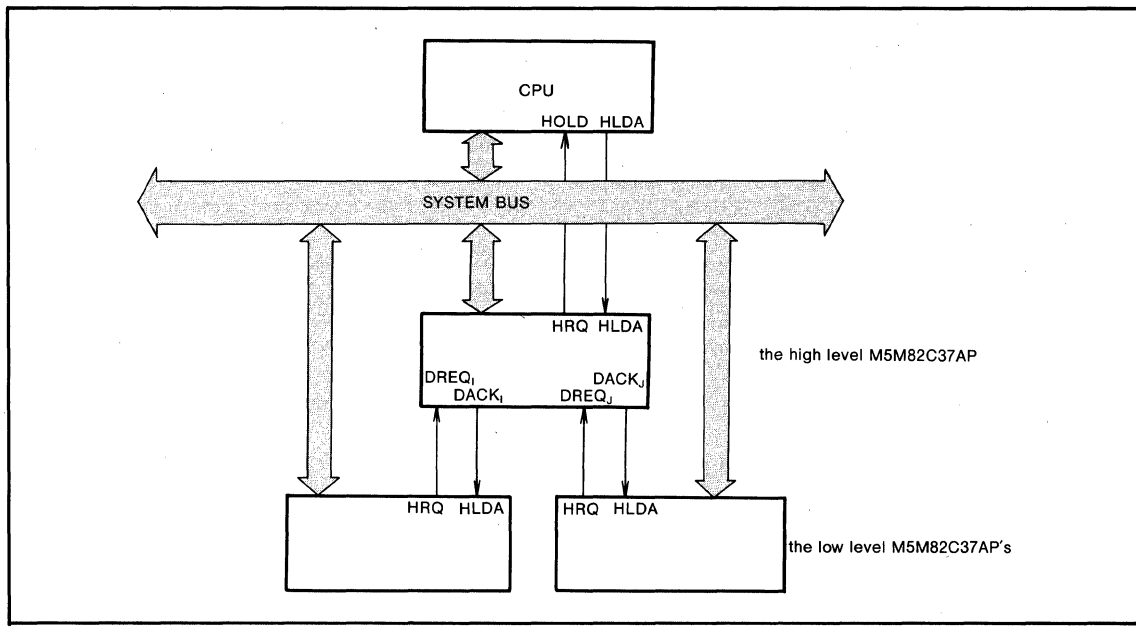

Fig.1 Example of a DMA system using a cascade connection

(5) Auto initialization feature (mode regsiter bit 4=1)
When bit 4 of the mode register is set to '1', the programmed channel enters the auto initialization mode. Auto initialization is performed when TC occurs and the contents of the base address/word count registers are loaded in the current address/word count registers. (The contents of the base address/word count registers are programmed to the same value as the current registers, at the same time.)

Note : If a channel is programmed for auto initialization the mask register bit for that channel is not set after TC. If it is not programmed for auto initialization, the mask register bit is set after TC, so the mask register bit must be reset to set this channel to DMA-enable.

(6) Extended write feafure (command register bit 5=1)
In normal DMA operation, the write pulse $\overline{MEMW}$ (or $\overline{IOW}$) falls down to low in the S_3 state. But, if extended write is programmed, the write pulse falls at the S_2 state and the width can be extended for one clock period.

(7) Compressed timing DMA feafure (command regsiter bit 3=1)
In normal DMA, the transfer for one word consists of three or four states.
If the compressed timing DMA is programmed, the S_3 state is not executed and the one word transfer consists of two or three states. In this mode, the write output ($\overline{IOW}$, $\overline{MEMW}$) falls to low in the S2 state as well as the read output ($\overline{IOR}$, $\overline{MEMR}$) . In memory-to-memory DMA operation, the compressed timing assignment is ignored.

REGISTERS

The following is a description of the registers of M5M82C37AP.

(1) Address registers
The M5M82C37AP has two 16-bit address registers for each DMA channel.
One is called the current address register. It holds the contents of the memory address at which DMA operation is performed and the contents are incremented (or decremented) at every word transfer. This register is read/write enabled when in the incative state. The other is the base address register. This register is a write-only register and is written at the same time the current address register is programmed. The contents of the base address register are loaded into the current address register when the channel has reached TC if the channel is programmed in the auto initialize mode.
The registers of the M5M82C37AP are read or written through an 8-bit data bus so the address register must be accessed twice, first the lower 8 bits, second the higher 8 bits. The M5M82C37AP has a first/last flip-flop which is toggled when the 16-bit regsiter is accessed. It selects the lower or higher byte.

(2) Word count registers
The M5M82C37AP has two 16-bit word count registers for each DMA channel.
One is called the current word count register. It holds the number of DMA transfer words, and the contents are decremented at the end of every word transfer. TC occurs when the contents of the word counter about to

decrement from 0000_{16} to $FFFF_{16}$.
The other is the base word counter, a write only register that is used for auto initialization like the base address register.
The read/write operation for the word count register is the same as for the address registers.

(3) Mode registers
The M5M82C37AP has four 6-bit length registers to select the DMA modes and types for the 4 DMA channels. They are write only registers.
To program one of these registers, the channel selection is done by the 2 LSBs of the written data allowing all four registers to assigned at the same address. The other 6 bits are written to one of the four registers. The bit assignment is shown in figure 2.

(4) Command register
This register is an 8-bit write only register used to define common operations for the four DMA channels. The bit assignment is shown in figure 3.
Command regsiter is set 00_{16} by reset.

(5) Mask register
This register is a 4-bit register with one mask bit for each DMA channel.
The four bits of this regsiter can be programmed simultaneously (fig. 4) or can be set or reset 1 bit at a time (fig. 5). All bits can be cleared by the clear mask register command.
After reset, the 4 mask bits are all set to '1'.

(6) Request register
This register is 4-bit register with one software request bit for each DMA channel.
One request bit can be set or reset at a time. (fig. 6)

Note : All the request bits are reset after the DMA operation of one channel. So, when the DMA is started by software request, other external DMA requests must be masked by setting all the mask register bits. (Software requests are not masked by the mask register.) All the request bits are set to '0' after reset.

(7) Status register
This register is an 8-bit read only register. The 4 MSBs show the status of the four DREQs. '1' means that the DREQ input is active.
The other four bits are the TC bits which are set to '1' when TC occurs. The lower 4 bits are reset after the status registers are read or after reset.
The relation between these bits and the channels is shown in fig. 7

(8) Temporary Register
This register is an 8-bit read only register.
It is used to store temporary data read during the first part of the memory-to-memory DMA operation.
When the CPU reads this register, the register contents are the data which were transfered in memory-to-memory transfer DMA immediately prior to the CPU read.

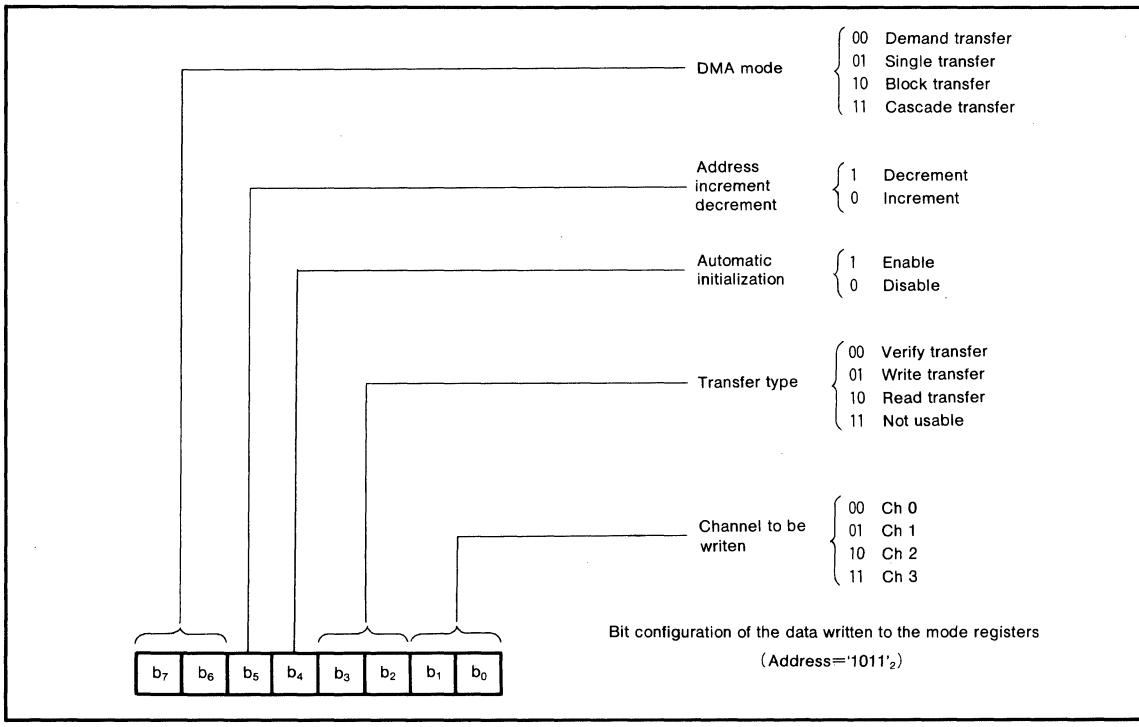

Fig.2 Mode registers

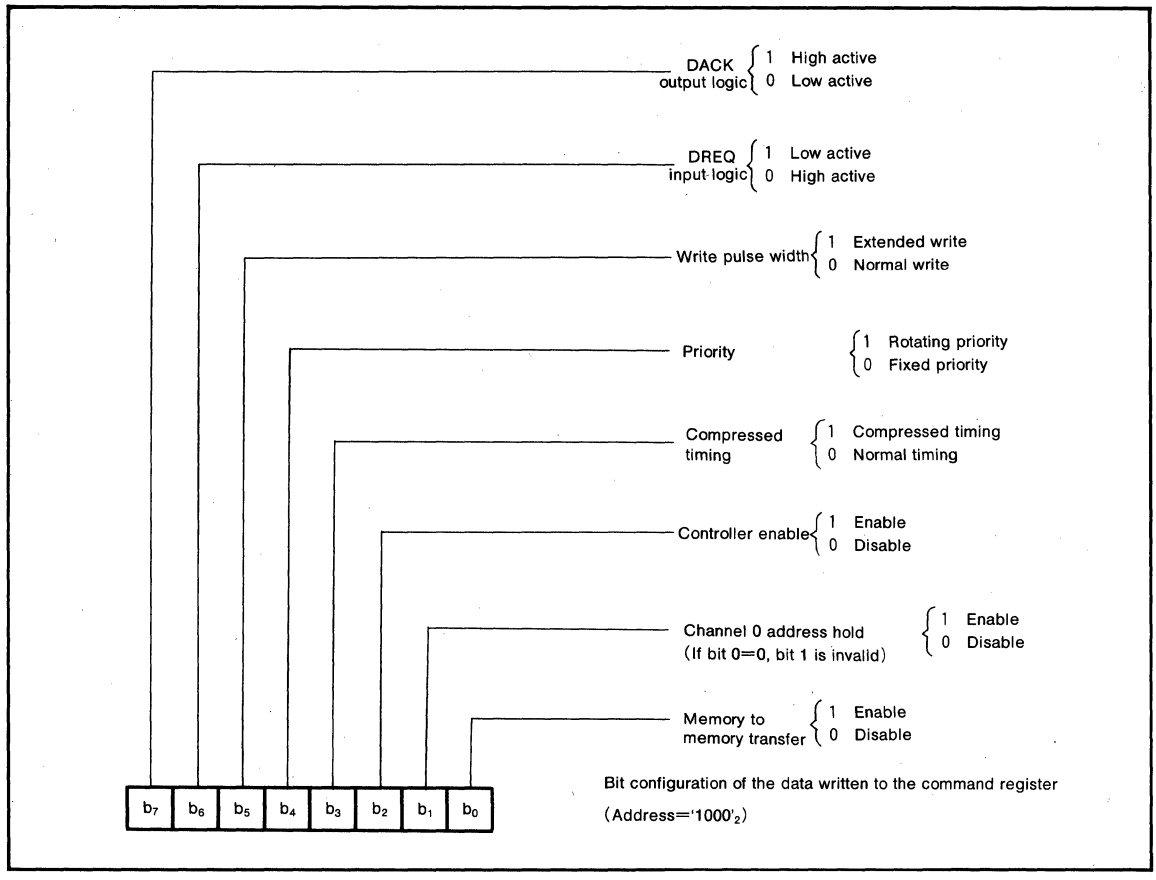

Fig.3 Command register

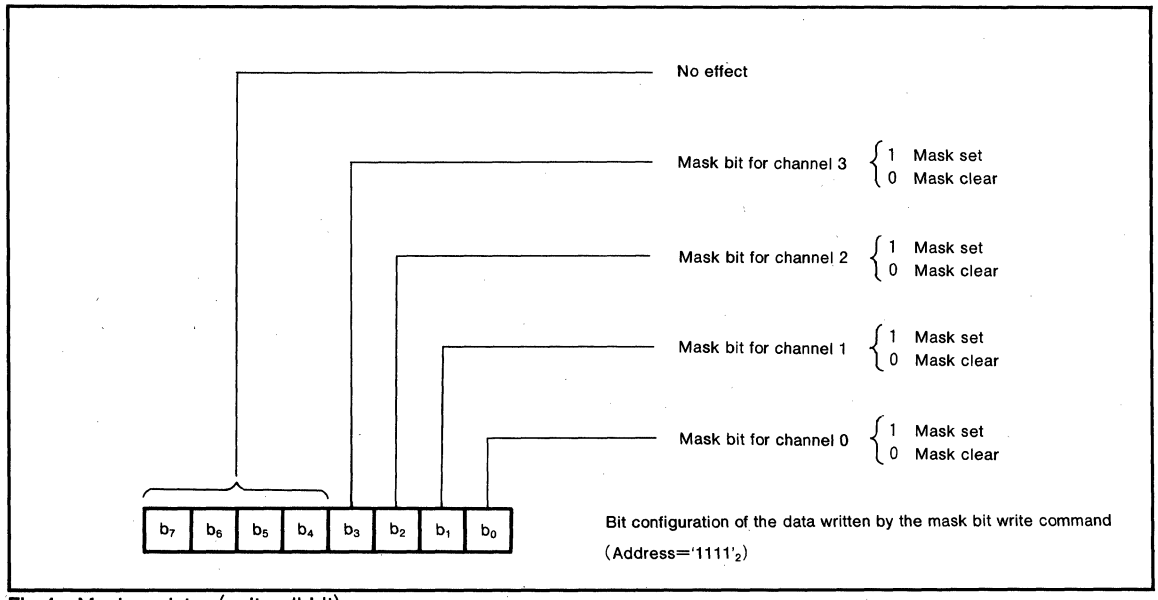

Fig.4 Mask register (write all bit)

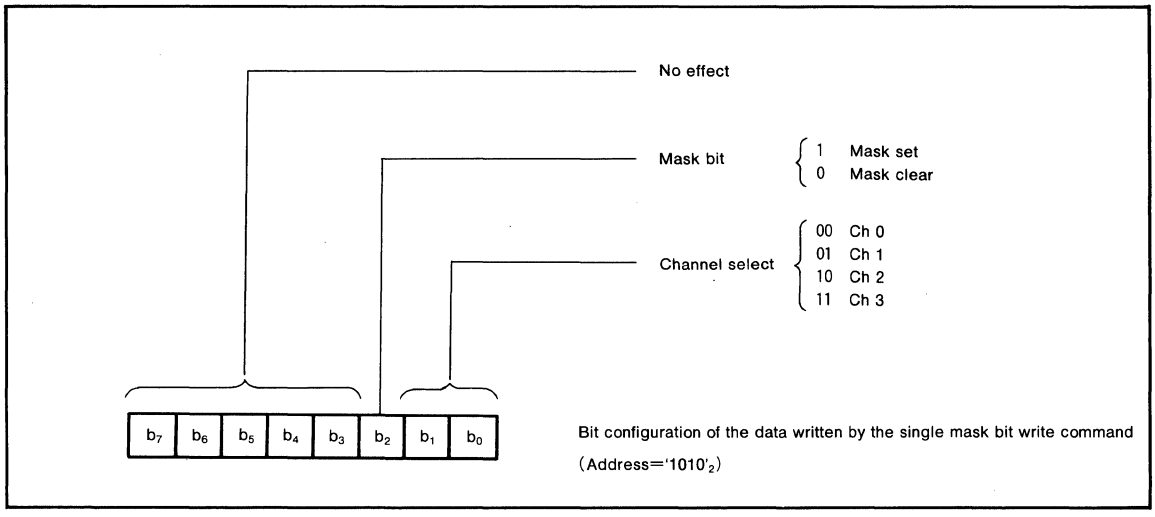

Fig.5 Mask register (write single bit)

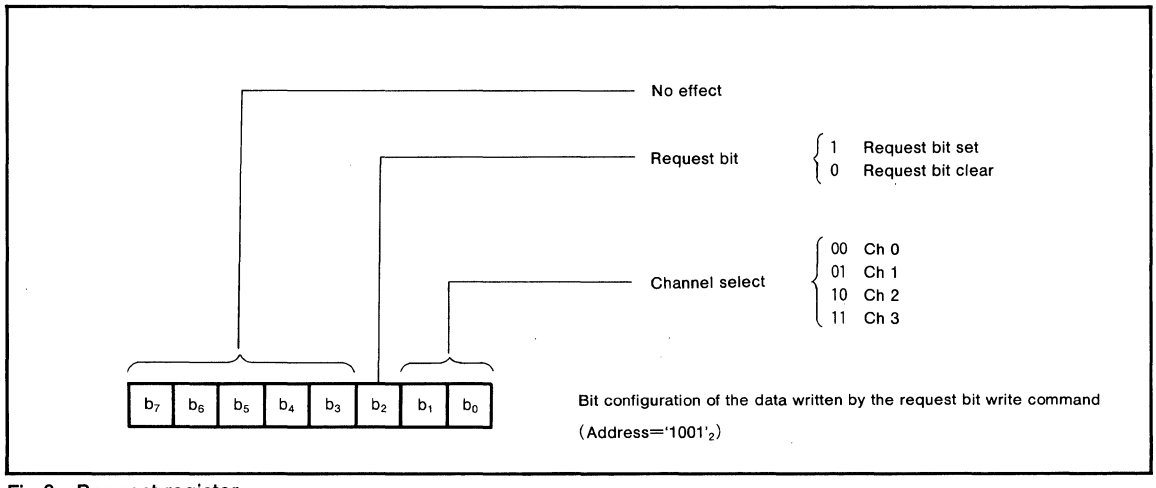

Fig.6 Request register

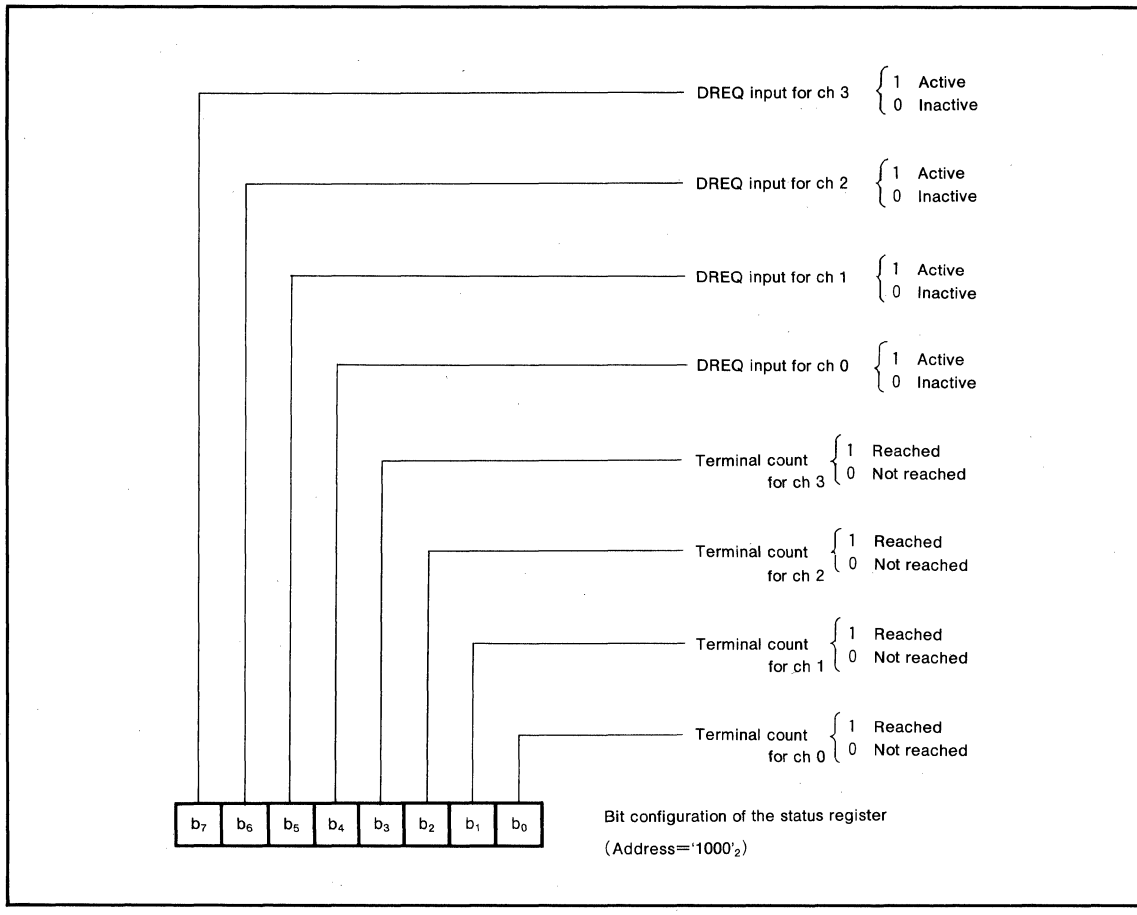

Fig.7 Status register

PROGRAMMING

The registers in the M5M82C37AP can be read or written when $\overline{CS}$ and HLDA inputs are low.

The address assignment is shown in fig. 8 and 9. Some of the write operations in these figures do not, in fact, write in any registers. They are called software commands. The following is a description of the software commands.

Clear first/last F/F

In reading or writing a 16-bit register, the higher and lower 8 bits are accessed separately. Selection is done by a first/last flip-flop which toggles when ever one of the 16-bit registers is accessed. This command clears the first/last flip-flop, so after this command is executed, the next accerss of the 16-bit register is begins at the lower 8 bits.

Master clear

This command executes a software reset.

Note : The following are the effects of the software reset for the M5M82C37AP.

- Mask bits are set for all the DMA channels.
- The command register is cleared to '00_{16}'. (Note that bit 2 is '0'.)
- The temporary register is cleared.
- The 4 TC bits of the status register are cleared.
- The first/last flip flop is reset.
- Software DMA request bits are cleared.

(When the hardware reset is performed, together with the above effects, DMA operation is terminated and the M5M82C37AP returns to the S_I state.)

Clear mask register

This command clears all the mask bits and enable DMA for all the channels.

Table 2 Read operation with the M5M82C37AP

A_3	A_2	A_1	A_0	$\overline{CS}$	HLDA	$\overline{RD}$	First Last F/F	REGISTER READ
0	0	0	0	0	0	0	0	CH0 Current address register bit7~bit0
0	0	0	0	0	0	0	1	CH0 Current address register bit15~bit8
0	0	0	1	0	0	0	0	CH0 Current word count register bit7~bit0
0	0	0	1	0	0	0	1	CH0 Current word count register bit15~bit8
0	0	1	0	0	0	0	0	CH1 Current address register bit7~bit0
0	0	1	0	0	0	0	1	CH1 Current address register bit15~bit8
0	0	1	1	0	0	0	0	CH1 Current word count register bit7~bit0
0	0	1	1	0	0	0	1	CH1 Current word count register bit15~bit8
0	1	0	0	0	0	0	0	CH2 Current address register bit7~bit0
0	1	0	0	0	0	0	1	CH2 Current address register bit15~bit8
0	1	0	1	0	0	0	0	CH2 Current word count register bit7~bit0
0	1	0	1	0	0	0	1	CH2 Current word count register bit15~bit8
0	1	1	0	0	0	0	0	CH3 Current address register bit7~bit0
0	1	1	0	0	0	0	1	CH3 Current address register bit15~bit8
0	1	1	1	0	0	0	0	CH3 Current word count register bit7~bit0
0	1	1	1	0	0	0	1	CH3 Current word count register bit15~bit8
1	0	0	0	0	0	0	X	Status register
1	0	0	1	0	0	0	X	Invalid
1	0	1	0	0	0	0	X	Invalid
1	0	1	1	0	0	0	X	Invalid
1	1	0	0	0	0	0	X	Invalid
1	1	0	1	0	0	0	X	Temporary register
1	1	1	0	0	0	0	X	Invalid
1	1	1	1	0	0	0	X	Invalid
X	X	X	X	1	X	X	X	Read operation is not executed.
X	X	X	X	X	1	X	X	Read operation is not executed.

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Table 3 Write operation with the M5M82C37AP

A_3	A_2	A_1	A_0	$\overline{CS}$	HLDA	$\overline{WR}$	First Last F/F	REGISTER WRITTEN
0	0	0	0	0	0	0	0	CH0 base and current address register bit7~bit0
0	0	0	0	0	0	0	1	CH0 base and current address register bit15~bit8
0	0	0	1	0	0	0	0	CH0 base and current word count register bit7~bit0
0	0	0	1	0	0	0	1	CH0 base and current word count register bit15~bit8
0	0	1	0	0	0	0	0	CH1 base and current address register bit7~bit0
0	0	1	0	0	0	0	1	CH1 base and current address register bit15~bit8
0	0	1	1	0	0	0	0	CH1 base and current word count register bit7~bit0
0	0	1	1	0	0	0	1	CH1 base and current word count register bit15~bit8
0	1	0	0	0	0	0	0	CH2 base and current address register bit7~bit0
0	1	0	0	0	0	0	1	CH2 base and current address register bit15~bit8
0	1	0	1	0	0	0	0	CH2 base and current word count register bit7~bit0
0	1	0	1	0	0	0	1	CH2 base and current word count register bit15~bit8
0	1	1	0	0	0	0	0	CH3 base and current address register bit7~bit0
0	1	1	0	0	0	0	1	CH3 base and current address register bit15~bit8
0	1	1	1	0	0	0	0	CH3 base and current word count register bit7~bit0
0	1	1	1	0	0	0	1	CH3 base and current word count register bit15~bit8
1	0	0	0	0	0	0	X	Command register
1	0	0	1	0	0	0	X	Request register
1	0	1	0	0	0	0	X	Single mask bit write
1	0	1	1	0	0	0	X	Mode register
1	1	0	0	0	0	0	X	Clear first/last flip-flop software commands
1	1	0	1	0	0	0	X	Master clear software commands
1	1	1	0	0	0	0	X	Clear all mask register bits software commands
1	1	1	1	0	0	0	X	Write all mask bits software commands
X	X	X	X	1	X	X	X	Write is not executed.
X	X	X	X	X	1	X	X	Write is not executed.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.3∼7	V
V_I	Input voltage		−0.3∼V_{CC}+0.3	V
V_O	Output voltage		−0.3∼V_{CC}+0.3	V
T_{opr}	Operating free-air temperature range		−20∼75	℃
T_{stg}	Storage temperature		−65∼150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage(GND)		0		V

ELECTRICAL CHARCTERISTICS (T_a=−20∼75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	Hign-level input voltage		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−200μA	2.4			V
		I_{OH}=−100μA(HRQ only)	3.2			V
V_{OL}	Low-level output voltage	I_{OL}=2.0mA(data bus) I_{OL}=3.2mA(other outputs)			0.45	V
I_I	Input current	V_I=0∼V_{CC}	−10		+10	μA
I_{OZ}	Off-state output current	V_I=0∼V_{CC}	−10		+10	μA
I_{CC}	Supply current	V_{IH}=V_{CC}, V_{IL}=V_{SS}, f_{CLK}=1/$t_C(\phi)$min.			15	mA

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TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

(i) SLAVE MODE

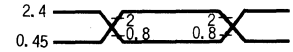
Symbol	Parameter	Alternate symbol	Limits						Unit
			M5M82C37AP		M5M82C37AP-4		M5M82C37AP-5		
			Min	Max	Min	Max	Min	Max	
$t_{su(CS-R)}$ $t_{su(A-R)}$	Address setup time before read	T_{AR}	50		50		50 [0]		ns
$t_{su(CS-W)}$	$\overline{CS}$ setup time before write	T_{CW}	200		150		150		ns
$t_{su(A-W)}$	Address setup time before write	T_{AW}	200		150		150		ns
$t_{su(DQ-W)}$	Data setup time before write	T_{DW}	200		150		100		ns
$t_{h(R-CS)}$ $t_{h(R-A)}$	Address hold time after read	T_{RA}	0		0		0		ns
$t_{h(W-CS)}$	$\overline{CS}$ hold time after write	T_{WC}	20		20		20 [0]		ns
$t_{h(W-A)}$	Address hold after write	T_{WA}	20		20		20 [0]		ns
$t_{h(W-DQ)}$	Data hold after write	T_{WD}	30		30		30 [0]		ns
$t_{w(R)}$	Read pulse width	T_{RW}	300		250		200		ns
$t_{w(W)}$	Write pulse width	T_{WWS}	200		200		160		ns
$t_{w(RESET)}$	Reset pulse width	T_{RSTW}	300		300		300		ns
$t_{su(VCC-RESET)}$	V_{CC} setup time before to reset	T_{RSTD}	500		500		500		ns
$t_{su(RESET-R)}$ $t_{su(RESET-W)}$	Reset setup time before read Reset setup time before Write	T_{RSTS}	$2t_{C(\phi)}$		$2t_{C(\phi)}$		$2t_{C(\phi)}$		ns

(ii) DMA MODE

Symbol	Parameter	Alternate symbol	Limits						Unit
			M5M82C37AP		M5M82C37AP-4		M5M82C37AP-5		
			Min	Max	Min	Max	Min	Max	
$t_{w(\phi)}$	Clock high-level pulse width	T_{CH}	120		100		80		ns
$t_{w(\overline{\phi})}$	Clock low-level pulse width	T_{CL}	150		110		68		ns
$t_{C(\phi)}$	Clock period	T_{CY}	320		250		200		ns
$t_{su(EOP-\phi)}$	External $\overline{EOP}$ setup time before clock	T_{EPS}	60		45		40		ns
$t_{w(EOP)}$	External $\overline{EOP}$ pulse width	T_{EPW}	300		225		220		ns
$t_{su(DREQ-\phi)}$	DREQ setup time before clock	T_{QS}	0		0		0		ns
$t_{su(READY-\phi)}$	READY setup time before clock	T_{RS}	100		60		60		ns
$t_{h(\phi-READY)}$	READY hold time before clock	T_{RH}	20		20		20		ns
$t_{su(HLDA-\phi)}$	HLDA setup time before clock	T_{HS}	100		75		75		ns
$t_{su(DQ-MEMR)}$	Data setup time before $\overline{MEMR}$	T_{IDS}	250		190		170		ns
$t_{h(MEMR-DQ)}$	Data hold time after $\overline{MEMR}$	T_{IDH}	0		0		0		ns

Note : A.C Testing waveform

Input pulse level	0.45~2.4V
Input pulse rise time	10ns
Input pulse fall time	10ns
Reference level input	V_{IH}=2V, V_{IL}=0.8V
Output	V_{OH}=2V, V_{OL}=0.8V



SWITCHING CHARACTERISTIC (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

(i) SLAVE MODE

Symbol	Parameter	Alternate symbol	Limits						Unit
			M5M82C37AP		M5M82C37AP-4		M5M82C37AP-5		
			Min	Max	Min	Max	Min	Max	
$t_{PZV(R-DQ)}$	Data enable time after read	T_{RDE}		200		200		140	ns
$t_{PVZ(R-DQ)}$	Data disable time after read	T_{RDF}	0	100	0	100	0	70	ns

(ii) DMA MODE

Symbol	Parameter	Alternate symbol		Limits						Unit
				M5M82C37AP		M5M82C37AP-4		M5M82C37AP-5		
				Min	Max	Min	Max	Min	Max	
$t_{PLH(\phi-AEN)}$	Propagation time from clock to AEN	T_{AEL}			300		225		200	ns
$t_{PHL(\phi-AEN)}$	Propagation time from clock to AEN	T_{AET}			200		150		130	ns
$t_{PZV(\phi-A)}$	Propagation time from clock to address active	T_{FAAB}			250		190		170	ns
$t_{PHL(\phi-A)}$	Propagation time from clock to address stable	T_{ASM}			250		190		170	ns
$t_{PVZ(\phi-A)}$	Propagation time from clock to address floating	T_{AFAB}			150		120		90	ns
$t_{PZV(\phi-DQ)}$	Propagation time from clock to data bus	T_{FADB}			300		225		200	ns
$t_{PVZ(\phi-DQ)}$	Propagation time from clock to data bus	T_{AFDB}			250		190		170	ns
$t_{PLH(\phi-ADSTB)}$	Propagation time from clock to ADSTB	T_{STL}			200		150		130	ns
$t_{PHL(\phi-ADSTB)}$	Propagation time from clock to ADSTB	T_{STT}			140		110		90	ns
$t_{su(DB-ADSTB)}$	Data output setup time before ADSTB	T_{ASS}		100		100		100		ns
$t_{h(ADSTB-DQ)}$	Data output hold time before ADSTB	T_{AHS}		50		40		30		ns
$t_{PZV(\phi-R)}$ $t_{PZV(\phi-W)}$	Propagation time from clock to read or write active	T_{FAC}			200		150		150	ns
$t_{PHL(\phi-R)}$ $t_{PHL(\phi-W)}$	Propagation time from clock to read or write	T_{DCL}			270		200		190	ns
$t_{PLH(\phi-R)}$	Propagation time from clock to read	T_{DCTR}			270		210		190	ns
$t_{PLH(\phi-W)}$	Propagation time from clock to write	T_{DCTW}			200		150		130	ns
$t_{PVZ(\phi-R)}$ $t_{PVZ(\phi-W)}$	Propagation time from clock to read or write floating	T_{AFC}			150		120		120	ns
$t_{h(R-A)}$	Address output hold time after read	T_{AHR}		$t_{C(\phi)}-100$		$t_{C(\phi)}-100$		$t_{C(\phi)}-100$		ns
$t_{h(W-A)}$	Address output hold time after write	T_{AHW}		$t_{C(\phi)}-50$		$t_{C(\phi)}-50$		$t_{C(\phi)}-50$		ns
$t_{su(DQ-MEMW)}$	Data output setup time before $\overline{MEMW}$	T_{ODV}		200		125		125		ns
$t_{h(MEMW-DQ)}$	Data output hold time after $\overline{MEMW}$	T_{ODH}		20		20		10		ns
$t_{PLH(\phi-DACK)}$	Propagation time from clock to $\overline{DACK}$	T_{AK}			250		220		170	ns
$t_{PHL(\phi-EOP)}$	Propagation time from clock to $\overline{EOP}$	T_{AK}			250		190		170	ns
$t_{PLH(\phi-EOP)}$	Propagation time from clock to $\overline{EOP}$	T_{AK}			250		190		170	ns
$t_{PLH(\phi-HRQ)}$ $t_{PHL(\phi-HRQ)}$	Propagation time from clock to HRQ	T_{DQ}	"H"2.0V		160		120		120	ns
			"H"3.3V		250		190		120	

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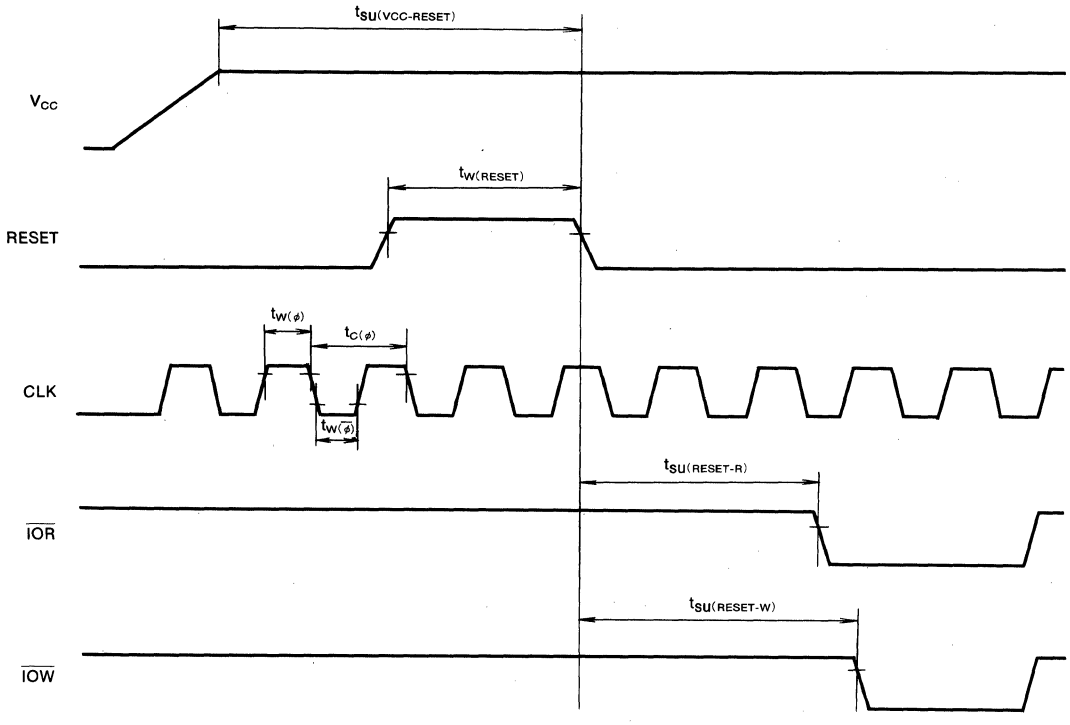
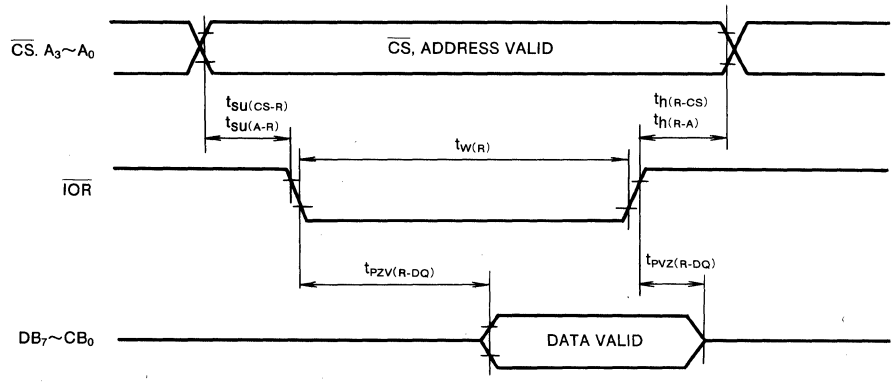
TIMING DIAGRAMS

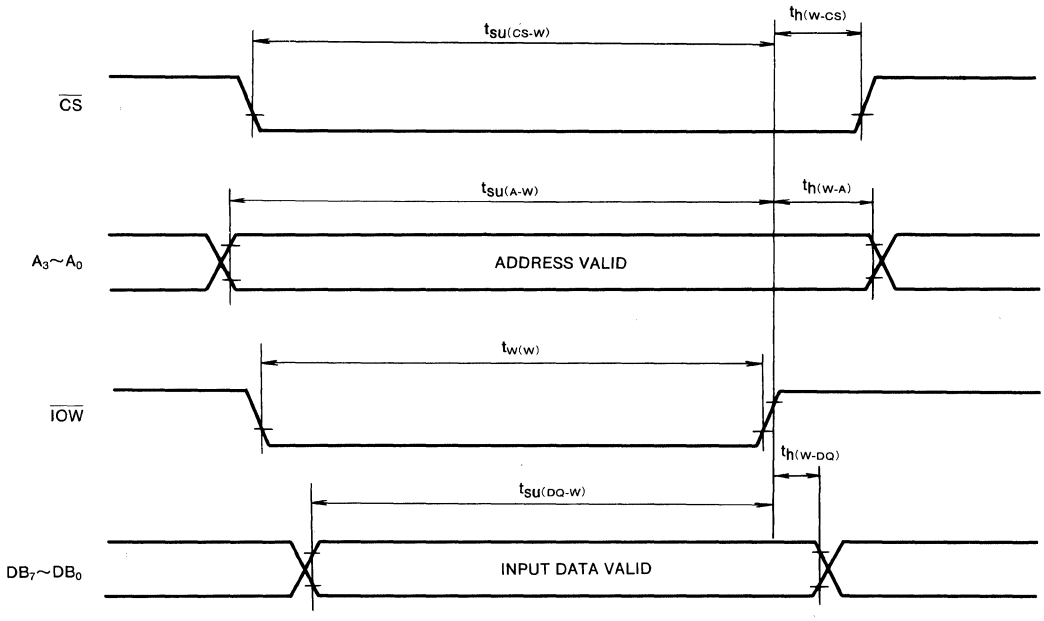
Reset timing



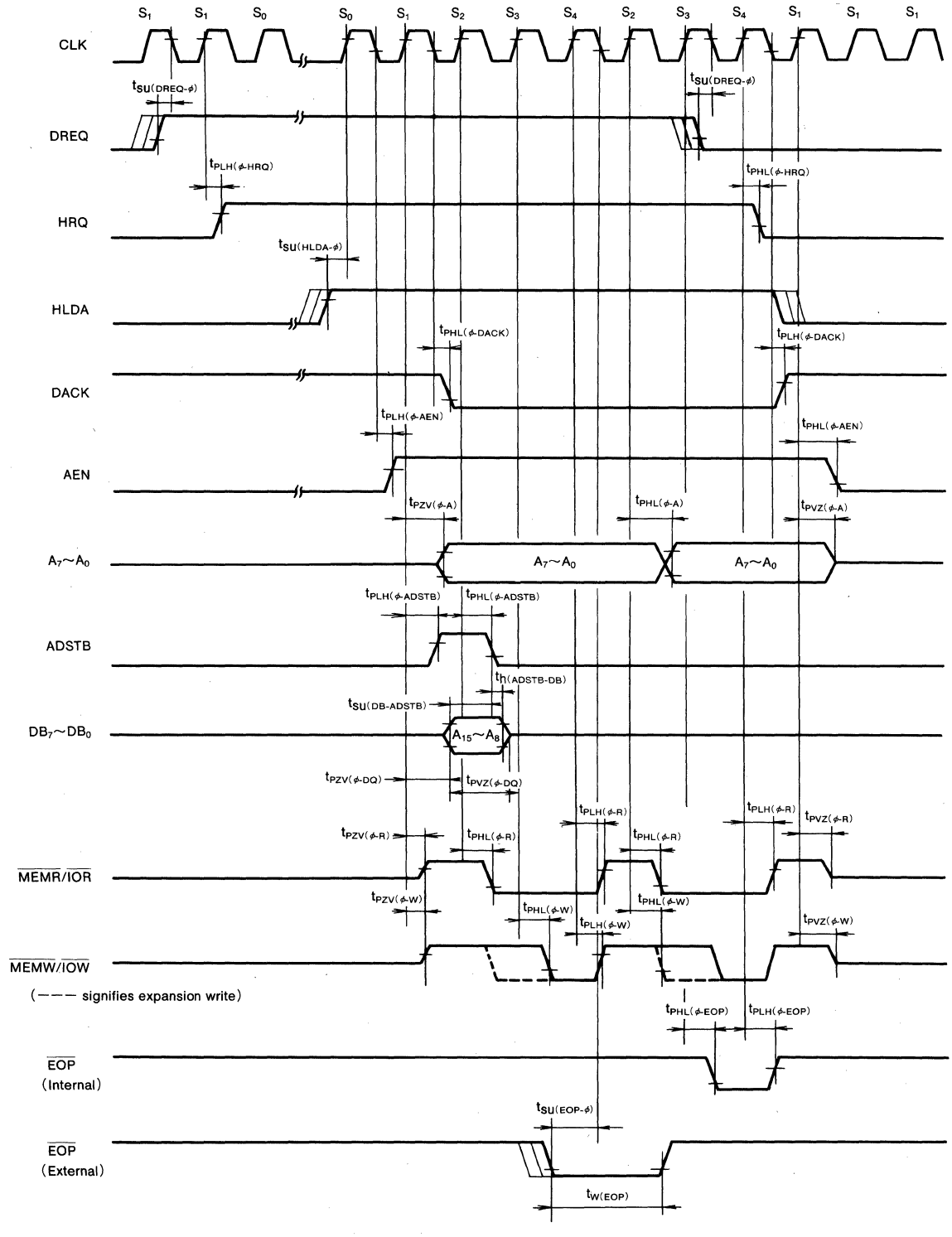
Slave mode timing (READ)



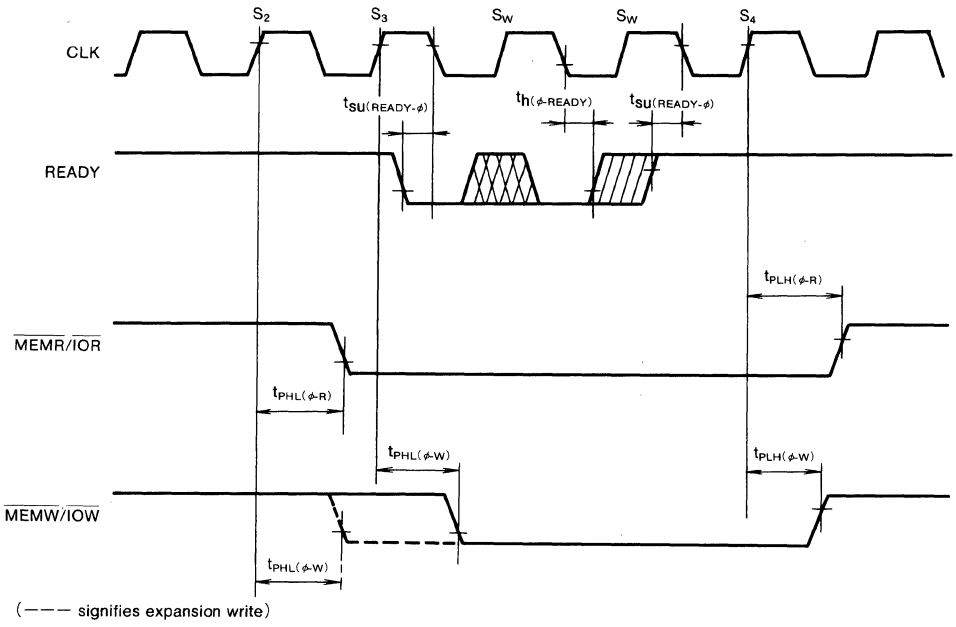
Slave mode timing (WRITE)



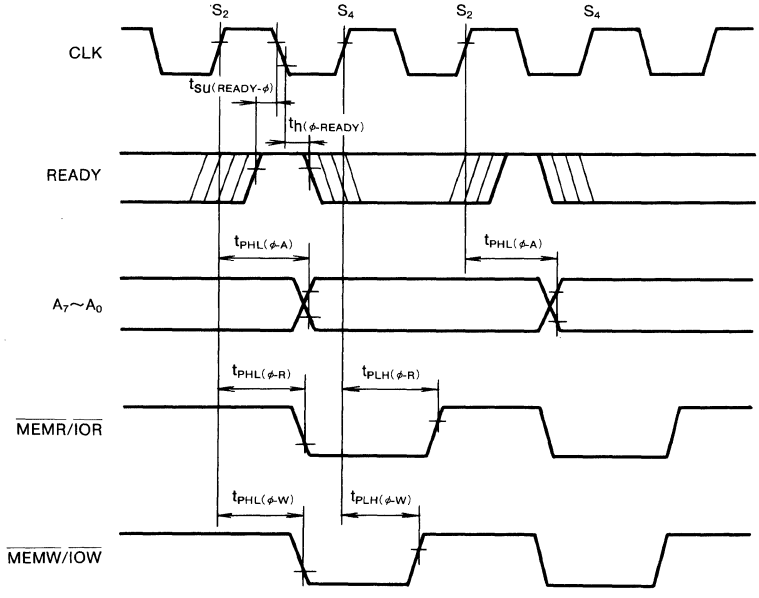
DMA transmit timing



READY input timing



(——— signifies expansion write)



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Inter-memory transmission