PRELIMINARY
Notice: This is not a final specification. Some parametric limits are Subject to change.

M5M82C37AFP,-4,-5

CMOS PROGRAMMABLE DMA CONTROLLER

DESCRIPTION

The M5M82C37AFP is a programmable 4-channel DMA (Direct Memory Access) controller. This device is specially designed to simplify data transfer at high trasfer rate for microcomputer systems.

Fabricated using the silicon-gate CMOS technology, the M5M82C37AFP operates using a single 5V power supply.

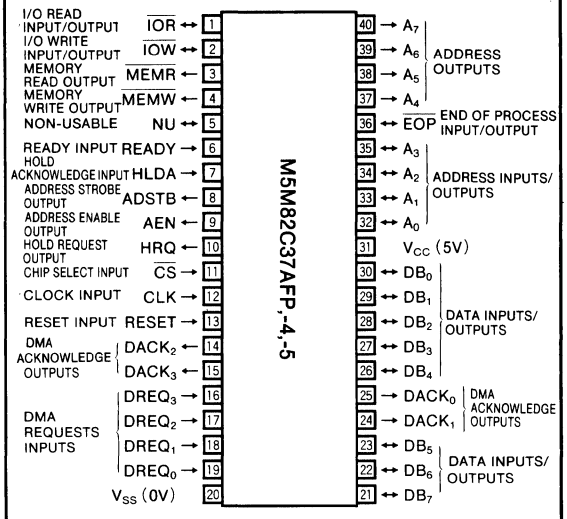
FEATURES

- 5V single supply, single TTL clock
- Four channel DMA controls with priority DMA request acknowledge functions
- DMA enable/disable, automatic initialization enable/disable, address increment/decrement programmability for each cannel
- Programmable DREQ input and DACK output logic polarity
- Direct connecting permits easy DMA channel expansion.
- Memory to memory data transfer
- EOP input/output permits DMA operation completion check as well as forcibly completing DMA operation.

APPLICATION

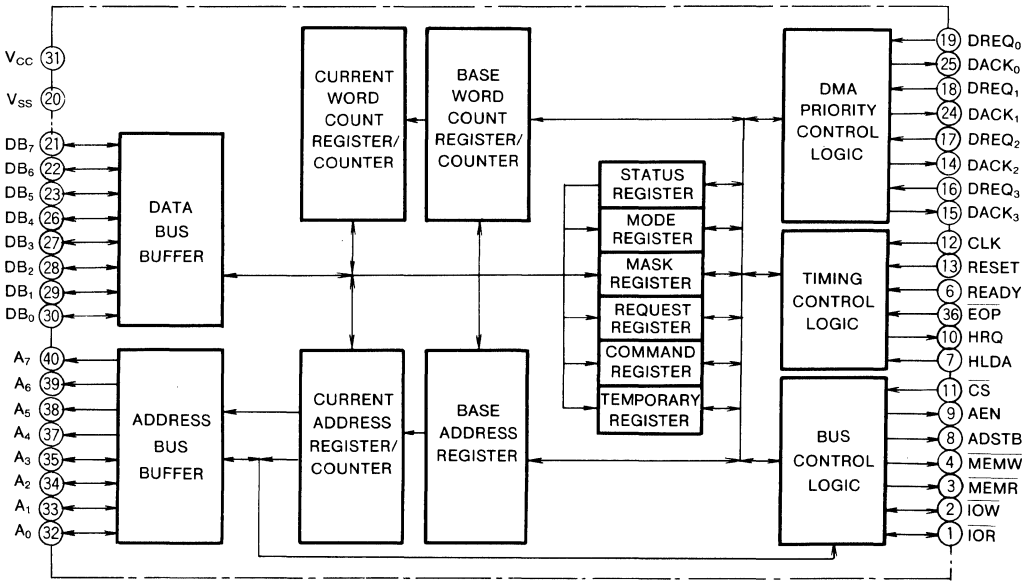
- DMA control of peripheral equipment such as floppy diskettes and CRT terminals that require high-speed data transfer.

PIN CONFIGURATION (TOP VIEW)



Outline 40P2R

BLOCK DIAGRAM



FUNCTION

M5M82C37AFP is a programmable DMA controller LSI used in microprocessor systems.

This device basically consists of a DMA request control block for acknowledging DMA requests, a CPU interface for exchanging data and commands with the CPU, a timing control circuit for controlling each of the various types of timing, and a register for holding and counting DMA addresses and number of transfer words.

After setting the transfer mode, starting address, and byte number in each of the registers and when a DMA request is made to an unmasked channel, the M5M82C37AFP requires use of the bus to the CPU. When the HLDA signal is received from the CPU, the DMA acknowledge signal is sent to DMA requesting channel with the highest priority and begins DMA operation.

During DMA operation, the contents of the low-byte of the transfer memory address are output through $A_7 \sim A_0$. Every time a change in the high-order 8-bit values is necessitated immediately after DMA operation has begun or due to borrowing or decrement during DMA operation, the change is output via pins $DB_7 \sim DB_0$ to the externally mounted latch circuit. After the address is transmitted, read and write signals are sent to the memories and peripherals activating DMA transfer.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.3∼7	V
V_I	Input voltage		−0.3∼V_{CC}+0.3	V
V_O	Output voltage		−0.3∼V_{CC}+0.3	V
T_{opr}	Operating free-air temperature range		−20∼75	℃
T_{stg}	Storage temperature		−65∼150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage(GND)		0		V

ELECTRICAL CHARCTERISTICS (T_a=−20∼75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	Hign-level input voltage		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−200μA	2.4			V
		I_{OH}=−100μA(HRQ only)	3.2			V
V_{OL}	Low-level output voltage	I_{OL}=2.0mA(data bus) I_{OL}=3.2mA(other outputs)			0.45	V
I_I	Input current	V_I=0∼V_{CC}	−10		+10	μA
I_{OZ}	Off-state output current	V_I=0∼V_{CC}	−10		+10	μA
I_{CC}	Supply current	V_{IH}=V_{CC}, V_{IL}=V_{SS}, f_{CLK}=1/$t_C(\phi)$min.			15	mA

TIMING REQUIREMENTS (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

(i) SLAVE MODE

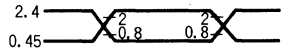
Symbol	Parameter	Alternate symbol	Limits						Unit
			M5M82C37AFP		M5M82C37AFP-4		M5M82C37AFP-5		
			Min	Max	Min	Max	Min	Max	
$t_{su(CS-R)}$ $t_{su(A-R)}$	Address setup time before read	T_{AR}	50		50		50〔0〕		ns
$t_{su(CS-W)}$	$\overline{CS}$ setup time before write	T_{CW}	200		150		150		ns
$t_{su(A-W)}$	Address setup time before write	T_{AW}	200		150		150		ns
$t_{su(DQ-W)}$	Data setup time before write	T_{DW}	200		150		100		ns
$t_{h(R-CS)}$ $t_{h(R-A)}$	Address hold time after read	T_{RA}	0		0		0		ns
$t_{h(W-CS)}$	$\overline{CS}$ hold time after write	T_{WC}	20		20		20〔0〕		ns
$t_{h(W-A)}$	Address hold after write	T_{WA}	20		20		20〔0〕		ns
$t_{h(W-DQ)}$	Data hold after write	T_{WD}	30		30		30〔0〕		ns
$t_{w(R)}$	Read pulse width	T_{RW}	300		250		200		ns
$t_{w(W)}$	Write pulse width	T_{WWS}	200		200		160		ns
$t_{w(RESET)}$	Reset pulse width	T_{RSTW}	300		300		300		ns
$t_{su(VCC-RESET)}$	V_{CC} setup time before to reset	T_{RSTD}	500		500		500		ns
$t_{su(RESET-R)}$ $t_{su(RESET-W)}$	Reset setup time before read Reset setup time before Write	T_{RSTS}	$2t_{C(\phi)}$		$2t_{C(\phi)}$		$2t_{C(\phi)}$		ns

(ii) DMA MODE

Symbol	Parameter	Alternate symbol	Limits						Unit
			M5M82C37AFP		M5M82C37AFP-4		M5M82C37AFP-5		
			Min	Max	Min	Max	Min	Max	
$t_{w(\phi)}$	Clock high-level pulse width	T_{CH}	120		100		80		ns
$t_{w(\overline{\phi})}$	Clock low-level pulse width	T_{CL}	150		110		68		ns
$t_{C(\phi)}$	Clock period	T_{CY}	320		250		200		ns
$t_{su(EOP-\phi)}$	External $\overline{EOP}$ setup time before clock	T_{EPS}	60		45		40		ns
$t_{w(EOP)}$	External $\overline{EOP}$ pulse width	T_{EPW}	300		225		220		ns
$t_{su(DREQ-\phi)}$	DREQ setup time before clock	T_{QS}	0		0		0		ns
$t_{su(READY-\phi)}$	READY setup time before clock	T_{RS}	100		60		60		ns
$t_{h(\phi-READY)}$	READY hold time before clock	T_{RH}	20		20		20		ns
$t_{su(HLDA-\phi)}$	HLDA setup time before clock	T_{HS}	100		75		75		ns
$t_{su(DQ-\overline{MEMR})}$	Data setup time before $\overline{MEMR}$	T_{IDS}	250		190		170		ns
$t_{h(\overline{MEMR}-DQ)}$	Data hold time after $\overline{MEMR}$	T_{IDH}	0		0		0		ns

Note : A.C Testing waveform

Input pulse level	0.45~2.4V
Input pulse rise time	10ns
Input pulse fall time	10ns
Reference level input	V_{IH}=2V, V_{IL}=0.8V
Output	V_{OH}=2V, V_{OL}=0.8V



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SWITCHING CHARACTERISTIC (T_a=−20~75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

(i) SLAVE MODE

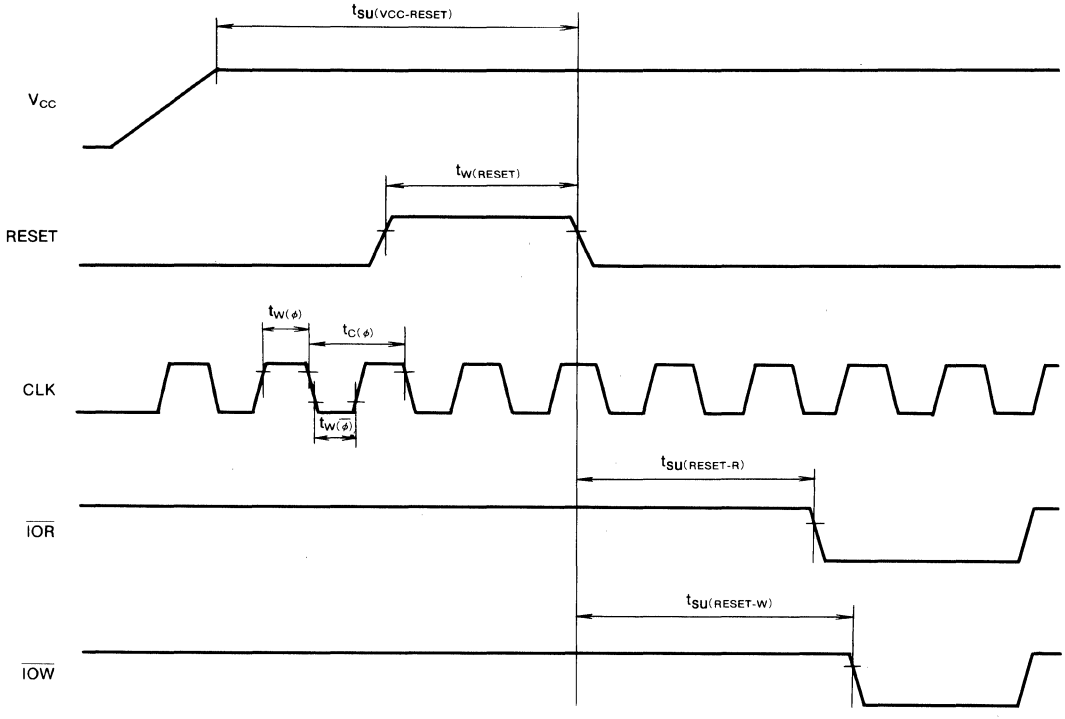
Symbol	Parameter	Alternate symbol	Limits						Unit
			M5M82C37AFP		M5M82C37AFP-4		M5M82C37AFP-5		
			Min	Max	Min	Max	Min	Max	
$t_{PZV(R-DQ)}$	Data enable time after read	T_{RDE}		200		200		140	ns
$t_{PVZ(R-DQ)}$	Data disable time after read	T_{RDF}	0	100	0	100	0	70	ns

(ii) DMA MODE

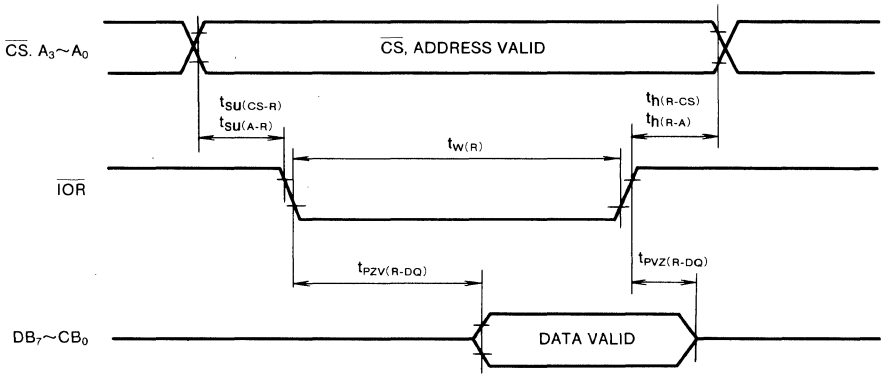
Symbol	Parameter	Alternate symbol	Limits						Unit
			M5M82C37AFP		M5M82C37AFP-4		M5M82C37AFP-5		
			Min	Max	Min	Max	Min	Max	
$t_{PLH(\phi-AEN)}$	Propagation time from clock to AEN	T_{AEL}		300		225		200	ns
$t_{PHL(\phi-AEN)}$	Propagation time from clock to AEN	T_{AET}		200		150		130	ns
$t_{PZV(\phi-A)}$	Propagation time from clock to address active	T_{FAAB}		250		190		170	ns
$t_{PHL(\phi-A)}$	Propagation time from clock to address stable	T_{ASM}		250		190		170	ns
$t_{PVZ(\phi-A)}$	Propagation time from clock to address floating	T_{AFAB}		150		120		90	ns
$t_{PZV(\phi-DQ)}$	Propagation time from clock to data bus	T_{FADB}		300		225		200	ns
$t_{PVZ(\phi-DQ)}$	Propagation time from clock to data bus	T_{AFDB}		250		190		170	ns
$t_{PLH(\phi-ADSTB)}$	Propagation time from clock to ADSTB	T_{STL}		200		150		130	ns
$t_{PHL(\phi-ADSTB)}$	Propagation time from clock to ADSTB	T_{STT}		140		110		90	ns
$t_{su(DB-ADSTB)}$	Data output setup time before ADSTB	T_{ASS}	100		100		100		ns
$t_{h(ADSTB-DQ)}$	Data output hold time before ADSTB	T_{AHS}	50		40		30		ns
$t_{PZV(\phi-R)}$ $t_{PZV(\phi-W)}$	Propagation time from clock to read or write active	T_{FAC}		200		150		150	ns
$t_{PHL(\phi-R)}$ $t_{PHL(\phi-W)}$	Propagation time from clock to read or write	T_{DCL}		270		200		190	ns
$t_{PLH(\phi-R)}$	Propagation time from clock to read	T_{DCTR}		270		210		190	ns
$t_{PLH(\phi-W)}$	Propagation time from clock to write	T_{DCTW}		200		150		130	ns
$t_{PVZ(\phi-R)}$ $t_{PVZ(\phi-W)}$	Propagation time from clock to read or write floating	T_{AFC}		150		120		120	ns
$t_{h(R-A)}$	Address output hold time after read	T_{AHR}	$t_{C(\phi)}-100$		$t_{C(\phi)}-100$		$t_{C(\phi)}-100$		ns
$t_{h(W-A)}$	Address output hold time after write	T_{AHW}	$t_{C(\phi)}-50$		$t_{C(\phi)}-50$		$t_{C(\phi)}-50$		ns
$t_{su(DQ-MEMW)}$	Data output setup time before $\overline{MEMW}$	T_{ODV}	200		125		125		ns
$t_{h(MEMW-DQ)}$	Data output hold time after $\overline{MEMW}$	T_{ODH}	20		20		10		ns
$t_{PLH(\phi-DACK)}$	Propagation time from clock to $\overline{DACK}$	T_{AK}		250		220		170	ns
$t_{PHL(\phi-EOP)}$	Propagation time from clock to $\overline{EOP}$	T_{AK}		250		190		170	ns
$t_{PLH(\phi-EOP)}$	Propagation time from clcok to $\overline{EOP}$	T_{AK}		250		190		170	ns
$t_{PLH(\phi-HRQ)}$ $t_{PHL(\phi-HRQ)}$	Propagation time from clock to HRQ	T_{DQ} "H"2.0V		160		120		120	ns
		T_{DQ} "H"3.3V		250		190		120	

TIMING DIAGRAMS

Reset timing



Slave mode timing (READ)



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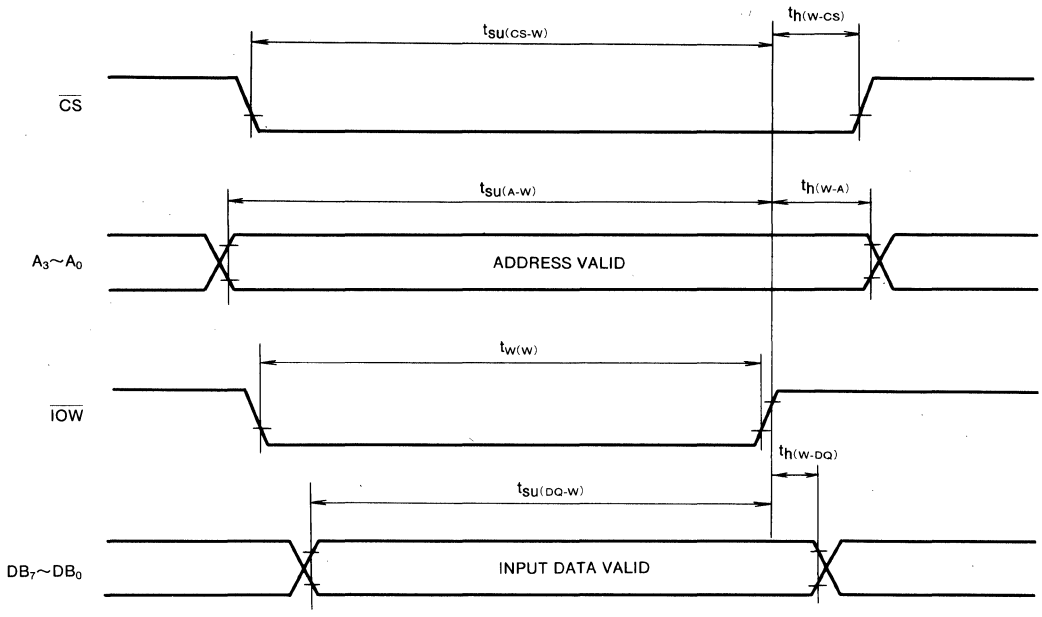
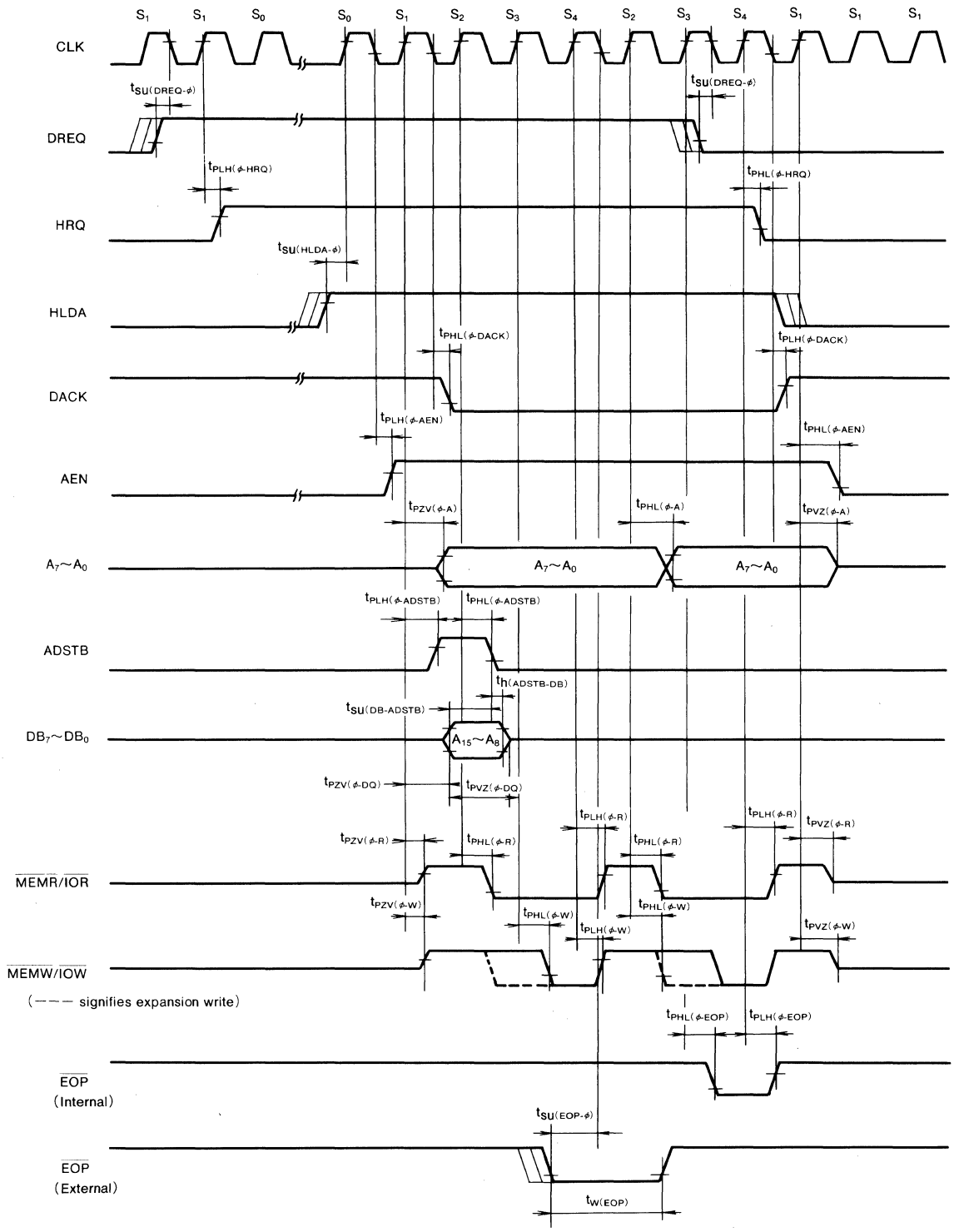
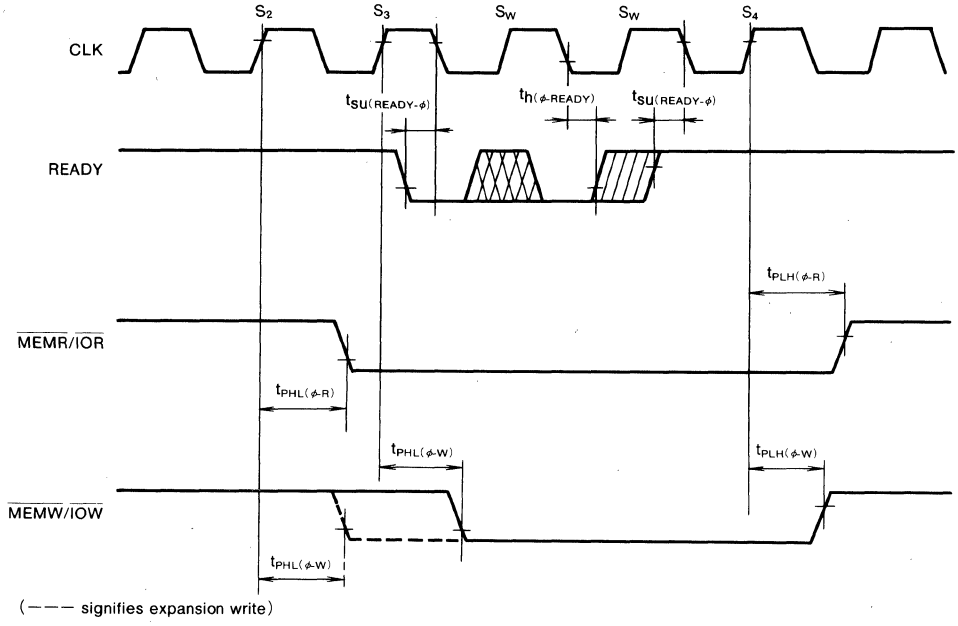
Slave mode timing (WRITE)



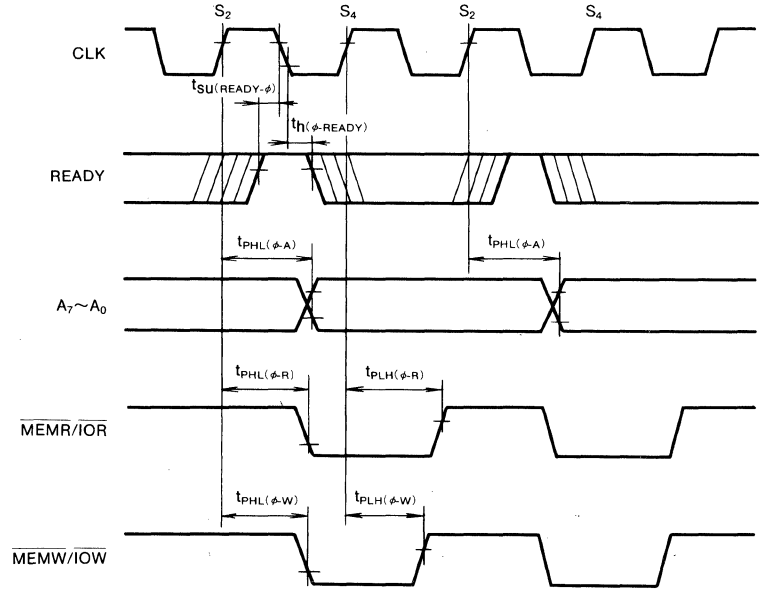
DMA transmit timing



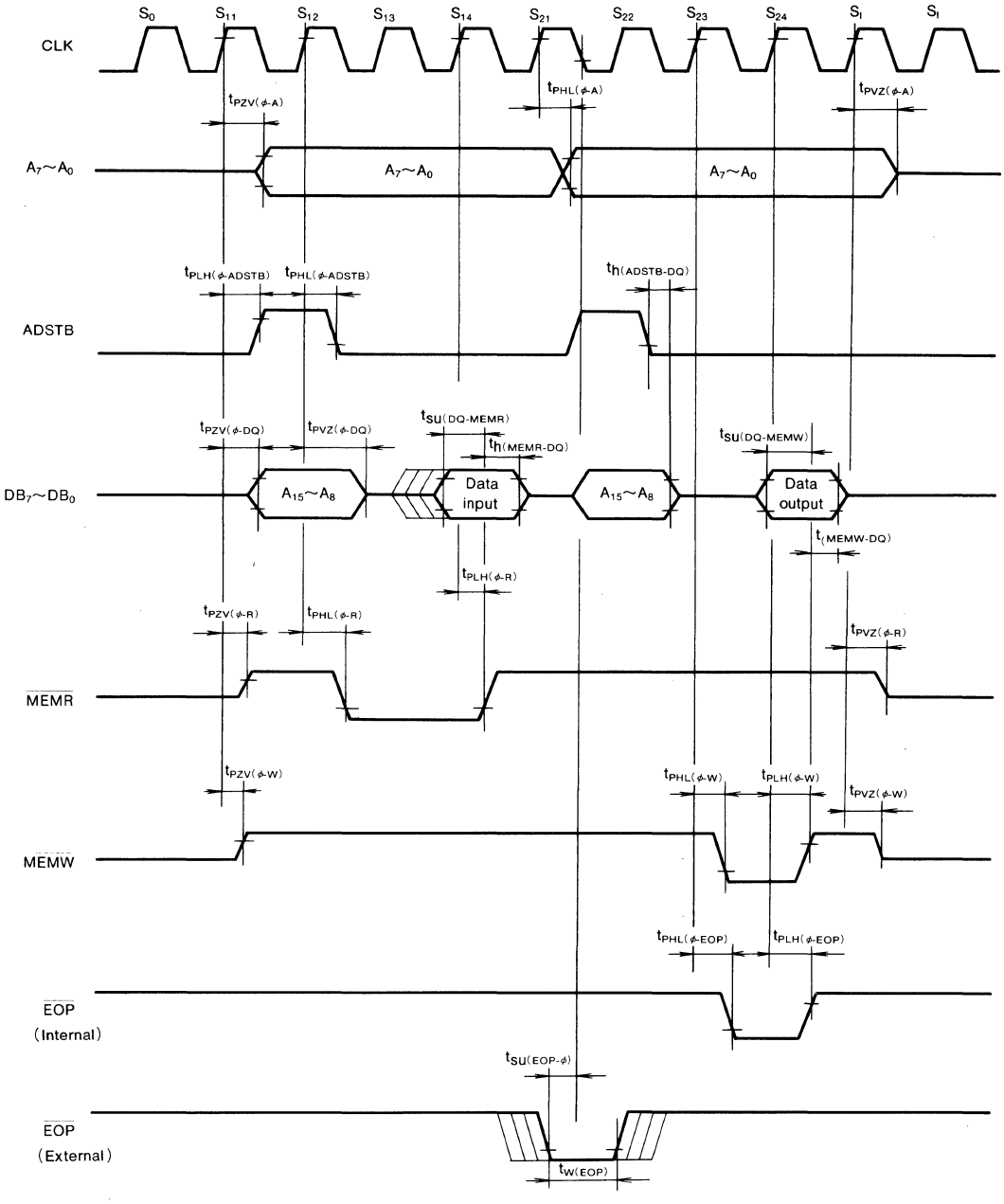
READY input timing



(——— signifies expansion write)



Inter-memory transmission



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