



() Preliminary Specifications

(✓) Final Specifications

| | |
|------------|---|
| Module | 15.6" FHD Color TFT-LCD |
| Model Name | G156HAN02.0 |
| Note | LED backlight with driving circuit design |

| | |
|----------------------------------|-------------|
| Customer | Date |
| _____ | _____ |
| Checked & Approved by | Date |
| _____ | _____ |
| Customer's sign back page | |

| | |
|---|-------------------|
| Approved by | Date |
| <u>Sean Lin</u> | <u>03/20/2017</u> |
| Prepared by | Date |
| <u>Sandy Su</u> | <u>03/20/2017</u> |
| General Display Business Division / AU Optronics corporation | |

2. General Description

G156HAN02.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 FHD, 1920(H) x 1080(V) screen and 16.2M colors (RGB 6-bits + FRC) with LED backlight driving circuit. All input signals are eDP(Embedded DisplayPort) interface compatible.

G156HAN02.0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

| Items | Unit | Specifications | | | |
|---|-----------|-------------------------------------|------------|-------|-------|
| Screen Diagonal | [mm] | 15.6" | | | |
| Active Area | [mm] | 344.16 x 193.59 | | | |
| Resolution | | 1920 x 3(RGB) x 1080 | | | |
| Pixel Pitch | [mm] | 0.17925 x 0.17925 | | | |
| Pixel Arrangement | | R.G.B. Vertical Stripe | | | |
| Display Mode | | AHVA, Normally Black | | | |
| Nominal Input Voltage VDD | [Volt] | +3.3 (Typ.) | | | |
| LCD Power Consumption | [Watt] | 0.98 (Max.) | | | |
| LED Power Consumption | [Watt] | 10.4 (Max.) | | | |
| Weight | [Grams] | 600 (Typ), 660 (Max) | | | |
| Physical Size Include bracket | [mm] | | Min. | Typ. | Max. |
| | | Length | 363.3 | 363.8 | 364.3 |
| | | Width | 215.4 | 215.9 | 216.4 |
| | | Thickness | | 8.8 | |
| Electrical Interface | | 2 Lane eDP | | | |
| Surface Treatment | | Anti-Reflection ≤ 1.5%, hardness 2H | | | |
| Support Color | | 16.2M colors (RGB 6-bits+FRC) | | | |
| Temperature Range | | | | | |
| | Operating | [°C] | -10 to +60 | | |
| Storage (Non-Operating) | [°C] | -20 to +60 | | | |
| RoHS Compliance | | Yes | | | |



2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

| Item | Unit | Conditions | Min. | Typ. | Max. | Note |
|--|-------------------|--|----------|----------|--------|---------|
| White Luminance | cd/m ² | I _{LED} =50mA Center average | 400 | 500 | - | 1, 2 |
| Luminance Uniformity | % | 9 Points | 75 | 80 | | 1, 2, 3 |
| Contrast Ratio | -- | | 700 | 1000 | - | 1, 4 |
| Response Time | msec | Rising + Falling | - | 25 | 35 | 1, 5 |
| Viewing Angle | degree | Horizontal (Right) CR = 10 (Left) | 80 80 | 89 89 | - - | 1, 6 |
| | | Vertical (Upper) CR = 10 (Lower) | 80 80 | 89 89 | - - | |
| Color / Chromaticity Coordinates (CIE 1931) | Red | Rx | 0.590 | 0.640 | 0.690 | 4 |
| | | Ry | 0.283 | 0.333 | 0.383 | |
| | Green | Gx | 0.252 | 0.302 | 0.352 | |
| | | Gy | 0.578 | 0.628 | 0.678 | |
| | Blue | Bx | 0.107 | 0.157 | 0.207 | |
| | | By | 0.000 | 0.050 | 0.100 | |
| | White | Wx | 0.263 | 0.313 | 0.363 | |
| | | Wy | 0.279 | 0.329 | 0.379 | |
| Color Gamut | % | | - | 72 | - | |

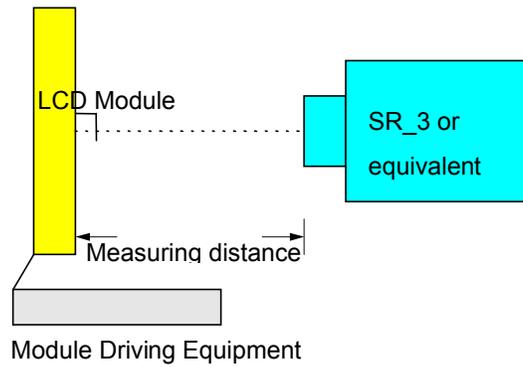
Note 1: Measurement method

Equipment Pattern Generator, Power Supply, Digital Voltmeter, Luminance meter (SR_3 or equivalent)

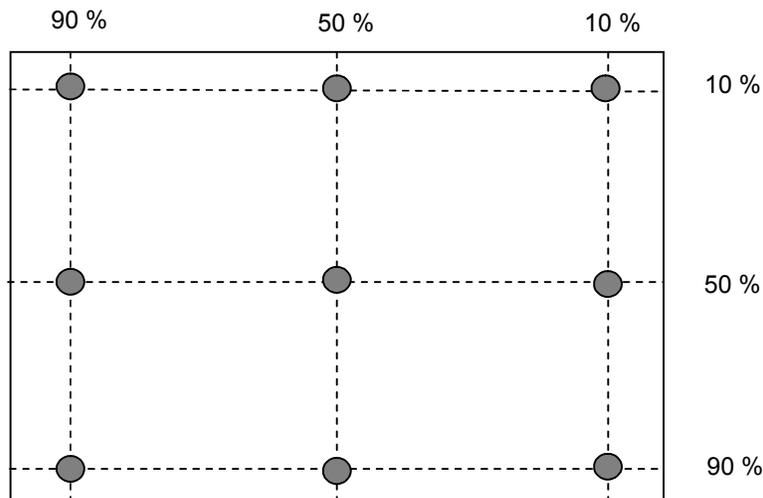
Aperture 1□with 50cm viewing distance

Test Point Center

Environment < 1 lux



Note 2: 9 points position



Note 3: The luminance uniformity of 9 points is defined by dividing the maximum luminance values by the minimum test point luminance. And measured by TOPCON SR-3

$$\delta_{w9} = \frac{\text{Minimum Luminance of 9 points}}{\text{Maximum Luminance of 9 points}}$$

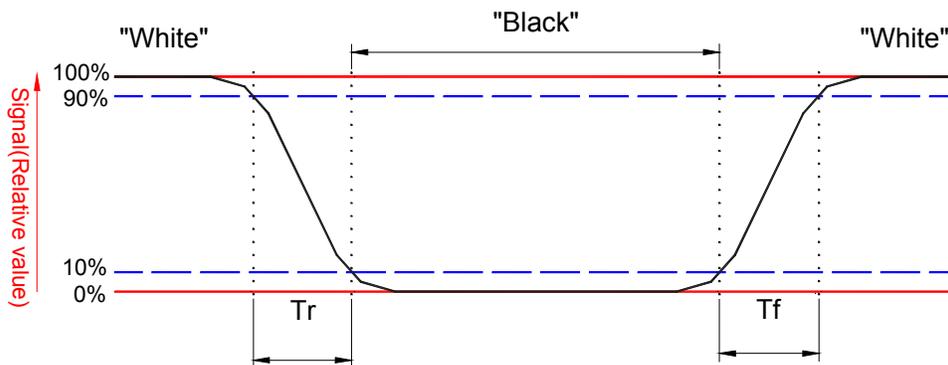
Note 4 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

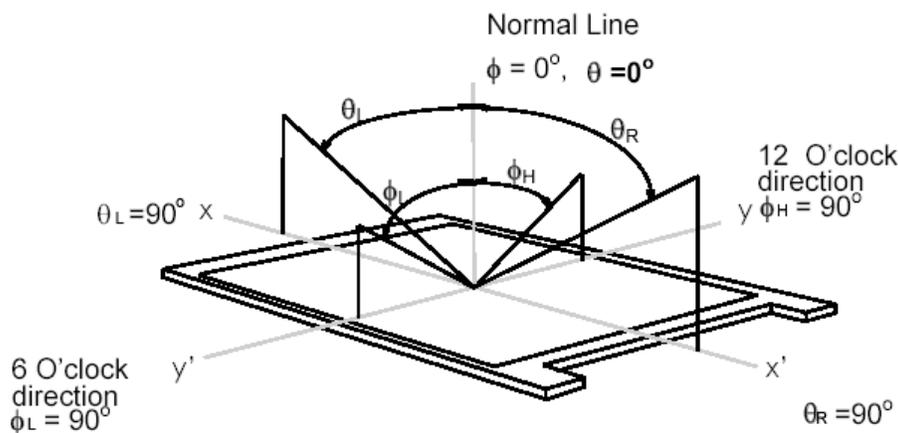
Note 5: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



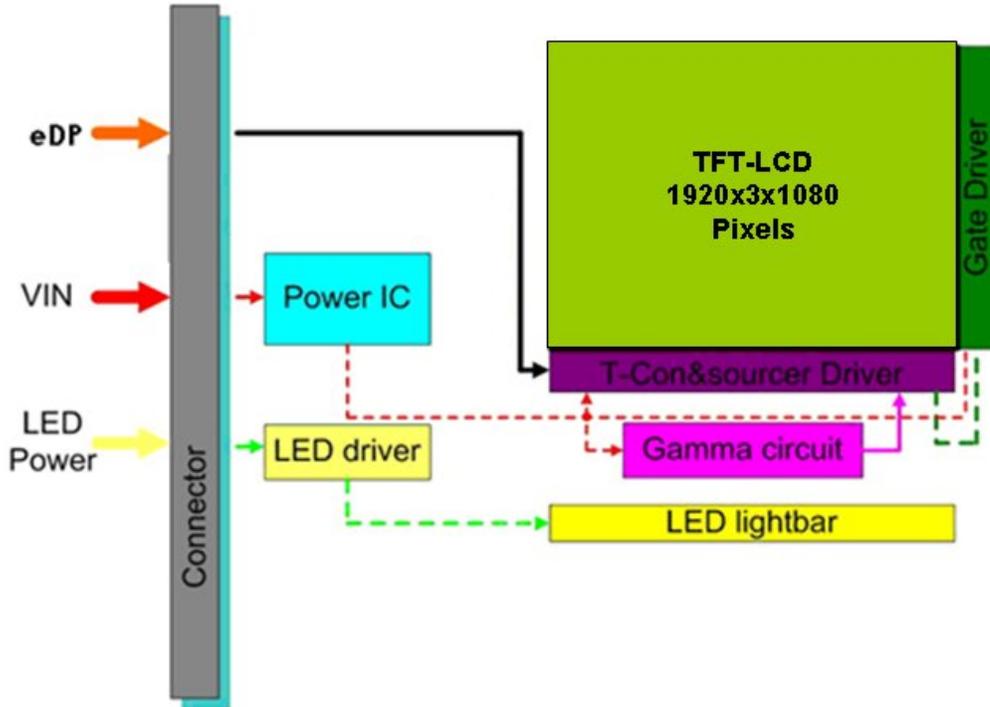
Note 6.: Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 15.6 inches wide Color TFT/LCD module.



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

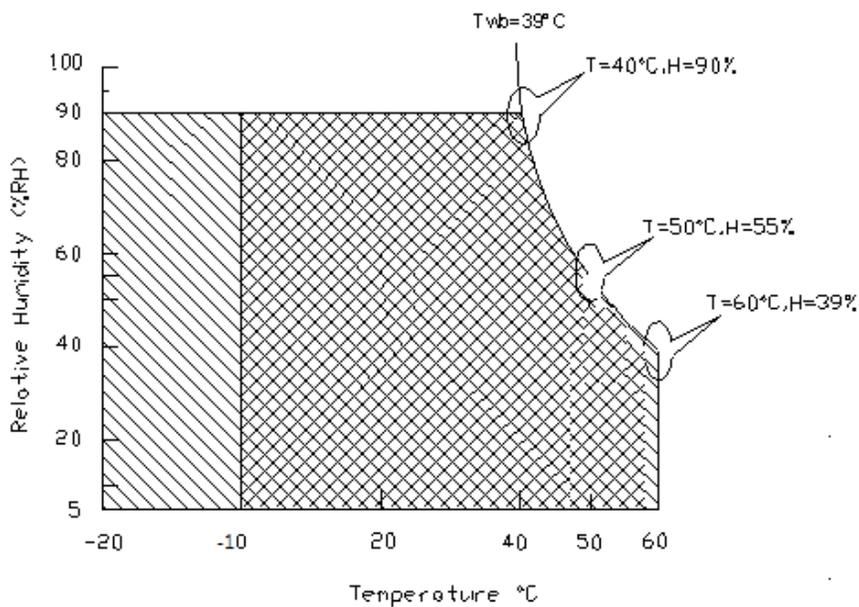
4.1 Absolute Ratings of TFT LCD Module

| Item | Symbol | Min | Max | Unit |
|-----------------|--------|------|------|--------|
| Logic/LCD Drive | Vin | -0.3 | +4.0 | [Volt] |

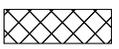
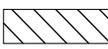
4.2 Absolute Ratings of Environment

| Item | Symbol | Min | Max | Unit |
|---------------------|--------|-----|-----|-------|
| Operating | TOP | -10 | +60 | [°C] |
| Operation Humidity | HOP | 5 | 95 | [%RH] |
| Storage Temperature | TST | -20 | +60 | [°C] |
| Storage Humidity | HST | 5 | 95 | [%RH] |

Note: Maximum Wet-Bulb should be 39 °C and no condensation.



Operating Range 

Storage Range  + 

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

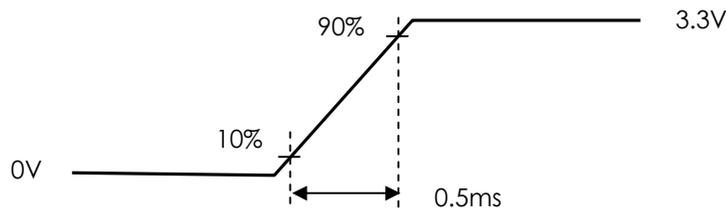
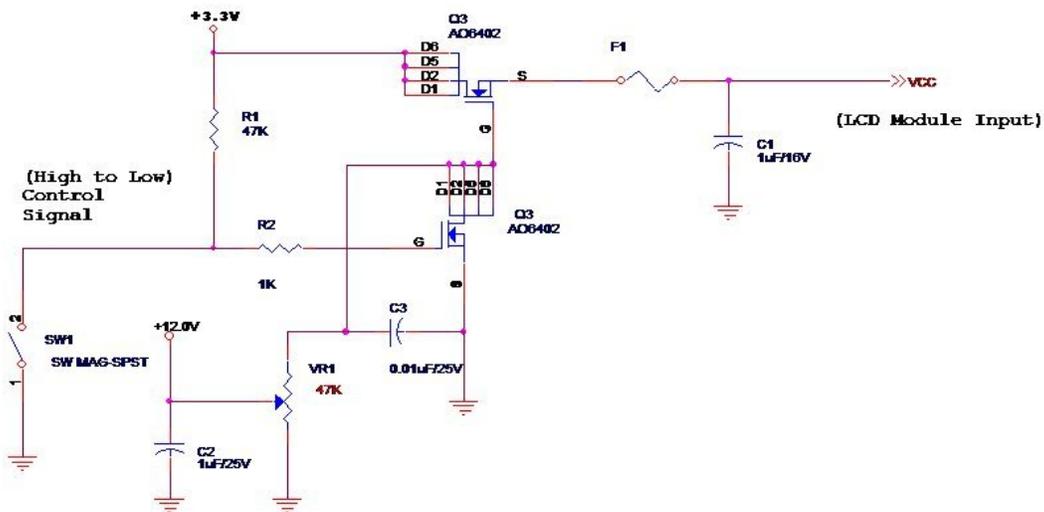
The power specification are measured under 25°C and frame frequency under 60Hz

| Symbol | Parameter | Min | Typ | Max | Units | Remark |
|--------|--|-----|------|------|----------|---------------------------------------|
| VDD | Logic/LCD Drive Voltage | 3.0 | 3.3 | 3.6 | [Volt] | |
| PDD | VDD Power | - | 0.79 | 0.98 | [Watt] | All Black Pattern (VDD=3.3V, at 60Hz) |
| IDD | IDD Current | - | 240 | 290 | [mA] | All Black Pattern (VDD=3.3V, at 60Hz) |
| IRush | Inrush Current | - | - | 2000 | [mA] | Note 1 |
| VDDrp | Allowable Logic/LCD Drive Ripple Voltage | - | - | 100 | [mV] p-p | All Black Pattern (VDD=3.3V, at 60Hz) |

Note 1 : Maximum Measurement Condition : White Pattern at 3.3V driving voltage. ($P_{max} = V_{3.3} \times I_{white}$)

Typical Measurement Condition: Mosaic Pattern

Note 2 : Measure Condition



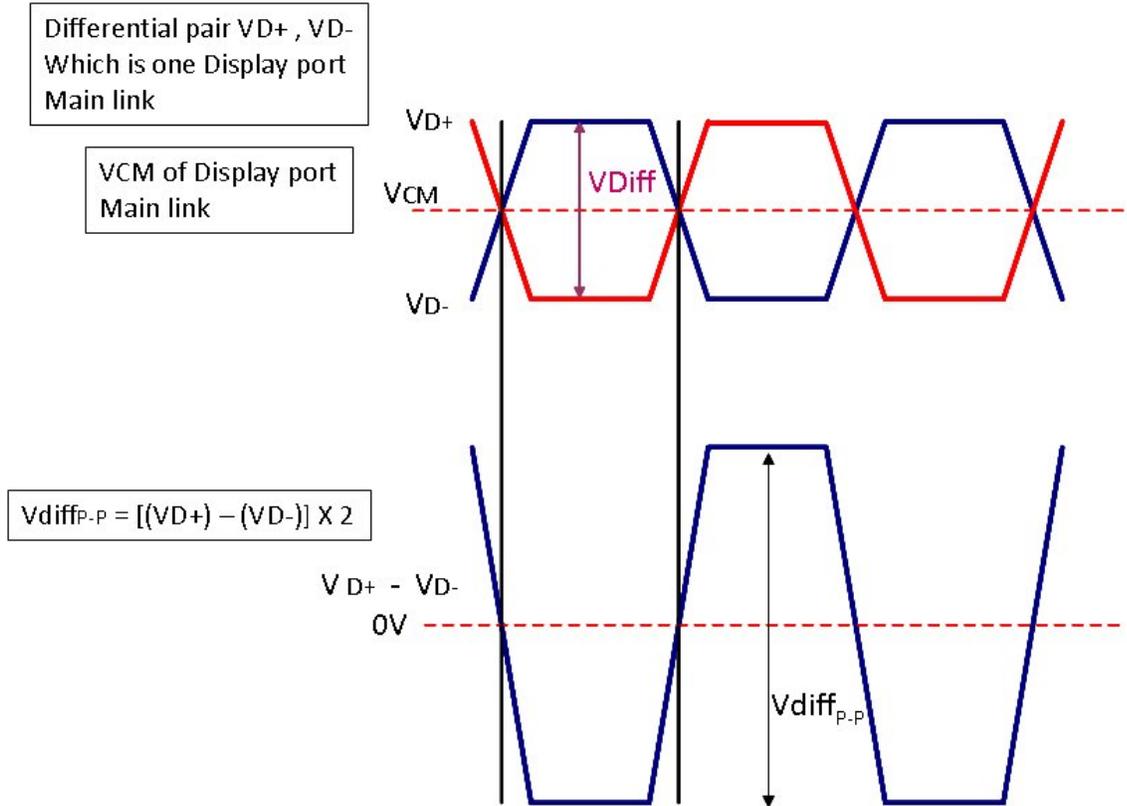
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

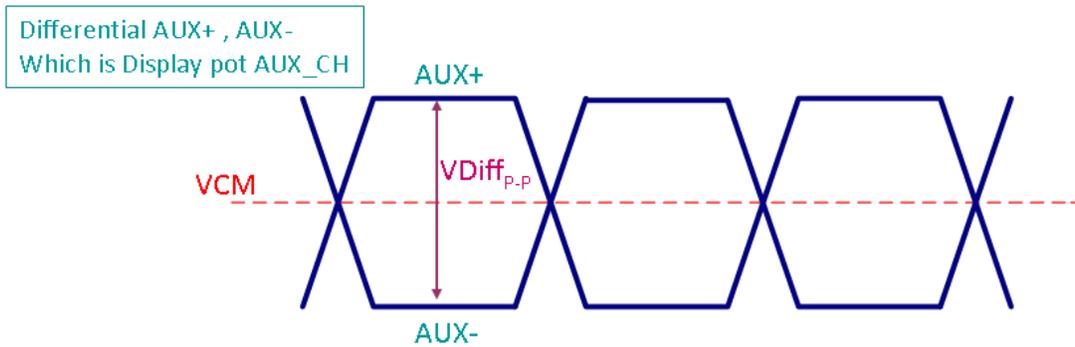
Display Port main link signal:



| Display port main link | | | | | |
|------------------------|--|-----|-----|------|------|
| | | Min | Typ | Max | unit |
| VCM | RX input DC Common Mode Voltage | | 0 | | V |
| VDiff _{P-P} | Peak-to-peak Voltage at a receiving Device | 100 | | 1320 | mV |

Follow as VESA display port standard V1.1a

Display Port AUX_CH signal:



| Display port AUX_CH | | | | | |
|----------------------|--|-----|-----|-----|------|
| | | Min | Typ | Max | unit |
| VCM | AUX DC Common Mode Voltage | | 0 | | V |
| VDiff _{P-P} | AUX Peak-to-peak Voltage at a receiving Device | 0.4 | 0.6 | 0.8 | V |

Follow as VESA display port standard V1.1a.

Display Port VHPD signal:

| Display port VHPD | | | | | |
|-------------------|-------------|------|-----|-----|------|
| | | Min | Typ | Max | unit |
| VHPD | HPD Voltage | 2.25 | | 3.6 | V |

Follow as VESA display port standard V1.1a.

5.2 Backlight Unit

5.2.1 LED characteristics

| Parameter | Symbol | Min | Typ | Max | Units | Condition |
|-----------------------------|--------|--------|-----|------|--------|-------------------------------|
| Backlight Power Consumption | PLED | - | 8.3 | 10.4 | [Watt] | (Ta=25°C), Note 1 Vin =12V |
| LED Life-Time | N/A | 50,000 | - | - | Hour | (Ta=25°C), Note 2,3 |

Note 1: Ta means ambient temperature of TFT-LCD module.

Note 2: If G156HAN02.0 module is driven at high ambient temperature & humidity condition. The operating life will be reduced.

Note 3: Operating life means brightness goes down to 50% initial brightness. Min. operating life time is estimated data.

5.2.2 Backlight input signal characteristics

| Parameter | Symbol | Min | Typ | Max | Units | Remark |
|-----------------------------|---------|------|-----|------|--------|--|
| LED Power Supply | VLED | 10.8 | 12 | 13.2 | [Volt] | Define as Connector Interface (Ta=25°C) |
| LED Enable Input High Level | VLED_EN | 2.5 | | 5.5 | [Volt] | |
| LED Enable Input Low Level | | 0 | | 0.9 | [Volt] | |
| PWM Logic Input High Level | VPWM_EN | 2.5 | | 5.5 | [Volt] | |
| PWM Logic Input Low Level | | 0 | | 0.9 | [Volt] | |
| PWM Input Frequency | FPWM | 200 | | 15K | Hz | |
| PWM Duty Ratio | Duty | 10 | | 100 | % | |

Note 1 : Recommended system pull up/down resistor no bigger than 10kohm.

Note 2 : If the PWM duty ratio(min) is set between 5% to 1% · the PWM input frequency should be set below 1KHz . The brightness-duty characteristic might not be able to keep in it's linearity if the dimming control is operated in 1% to 5% range.

6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

| Connector Name / Designation | For Signal Connector |
|------------------------------|-----------------------------------|
| Manufacturer | IPEX or compatible |
| Type / Part Number | IPEX 20455-030E-76B or compatible |
| Mating Housing/Part Number | IPEX 20453-030T-11 or compatible |

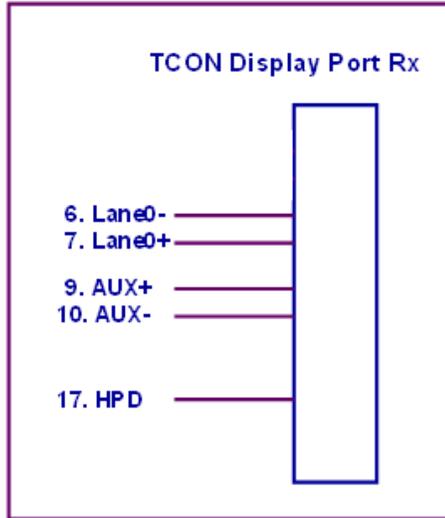
6.2.2 Pin Assignment (2 Lane)

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

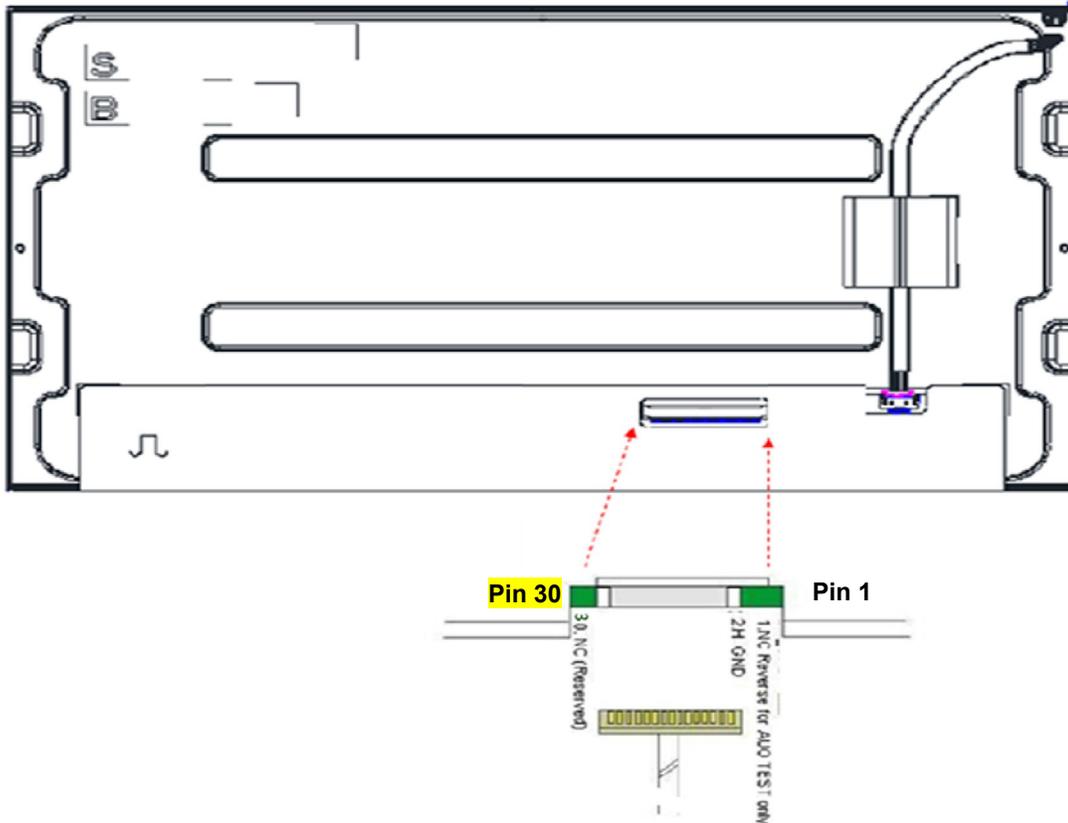
| PIN NO | Symbol | Function |
|--------|---------------------|---------------------------------------|
| 1 | NC | Reverse for AUO TEST only |
| 2 | H_GND | High Speed Ground |
| 3 | Lane1_N | Comp Signal Lane 1 |
| 4 | Lane1_P | True Signal Link Lane 1 |
| 5 | H_GND | High Speed Ground |
| 6 | Lane0_N | Comp Signal Link Lane 0 |
| 7 | Lane0_P | True Signal Link Lane 0 |
| 8 | H_GND | High Speed Ground |
| 9 | AUX_CH_P | True Signal Auxiliary Ch. |
| 10 | AUX_CH_N | Comp Signal Auxiliary Ch. |
| 11 | H_GND | High Speed Ground |
| 12 | LCD_VCC | LCD logic and driver power |
| 13 | LCD_VCC | LCD logic and driver power |
| 14 | LCD_Self_Test or NC | LCD Panel Self Test Enable (Optional) |
| 15 | LCD_GND | LCD logic and driver ground |
| 16 | LCD_GND | LCD logic and driver ground |
| 17 | HPD | HPD signale pin |
| 18 | BL_GND | Backlight_ground |
| 19 | BL_GND | Backlight_ground |
| 20 | BL_GND | Backlight_ground |
| 21 | BL_GND | Backlight_ground |
| 22 | BL_Enable | Backlight On / Off |
| 23 | BL_PWM_DIM | System PWM signal Input |
| 24 | NC | Reverse for AUO TEST only |
| 25 | NC | Reverse for AUO TEST only |
| 26 | BL_PWR | Backlight power (5V~21V) |
| 27 | BL_PWR | Backlight power (5V~21V) |
| 28 | BL_PWR | Backlight power (5V~21V) |
| 29 | BL_PWR | Backlight power (5V~21V) |
| 30 | NC | No Connect (Reserved for CM) |

Note1 : start from right side refer to next page illustration.

Note2 : Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of **eDP inputs** are as following.



Note3 : Connector Illustration



6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 1920x1080 /60Hz manufacturing guide line timing.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | |
|--------------------|-----------------|----------|------|------|------|-------------|
| Frame Rate | - | - | 60 | - | Hz | |
| Clock frequency | $1 / T_{Clock}$ | - | 141 | - | MHz | |
| Vertical Section | Period | T_V | 1090 | 1116 | 1880 | T_{Line} |
| | Active | T_{VD} | 1080 | | | |
| | Blanking | T_{VB} | 10 | 36 | 800 | |
| Horizontal Section | Period | T_H | 2080 | 2104 | 2320 | T_{Clock} |
| | Active | T_{HD} | 1920 | | | |
| | Blanking | T_{HB} | 160 | 184 | 400 | |

Note 1 : DE mode only

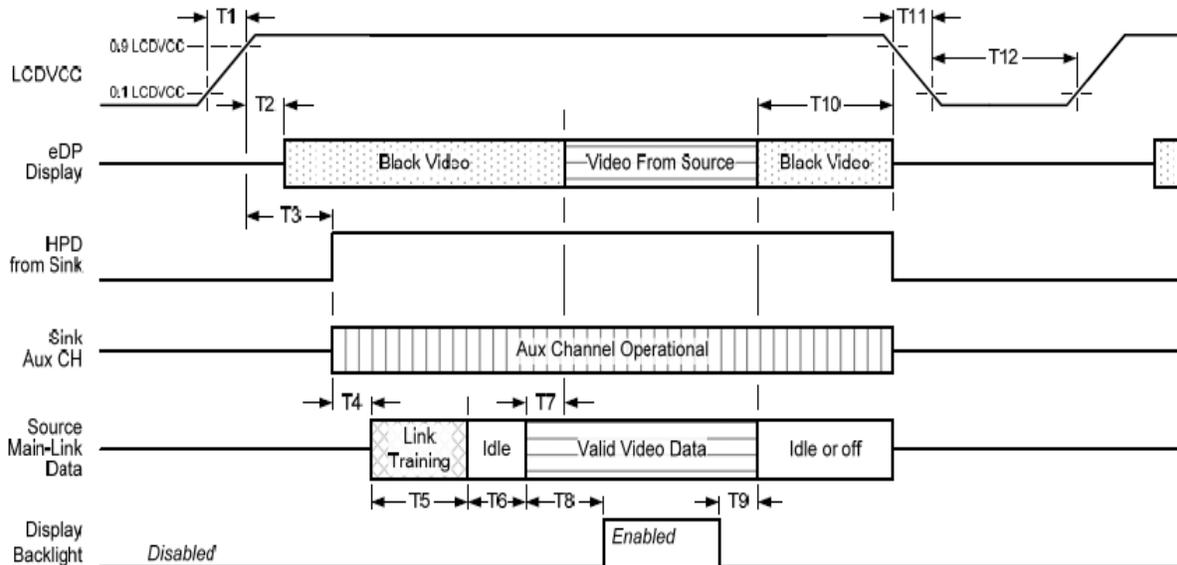
Note 2 : The maximum clock frequency = $(960+B) * (1080+A) * 60 < 80\text{MHz}$

6.4 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.

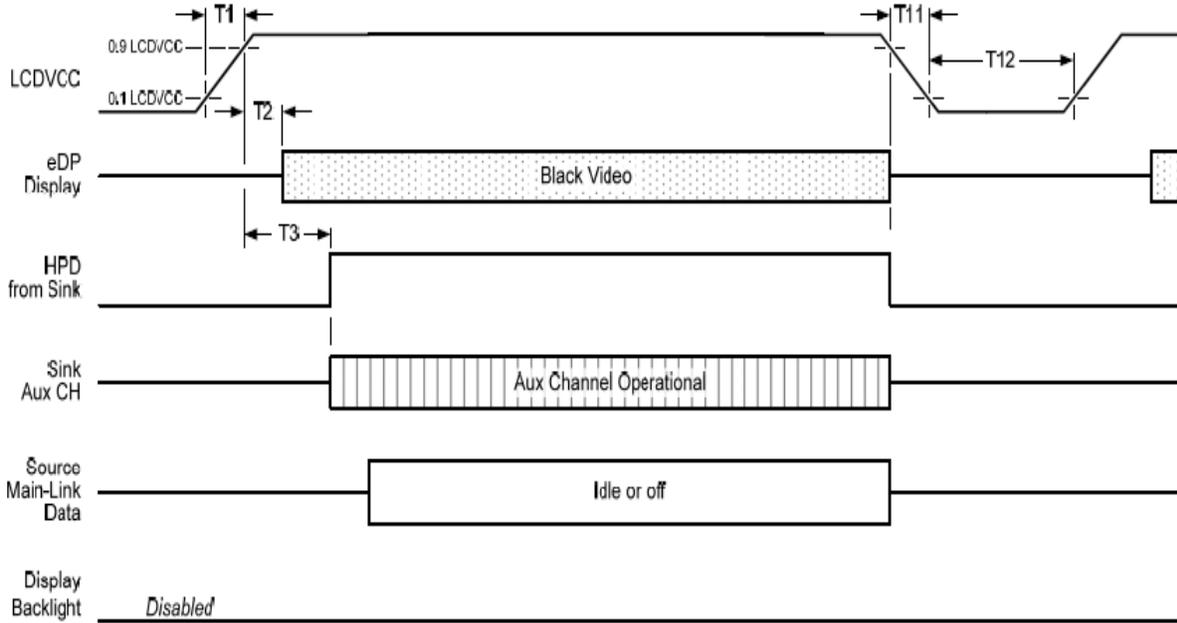
Signals from any system shall be Hi-Z state or low level when VDD is off

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only



Display Port panel power sequence timing parameter:

| Timing parameter | Description | Reqd. by | Limits | | | Notes |
|------------------|---|----------|--------|------|-------|---|
| | | | Min. | Typ. | Max. | |
| T1 | power rail rise time, 10% to 90% | source | 0.5ms | | 10ms | |
| T2 | delay from LCDVDD to black video generation | sink | 0ms | | 200ms | prevents display noise until valid video data is received from the source |
| T3 | delay from LCDVDD to HPD high | sink | 0ms | | 200ms | sink AUX_CH must be operational upon HPD high. |
| T4 | delay from HPD high to link training initialization | source | | | | allows for source to read link capability and initialize. |
| T5 | link training duration | source | | | | dependant on source link to read training protocol. |
| T6 | link idle | source | | | | Min accounts for required BS-Idle pattern. Max allows for source frame synchronization. |
| T7 | delay from valid video data from source to video on display | sink | 0ms | | 50ms | max allows sink validate video data and timing. |
| T8 | delay from valid video data from source to backlight enable | source | | | | source must assure display video is stable. |
| T9 | delay from backlight disable to end of valid video data | source | | | | source must assure backlight is no longer illuminated. |
| T10 | delay from end of valid video data from source to power off | source | 0ms | | 500ms | |
| T11 | power rail fall time, 90% to 10% | source | | | 10ms | |
| T12 | power off time | source | 500ms | | | |

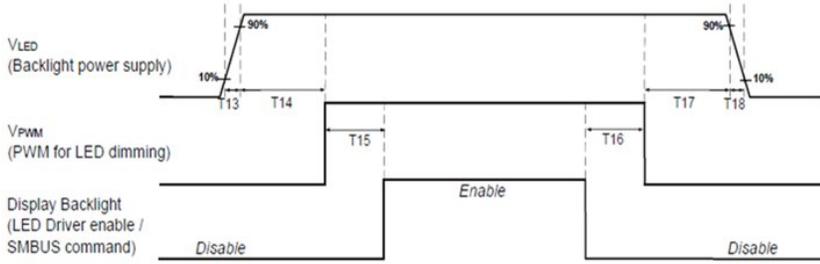
Note 1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:

- upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
- when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

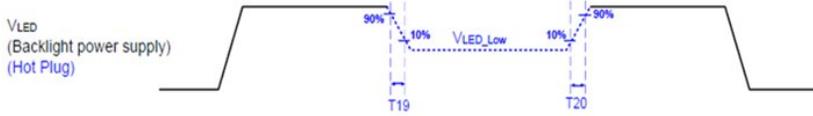
Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCD VDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:



Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



| | Min (ms) | Max (ms) |
|-----|----------------|----------|
| T13 | 0.5 | 10 |
| T14 | 10 | - |
| T15 | 10 | - |
| T16 | 10 | - |
| T17 | 10 | - |
| T18 | 0.5 | 10 |
| T19 | 1 ^A | - |
| T20 | 1 ^A | - |

Seamless change: $T19/T20 = 5 \times T_{PWM}^*$

^A $T_{PWM} = 1/PWM \text{ Frequency}$

7. Panel Reliability Test

| Items | Required Condition | Note |
|----------------------------|---|----------|
| Temperature Humidity Bias | Ta= 50°C, 80%RH, 300h | Note 1,2 |
| High Temperature Operation | Ta= 60°C, Dry, 300h | |
| Low Temperature Operation | Ta= -10°C, 300h | |
| High Temperature Storage | Ta= 60°C, 300h | |
| Low Temperature Storage | Ta= -20°C, 300h | |
| Thermal Shock Test | Ta= -20°Cto 60°C, Duration at 30 min, 100 cycles | |
| Vibration | Test method: Non-Operation Acceleration: 1.5 G Frequency: 10 - 200 -10Hz Sweep: Sine wave vibration; 30 minutes each axis (X, Y, Z) | |
| Mechanical Shock | Test method: Non-Operation Acceleration: 50 G; Wave: Half-sine Active time: 20 ms Direction: ±X,±Y,±Z (one time for each axis) | |
| Drop Test | Height: 46 cm, package test | |
| ESD | Contact : ±8 KV Air : ±15 KV | Note 1 |

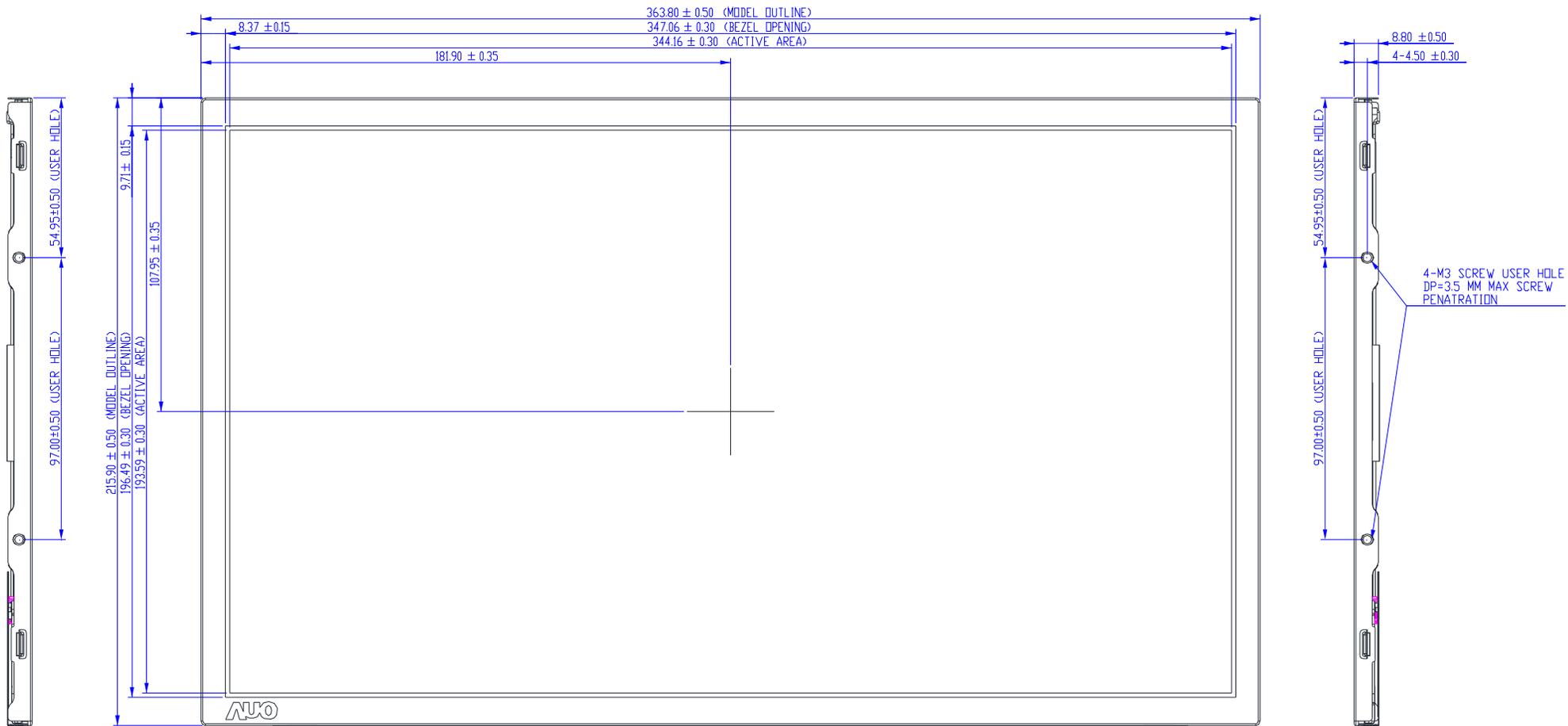
Note 1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable.
No data lost, No hardware failures.

Note 2:

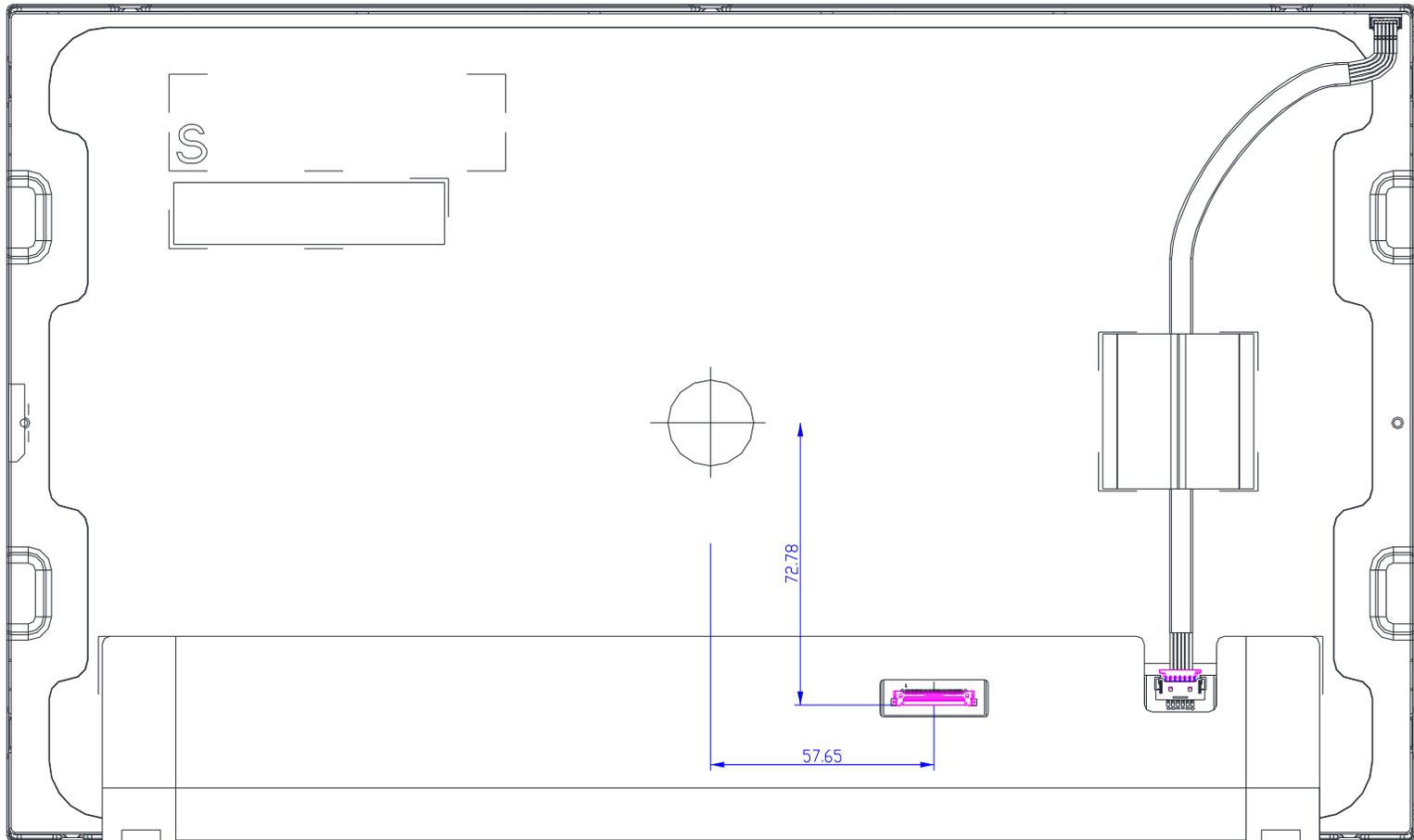
- Water condensation is not allowed for each test items.
- Each test is done by new TFT-LCD module. Don't use the same TFT-LCD module repeatedly for reliability test.
- The reliability test is performed only to examine the TFT-LCD module capability.
- To inspect TFT-LCD module after reliability test, please store it at room temperature and room humidity for 24 hours at least in advance.
- No function failure occurs. Mura shall be ignored after high temperature reliability test

8. Mechanical Characteristics

8.1 LCM Outline Dimension (Front View)

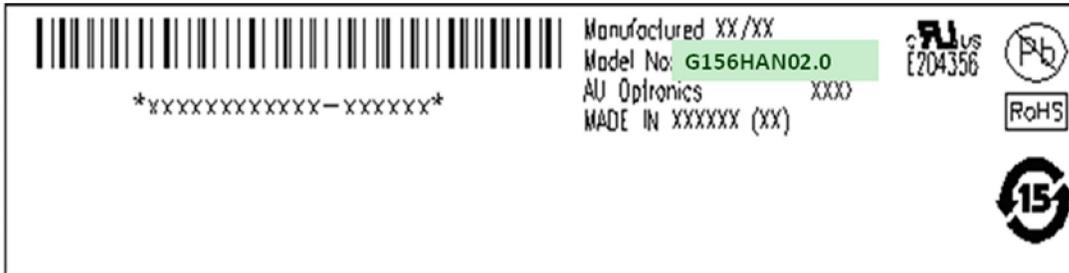


8.2 LCM Outline Dimension (Rear View)



9. Shipping and Package

9.1 Shipping Label Format



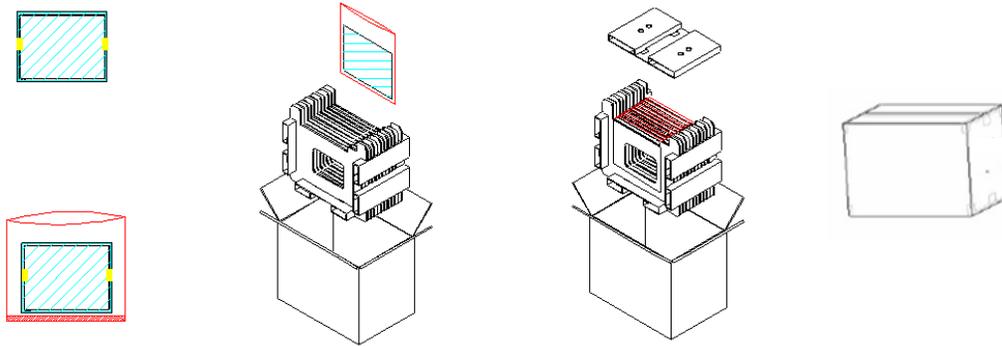
Note 1: For Pb Free products, AUO will add  for identification.

Note 2: For RoHS compatible products, AUO will add  for identification.

Note 3: For China RoHS compatible products, AUO will add  for identification.

Note 4: The Green Mark will be presented only when the green documents have been ready by AUO Internal Green Team.

9.2 Carton Package



Max capacity : 16 TFT-LCD module per carton

Max weight: 13.2 kg per carton

Outside dimension of carton: 450mm(L)*375mm(W)*319mm(H)

Pallet size : 1150 mm * 910 mm * 132mm

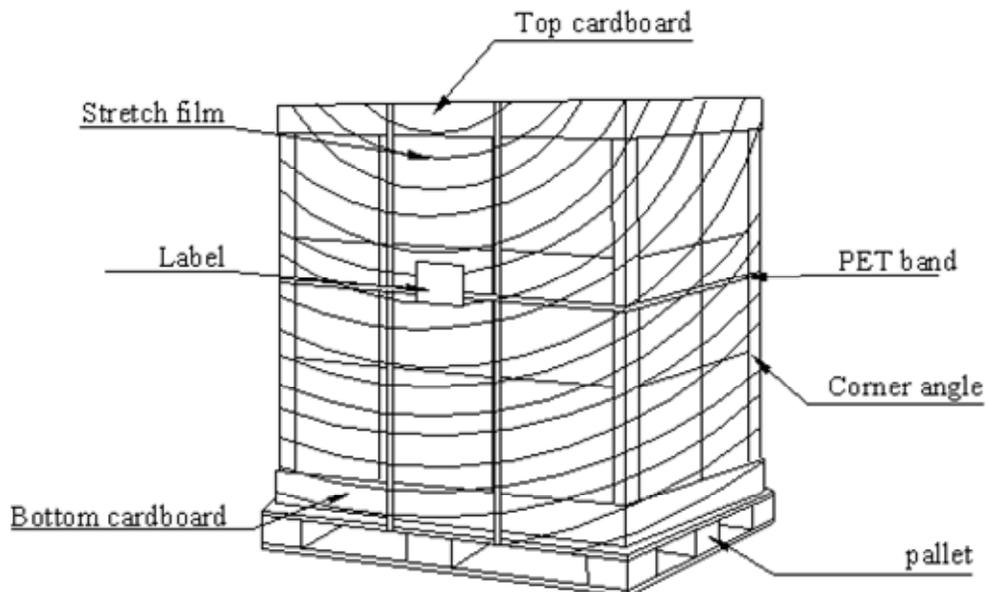
Box stacked

Module by air : (2 *3) *4 layers , one pallet put 24 boxes , total 384pcs module

Module by sea : (2 *3) *4 layers+(2 *3) *1 layers , two pallet put 30 boxes , total 480pcs module

Module by sea_HQ : (2 *3) *4 layers+(2 *3) *2 layers , two pallet put 42 boxes , total 576 pcs module

9.3 Shipping Package of Palletizing Sequence



10. Handling guide

This is a LCD model, and please be cautious when pulling it out of package or assembling it onto platform. Careless handlings, e.g. twist, bending, pressing, or collision, will result malfunction of LCD models.

(1) Handling method notice



Do not lift and hold the panel with single hand at right or left side from tray.



Lift and hold the panel up with both hands from tray.

(2) On the table notice



Do not press edge of panel to avoid glass broken.



Do not press the surface of the panel to avoid the glass broken or polarizer scratch.

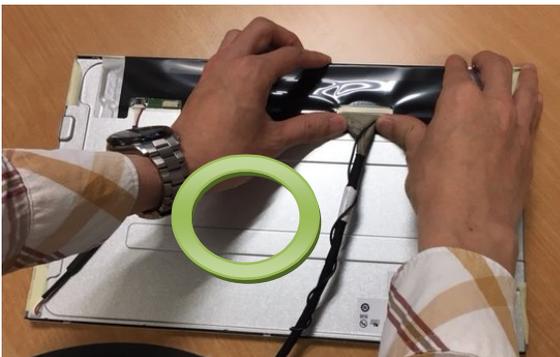


Do not put anything or tool on the panel to avoid the glass broken or polarizer scratch.

(3) Cable assembly notice



Do not insert the connector with single hand and touching the PCBA.



Insert the connector by pushing right and left edge.

11. Appendix: EDID Description

| Address | FUNCTION | Value | Value | Value | Note |
|---------|----------------------|-------|----------|-------|------|
| HEX | | HEX | BIN | DEC | |
| 00 | Header | 00 | 00000000 | 0 | |
| 01 | | FF | 11111111 | 255 | |
| 02 | | FF | 11111111 | 255 | |
| 03 | | FF | 11111111 | 255 | |
| 04 | | FF | 11111111 | 255 | |
| 05 | | FF | 11111111 | 255 | |
| 06 | | FF | 11111111 | 255 | |
| 07 | | 00 | 00000000 | 0 | |
| 08 | EISA Manuf. Code LSB | 06 | 00001110 | 6 | |
| 09 | Compressed ASCII | AF | 10101111 | 175 | |

| | | | | |
|----|--|----|----------|-----|
| 0A | Product Code | ED | 11101101 | 237 |
| 0B | hex, LSB first | 30 | 00110000 | 48 |
| 0C | 32-bit ser # | 00 | 00000000 | 0 |
| 0D | | 00 | 00000000 | 0 |
| 0E | | 00 | 00000000 | 0 |
| 0F | | 00 | 00000000 | 0 |
| 10 | Week of manufacture | 21 | 00100001 | 33 |
| 11 | Year of manufacture | 17 | 00010111 | 23 |
| 12 | EDID Structure Ver. | 01 | 00000001 | 1 |
| 13 | EDID revision # | 04 | 00000100 | 4 |
| 14 | Video input def. (digital I/P, non-TMDS, CRGB) | 95 | 10010101 | 149 |
| 15 | Max H image size (rounded to cm) | 22 | 00100010 | 34 |
| 16 | Max V image size (rounded to cm) | 13 | 00010011 | 19 |
| 17 | Display Gamma $(=\text{gamma} \times 100) - 100$ | 78 | 01111000 | 120 |
| 18 | Feature support (no DPMS, Active OFF, RGB, tmg Blk#1) | 02 | 00000010 | 2 |
| 19 | Red/green low bits (Lower 2:2:2 bits) | E2 | 11100010 | 226 |
| 1A | Blue/white low bits (Lower 2:2:2 bits) | 95 | 10010101 | 149 |
| 1B | Red x (Upper 8 bits) | A3 | 10100011 | 163 |
| 1C | Red y/ highER 8 bits | 54 | 01010100 | 84 |
| 1D | Green x | 52 | 01010010 | 82 |
| 1E | Green y | 99 | 10011001 | 153 |
| 1F | Blue x | 26 | 00100110 | 38 |
| 20 | Blue y | 0F | 00001111 | 15 |
| 21 | White x | 50 | 01010000 | 80 |
| 22 | White y | 54 | 01010100 | 84 |
| 23 | Established timing 1 | 00 | 00000000 | 0 |
| 24 | Established timing 2 | 00 | 00000000 | 0 |
| 25 | Established timing 3 | 00 | 00000000 | 0 |
| 26 | Standard timing #1 | 01 | 00000001 | 1 |
| 27 | | 01 | 00000001 | 1 |
| 28 | Standard timing #2 | 01 | 00000001 | 1 |
| 29 | | 01 | 00000001 | 1 |
| 2A | Standard timing #3 | 01 | 00000001 | 1 |
| 2B | | 01 | 00000001 | 1 |
| 2C | Standard timing #4 | 01 | 00000001 | 1 |
| 2D | | 01 | 00000001 | 1 |
| 2E | Standard timing #5 | 01 | 00000001 | 1 |
| 2F | | 01 | 00000001 | 1 |
| 30 | Standard timing #6 | 01 | 00000001 | 1 |
| 31 | | 01 | 00000001 | 1 |
| 32 | Standard timing #7 | 01 | 00000001 | 1 |
| 33 | | 01 | 00000001 | 1 |
| 34 | Standard timing #8 | 01 | 00000001 | 1 |
| 35 | | 01 | 00000001 | 1 |
| 36 | Pixel Clock/10000 LSB | 14 | 00010100 | 20 |
| 37 | Pixel Clock/10000 USB | 37 | 00110111 | 55 |
| 38 | Horz active Lower 8bits | 80 | 10000000 | 128 |

| | | | | | |
|----|---|----|----------|-----|---|
| 39 | Horz blanking Lower 8bits | B8 | 10111000 | 184 | |
| 3A | HorzAct:HorzBlnk Upper 4:4 bits | 70 | 01110000 | 112 | |
| 3B | Vertical Active Lower 8bits | 38 | 00111000 | 56 | |
| 3C | Vertical Blanking Lower 8bits | 24 | 00100100 | 36 | |
| 3D | Vert Act : Vertical Blanking (upper 4:4 bit) | 40 | 01000000 | 64 | |
| 3E | HorzSync. Offset | 10 | 00010000 | 16 | |
| 3F | HorzSync.Width | 10 | 00010000 | 16 | |
| 40 | VertSync.Offset : VertSync.Width | 3E | 00111110 | 62 | |
| 41 | Horz&Vert Sync Offset/Width Upper 2bits | 00 | 00000000 | 0 | |
| 42 | Horizontal Image Size Lower 8bits | 58 | 01011000 | 88 | |
| 43 | Vertical Image Size Lower 8bits | C1 | 11000001 | 193 | |
| 44 | Horizontal & Vertical Image Size (upper 4:4 bits) | 10 | 00010000 | 16 | |
| 45 | Horizontal Border <i>(zero for internal LCD)</i> | 00 | 00000000 | 0 | |
| 46 | Vertical Border <i>(zero for internal LCD)</i> | 00 | 00000000 | 0 | |
| 47 | Signal <i>(non-intr, norm, no stero, sep sync, neg pol)</i> | 18 | 00011000 | 24 | |
| 48 | Detailed timing/monitor | B8 | 10111000 | 184 | |
| 49 | descriptor #2 | 24 | 00100100 | 36 | |
| 4A | | 80 | 10000000 | 128 | |
| 4B | | B8 | 10111000 | 184 | |
| 4C | | 70 | 01110000 | 112 | |
| 4D | | 38 | 00111000 | 56 | |
| 4E | | 24 | 00100100 | 36 | |
| 4F | | 40 | 01000000 | 64 | |
| 50 | | 10 | 00010000 | 16 | |
| 51 | | 10 | 00010000 | 16 | |
| 52 | | 3E | 00111110 | 62 | |
| 53 | | 00 | 00000000 | 0 | |
| 54 | | 58 | 01011000 | 88 | |
| 55 | | C1 | 11000001 | 193 | |
| 56 | | 10 | 00010000 | 16 | |
| 57 | | 00 | 00000000 | 0 | |
| 58 | | 00 | 00000000 | 0 | |
| 59 | | 18 | 00011000 | 24 | |
| 5A | Detailed timing/monitor | 00 | 00000000 | 0 | |
| 5B | descriptor #3 | 00 | 00000000 | 0 | |
| 5C | | 00 | 00000000 | 0 | |
| 5D | | FE | 11111110 | 254 | |
| 5E | | 00 | 00000000 | 0 | |
| 5F | Manufacture | 41 | 01000001 | 65 | A |
| 60 | Manufacture | 55 | 01010101 | 85 | U |
| 61 | Manufacture | 4F | 01001111 | 79 | O |
| 62 | | 0A | 00001010 | 10 | |
| 63 | | 20 | 00100000 | 32 | |
| 64 | | 20 | 00100000 | 32 | |
| 65 | | 20 | 00100000 | 32 | |
| 66 | | 20 | 00100000 | 32 | |
| 67 | | 20 | 00100000 | 32 | |
| 68 | | 20 | 00100000 | 32 | |

| | | | | | |
|-----------|-------------------------|----|----------|-----|---|
| 69 | | 20 | 00100000 | 32 | |
| 6A | | 20 | 00100000 | 32 | |
| 6B | | 20 | 00100000 | 32 | |
| 6C | Detailed timing/monitor | 00 | 00000000 | 0 | |
| 6D | descriptor #4 | 00 | 00000000 | 0 | |
| 6E | | 00 | 00000000 | 0 | |
| 6F | | FE | 11111110 | 254 | |
| 70 | | 00 | 00000000 | 0 | |
| 71 | Manufacture P/N | 42 | 01000010 | 66 | B |
| 72 | Manufacture P/N | 31 | 00110001 | 49 | 1 |
| 73 | Manufacture P/N | 35 | 00110101 | 53 | 5 |
| 74 | Manufacture P/N | 36 | 00110110 | 54 | 6 |
| 75 | Manufacture P/N | 48 | 01001000 | 72 | H |
| 76 | Manufacture P/N | 41 | 01000001 | 65 | A |
| 77 | Manufacture P/N | 4E | 01001110 | 78 | N |
| 78 | Manufacture P/N | 30 | 00110000 | 48 | 0 |
| 79 | Manufacture P/N | 33 | 00110011 | 51 | 3 |
| 7A | Manufacture P/N | 2E | 00101110 | 46 | . |
| 7B | Manufacture P/N | 30 | 00110000 | 48 | 0 |
| 7C | | 20 | 00100000 | 32 | |
| 7D | | 0A | 00001010 | 10 | |
| 7E | Extension Flag | 00 | 00000000 | 0 | |
| 7F | Checksum | D9 | 11011001 | 217 | |