MOS Memories

FUJITSU

■ MBM27128-20, MBM27128-25, MBM27128-30

UV Erasable 131,072-Bit
## Read Only Memory

Description

The Fujitsu MBM27128 is a high speed 131,072-bit static N-chan-nel MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation are important.

A 28-pin dual in-line package or leadless chip carrier (32-pin) with a transparent lid is used to package the MBM27128. The trans-parent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM27128 is fabricated using N-channel double polysilicon gate technology with single transistor stacked gate cells. It is organized as 16,384 words by 8-bits for use in microprocessor ap-plications. Single +5V operation greatly facilitates its use in single supply systems.

Features

- ■ Organized as 16,384 x 8 fully decoded
- ■ Low power requirement: [550 mW (act), 193 mW (standby)]
- ■ No clocks required (fully static operation)
- ■ Programmable utilizing the Quick Pro™ Algorithm
- ■ Program compatible with the Intel int$_e$ligent Programming™ Algorithm
- ■ Fast Access Time:
  MBM27128-20   200 ns max.
  MBM27128-25   250 ns max.
  MBM27128-30   300 ns max.

- ■ TTL compatible inputs/outputs
- ■ Three-state output with OR-tie capability
- ■ Output Enable $\overline{G}$ pin provides precise control of the data bus
- ■ Single +5V operation
- ■ Standard 28-pin DIP package
- ■ Pin compatible with Intel 27128

Cerdip Package
DIP-28C-C01

Ceramic Package
LCC-32C-A01
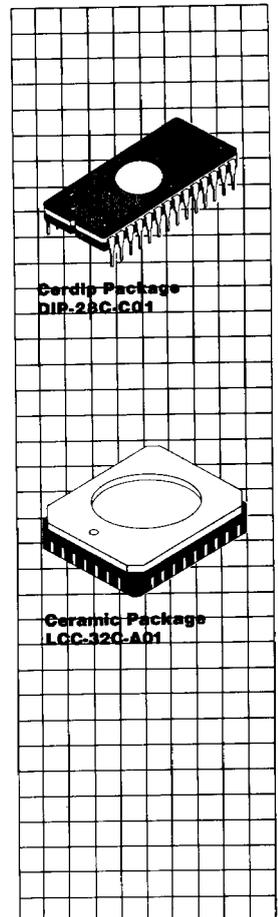
Quick Pro™ is a trademark of Fujitsu Microelectronics Inc.
int$_e$ligent Programming™ is a trademark of Intel Corporation.

MBM27128-20
MBM27128-25
MBM27128-30

MBM27128 Block Diagram and Pin Assignments
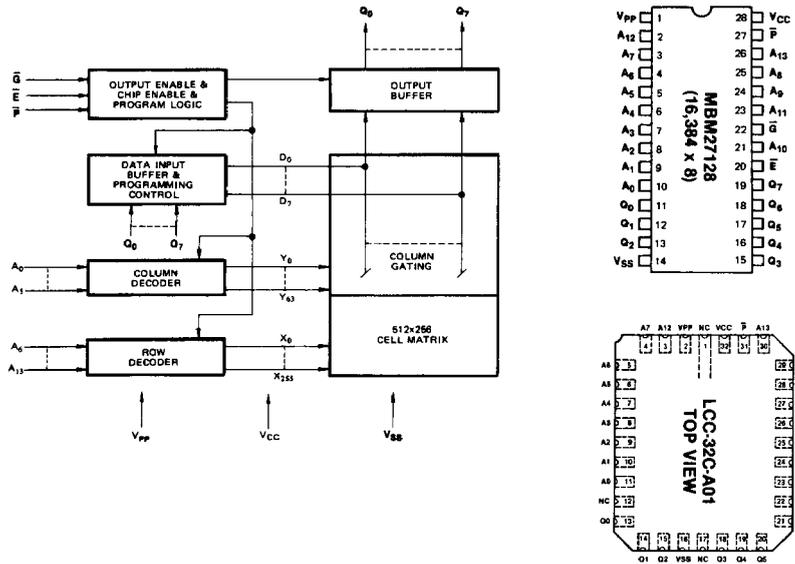
Absolute Maximum Ratings
(See Note)

Parameter	Symbol		Unit
Temperature Under Bias	T_A	−25 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C
Inputs/Outputs with Respect to V_{SS}	V_{IN}, V_{OUT}	−0.6 to +7	V
V_{PP} with Respect to V_{SS}	V_{PP}	−0.6 to +22	V
V_{CC} with Respect to V_{SS}	V_{CC}	−0.6 to +7	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Functions and Pin Connections

Function (DIP Pin No.)

Mode	Address Input A_0-A_{13} (2-10, 23-26, 21)	Data Q_0-Q_7 (11-13, 15-19)	$\overline{E}$ (20)	$\overline{G}$ (22)	$\overline{P}$ (27)	V_{CC} (28)	V_{PP} (1)	V_{SS} (14)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	V_{SS}
Output Disable	Don't Care	High Z	V_{IL}	V_{IH} / Don't Care	Don't Care / V_{IL}	V_{CC}	V_{CC}	V_{SS}
Stand by	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{CC}	V_{SS}
Program	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	V_{CC}	V_{PP}	V_{SS}
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{PP}	V_{SS}
Program Inhibit	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{PP}	V_{SS}

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Capacitance
($T_A = 25°C$, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance ($V_{IN} = 0V$)	C_{IN}	—	4	6	pF
Ouput Capacitance ($V_{OUT} = 0V$)	C_{OUT}	—	8	12	pF

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
V_{CC} Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
V_{PP} Supply Voltage	V_{PP}	$V_{CC} - 0.6$	—	$V_{CC} + 0.6$	V	0°C to +70°C
Input High Voltage	V_{IH}	2.0	—	$V_{CC} + 1$	V	
Input Low Voltage	V_{IL}	−0.1	—	0.8	V	

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current ($V_{IN} = 5.5V$)	I_{LI}	—	—	10	μA
Output Leakage Current ($V_{OUT} = 5.5V$)	I_{LO}	—	—	10	μA
V_{CC} Standby Current ($\overline{E} = V_{IH}$)	I_{CC1}	—	—	35	mA
V_{CC} Supply Current ($\overline{E} = V_{IL}$)	I_{CC2}	—	—	100	mA
V_{PP} Supply Current ($V_{PP} = V_{CC} \pm 0.6V$)	I_{PP}	—	—	5	mA
Output Low Voltage ($V_{OL} = 2.1mA$)	V_{OL}	—	—	0.45	V
Output High Voltage ($I_{OH} = -400μA$)	V_{OH}	2.4	—	—	V

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol Alternate	Standard*	MBM27128-20 Min	MBM27128-20 Max	MBM27128-25 Min	MBM27128-25 Max	MBM27128-30 Min	MBM27128-30 Max	Unit
Address Access Time	t_{ACC}	TAVQV		200		250		300	ns
$\overline{E}$ to Output Delay	t_{CE}	TELQV		200		250		300	ns
$\overline{G}$ to Output Delay	t_{OE}	TGLQV		70		100		120	ns
Address to Hold Time	t_{OH}	TAXQX	0		0		0		ns
$\overline{E}$ or $\overline{G}$ High to Output Float	t_{DF}	TGHQZ, TEHQZ	0	60	0	60	0	105	ns

AC Test Conditions
(Including programming)

Input Pulse levels:	0.8V to 2.2V
Input Rise and Fall Time:	≤20nsec
Timing Measurement Reference Levels:	1.0V and 2.0V for inputs
	0.8V and 2.0V for outputs
Output Load:	1 TTL gate and $C_L = 100$ pF

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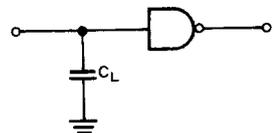
Operation Timing Diagram
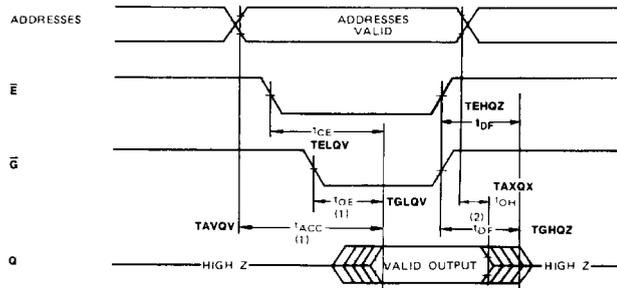
Note 1. $\bar{G}$ may be delayed up to TAVQV-TGLQV after falling edge of $\bar{E}$ without impact on TAVQV.

Notes 2. TGHDZ or TEHQZ is specified from $\bar{G}$ or $\bar{E}$ respectively, which ever occurs first.

Programming/Erasing Information

Memory Cell Description

The MBM27128 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 1). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 2). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 2.

Conventional Programming

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27128 has all 131,072-bits in the "1" or high state. "0's" are loaded into the MBM27128

through the procedure of programming.

The programming mode is entered when +21V is applied to the V_{PP} pin and $\bar{E}$ and $\bar{P}$ are both at V_{IL}. During programming, $\bar{E}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and V_{SS} is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. Eight bit patterns are placed on the respective output pins. The voltage levels should be standard TTL levels. When both

the address and data are stable, 50 msec, TTL low level pulse is applied to the $\bar{P}$ input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\bar{P}$ input is prohibited when programming.

Fig. 1 — Memory Cell
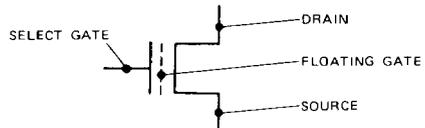
Fig. 2 — Memory Cell Threshold Shift
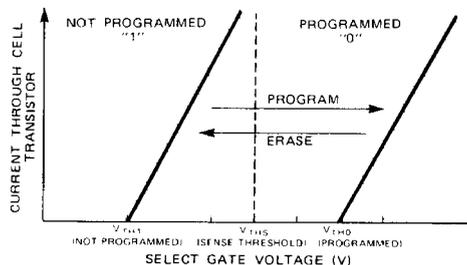
Programming/Erasure
Information, continued

"Quick Pro™" Programming

In addition to the standard 50 millisecond pulse width programming procedure, the MBM27128 can be programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The algorithm (shown in figure 3) utilizes a sequence of 1 millisecond pulse to program each location. This algorithm will typically yield a savings of 86% in programming time per device when utilized in commercially available programmers. However, in custom programmer designs that require less overhead the savings can be even greater.

The programming mode is entered when +6V is applied to the VCC pin followed by applying +21V to VPP pin. A TTL low input must be applied to the E input and a TTL high input must be applied to the G input. After the programming voltages and TTL levels have stabilized, a sequence of 1 millisecond pulses must be applied to the P pin for programming. After each pulse, a pulse counter must be incremented and the location should be checked for accuracy. Upon verification, an additional sequence of 1 millisecond pulses equal to the present value of the pulse counter must be applied to the location to ensure proper levels of stored charge. An alternate approach to the additional pulses would be to apply a single TTL low pulse with a width equivalent to the value of the pulse counter multiplied by 1 millisecond. When the pulse counter reaches a maximum of 20, the verification procedure is skipped and a flag is set to indicate a program failure. Upon completion of programming of the entire device, a final array verification (all locations) is required. All Fujitsu devices will typically require only two 1 millisecond pulses (one initial and one additional) to reach sufficient stored charge levels.

Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the MBM27128 to an ultraviolet light source. A dosage of 15W-seconds/cm² is required to completely erase an MBM27128. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with intensity of 12,000µW/cm² for 15 to 20 minutes. The MBM27128 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM27128 and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM27128 and such exposure should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

Figure 3. — Quick Pro™ Flow Chart

$V_{CC} = 6V \pm 0.25V$
$V_{PP} = 21V \pm 0.5V$

$T_{pw} = 1$ ms $\pm 50\mu$s
(* = X ms ± 5%)

Q: START ADDRESS
N: STOP ADDRESS

MAXIMUM 40 ms + α/BYTE
MINIMUM 2 ms + α/BYTE

(FOR EXAMPLE
64K BIT EPROM
MAXIMUM 320sec + β
MINIMUM 16sec + β)
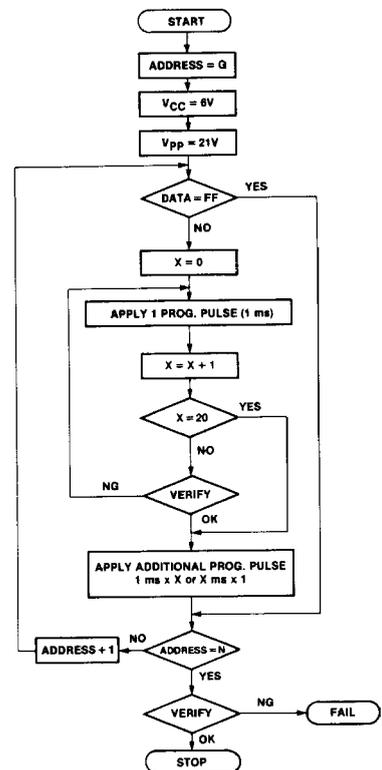
QUICK PRO™ IS A TRADEMARK OF FUJITSU LIMITED

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Programming Characteristics

DC Characteristics

($T_A = 25 \pm 5°C$,
$V_{CC} = 5V \pm 5\%$ (Conventional),
$V_{CC} = 6V \pm 0.25V$ (Quick Pro™)
$V_{PP} = 21V \pm 0.5V$)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	—	10	μA	$V_{IN} = 5.25V/0.45V$
V_{PP} Supply Current During Programming Pulse	I_{PP2}	—	30	mA	$\overline{E} = \overline{P} = V_{IL}$
V_{PP} Supply Current During Verify	I_{PP3}	—	5	mA	$\overline{E} = V_{IL}$ $\overline{P} = V_{IH}$
V_{PP} Supply Current Program Inhibit (Active)	I_{PP4}	—	5	mA	$\overline{E} = V_{IH}$
V_{CC} Supply Current Program Inhibit	I_{CC1}	—	35	mA	$\overline{E} = V_{IH}$
V_{CC} Supply Current Program & Verify	I_{CC2}	—	100	mA	—
Input Low Voltage	V_{IL}	−0.1	+0.8	V	—
Input High Voltage	V_{IH}	2.0	$V_{CC} +1$	V	—
Output Low Voltage During Verify	V_{OL}	—	0.45	V	$I_{OL} = 2.1$ mA
Output High Voltage During Verify	V_{OH}	2.4	—	V	$I_{OH} = -400\mu A$

Note 1. V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

Note 2. V_{PP} must not be greater than 21.5 volts including overshot. Permanent device change may occur if the device is taken out or put into socket remaining $V_{PP} = 21$ volts. Also, during $\overline{E} = \overline{P} = V_{IL}$, V_{PP} must not be switched from V_{CC} to 21 volts or vise-versa.

AC Characteristics

($T_A = 25 \pm 5°C$,
$V_{CC} = 5V \pm 5\%$ (Conventional),
$V_{CC} = 6V \pm 0.25V$ (Quick Pro™)
$V_{PP} = 21V \pm 0.5V$)

Parameter		Symbol	Min	Typ	Max	Unit
Address Setup Time		TAVPL	2	—	—	μS
Chip Enable Setup Time		TELPL	2	—	—	μS
Output Enable Time	1	TDZGL	2	—	—	μS
Data Setup Time		TDVPL	2	—	—	μS
Address Hold Time		TGHAX	0	—	—	μS
Data Hold Time	1	TPHDZ	2	—	—	μS
Output Enable to Output Float Delay		TGHQZ	—	—	130	ns
Data Valid from Output Enable		TGLQV	—	—	150	ns
V_{PP} Setup Time		TVPPHPL	2	—	—	μS
$\overline{P}$ Pulse Width-Conventional		TPLPH	25	50	55	ms
$\overline{P}$ Pulse Width-Quick-Pro™		TPLPH	0.95	1.00	1.05	ms

Note 1 TPHDZ + TDZGL ≥ 50μs.

Programming Waveform

MBM27128-20
MBM27128-25
MBM27128-30

Package Dimensions
Dimensions in inches
(millimeters)

**28-Lead Cerdip
(With Transparent Lid)
Dual In-Line Package
DIP-28C-C01**

R .025(0.64)
REF

.350(8.89)DIA
TYP

.570(14.48)
.595(15.11)

.600(15.24)
.625(15.88)

0°~15°

.600(15.24)REF

.008(0.20)
.014(0.36)

1,435(36.45)
1,500(38.10)

.100(2.54)MAX

.230(5.84)MAX

.120(3.05)
.150(3.81)

.090(2.29)
.110(2.79)

.042(1.07)
.062(1.57)

.032(0.81)
REF

.020(0.51)
.050(1.27)

1.300(33.02)REF

.013(0.33)
.023(0.58)

**32-Pin Leadless Chip Carrier
LCC-32C-A01**

*PIN 1 INDEX

.280(7.11)
DIA TYP

.545(13.84)
.560(14.22)

R.008(0.20)TYP
(32PLCS)

.015(0.38)

PIN 1 INDEX

.400(10.16)
TYP

.050(1.27)
TYP

.040(1.02)TYP
(3PLCS)

.050(1.27)
TYP

.025(0.64)
TYP

.045(1.14)TYP

.445(11.30)
.460(11.68)

.130(3.30)MAX

.300(7.62)TYP

*Shape of Pin 1 index: Subject to change without notice

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