



MM54C30/MM74C30 8-Input NAND Gate

General Description

The logical gate employs complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption and high noise immunity. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers familiar with the standard 54/74 logic family.

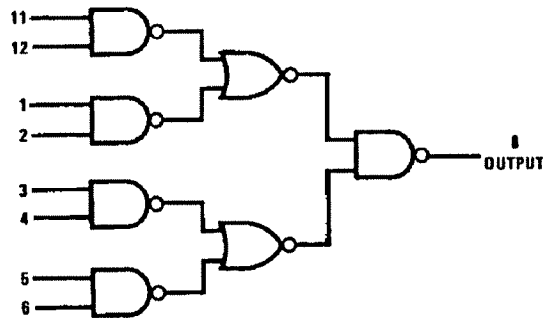
All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

- Wide supply voltage range
- Guaranteed noise margin
- High noise immunity
- Low power
- TTL compatibility

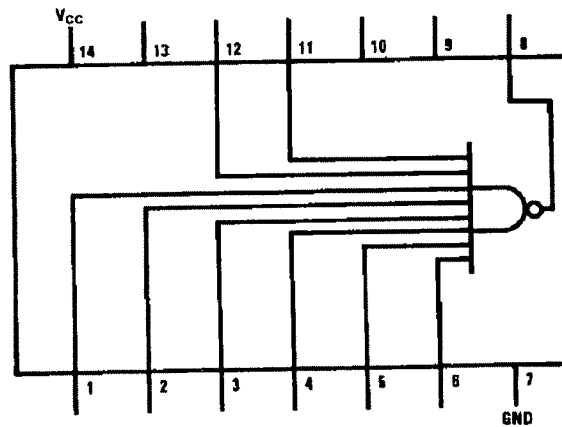
3.0V to 15V
1.0V
0.45 V_{CC} (typ.)
Fan out of 2
driving 74L

Logic and Connection Diagrams



TL/F/5880-1

Dual-In-Line Package



TL/F/5880-2

Top View

Order Number MM54C30* or MM74C30*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at any Pin $-0.3V$ to $V_{CC} + 0.3V$

Operating Temperature Range (T_A)

MM54C30 $-55^{\circ}C$ to $+125^{\circ}C$

MM74C30 $-40^{\circ}C$ to $+85^{\circ}C$

Storage Temperature Range (T_S) $-65^{\circ}C$ to $+150^{\circ}C$

Power Dissipation (P_D)

Dual-In-Line 700 mW

Small Outline 500 mW

Operating V_{CC} Range 3.0V to 15V

Absolute Maximum V_{CC} 18V

Lead Temperature (T_L)
(Soldering, 10 seconds) $260^{\circ}C$

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	3.5			V
		$V_{CC} = 10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$			1.5	V
		$V_{CC} = 10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V, I_O = -10 \mu A$	4.5			V
		$V_{CC} = 10V, I_O = -10 \mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V, I_O = 10 \mu A$			0.5	V
		$V_{CC} = 10V, I_O = 10 \mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.01	15	μA

CMOS/LPTTL INTERFACE

$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
		74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$			0.8	V
		74C, $V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V, I_O = -360 \mu A$	2.4			V
		74C, $V_{CC} = 4.75V, I_O = -360 \mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V, I_O = 360 \mu A$			0.4	V
		74C, $V_{CC} = 4.75V, I_O = 360 \mu A$			0.4	V

OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (short circuit current)

I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5V, V_{OUT} = 0V$ $T_A = 25^{\circ}C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V, V_{OUT} = 0V$ $T_A = 25^{\circ}C$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5V, V_{OUT} = V_{CC}$ $T_A = 25^{\circ}C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V, V_{OUT} = V_{CC}$ $T_A = 25^{\circ}C$	8.0	16		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

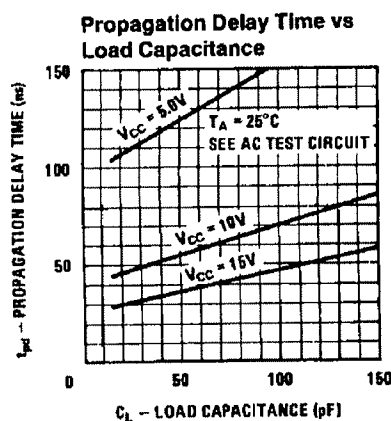
AC Electrical Characteristics* $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5\text{V}$		125	180	ns
		$V_{CC} = 10\text{V}$		55	90	ns
C_{IN}	Input Capacitance	(Note 2)		4.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		26		pF

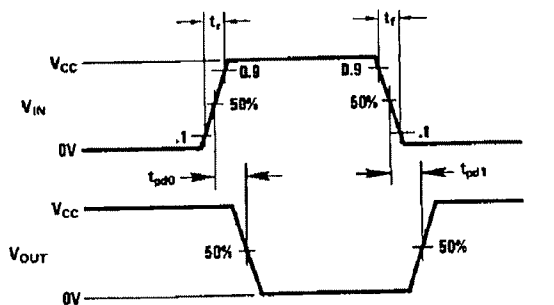
*AC Parameters are guaranteed by DC correlated testing.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics, application note—AN-90.

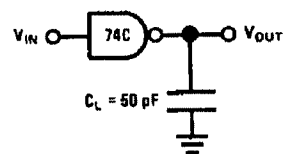
Typical Performance Characteristics

TL/F/5880-3

Switching Time Waveforms

TL/F/5880-4

Note: Delays Measured with Input t_r , $t_f = 20\text{ ns}$.

AC Test Circuit

TL/F/5880-5