The better Display Solution

LCD Module
TFT070C008000480T1B102

DATA SHEET

Product specification V 1.0

Approval of Specification

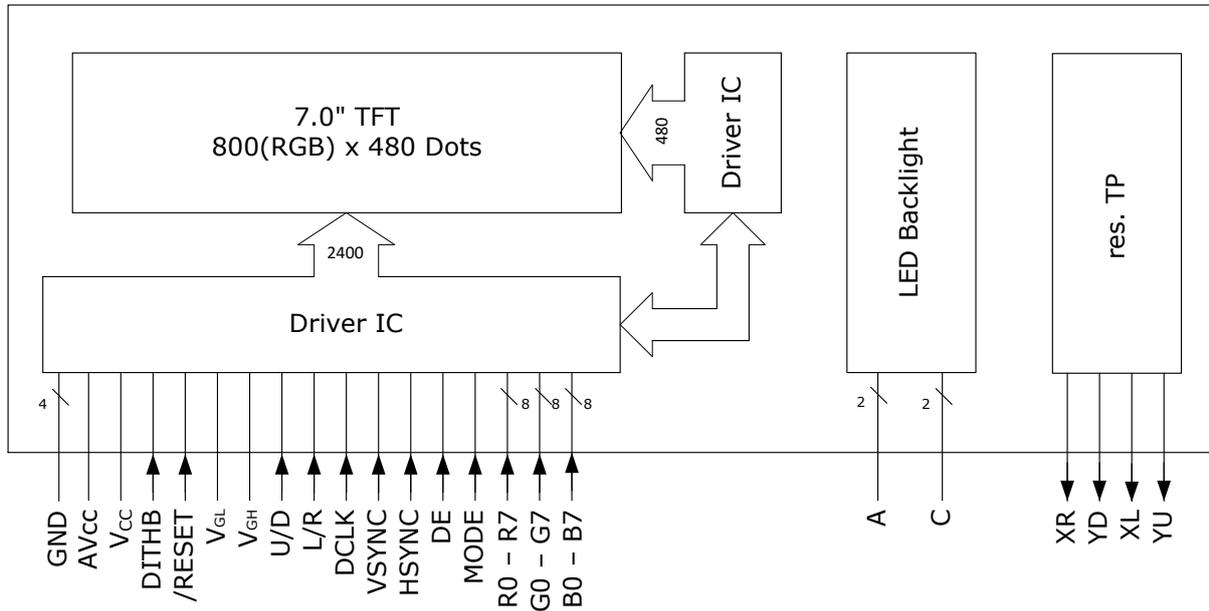|	Approved by	Date
admatec	Dipl.-Ing. H. Gharbi	2016-07-20
Customer		

This product complies to EU directive 2002/95/EC (RoHS) of January 27th, 2003.

1 General data

Table 1.1: General data

No.	Item	Content
1.	module size	164.9 mm (W) * 100.0 mm (H) * 6.8 mm (D)
2.	visible area	156.68 mm (W) * 88.52 mm (H)
3.	active area	154.08 mm (W) * 85.92 mm (H)
4.	dot pitch	0.064 mm (W) * 0.179 mm (H)
5.	number of dots	800 *3(RGB)(W) * 480 (H)
6.	LCD type	TFT, 16.7M, transmissive
7.	backlight	LED white
8.	controller	HX8264-D and HX8664-B
9.	interface	24-bit RGB
10.	touch panel	resistive (res)
11.	weight	195 g (approx.)

5 Block diagram

Figure 5.1 : Block diagram of TFT070C008000480T1B102

6 Interface description

6.1 Interface of LCD

Table 6.1: LCD interface description

Symbol	Pin no.	IO	Function
A	1	PWR	backlight anode
A	2	PWR	backlight anode
C	3	PWR	backlight cathode
C	4	PWR	backlight cathode
GND	5	PWR	ground
NC	6	--	not connected
V$_{CC}$	7	PWR	power supply
MODE	8	I	Mode selection: "H" => DE mode "L" => SYNC mode
DE	9	I	data enable signal, active high
VSYNC	10	I	vertical synchronous signal, negative polarity
HSYNC	11	I	horizontal synchronous signal, negative polarity
B7	12	I	blue data bus
B6	13	I	
B5	14	I	
B4	15	I	
B3	16	I	
B2	17	I	
B1	18	I	
B0	19	I	
G7	20	I	green data bus
G6	21	I	
G5	22	I	
G4	23	I	
G3	24	I	
G2	25	I	
G1	26	I	
G0	27	I	
R7	28	I	red data bus
R6	29	I	
R5	30	I	
R4	31	I	
R3	32	I	
R2	33	I	
R1	34	I	
R0	35	I	
GND	36	PWR	ground
DCLK	37	I	clock for input data
GND	38	PWR	ground

L/R	39	I	source left or right sequence control
U/D	40	I	gate up or down scan control
V$_{GH}$	41	PWR	positive power of TFT
V$_{GL}$	42	PWR	negative power of TFT
AV$_{CC}$	43	PWR	analog power supply
/RESET	44	I	reset pin
NC	45	--	not connected
NC	46	--	not connected
DITHB	47	I	internal dithering setting: "H" => 6bit resolution "L" => 8bit resolution
GND	48	PWR	ground
NC	49	--	not connected
NC	50	--	not connected

FPC: 50 pin, 0.5 mm pitch

6.2 Interface of res. TP

Table 6.2: Res. TP interface description

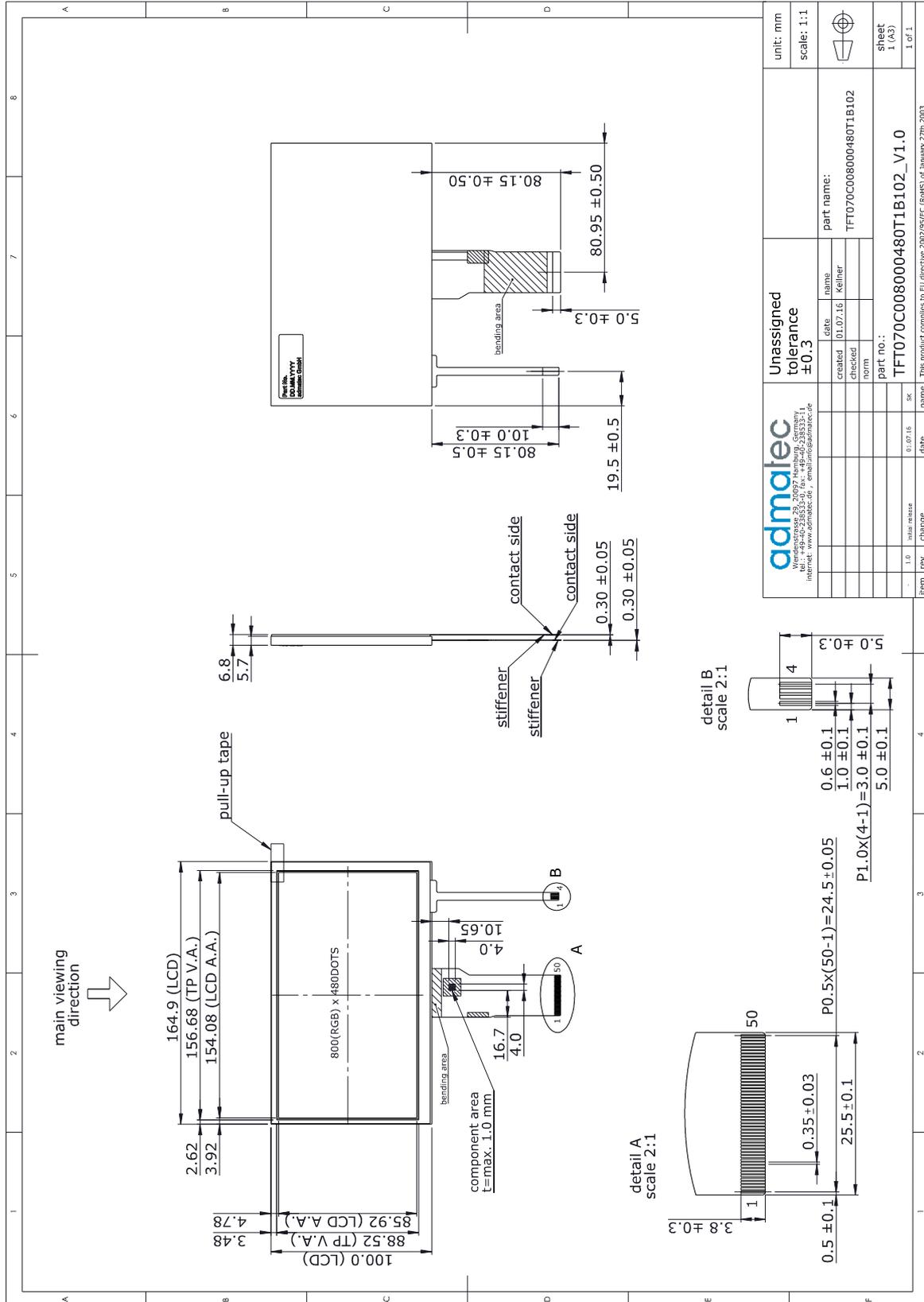| Symbol	Pin no.	IO	Function
XL	1	O	left
YD	2	O	down
XR	3	O	right
YU	4	O	up

FPC: 4 pin, 1.0mm pitch

10 Drawing

Fig 10.1: Drawing of TFT070C008000480T1B102