

M5M5255BP,FP,KP-70,-85,-10,-12,-70L,-85L,-10L,-12L,-70LL,-85LL,-10LL,-12LL

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5255BP, FP, KP is a 262144-bit CMOS static RAM organized as 32768-words by 8-bits which is fabricated using high-performance double polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM.

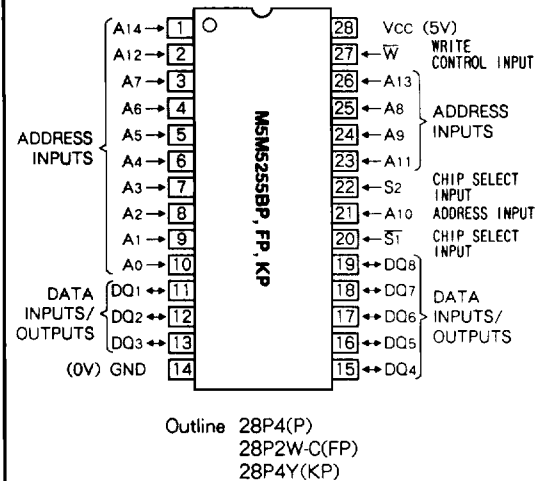
The M5M5255BP, FP, KP provides two chip select input ($\overline{S_1}$, S_2). It is ideal for battery back up application.

FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5255BP, FP, KP-70	70ns	70mA	2mA
M5M5255BP, FP, KP-85	85ns		
M5M5255BP, FP, KP-10	100ns		
M5M5255BP, FP, KP-12	120ns		
M5M5255BP, FP, KP-70L	70ns	70mA	100 μ A
M5M5255BP, FP, KP-85L	85ns		(V _{CC} = 5.5V)
M5M5255BP, FP, KP-10L	100ns		50 μ A
M5M5255BP, FP, KP-12L	120ns		(V _{CC} = 3.0V)
M5M5255BP, FP, KP-70LL	70ns	70mA	20 μ A
M5M5255BP, FP, KP-85LL	85ns		(V _{CC} = 5.5V)
M5M5255BP, FP, KP-10LL	100ns		10 μ A
M5M5255BP, FP, KP-12LL	120ns		(V _{CC} = 3.0V)

- Single +5V power supply
- No clocks, no refresh
- Data-hold on +2V power supply
- Directly TTL compatible: All inputs and outputs
- Three-state outputs: OR-tie capability
- Simple memory expansion by $\overline{S_1}$, S_2
- Common data I/O

PIN CONFIGURATION (TOP VIEW)



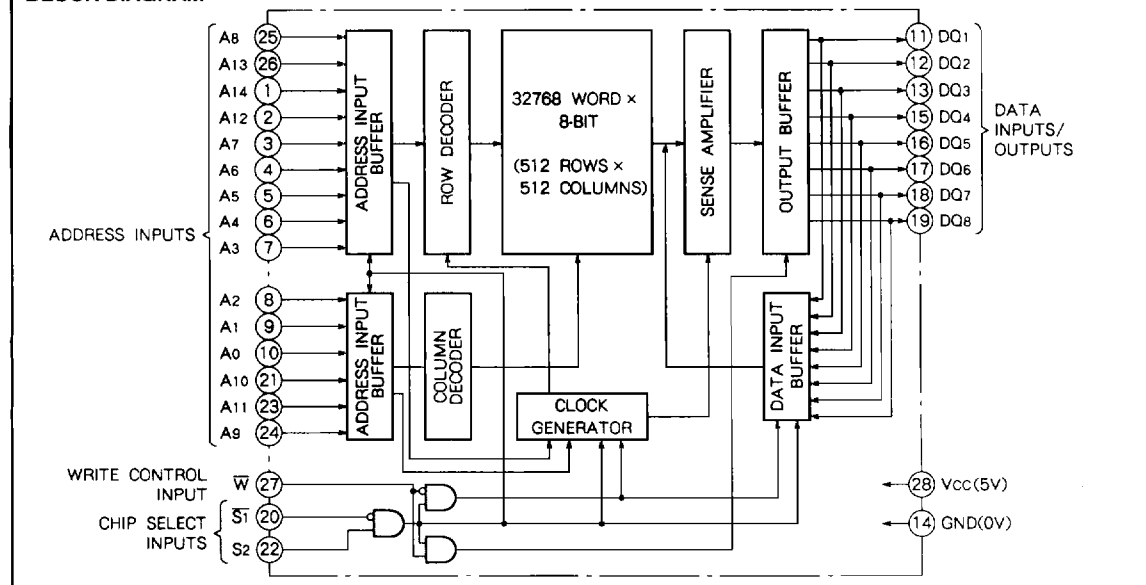
Package

- M5M5255BP28pin 600mil DIP
- M5M5255BKP28pin 300mil DIP
- M5M5255BFP28pin small outline package(SOP)

APPLICATION

Small capacity memory units

BLOCK DIAGRAM



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FUNCTION

The operation mode of the M5M5255BP, FP, KP is determined by a combination of the device control inputs $\overline{S_1}$, S_2 , and $\overline{W}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S_1}$ and the high level S_2 . The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S_1}$ or S_2 , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained.

A read cycle is executed by setting $\overline{W}$ at a high level while $\overline{S_1}$ and S_2 are in an active state ($\overline{S_1} = L$, $S_2 = H$)

When setting $\overline{S_1}$ at a high level or S_2 at a low level, the chip is in a non-selectable mode in which both reading and

writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S_1}$ and S_2 . The power supply current is reduced as low as the stand-by current which is specified as I_{cc3} or I_{cc4} , and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S_1}$	S_2	$\overline{W}$	Mode	DQ	I _{cc}
H	X	X	Non selection	High-impedance	Stand-by
X	L	X	Non selection	High-impedance	Stand-by
L	H	L	Write	Din	Active
L	H	H	Read	Dout	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage	With respect to GND	- 0.3 ~ 7	V
V _i	Input voltage		- 0.3 ~ V _{cc} + 0.3	V
V _o	Output voltage		0 ~ V _{cc}	V
T _{opr}	Operating temperature	T _a = 25 °C	0 ~ 70	°C
T _{stg}	Storage temperature		- 65 ~ 150	°C

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70 °C, V_{cc} = 5V ± 10 %, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{IH}	High input voltage		2.2		V _{cc} +0.3	V
V _{IL}	Low input voltage		- 0.3		0.8	V
V _{OH}	High output voltage	I _{OH} = - 1mA	2.4			V
V _{OL}	Low output voltage	I _{OL} = 2mA			0.4	V
I _i	Input leakage current	V _i = 0 ~ V _{cc}			± 1	μA
I _o	Output leakage current	$\overline{S_1} = V_{IH}$ or $S_2 = V_{IL}$ V _{I/O} = 0 ~ V _{cc}			± 1	μA
I _{cc1}	Active supply current(AC MOS level)	$\overline{S_1} < 0.2$, $S_2 > V_{cc} - 0.2$ output open Other inputs < 0.2 or > V _{cc} - 0.2 Min cycle		30	65	mA
I _{cc2}	Active supply current(AC TTL level)	$\overline{S_1} = V_{IL}$ or $S_2 = V_{IH}$ output open Other inputs = V _{IL} or V _{IH} Min cycle		35	70	mA
I _{cc3}	Stand by supply current	1). $S_2 \leq 0.2V$, Other inputs = 0 ~ V _{cc}			2	mA
		2). $\overline{S_1} \geq V_{cc} - 0.2V$, $S_2 \geq V_{cc} - 0.2V$, Other inputs = 0 ~ V _{cc}			100	μA
		BP,FP,KP-L BP,FP,KP-LL			20	μA
I _{cc4}	Stand by supply current	1). $S_2 = V_{IL}$ 2). $\overline{S_1} = V_{IH}$, $S_2 = V_{IH}$ Other inputs = 0 ~ V _{cc}			3	mA
C _i	Input capacitance (T _a = 25 °C)	V _i = GND, V _i = 25mVrms, f = 1MHz			6	pF
C _o	Output capacitance (T _a = 25 °C)	V _o = GND, V _o = 25mVrms, f = 1MHz			8	pF

Note 1. Direction for current flowing into IC is indicated as positive (no mark)

2. Typical value is V_{cc} = 5V, T_a = 25 °C

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SWITCHING CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V ± 10%, unless otherwise noted)

Read cycle

Symbol	Parameter	Limits												Unit
		M5M5255-70			M5M5255-85			M5M5255-10			M5M5255-12			
		M5M5255-70L			M5M5255-85L			M5M5255-10L			M5M5255-12L			
		M5M5255-70LL			M5M5255-85LL			M5M5255-10LL			M5M5255-12LL			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
tCR	Read cycle time	70			85			100			120			ns
ta(A)	Address access time			70			85			100			120	ns
ta(S1)	Chip select 1 access time			70			85			100			120	ns
ta(S2)	Chip select 2 access time			70			85			100			120	ns
tdis(S1)	Output disable time after S ₁ high			30			30			35			40	ns
tdis(S2)	Output disable time after S ₂ low			30			30			35			40	ns
ten(S1)	Output enable time after S ₁ low	5			10			10			10			ns
ten(S2)	Output enable time after S ₂ high	5			10			10			10			ns
tv(A)	Data valid time after address change	20			20			20			20			ns

TIMING REQUIREMENTS (Ta = 0~70°C, Vcc = 5V ± 10%, unless otherwise noted)

Write cycle

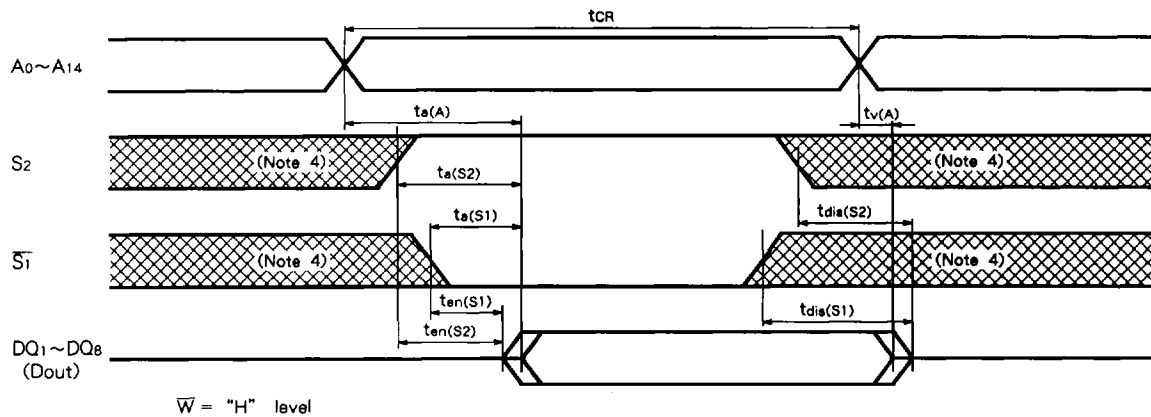
Symbol	Parameter	Limits												Unit
		M5M5255-70			M5M5255-85			M5M5255-10			M5M5255-12			
		M5M5255-70L			M5M5255-85L			M5M5255-10L			M5M5255-12L			
		M5M5255-70LL			M5M5255-85LL			M5M5255-10LL			M5M5255-12LL			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
tCW	Write cycle time	70			85			100			120			ns
tw(W)	Write pulse width	55			60			60			70			ns
tsu(A)	Address set up time	0			0			0			0			ns
tsu(A-WH)	Address set up time with respect to $\overline{W}$ high	65			75			80			85			ns
tsu(S1)	Chip select set up time	65			75			80			85			ns
tsu(S2)	Chip select set up time	65			75			80			85			ns
tsu(D)	Data set up time	30			35			35			40			ns
th(D)	Data hold time	0			0			0			0			ns
trec(W)	Write recovery time	0			0			0			0			ns
tdis(W)	Output disable time after $\overline{W}$ low			25			30			35			40	ns
ten(W)	Output enable time after $\overline{W}$ high	5			5			10			10			ns

**M5M5255BP,FP,KP-70,-85,-10,-12,-70L,-85L,
-10L,-12L,-70LL,-85LL,-10LL,-12LL**

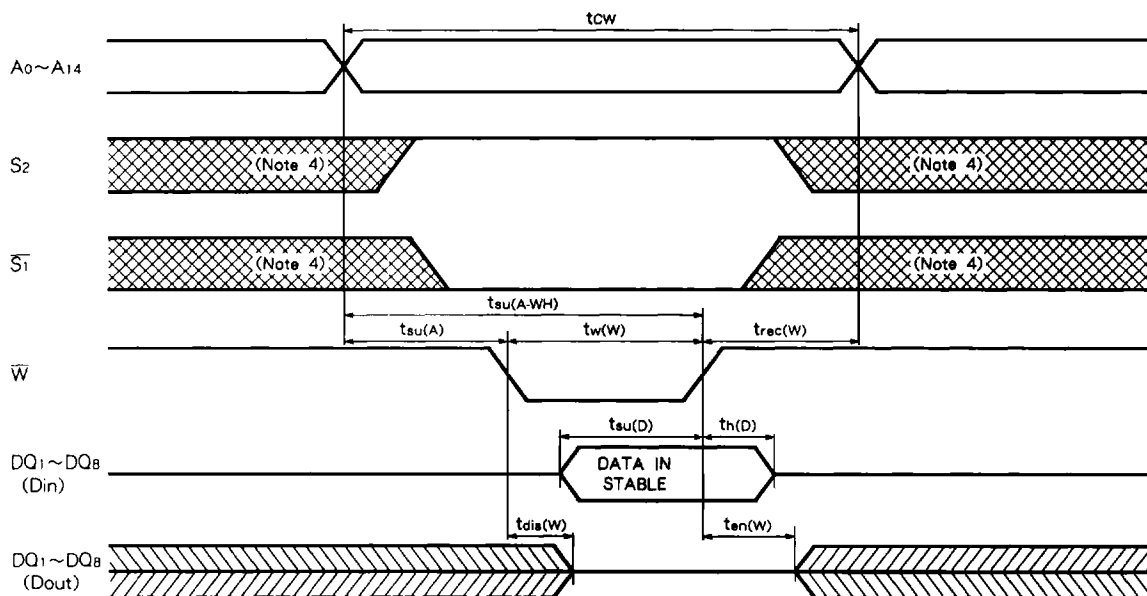
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TIMING DIAGRAM

Read cycle



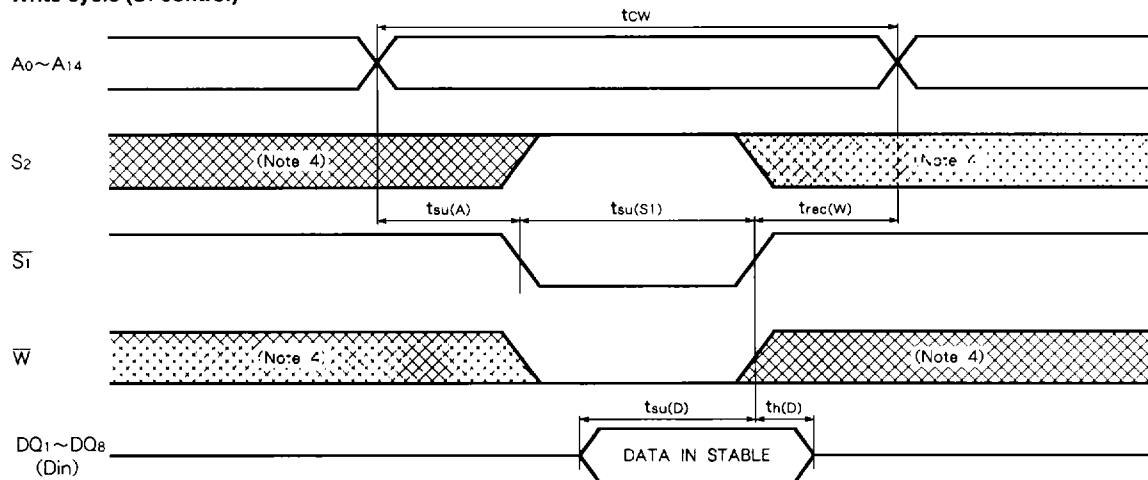
Write cycle ($\bar{W}$ control)



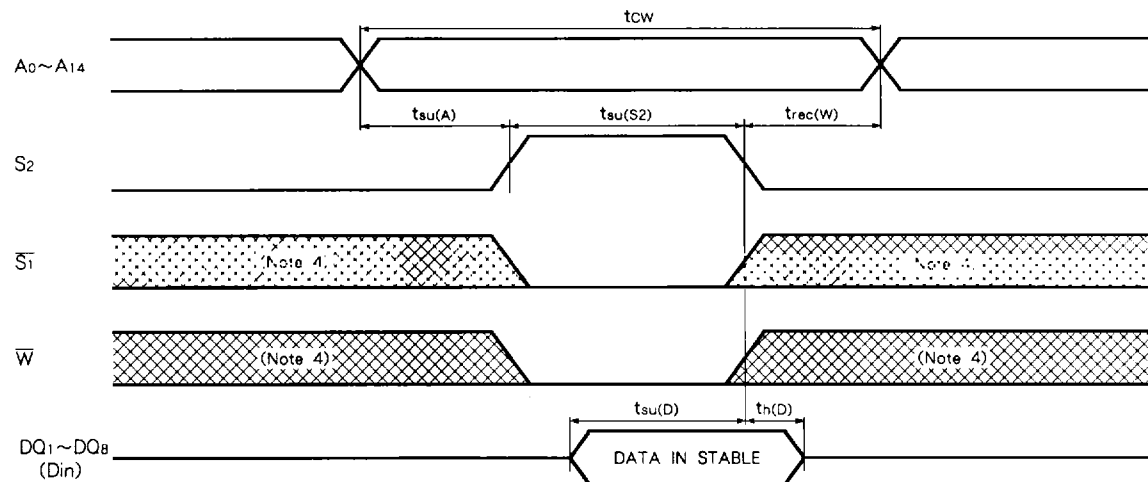
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Write cycle ($\overline{S1}$ control)



Write cycle ($S2$ control)



Note 3 : Test condition

Input pulse levels..... $V_{IH} = 2.4V$, $V_{IL} = 0.6V$

Input rise and fall time10ns

Reference levels $V_{OH} = V_{OL} = 1.5V$

Transition is measured $\pm 500mV$ from steady state voltage.(for t_{en} , t_{dis})

Output loads..... Fig. 1, $C_L = 100pF$ (BP, FP, KP-85, -10, -12, -85L, -10L, -12L, -85LL, -10LL, -12LL)

$C_L = 30pF$ (BP, FP, KP-70, -70L, -70LL)

$C_L = 5pF$ (for t_{en} , t_{dis})

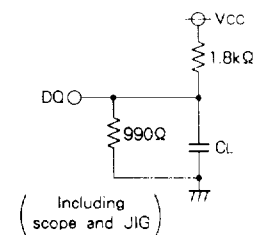


Fig. 1 Output load

Note 4. Hatching indicates the state is don't care.

5. Writing is executed while $S2$ high overlaps $\overline{S1}$ and $\overline{W}$ low.

6. If $\overline{W}$ goes low simultaneously with or prior to $\overline{S1}$ low or $S2$ high, the output remains in the high-impedance state.

7. Don't apply inverted phase signal externally when DQ pin is in output mode.

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POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{CC(PD)}	Power down supply voltage		2			V
V _{I(S1)}	Chip select input S ₁	2.2V ≤ V _{CC(PD)}	2.2			V
		2V ≤ V _{CC(PD)} ≤ 2.2V		V _{CC(PD)}		
V _{I(S2)}	Chip select input S ₂	4.5V ≤ V _{CC(PD)}			0.8	V
		V _{CC(PD)} < 4.5V			0.2	V
I _{CC(PD)}	Power down supply current	V _{CC} =3V, Other inputs=0~3V			2	mA
		1). S ₂ ≤ 0.2V 2). S ₁ ≥ V _{CC} -0.2V, S ₂ ≥ V _{CC} -0.2V			50	μA
					10*	μA

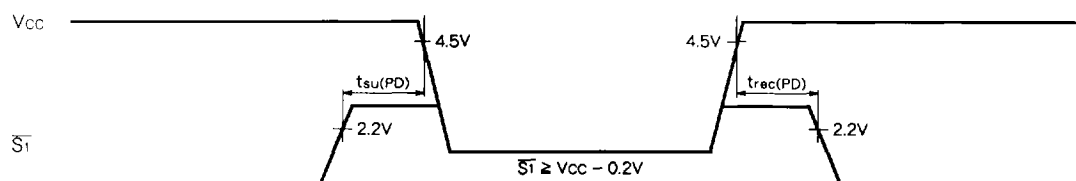
* Ta = 25°C, I_{CC(PD)} = 1 μA

TIMING REQUIREMENTS (Ta = 0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t _{su(PD)}	Power down setup time		0			ns
t _{rec(PD)}	Power down recovery time		t _{CR}			ns

POWER DOWN CHARACTERISTICS

S₁ control



S₂ control

