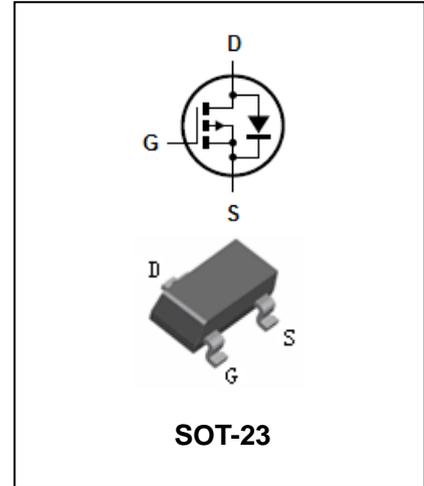


## P-Channel Enhancement Mode Vertical D-MOS Transistor

### BSS84

#### FEATURES

- Voltage controlled p-channel small signal switch
- High density cell design for low RDS(ON)
- High saturation current



#### APPLICATIONS

- Line current interrupter in telephone sets
- Relay, high speed and line transformer drivers

#### ORDERING INFORMATION

Type No.	Marking	Package Code
BSS84	SP	SOT-23

#### MAXIMUM RATING @ Ta=25°C unless otherwise specified

Symbol	Parameter	Value	Units	
V <sub>DS</sub>	Drain-Source voltage	-50	V	
V <sub>GSO</sub>	Gate -Source voltage	±20	V	
I <sub>D</sub>	Drain current (Note 1)	Continuous Pulse	-130 -520	mA
P <sub>D</sub>	Power Dissipation (Note 1)	0.36	W	
	Derate Above 25°C	2.9	mW/°C	
R <sub>θJA</sub>	Thermal resistance, Junction-to-Ambient	350	°C/W	
T <sub>J</sub> , T <sub>stg</sub>	Operating Junction and Storage Temperature	-55 to +150	°C	
T <sub>L</sub>	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300	°C	

## P-Channel Enhancement Mode Vertical D-MOS Transistor

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#### ELECTRICAL CHARACTERISTICS @ Ta=25°C unless otherwise specified

Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-50	-	-	V
Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	$I_D = -250 \mu A$ , Referenced to 25°C	-	-48	-	mV/°C
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-1mA$	-0.8	-1.7	-2	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(th)}/\Delta T_J$	$I_D = -1 mA$ , Referenced to 25°C	-	3	-	mV/°C
Gate-body Leakage	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-50V, V_{GS}=0V$	-	-	-15	$\mu A$
		$V_{DS}=-50V, V_{GS}=0V$ $T_J=125^\circ C$	-	-	-60	$\mu A$
Drain-Source on-resistance	$R_{DS(ON)}$	$V_{GS} = -5 V, I_D = -0.1 A$	-	1.2	10	$\Omega$
		$V_{GS} = -5 V, I_D = -0.1 A$ $T_J=125^\circ C$	-	1.9	17	
On-State Drain Current	$I_{D(on)}$	$V_{GS}=-5 V, V_{DS}=-10 V$	-0.6	-	-	A
Forwards Transfer admittance	$ y_{fs} $	$V_{DS}=-25V, I_D=-0.1A$	0.05	0.6	-	S
Input capacitance	$C_{ISS}$	$V_{DS}=-25V, V_{GS}=0V, f=1MHz$	-	73	-	$\mu F$
Output capacitance	$C_{OSS}$		-	10	-	
Reverse transfer capacitance	$C_{RSS}$		-	5	-	
Gate Resistance	RG	$V_{GS}=-15 mV, f=1.0 MHz$	-	9	-	$\Omega$
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD}=-30 V, I_D=-0.27A,$ $V_{GS}=-10 V, R_{GEN}=6 \Omega$	-	2.5	5	ns
Turn-On Rise Time	$t_r$		-	6.3	13	
Turn-Off Delay Time	$t_{D(OFF)}$		-	10	20	
Turn-Off Fall Time	$t_f$		-	4.8	9.6	
Total Gate Charge	$Q_g$	$V_{DS}=-25 V, I_D=-0.1A,$ $V_{GS}=-5 V$	-	0.9	1.3	nC
Gate-Source Charge	$Q_{gs}$		-	0.2	-	
Gate-Drain Charge	$Q_{gd}$		-	0.3	-	
Maximum Continuous Drain-Source Diode Forward Current	$I_S$		-	-	-0.13	A

## P-Channel Enhancement Mode Vertical D-MOS Transistor

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Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
Drain–Source Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_S=-0.26 A$ (Note 2)	-	-0.8	-1.4	V
Diode Reverse Recovery Time	$t_{rr}$	$I_F=-0.10A$	-	10	-	nS
Diode Reverse Recovery Charge	$Q_{rr}$	$d_{iF}/d_t=100 A/\mu s$ (Note 2)	-	3	-	nC

**Notes:**

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.
- Pulse Test: Pulse Width  $\delta$  300 us, Duty Cycle  $\leq 2.0\%$

# P-Channel Enhancement Mode Vertical D-MOS Transistor

## BSS84

TYPICAL CHARACTERISTICS @  $T_a=25^\circ\text{C}$  unless otherwise specified

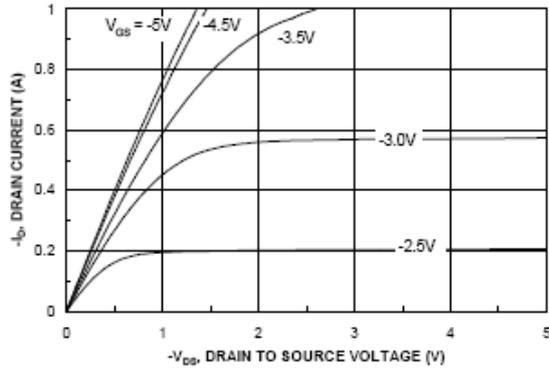


Figure 1. On-Region Characteristics.

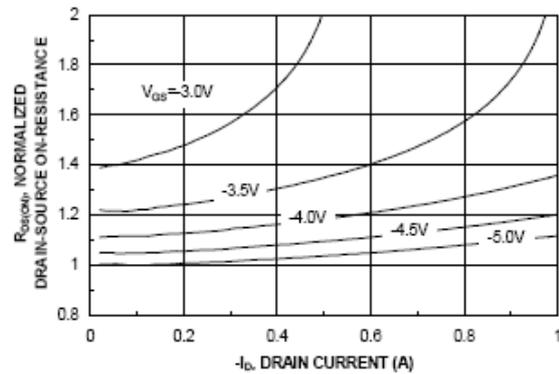


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

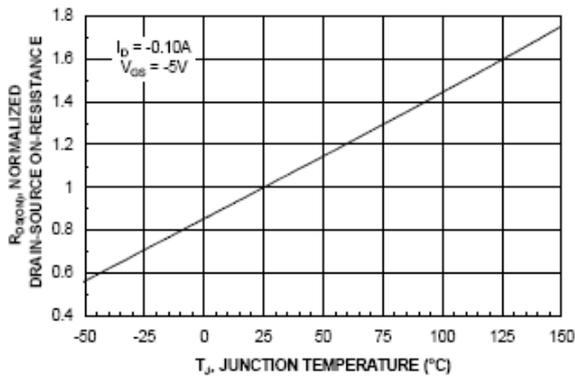


Figure 3. On-Resistance Variation with Temperature.

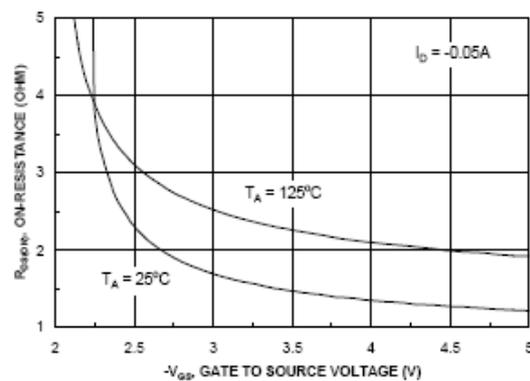


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

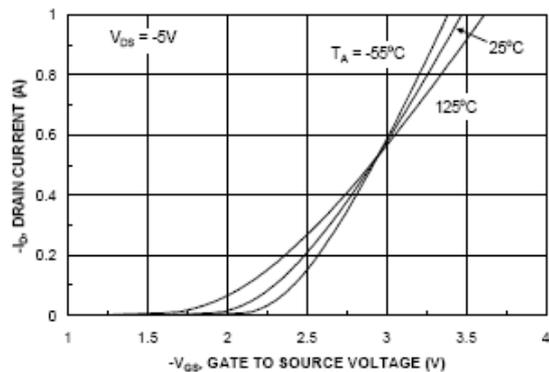


Figure 5. Transfer Characteristics.

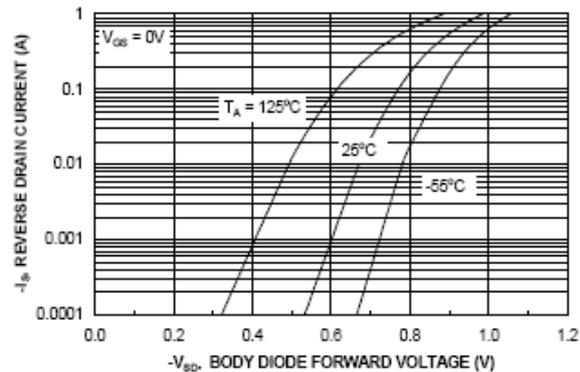


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

# P-Channel Enhancement Mode Vertical D-MOS Transistor

## BSS84

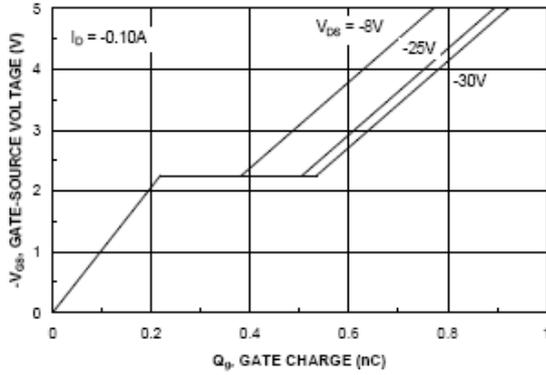


Figure 7. Gate Charge Characteristics.

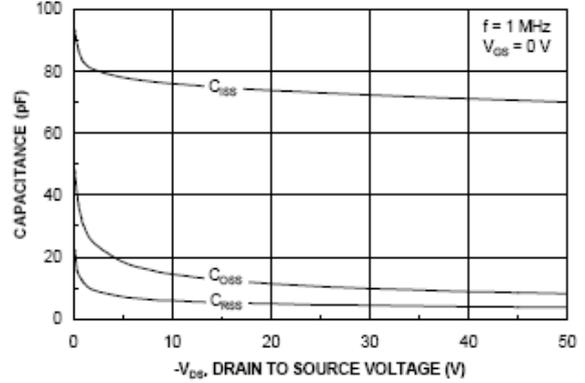


Figure 8. Capacitance Characteristics.

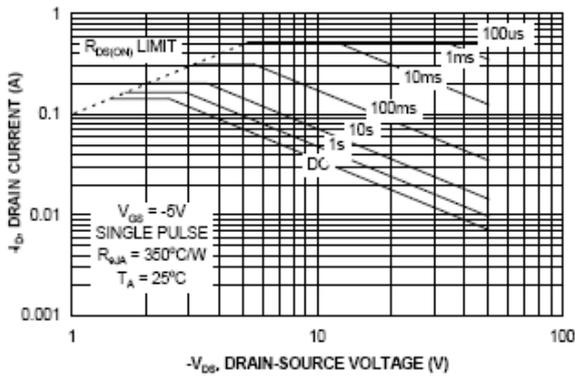


Figure 9. Maximum Safe Operating Area.

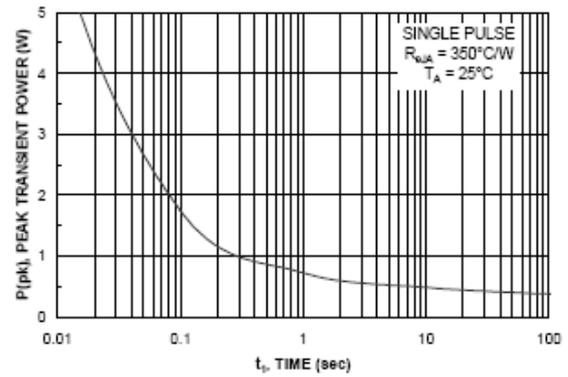


Figure 10. Single Pulse Maximum Power Dissipation.

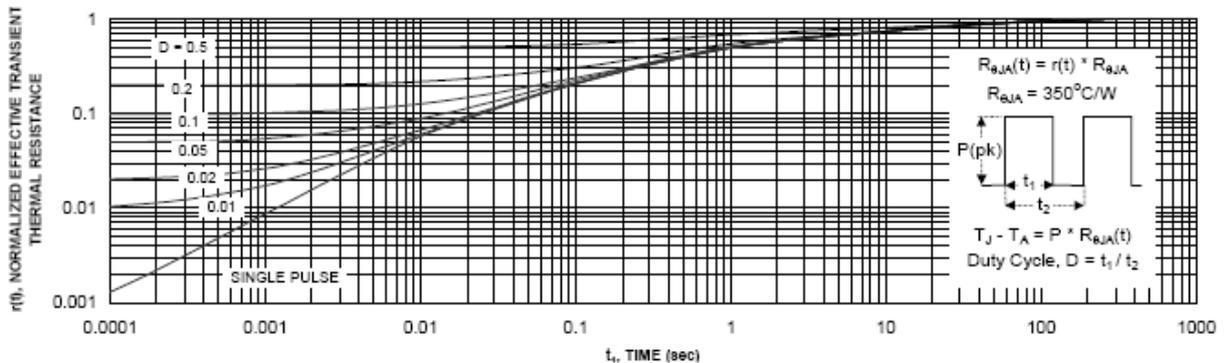


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1a. Transient thermal response will change depending on the circuit board design.

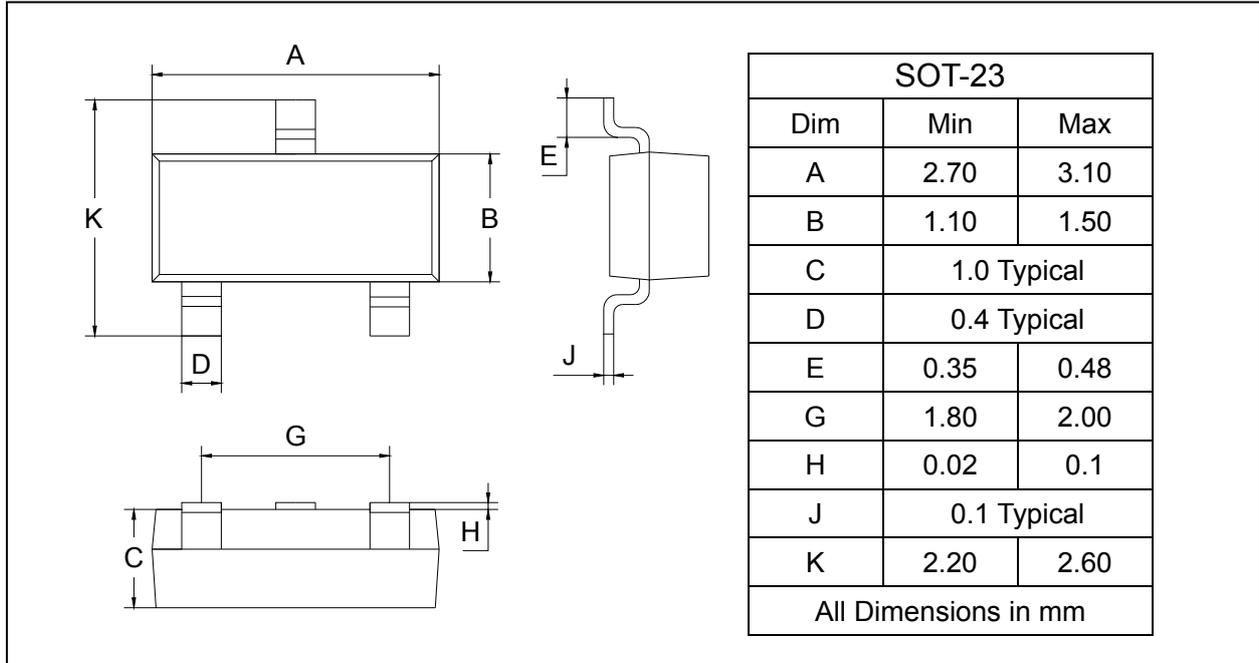
## P-Channel Enhancement Mode Vertical D-MOS Transistor

# BSS84

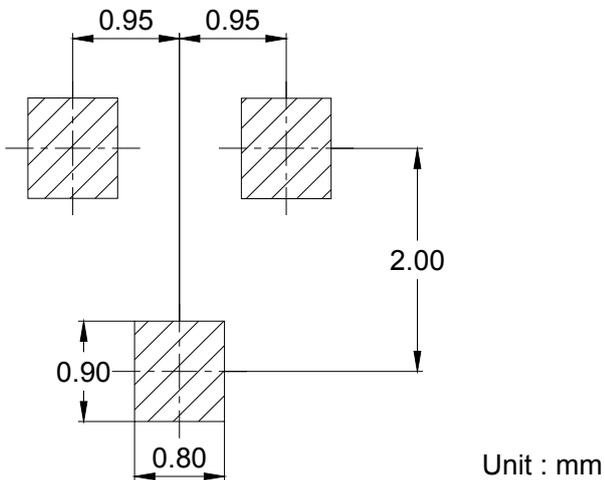
### PACKAGE OUTLINE

Plastic surface mounted package

SOT-23



### SOLDERING FOOTPRINT



### PACKAGE INFORMATION

Device	Package	Shipping
BSS84	SOT-23	3000/Tape&Reel