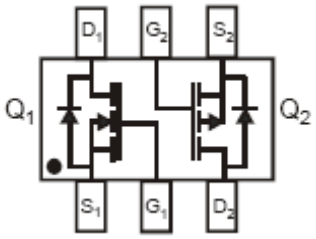
Complementary Pair Enhancement Mode Field Effect Transistor

BSS8402DW

FEATURES

- Low On-Resistance.
- Low Gate Threshold Voltage.
- Low Input Capacitance.
- Fast Switching Speed.
- Low Input/Output Leakage.
- Complementary Pair.

Lead-free



SOT-363

ORDERING INFORMATION

Type No.	Marking	Package Code
BSS8402DW	KNP	SOT-363

MAXIMUM RATING – Total Device @ Ta=25℃ unless otherwise specified

Symbol	**Parameter**	**Value**	**Units**
P_D	Power Dissipation	200	mW
$R_{\theta JA}$	Thermal resistance,Junction-to-Ambient	625	℃/W
T_J, Tstg	Junction and Storage Temperature	-55 to +150	℃

Maximum Ratings N-CHANNEL –Q_1, 2N7002 Section

@ Ta=25℃ unless otherwise specified

Symbol	**Parameter**	**Value**	**Units**
V_{DSS}	Drain-Source voltage	60	V
V_{DGR}	Drain-Gate voltage(R_{GS}≤1.0MΩ)	60	V
V_{GSS}	Gate -Source voltage continuous Pulsed	±20 ±40	V
I_D	Drain current continuous continuous@100℃ Pulsed	115 73 800	mA

Complementary Pair Enhancement Mode Field Effect Transistor
BSS8402DW

Maximum Ratings P-CHANNEL –Q_2, BSS84 Section

@ Ta=25℃ unless otherwise specified

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source voltage	-50	V
V_{DGR}	Drain-Gate voltage(R_{GS}≤1.0MΩ)	-50	V
V_{GSS}	Gate -Source voltage continuous	±20	V
I_D	Drain current continuous	-130	mA

ELECTRICAL CHARACTERISTICS @ Ta=25℃ unless otherwise specified

Q_1,2N7002 Section

Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=10μA	60	70	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1	-	2.5	V
Gate-body Leakage Forward Reverse	I_{GSS}	V_{DS}=0V, V_{GS}=20V V_{DS}=0V, V_{GS}=-20V	- -	- -	100 -100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0V	-	-	1	μA
		V_{DS}=60V,V_{GS}=0V,T_j=125℃	-	-	500	
On-state Drain Current	$I_{D(On)}$	V_{GS}=10V, V_{DS}=7.5V	0.5	1.0	-	A
Drain-Source on-voltage	$V_{DS(ON)}$	V_{GS}=10V,I_D=500mA V_{GS}=5V,I_D=50mA	- -	0.6 0.09	3.75 1.5	V
Forward transconductance	g_{FS}	V_{DS}=10V,I_D=200mA	80	-	-	mS
Static drain-Source on-resistance	$R_{DS(ON)}$	V_{GS}=5.0V,I_D=50mA V_{GS}=10V,I_D=500mA, T_j=125℃	- -	3.2 4.4	7.5 13.5	Ω
Input capacitance	C_{ISS}	V_{DS}=25V,V_{GS}=0V,f=1.0MHz	-	22	50	pF
Output capacitance	C_{OSS}		-	11	25	
Reverse transfer capacitance	C_{RSS}		-	2	5	
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = 30V, I_D= 0.2A, R_L = 150Ω, V_{GS}= 10V, R_{GEN}= 25Ω	-	7	20	ns
Turn-Off Delay Time	$t_{D(OFF)}$		-	11	20	ns

Complementary Pair Enhancement Mode Field Effect Transistor
BSS8402DW

ELECTRICAL CHARACTERISTICS @ Ta=25℃ unless otherwise specified

Q_2,BSS84 Section

Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250μA	-50	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-1mA	-0.8	-	-2	
Gate-body Leakage Forward Reverse	I_{GSS}	V_{DS}=0V, V_{GS}=20V V_{DS}=0V, V_{GS}=-20V	- -	- -	100 -100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-50V, V_{GS}=0V,T_j=25℃	-	-	-15	nA
		V_{DS}=-50V, V_{GS}=0V,T_j=125℃	-	-	-60	
		V_{DS}=-25V,V_{GS}=0V,T_j=25℃	-	-	-100	
Forward transconductance	g_{FS}	V_{DS}=-25V,I_D=-0.1A	0.05	-	-	S
Static drain-Source on-resistance	$R_{DS(ON)}$	V_{GS}=-5V,I_D=-0.1A	-	-	10	Ω
On-state drain current	$I_{D(ON)}$	V_{GS}=10V,V_{DS}=7.5V	0.5	1.0	-	A
Input capacitance	C_{ISS}	V_{DS}=-25V,V_{GS}=0V,f=1.0MHz	-	-	45	pF
Output capacitance	C_{OSS}		-	-	25	
Reverse transfer capacitance	C_{RSS}		-	-	12	
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} =-30V, I_D=-0.27A, V_{GS}=-10V,R_{GEN}= 50Ω	-	10	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$		-	18	-	ns

TYPICAL CHARACTERISTICS @ Ta=25℃ unless otherwise specified

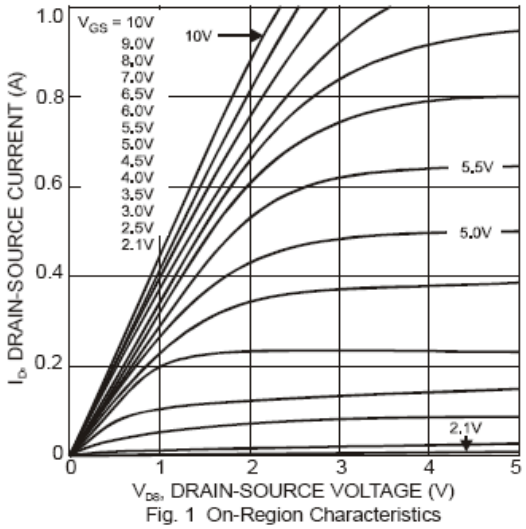


Fig. 1 On-Region Characteristics

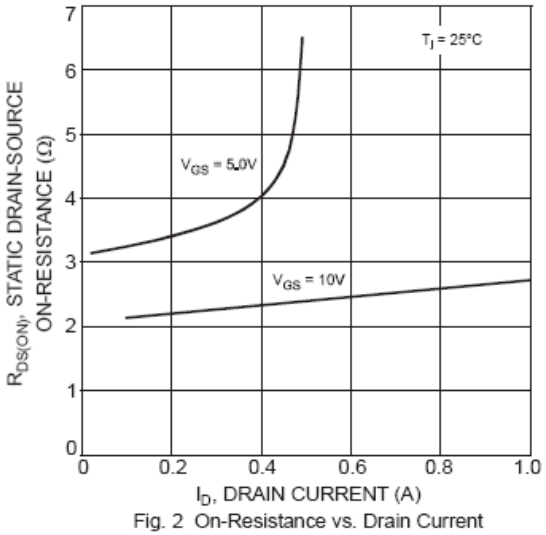


Fig. 2 On-Resistance vs. Drain Current

Complementary Pair Enhancement Mode Field Effect Transistor
BSS8402DW

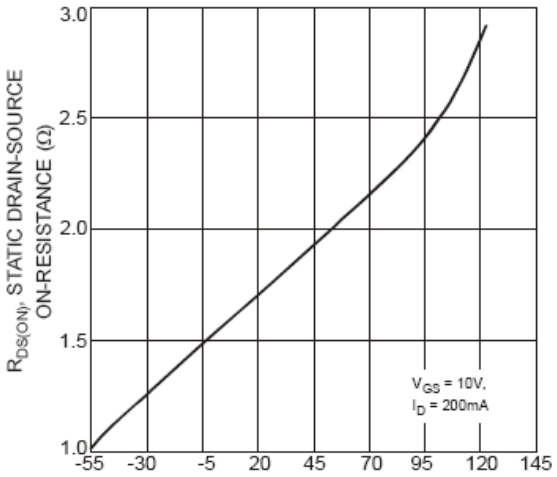


Fig. 3 On-Resistance vs. Junction Temperature

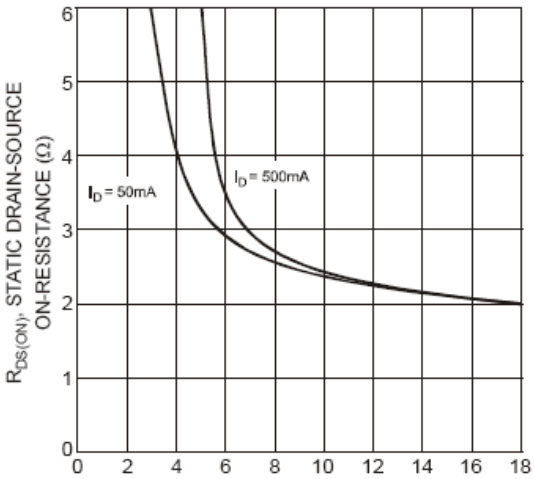


Fig. 4 On-Resistance vs. Gate-Source Voltage

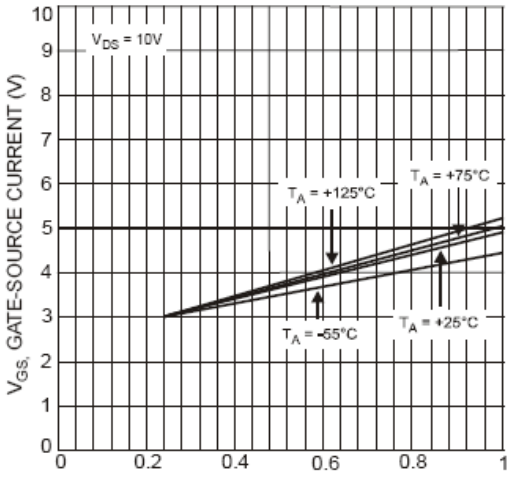


Fig. 5 Typical Transfer Characteristics

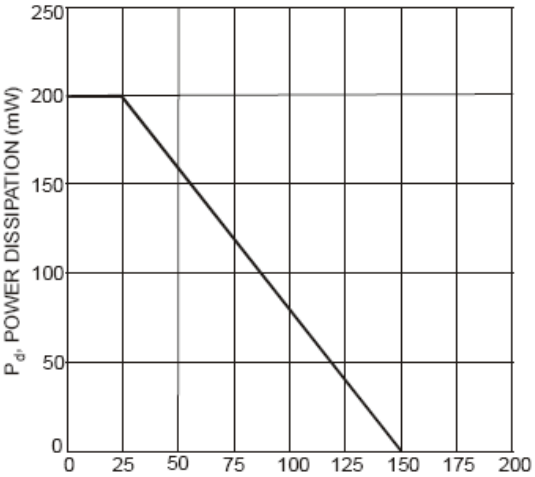


Fig. 6 Max Power Dissipation vs. Ambient Temperature

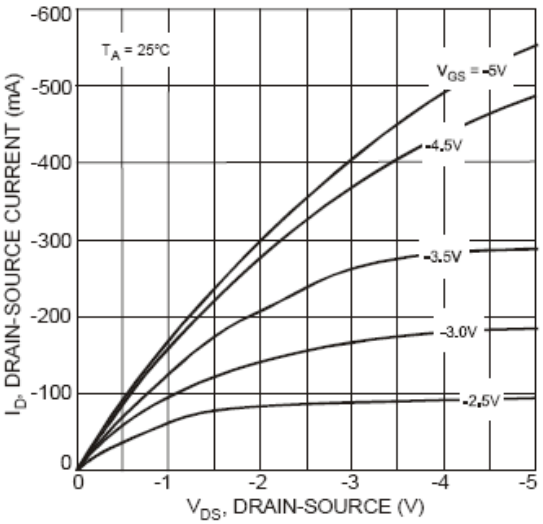


Fig. 7 Drain-Source Current vs. Drain-Source Voltage

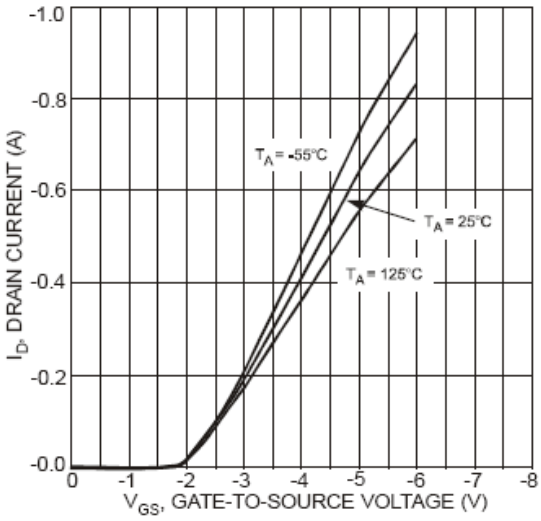


Fig. 8 Drain Current vs. Gate-Source Voltage

Complementary Pair Enhancement Mode Field Effect Transistor

BSS8402DW

Fig. 7 Drain-Source Current vs. Drain-Source Voltage

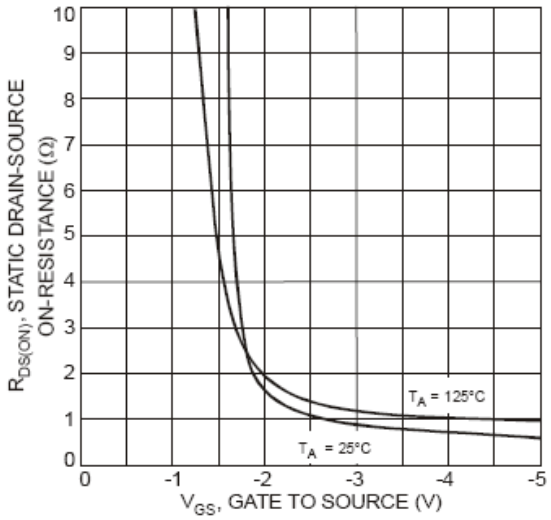


Fig. 8 Drain Current vs. Gate-Source Voltage

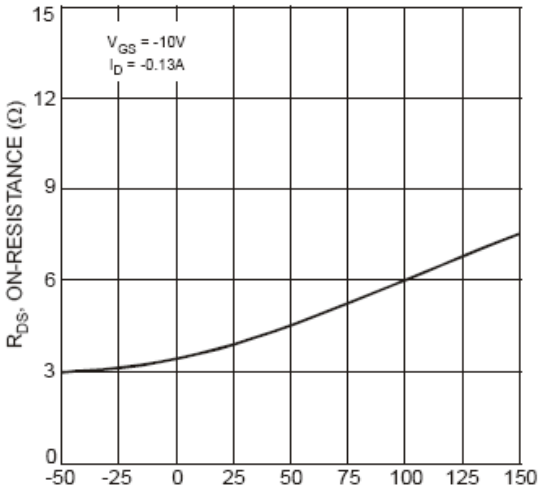


Fig. 9 On-Resistance vs. Gate-Source Voltage

Fig. 10 On-Resistance vs. Junction Temperature

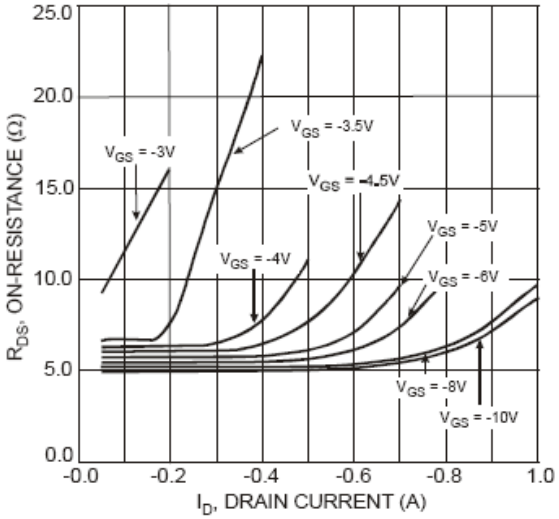
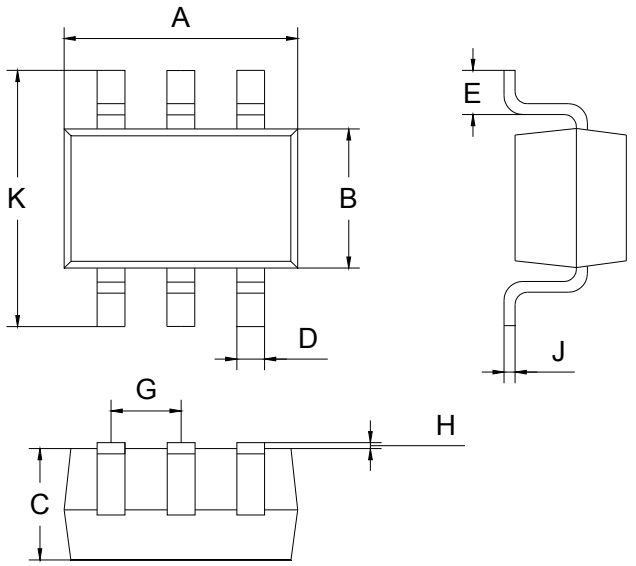


Fig. 11 On-Resistance vs. Drain Current

Complementary Pair Enhancement Mode Field Effect Transistor
BSS8402DW

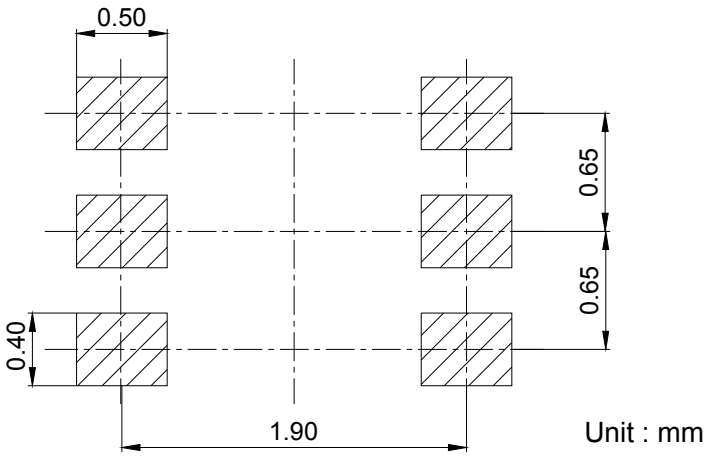
PACKAGE OUTLINE

Plastic surface mounted package SOT-363



SOT-363		
Dim	Min	Max
A	2.00	2.20
B	1.15	1.35
C	0.95 Typical	
D	0.25 Typical	
E	0.25	0.40
G	0.60	0.70
H	0.02	0.10
J	0.10 Typical	
K	2.2	2.4
All Dimensions in mm		

SOLDERING FOOTPRINT



PACKAGE INFORMATION

Device	Package	Shipping
BSS8402DW	SOT-363	3000/Tape&Reel