DATA SHEET

GPY0031A
GPY0032A

2.0W Audio Power Amplifier

Mar. 14, 2014

Version 1.5

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AUDIO DRIVER

1. GENERAL DESCRIPTION

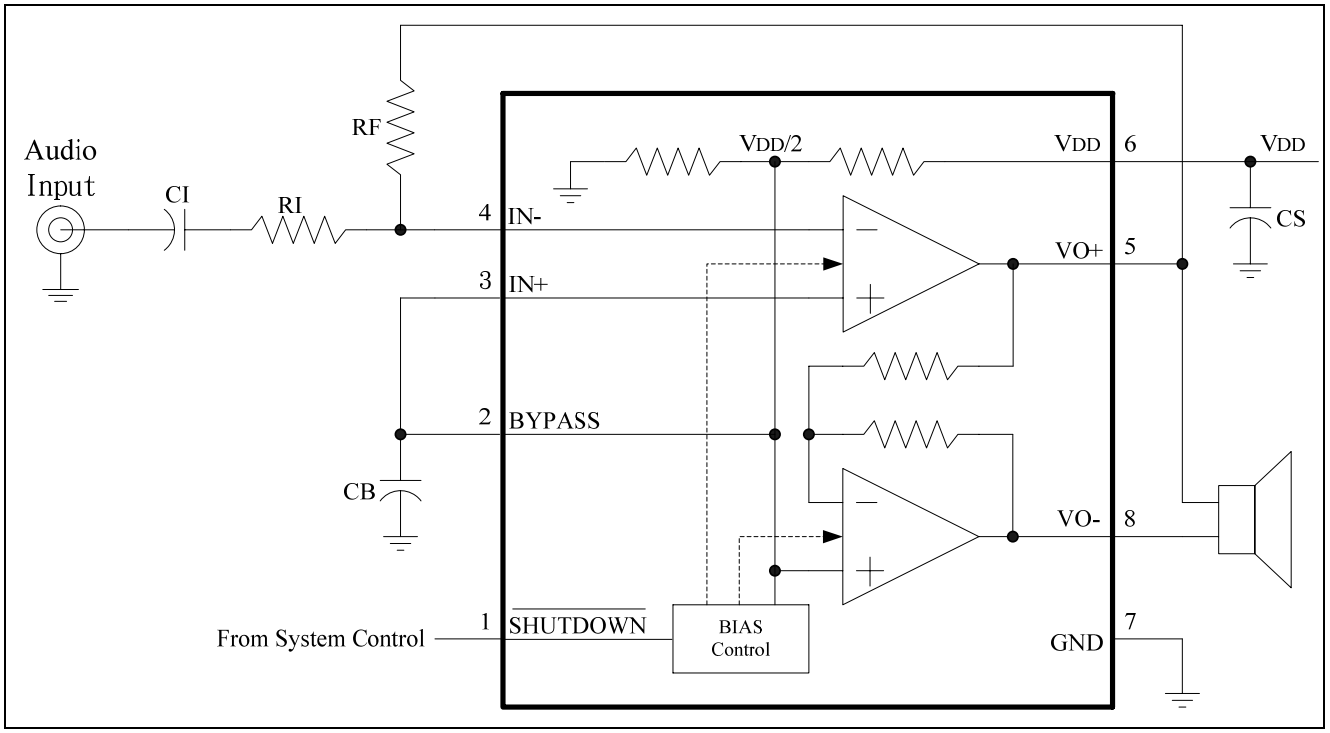
The GPY0031A (a bridge-tied load (BTL) and GPY0032A (a BTL or singled-ended (SE)), are audio amplifiers, designed especially for low-voltage applications which normally require internal speaker. Operating on 5V power supply, GPY0031A / 32A is able to deliver 2.0W of successive average power into 4Ω load at less than 10% of THD+N throughout voice band frequencies and embedded the de-pop circuit to minimize the turn-on and turn-off pop noise. Normally, it is applied for GPC series, GPF series, GPL series and other GENERALPLUS products. The GPY0031A / 32A are easily to be used in various applications and products.

2. FEATURES

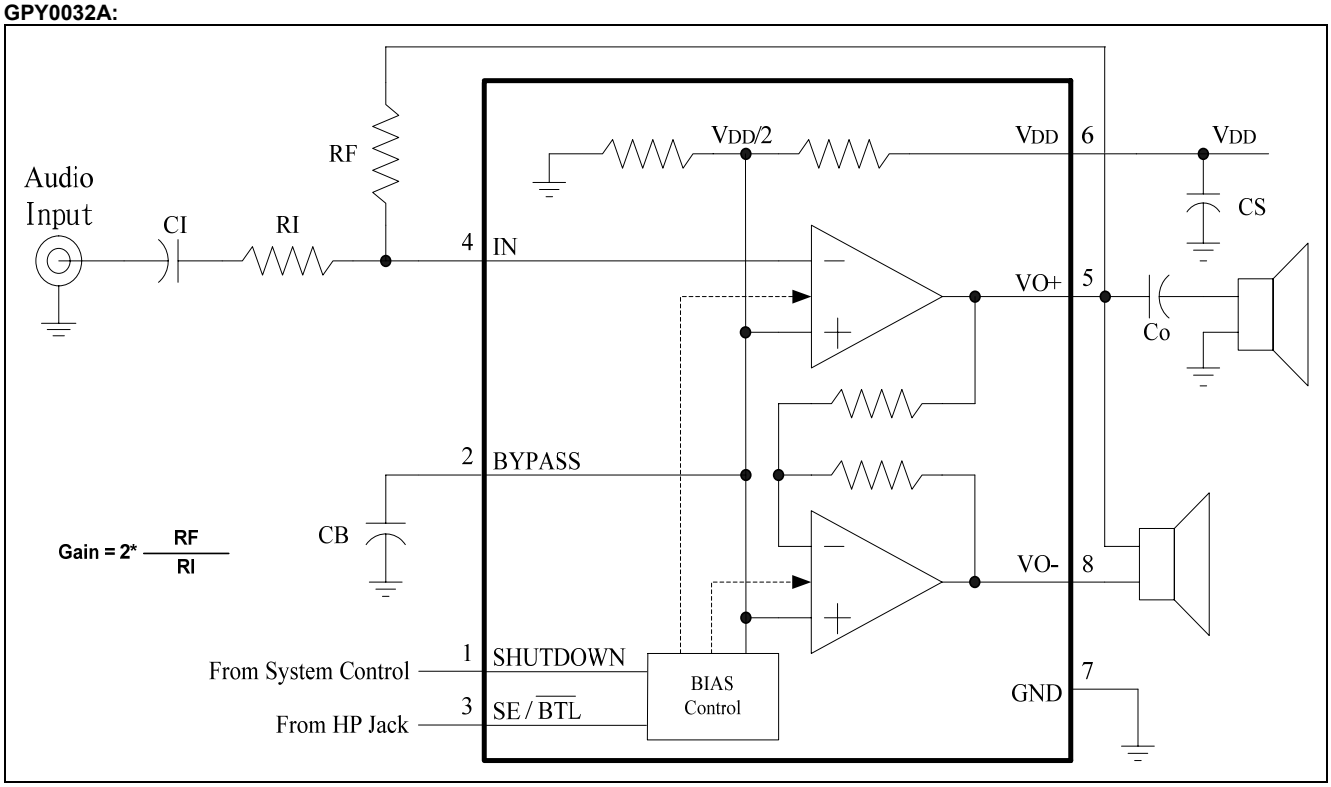
- Wide Operation Range: 2.0V – 6.8V
- Bridge-Tied Load (BTL) (For GPY0031A)
- Bridge-Tied Load (BTL) or Single-Ended (SE) Modes Operation (For GPY0032A)
- Low Distortion: THD+N = 0.15% (Typ.)
  (For VDD = 5.0V, R_L = 4.0Ω & P_{out} = 630mW)
- High Output Power: P_{OUT} = 1.6W
  (For VDD = 5.0V, THD+N =1.0%, f =1.0KHz & R_L = 4Ω)
- Low Shutdown Current: 1.0μA
- Minimize the turn-on and turn-off pop noise
- Thermal Shutdown Protection
- Over Current Protection

3. BLOCK DIAGRAM

GPY0031A:



GPY0032A:


Audio Input
CI
RI
RF
4
IN
VDD/2
VDD
6
VDD
CS
VO+
5
Co
2
BYPASS
CB
Gain = 2* RF/RI
VO-
8
1
SHUTDOWN
From System Control
3
SE / BTL
From HP Jack
BIAS Control
7
GND

4. SIGNAL DESCRIPTIONS

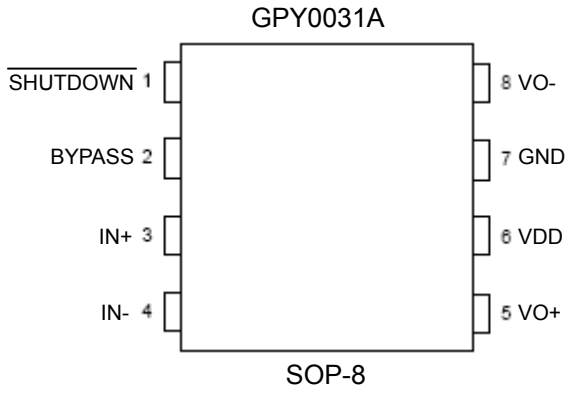
GPY0031A:

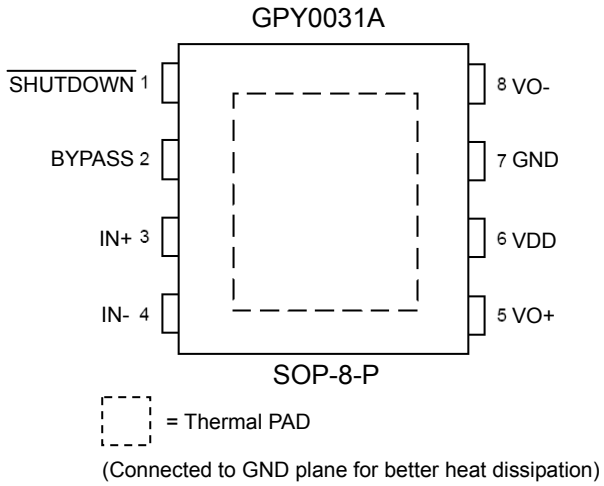
Mnemonic	PIN No.	Type	Description	Electrical Characteristics
$\overline{\text{SHUTDOWN}}$	1	I	Shutdown mode control signal input. Active Low.	-
BYPASS	2	I	BYPASS is internal mid-supply bias. This pin should be connected to a 0.1uF ~ 2.2uF capacitor.	VDD/2
IN+	3	I	IN+ is non-inverting input	-
IN-	4	I	IN- is inverting input	-
VO+	5	O	VO+ is positive BTL output	-
VDD	6	I	Power VDD	2.0V – 6.8V
GND	7	I	Power Ground	-
VO-	8	O	VO- is negative BTL output	-

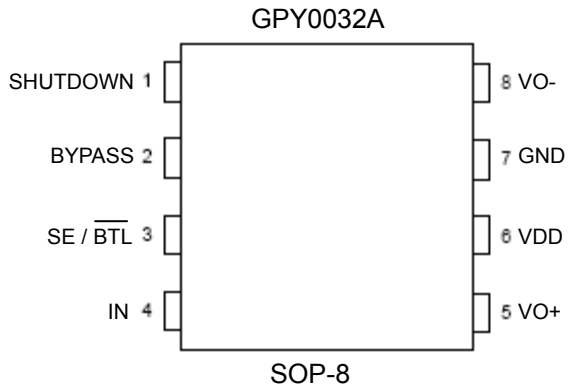
GPY0032A:

Mnemonic	PIN No.	Type	Description	Electrical Characteristics
SHUTDOWN	1	I	Shutdown mode control signal input. Active High.	-
BYPASS	2	I	BYPASS is internal mid-supply bias. This pin should be connected to a 0.1uF ~ 2.2uF capacitor.	VDD/2
SE / $\overline{\text{BTL}}$	3	I	When SE / $\overline{\text{BTL}}$ is held low, GPY0032A is in BTL mode. When SE/ $\overline{\text{BTL}}$ is high, GPY0032A is in SE mode.	-
IN	4	I	Audio input	-
VO+	5	O	VO+ is positive output for BTL mode and SE mode	-
VDD	6	I	Power VDD	2.0V – 6.8V
GND	7	I	Power Ground	-
VO-	8	O	VO- is negative BTL output	-

4.1. Package Pin Assignment







5. ELECTRICAL SPECIFICATIONS

5.1. Absolute Maximum Ratings

Characteristics	Symbol	Rating
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating free-air Temperature Range	T_A	-40℃ to + 85℃
Operating junction Temperature Range	T_J	-40℃ to + 150℃
Storage Temperature	T_{STO}	-50℃ to + 150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

5.2. Thermal Characteristics

Characteristics	Symbol	Value	Unit
SOP-8 Package Thermal Resistance	R_{THJA}	150	℃/W
SOP-8-P Package Thermal Resistance	R_{THJA}	60	℃/W

5.3. DC Characteristics (V_{DD}=5.0V, T_A = 25°C unless otherwise specified)

GPY0031A:

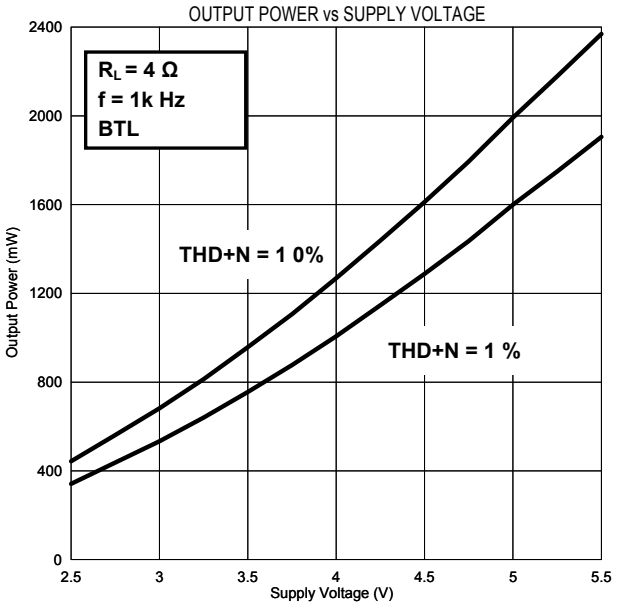
Item	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Operation Voltage	Temperature = 25℃	V_{DD}	2.00	-	6.8	V
	Temperature = -20℃	V_{DD}	2.15	-	6.8	V
	Temperature = -40℃	V_{DD}	2.25	-	6.8	V
Shutdown Current	$\overline{SHUTDOWN}$=GND	I_{STBY}	-	0.1	1.0	uA
Operating Current	V_{DD} = 5.0V, $\overline{SHUTDOWN}$ =V_{DD}, No Load	I_{DD}	-	4.0	-	mA
Reference Voltage	V_{DD} = 5.0V, $\overline{SHUTDOWN}$ =V_{DD}	V_{REF}	-	V_{DD} /2	-	V
Total Harmonic Distortion + Noise	V_{DD} = 5.0V, R_L = 4.0Ω, P_{OUT} = 630mW	THD+N	-	0.15	-	%
	V_{DD} = 5.0V, R_L = 8.0Ω, P_{OUT} = 630mW	THD+N	-	0.15	-	%
Output Power	V_{DD} = 5.0V, THD+N = 1%, f = 1.0KHz & R_L = 4.0Ω	P_{OUT}	-	1600	-	mW
	V_{DD} = 5.0V, THD+N = 1%, f = 1.0KHz & R_L = 8.0Ω	P_{OUT}	-	1150	-	mW
	V_{DD} = 5.0V, THD+N = 10%, f = 1.0KHz & R_L = 4.0Ω	P_{OUT}	-	2000	-	mW
	V_{DD} = 5.0V, THD+N = 10%, f = 1.0KHz & R_L = 8.0Ω	P_{OUT}	-	1400	-	mW
Output Offset Voltage	V_{IN}=0V	V_{OS}	-	-	30	mV
Power Rejection Ratio	f = 1kHz	PSRR	-	70	-	dB
Enable Time	V_{DD} = 5.0V, CI=0.47μF, CB=1.0μF	T_{ON}	-	70	-	ms
Shutdown Time	V_{DD} = 5.0V, CI=0.47μF, CB=1.0μF	T_{OFF}	-	70	-	ms
Current Limitation	V_{DD} = 5.0V, CI=0.47μF, CB=1.0μF	I_{LMT}	-	850	-	mA

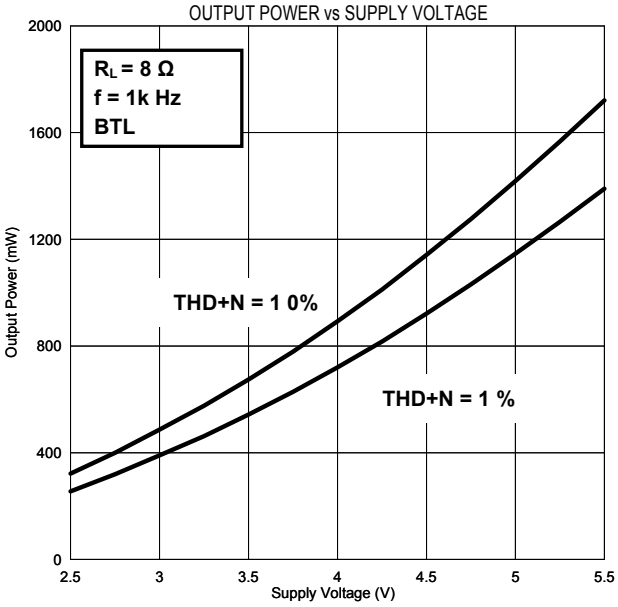
GPY0032A:

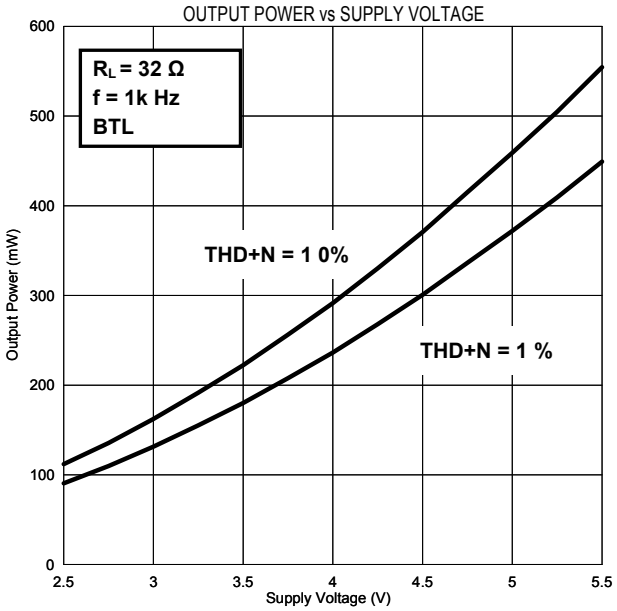
Item	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Operation Voltage	Temperature = 25°C	V_{DD}	2.00	-	6.8	V
	Temperature = -20°C	V_{DD}	2.15	-	6.8	V
	Temperature = -40°C	V_{DD}	2.25	-	6.8	V
Shutdown Current	SHUTDOWN=VDD	I_{STBY}	-	0.1	1.0	uA
Operating Current	V_{DD} = 5.0V, SHUTDOWN =GND, No Load	I_{DD}	-	4.0	-	mA
Reference Voltage	V_{DD} = 5.0V, SHUTDOWN =GND	V_{REF}	-	V_{DD} /2	-	V
Total Harmonic Distortion + Noise	V_{DD} = 5.0V, R_L = 4.0Ω, P_{OUT} = 630mW	THD+N	-	0.15	-	%
	V_{DD} = 5.0V, R_L = 8.0Ω, P_{OUT} = 630mW	THD+N	-	0.15	-	%
Output Power	V_{DD} = 5.0V, THD+N = 1%, f = 1.0KHz & R_L = 4.0Ω	P_{OUT}	-	1600	-	mW
	V_{DD} = 5.0V, THD+N = 1%, f = 1.0KHz & R_L = 8.0Ω	P_{OUT}	-	1150	-	mW
	V_{DD} = 5.0V, THD+N = 10%, f = 1.0KHz & R_L = 4.0Ω	P_{OUT}	-	2000	-	mW
	V_{DD} = 5.0V, THD+N = 10%, f = 1.0KHz & R_L = 8.0Ω	P_{OUT}	-	1400	-	mW
Output Offset Voltage	V_{IN}=0V	V_{OS}	-	-	30	mV
Power Rejection Ratio	f = 1kHz	PSRR	-	70	-	dB
Enable Time	V_{DD} = 5.0V, SE / $\overline{BTL}$ = GND, CB=1.0μF	T_{ON}	-	70	-	ms
	V_{DD} = 5.0V, SE / $\overline{BTL}$ = V_{DD}, CB=1.0μF		-	200	-	ms
Shutdown Time	V_{DD} = 5.0V, SE / $\overline{BTL}$=GND, CB=1.0μF	T_{OFF}	-	70	-	ms
	V_{DD} = 5.0V, SE / $\overline{BTL}$ = V_{DD}, CB=1.0μF		-	200	-	ms
Current Limitation	V_{DD} = 5.0V, CI=0.47μF, CB=1.0μF	I_{LMT}	-	850	-	mA

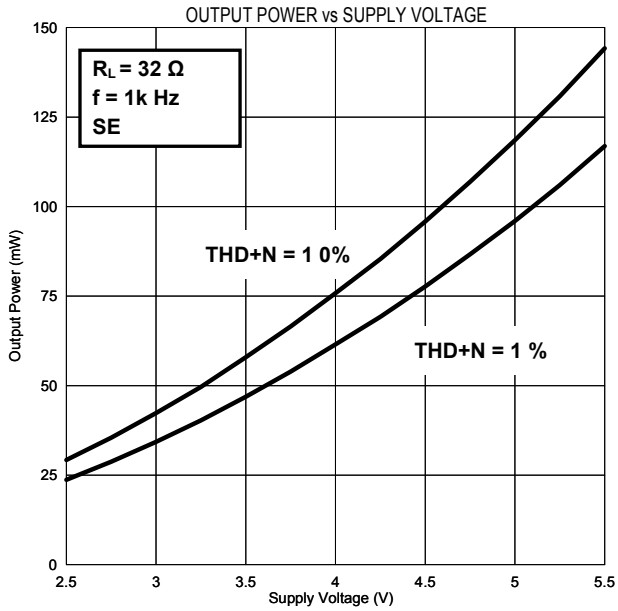
5.4. Typical Performance Characteristics

5.4.1. Output power vs. supply voltage

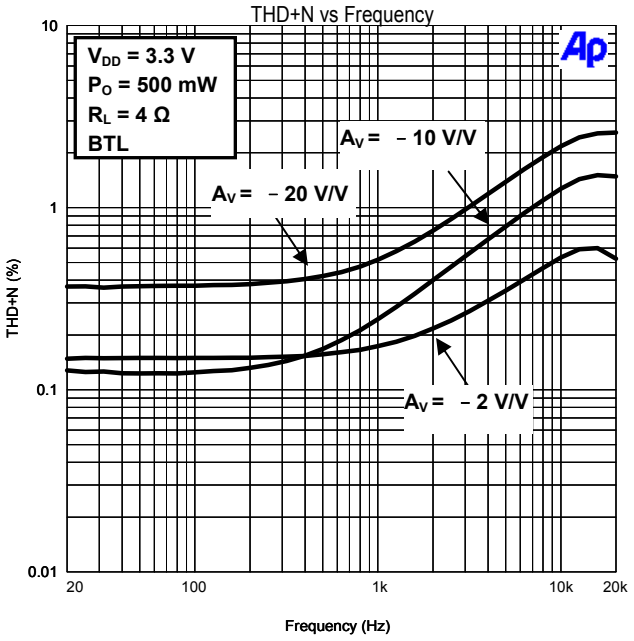


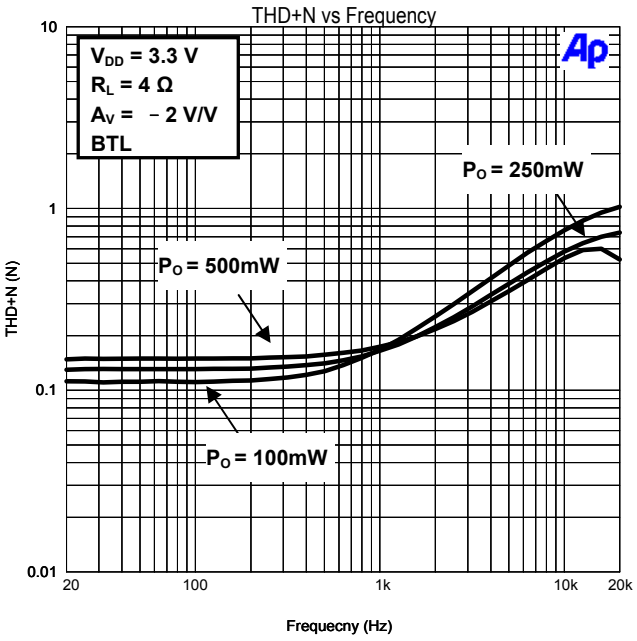


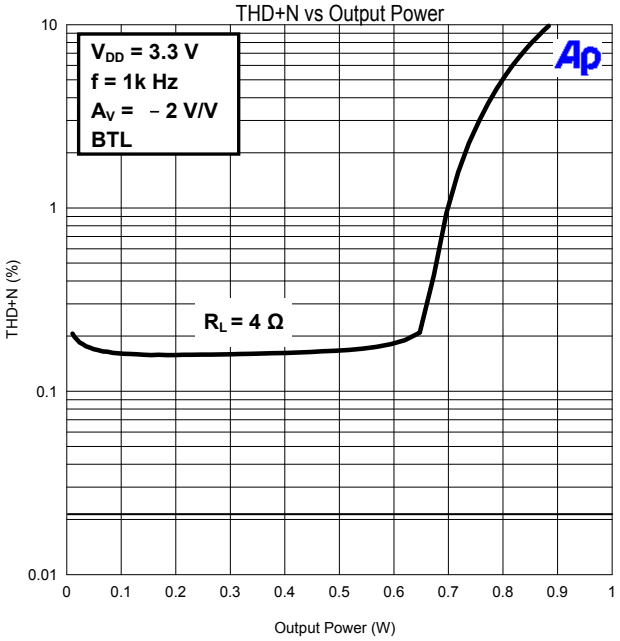


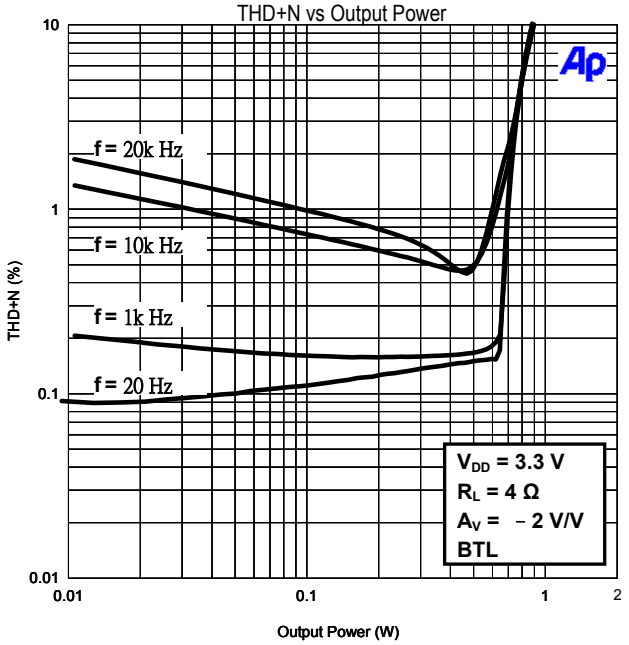


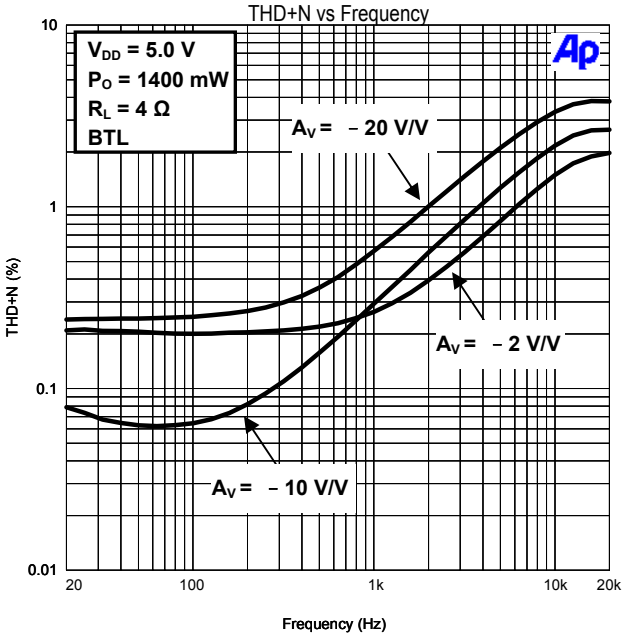
5.4.2. THD+N

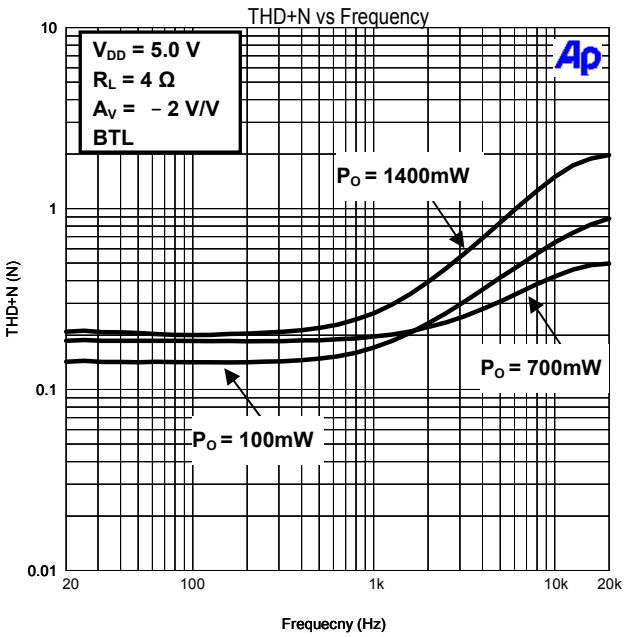

THD+N vs Frequency
V_{DD} = 3.3 V
P_O = 500 mW
R_L = 4 Ω
BTL
A_V = – 10 V/V
A_V = – 20 V/V
A_V = – 2 V/V
THD+N (%)
10
1
0.1
0.01
20
100
1k
10k
20k
Frequency (Hz)

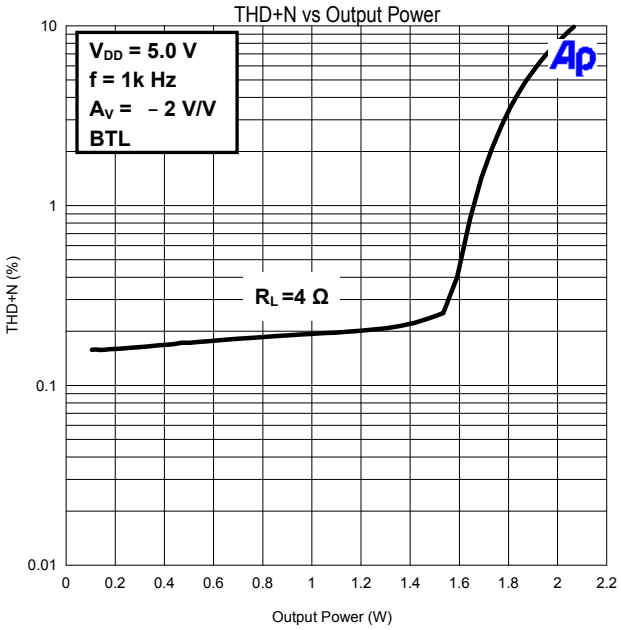

THD+N vs Frequency
V_{DD} = 3.3 V
R_L = 4 Ω
A_V = – 2 V/V
BTL
P_O = 250mW
P_O = 500mW
P_O = 100mW
THD+N (N)
10
1
0.1
0.01
20
100
1k
10k
20k
Frequecny (Hz)

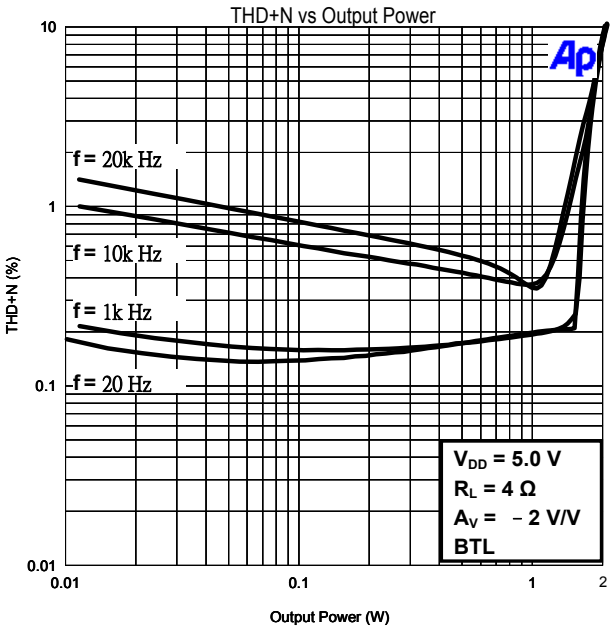

THD+N vs Output Power
V_{DD} = 3.3 V
f = 1k Hz
A_V = – 2 V/V
BTL
R_L = 4 Ω
THD+N (%)
10
1
0.1
0.01
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Output Power (W)

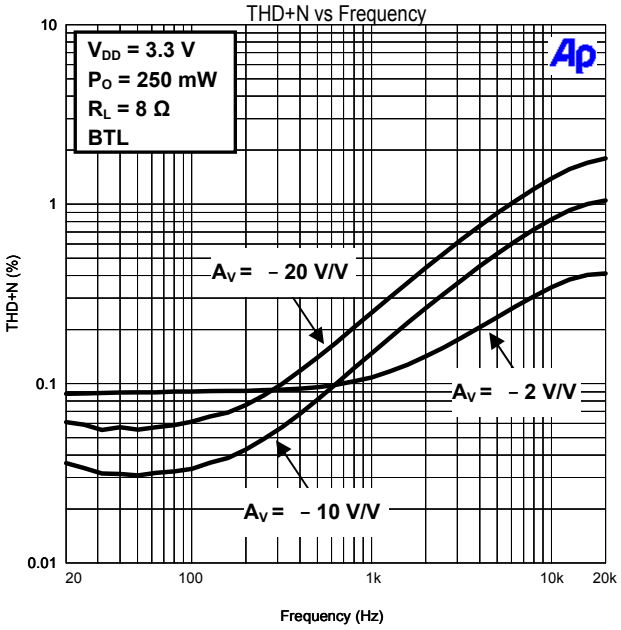

THD+N vs Output Power
f = 20k Hz
f = 10k Hz
f = 1k Hz
f = 20 Hz
V_{DD} = 3.3 V
R_L = 4 Ω
A_V = – 2 V/V
BTL
THD+N (%)
10
1
0.1
0.01
0.01
0.1
1
2
Output Power (W)

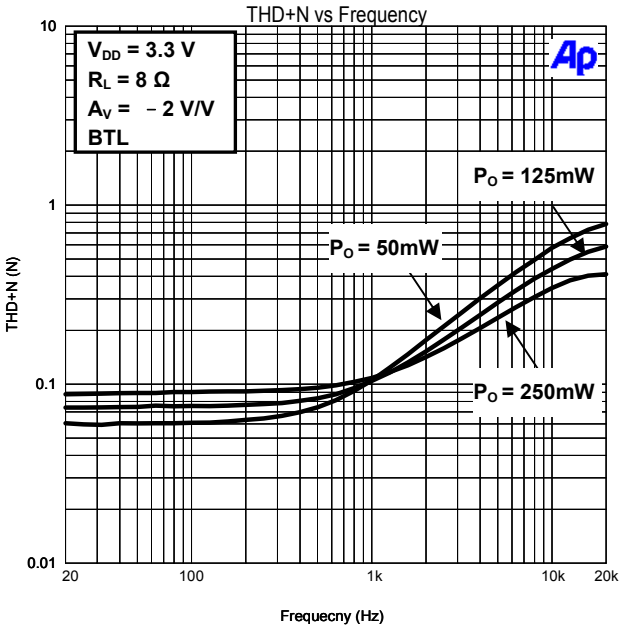

THD+N vs Frequency
V_{DD} = 5.0 V
P_O = 1400 mW
R_L = 4 Ω
BTL
A_V = – 20 V/V
A_V = – 2 V/V
A_V = – 10 V/V
THD+N (%)
10
1
0.1
0.01
20
100
1k
10k
20k
Frequency (Hz)

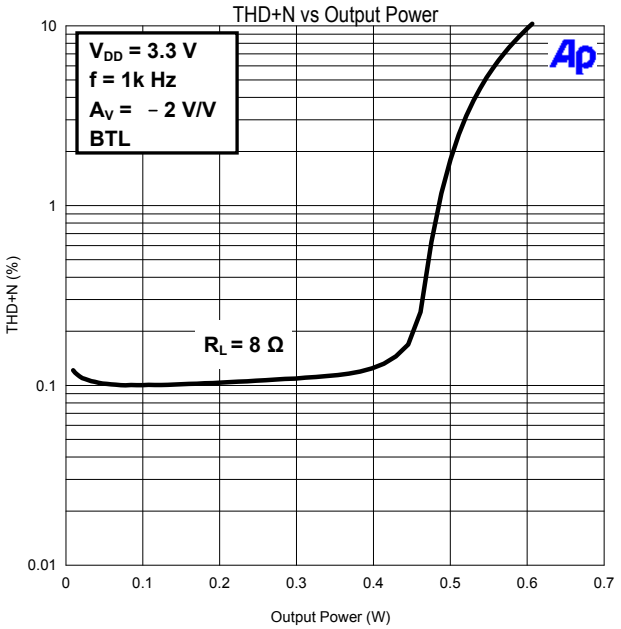

THD+N vs Frequency
V_{DD} = 5.0 V
R_L = 4 Ω
A_V = – 2 V/V
BTL
P_O = 1400mW
P_O = 700mW
P_O = 100mW
THD+N (N)
10
1
0.1
0.01
20
100
1k
10k
20k
Frequecny (Hz)

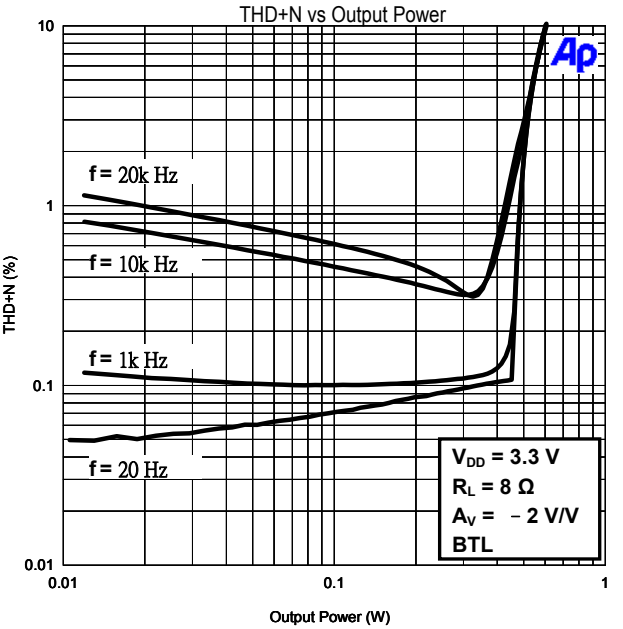

THD+N vs Output Power
V_{DD} = 5.0 V
f = 1k Hz
A_V = – 2 V/V
BTL
R_L =4 Ω
THD+N (%)
10
1
0.1
0.01
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
2.2
Output Power (W)

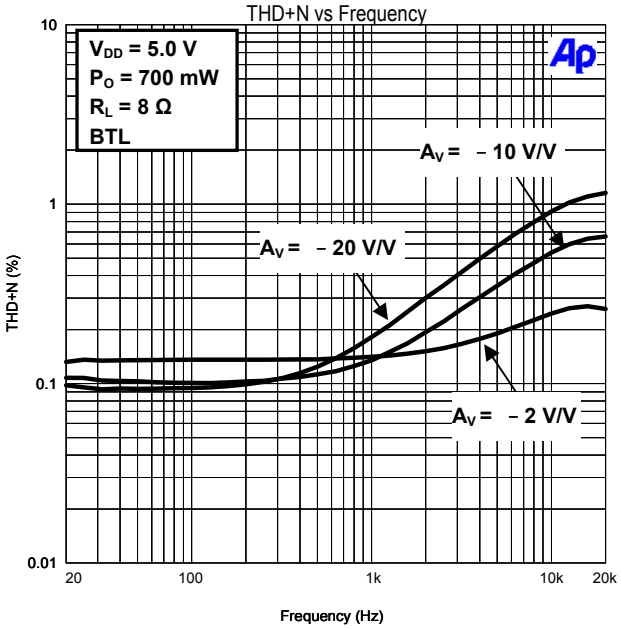

THD+N vs Output Power
f = 20k Hz
f = 10k Hz
f = 1k Hz
f = 20 Hz
V_{DD} = 5.0 V
R_L = 4 Ω
A_V = – 2 V/V
BTL
THD+N (%)
10
1
0.1
0.01
0.01
0.1
1
2
Output Power (W)

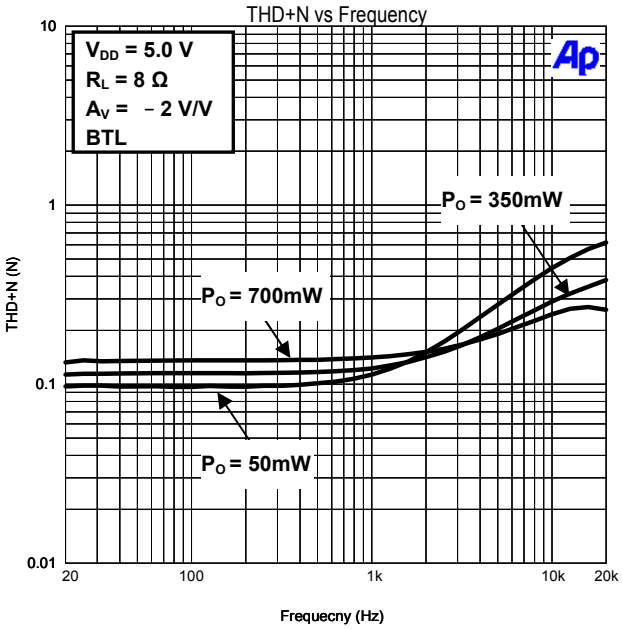

THD+N vs Frequency
V_{DD} = 3.3 V
P_O = 250 mW
R_L = 8 Ω
BTL
A_V = －20 V/V
A_V = －2 V/V
A_V = －10 V/V
THD+N (%)
10
1
0.1
0.01
20
100
1k
10k
20k
Frequency (Hz)

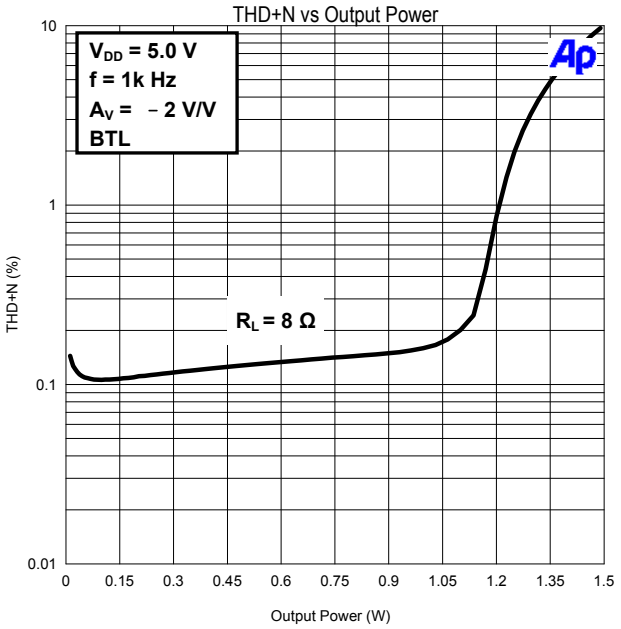

THD+N vs Frequency
V_{DD} = 3.3 V
R_L = 8 Ω
A_V = －2 V/V
BTL
P_O = 125mW
P_O = 50mW
P_O = 250mW
THD+N (N)
10
1
0.1
0.01
20
100
1k
10k
20k
Frequecny (Hz)

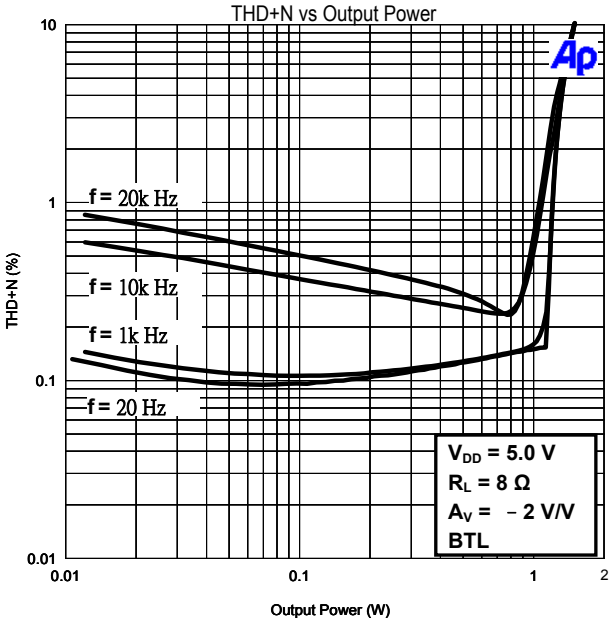

THD+N vs Output Power
V_{DD} = 3.3 V
f = 1k Hz
A_V = －2 V/V
BTL
R_L = 8 Ω
THD+N (%)
10
1
0.1
0.01
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
Output Power (W)

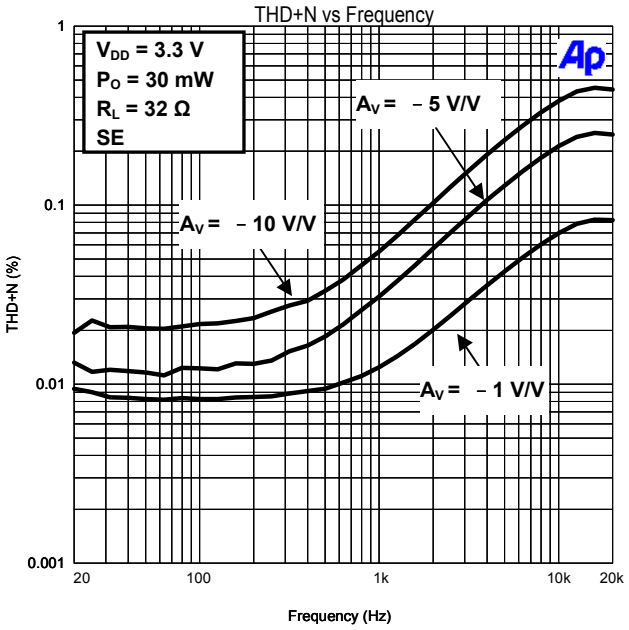

THD+N vs Output Power
f = 20k Hz
f = 10k Hz
f = 1k Hz
f = 20 Hz
V_{DD} = 3.3 V
R_L = 8 Ω
A_V = －2 V/V
BTL
THD+N (%)
10
1
0.1
0.01
0.01
0.1
1
Output Power (W)

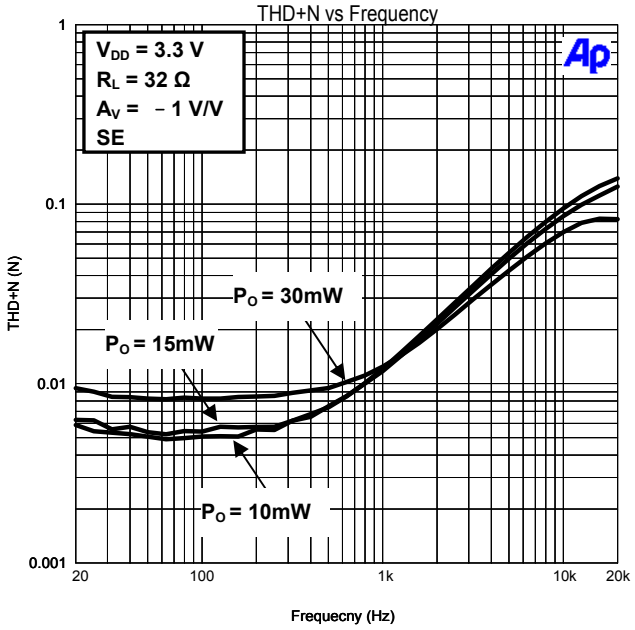

THD+N vs Frequency
V_{DD} = 5.0 V
P_O = 700 mW
R_L = 8 Ω
BTL
A_V = －10 V/V
A_V = －20 V/V
A_V = －2 V/V
THD+N (%)
10
1
0.1
0.01
20
100
1k
10k
20k
Frequency (Hz)

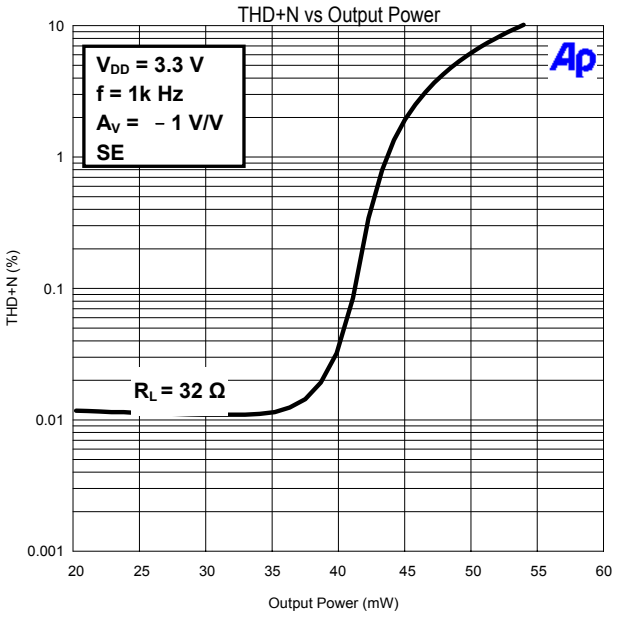

THD+N vs Frequency
V_{DD} = 5.0 V
R_L = 8 Ω
A_V = －2 V/V
BTL
P_O = 350mW
P_O = 700mW
P_O = 50mW
THD+N (N)
10
1
0.1
0.01
20
100
1k
10k
20k
Frequecny (Hz)

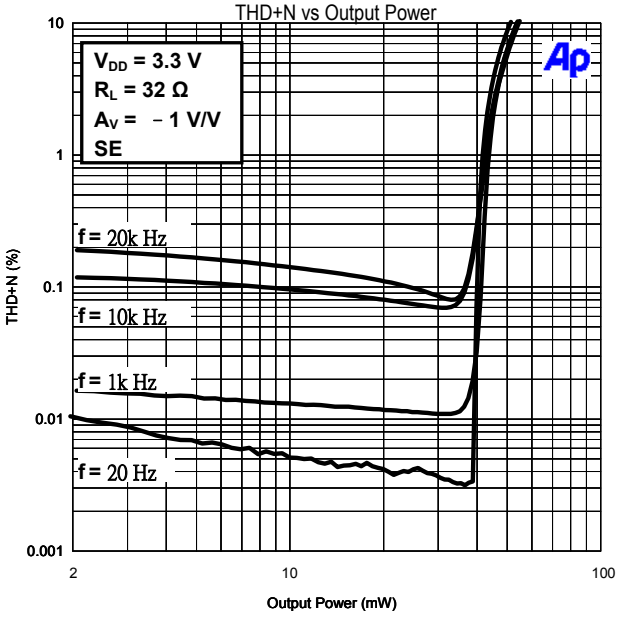

THD+N vs Output Power
V_{DD} = 5.0 V
f = 1k Hz
A_V = －2 V/V
BTL
R_L = 8 Ω
THD+N (%)
10
1
0.1
0.01
0
0.15
0.3
0.45
0.6
0.75
0.9
1.05
1.2
1.35
1.5
Output Power (W)

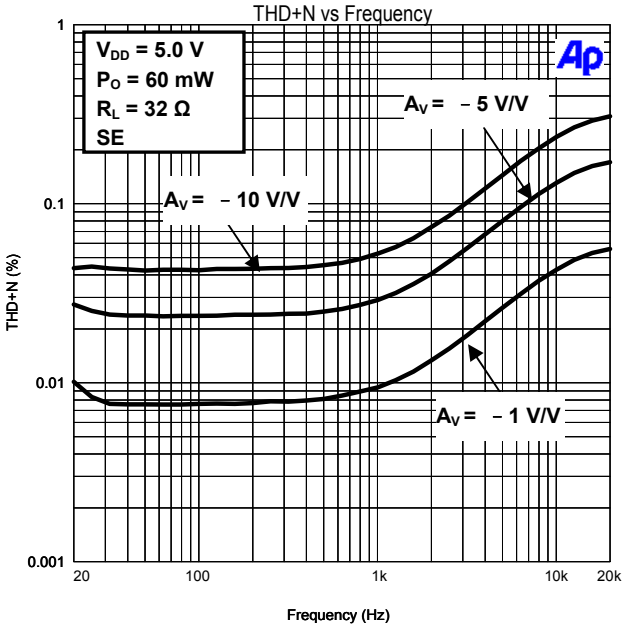

THD+N vs Output Power
f = 20k Hz
f = 10k Hz
f = 1k Hz
f = 20 Hz
V_{DD} = 5.0 V
R_L = 8 Ω
A_V = －2 V/V
BTL
THD+N (%)
10
1
0.1
0.01
0.01
0.1
1
2
Output Power (W)

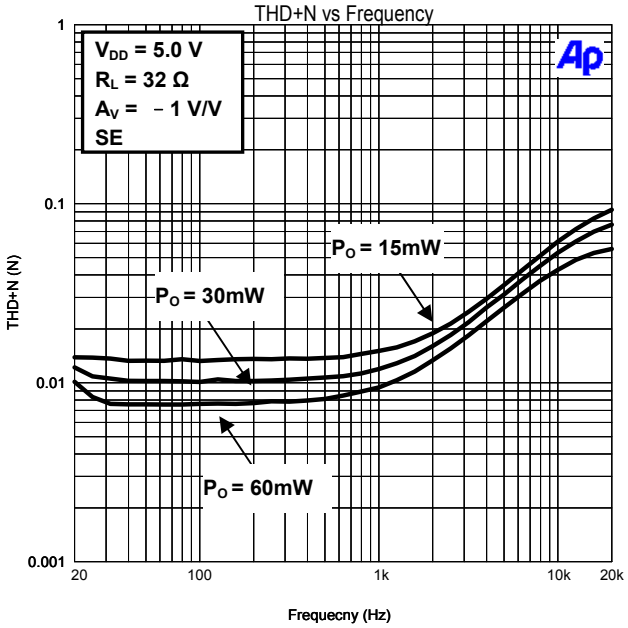

THD+N vs Frequency
VDD = 3.3 V
PO = 30 mW
RL = 32 Ω
SE
AV = – 5 V/V
AV = – 10 V/V
AV = – 1 V/V
THD+N (%)
1
0.1
0.01
0.001
20
100
1k
10k
20k
Frequency (Hz)

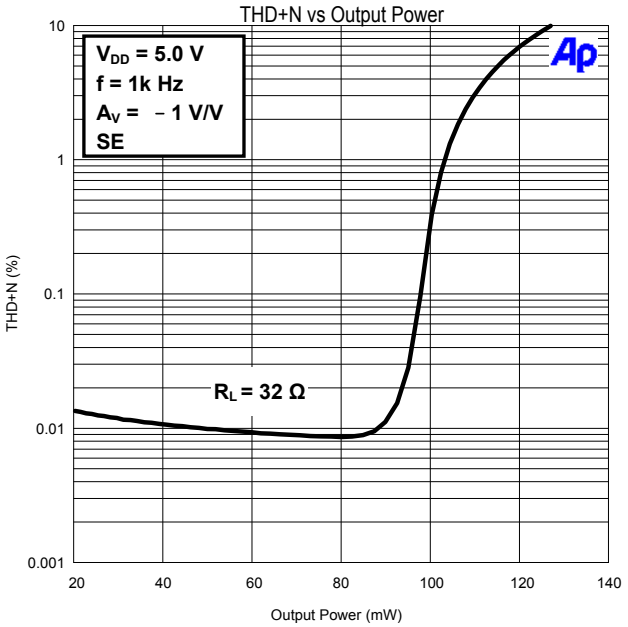

THD+N vs Frequency
VDD = 3.3 V
RL = 32 Ω
AV = – 1 V/V
SE
PO = 30mW
PO = 15mW
PO = 10mW
THD+N (N)
1
0.1
0.01
0.001
20
100
1k
10k
20k
Frequecny (Hz)

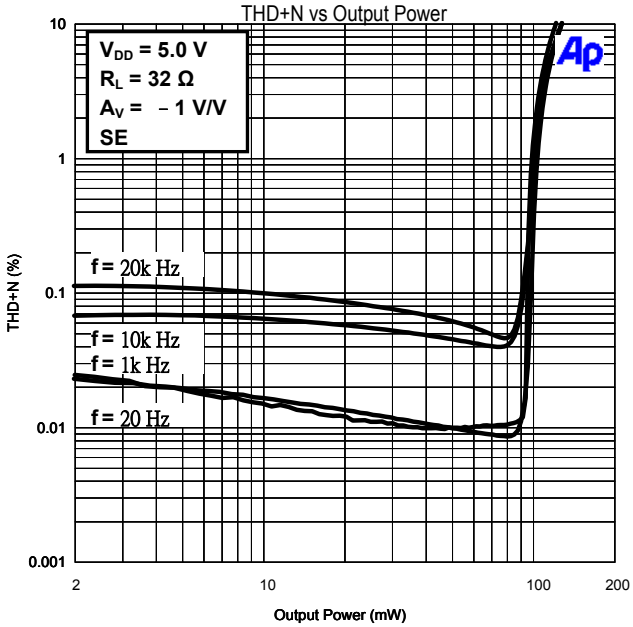

THD+N vs Output Power
VDD = 3.3 V
f = 1k Hz
AV = – 1 V/V
SE
RL = 32 Ω
THD+N (%)
10
1
0.1
0.01
0.001
20
25
30
35
40
45
50
55
60
Output Power (mW)

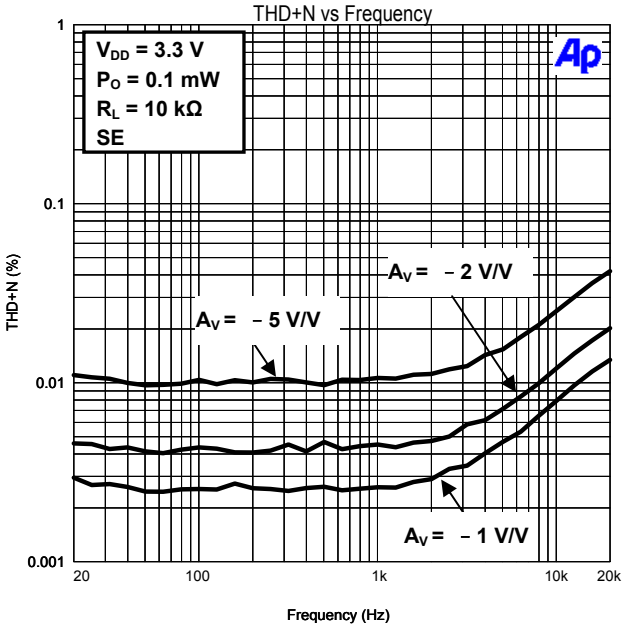

THD+N vs Output Power
VDD = 3.3 V
RL = 32 Ω
AV = – 1 V/V
SE
f = 20k Hz
f = 10k Hz
f = 1k Hz
f = 20 Hz
THD+N (%)
10
1
0.1
0.01
0.001
2
10
100
Output Power (mW)

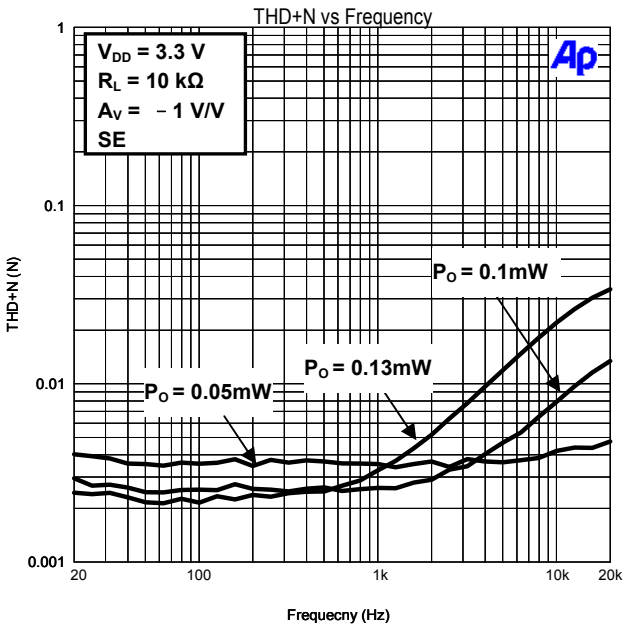

THD+N vs Frequency
V_{DD} = 5.0 V
P_O = 60 mW
R_L = 32 Ω
SE
A_V = – 5 V/V
A_V = – 10 V/V
A_V = – 1 V/V
THD+N (%)
1
0.1
0.01
0.001
20
100
1k
10k
20k
Frequency (Hz)

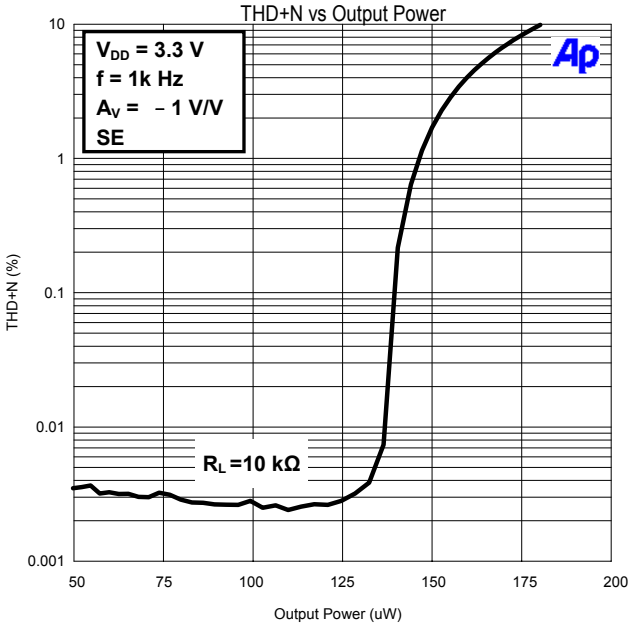

THD+N vs Frequency
V_{DD} = 5.0 V
R_L = 32 Ω
A_V = – 1 V/V
SE
P_O = 15mW
P_O = 30mW
P_O = 60mW
THD+N (N)
1
0.1
0.01
0.001
20
100
1k
10k
20k
Frequecny (Hz)

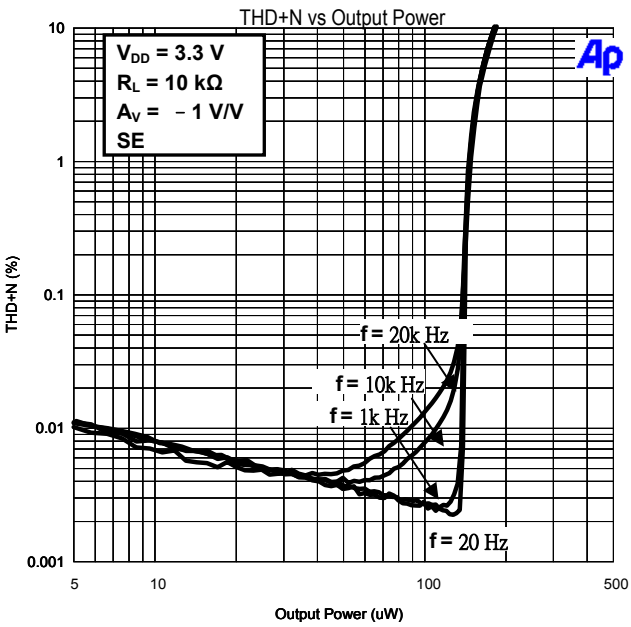

THD+N vs Output Power
V_{DD} = 5.0 V
f = 1k Hz
A_V = – 1 V/V
SE
R_L = 32 Ω
THD+N (%)
10
1
0.1
0.01
0.001
20
40
60
80
100
120
140
Output Power (mW)

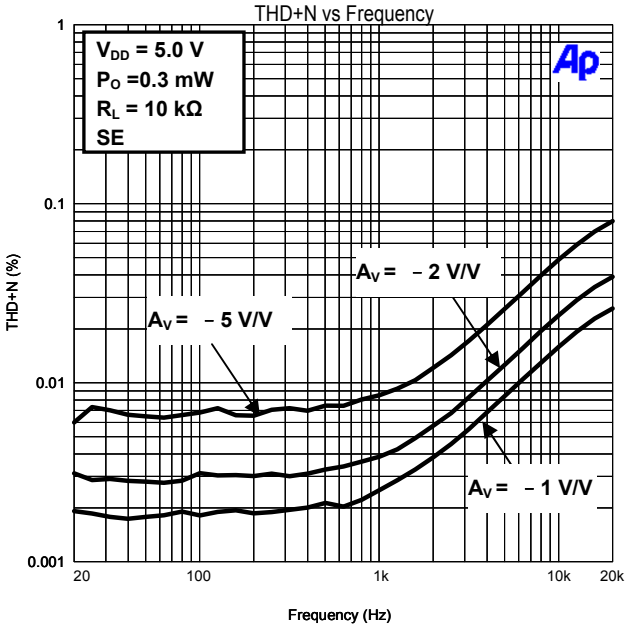

THD+N vs Output Power
V_{DD} = 5.0 V
R_L = 32 Ω
A_V = – 1 V/V
SE
f = 20k Hz
f = 10k Hz
f = 1k Hz
f = 20 Hz
THD+N (%)
10
1
0.1
0.01
0.001
2
10
100
200
Output Power (mW)

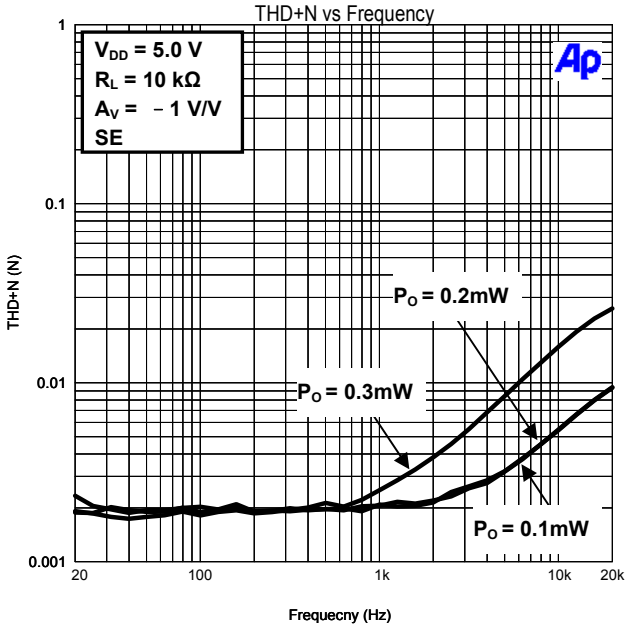

THD+N vs Frequency
V_{DD} = 3.3 V
P_O = 0.1 mW
R_L = 10 kΩ
SE
A_V = – 2 V/V
A_V = – 5 V/V
A_V = – 1 V/V
THD+N (%)
Frequency (Hz)

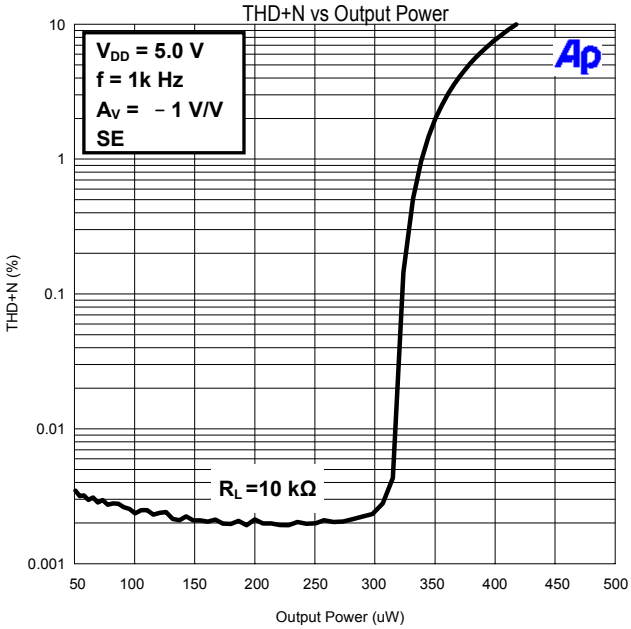

THD+N vs Frequency
V_{DD} = 3.3 V
R_L = 10 kΩ
A_V = – 1 V/V
SE
P_O = 0.1mW
P_O = 0.13mW
P_O = 0.05mW
THD+N (N)
Frequecny (Hz)

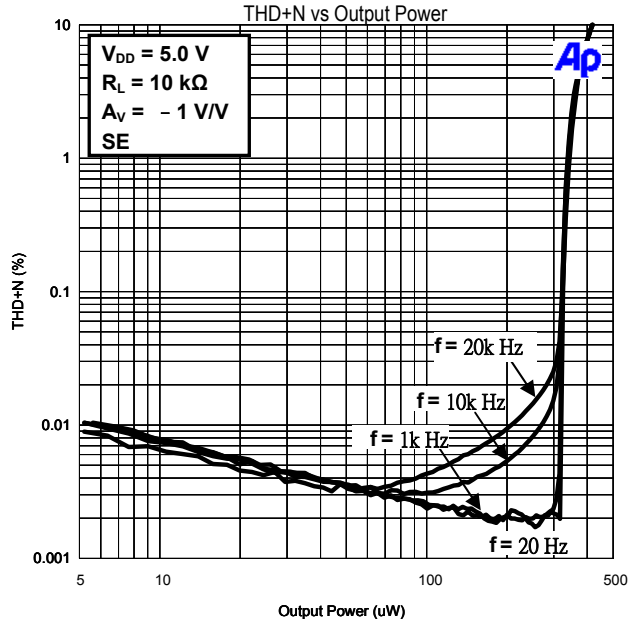

THD+N vs Output Power
V_{DD} = 3.3 V
f = 1k Hz
A_V = – 1 V/V
SE
R_L =10 kΩ
THD+N (%)
Output Power (uW)


THD+N vs Output Power
V_{DD} = 3.3 V
R_L = 10 kΩ
A_V = – 1 V/V
SE
f = 20k Hz
f = 10k Hz
f = 1k Hz
f = 20 Hz
THD+N (%)
Output Power (uW)

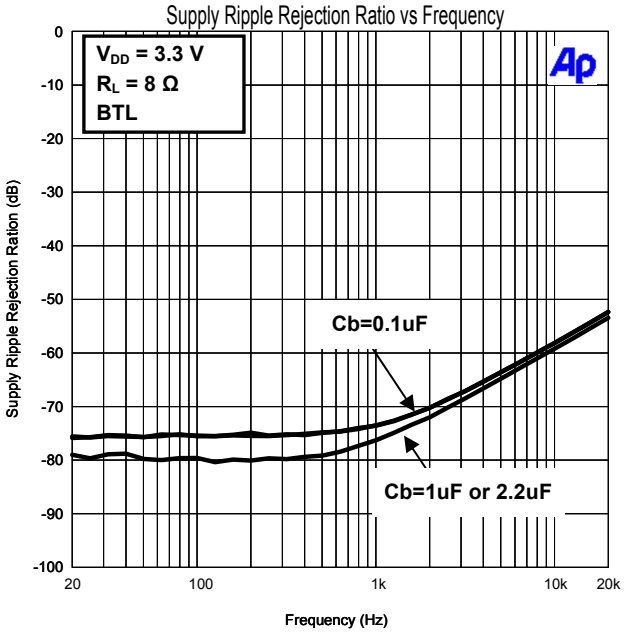

THD+N vs Frequency
VDD = 5.0 V
PO =0.3 mW
RL = 10 kΩ
SE
AV = – 2 V/V
AV = – 5 V/V
AV = – 1 V/V
THD+N (%)
Frequency (Hz)
1
0.1
0.01
0.001
20
100
1k
10k
20k

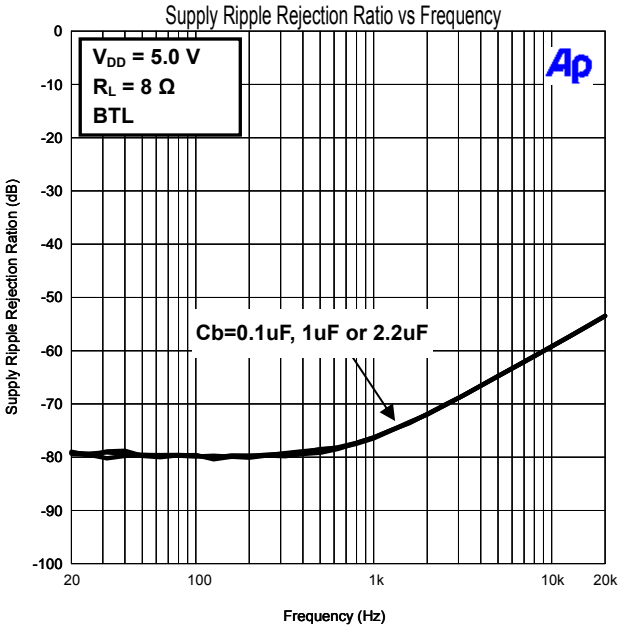

THD+N vs Frequency
VDD = 5.0 V
RL = 10 kΩ
AV = – 1 V/V
SE
PO = 0.2mW
PO = 0.3mW
PO = 0.1mW
THD+N (N)
Frequecny (Hz)
1
0.1
0.01
0.001
20
100
1k
10k
20k

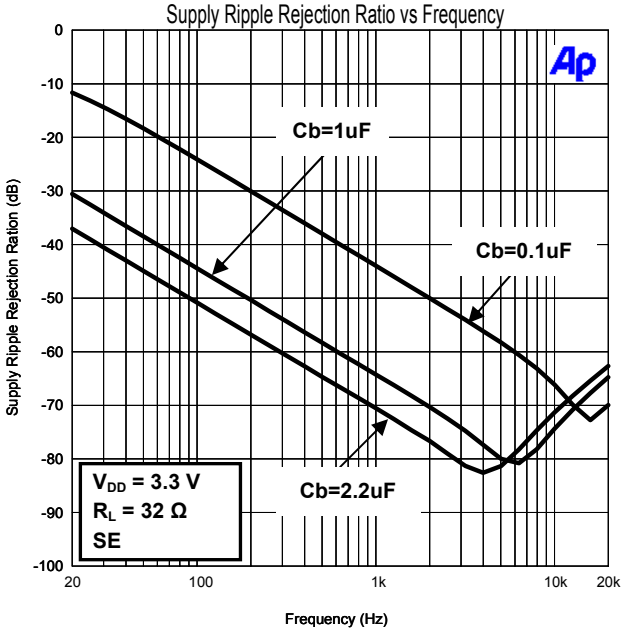

THD+N vs Output Power
VDD = 5.0 V
f = 1k Hz
AV = – 1 V/V
SE
RL =10 kΩ
THD+N (%)
Output Power (uW)
10
1
0.1
0.01
0.001
50
100
150
200
250
300
350
400
450
500

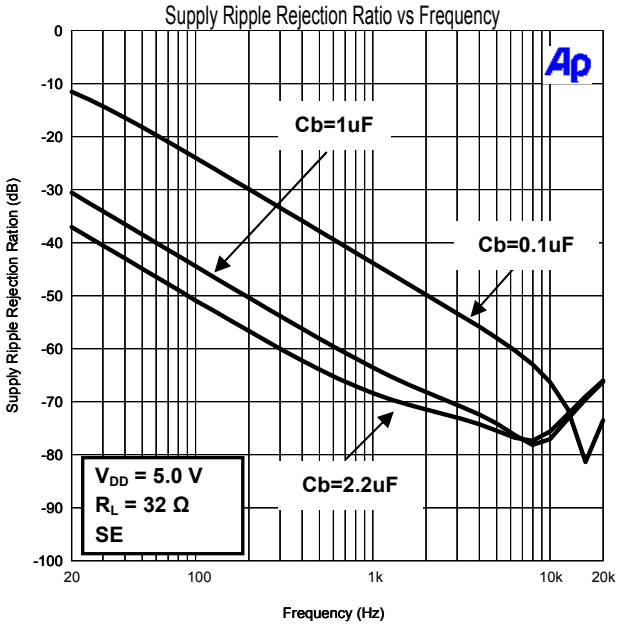

THD+N vs Output Power
VDD = 5.0 V
RL = 10 kΩ
AV = – 1 V/V
SE
f = 20k Hz
f = 10k Hz
f = 1k Hz
f = 20 Hz
THD+N (%)
Output Power (uW)
10
1
0.1
0.01
0.001
5
10
100
500

5.4.3. Supply ripple rejection ratio vs. frequency

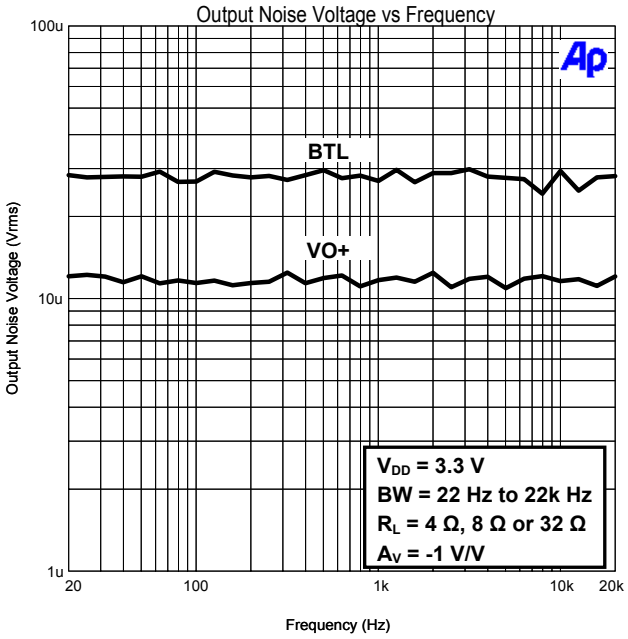


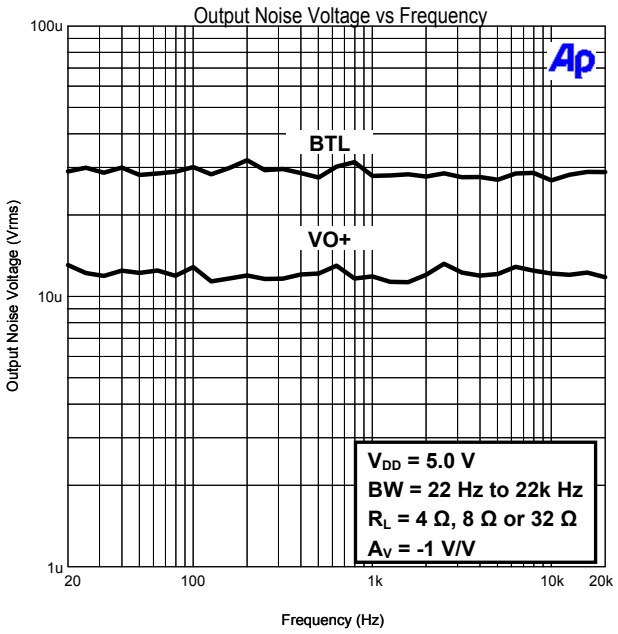






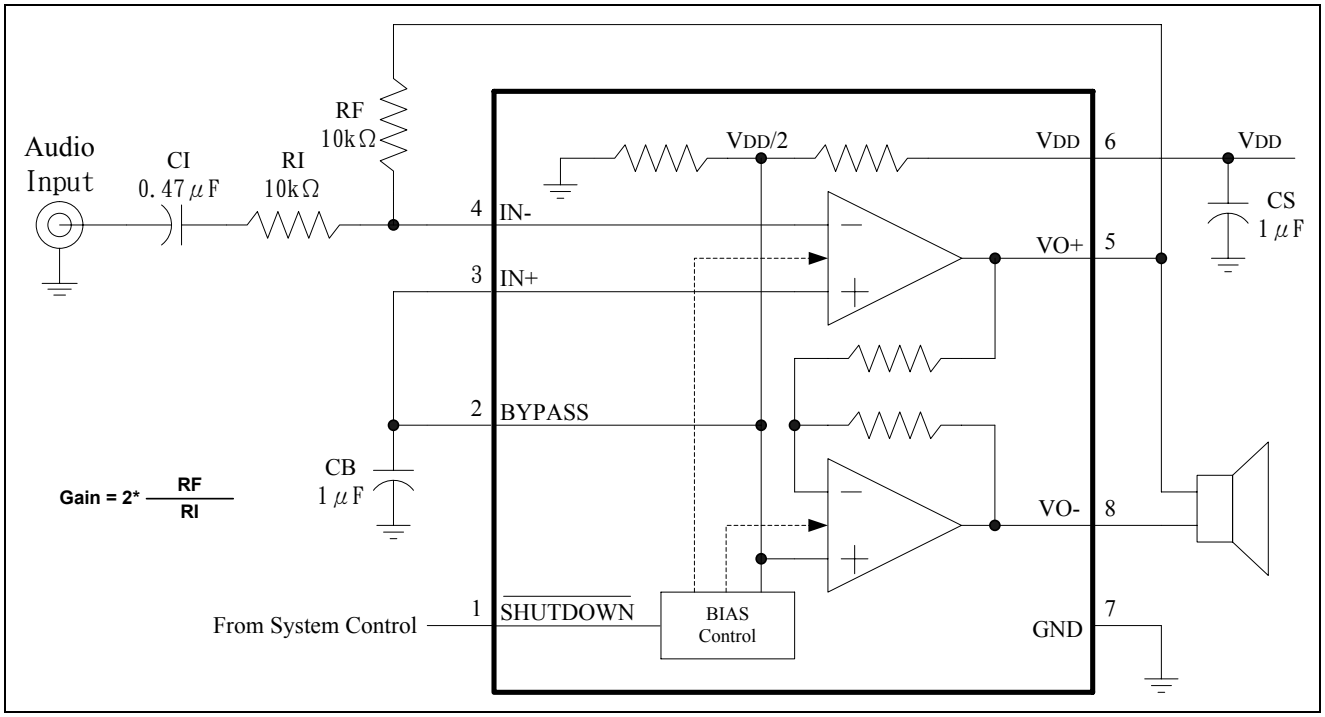
5.4.4. Noise


Output Noise Voltage vs Frequency
100u
10u
1u
Output Noise Voltage (Vrms)
BTL
VO+
VDD = 3.3 V
BW = 22 Hz to 22k Hz
RL = 4 Ω, 8 Ω or 32 Ω
AV = -1 V/V
20
100
1k
10k
20k
Frequency (Hz)

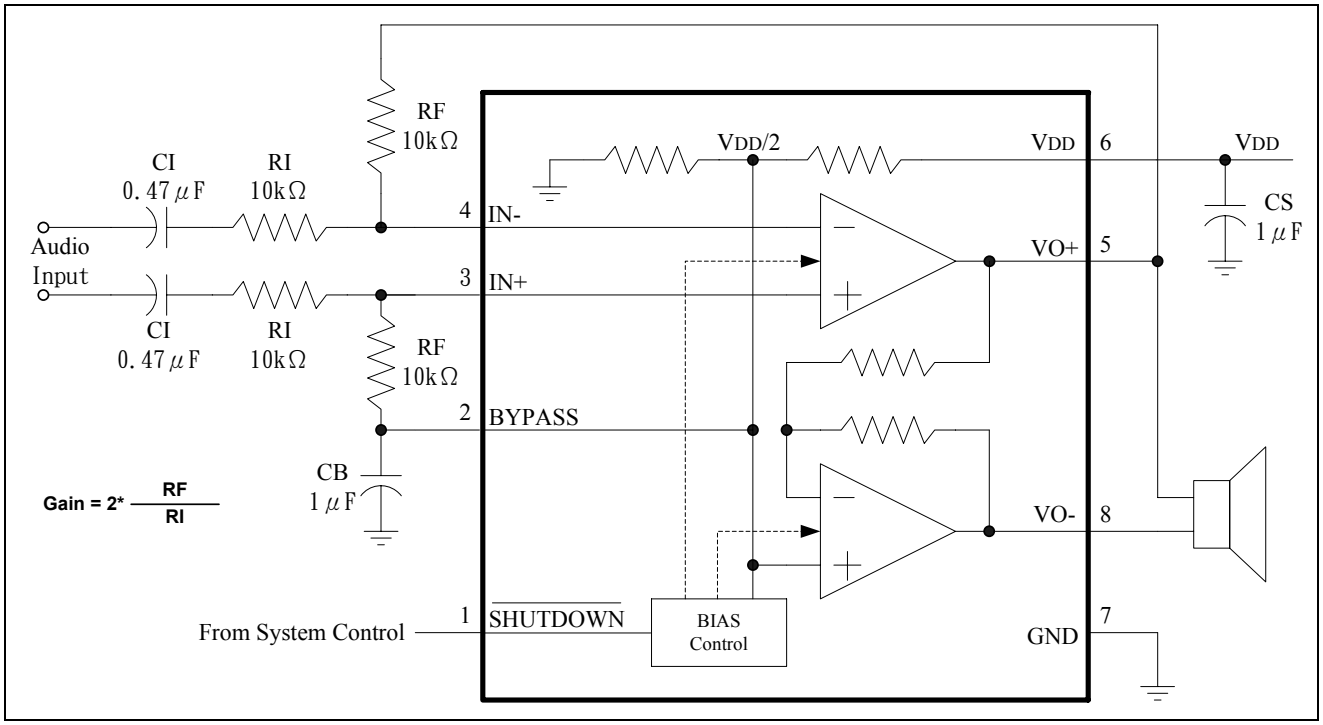

Output Noise Voltage vs Frequency
100u
10u
1u
Output Noise Voltage (Vrms)
BTL
VO+
VDD = 5.0 V
BW = 22 Hz to 22k Hz
RL = 4 Ω, 8 Ω or 32 Ω
AV = -1 V/V
20
100
1k
10k
20k
Frequency (Hz)

6. APPLICATION INFORMATION

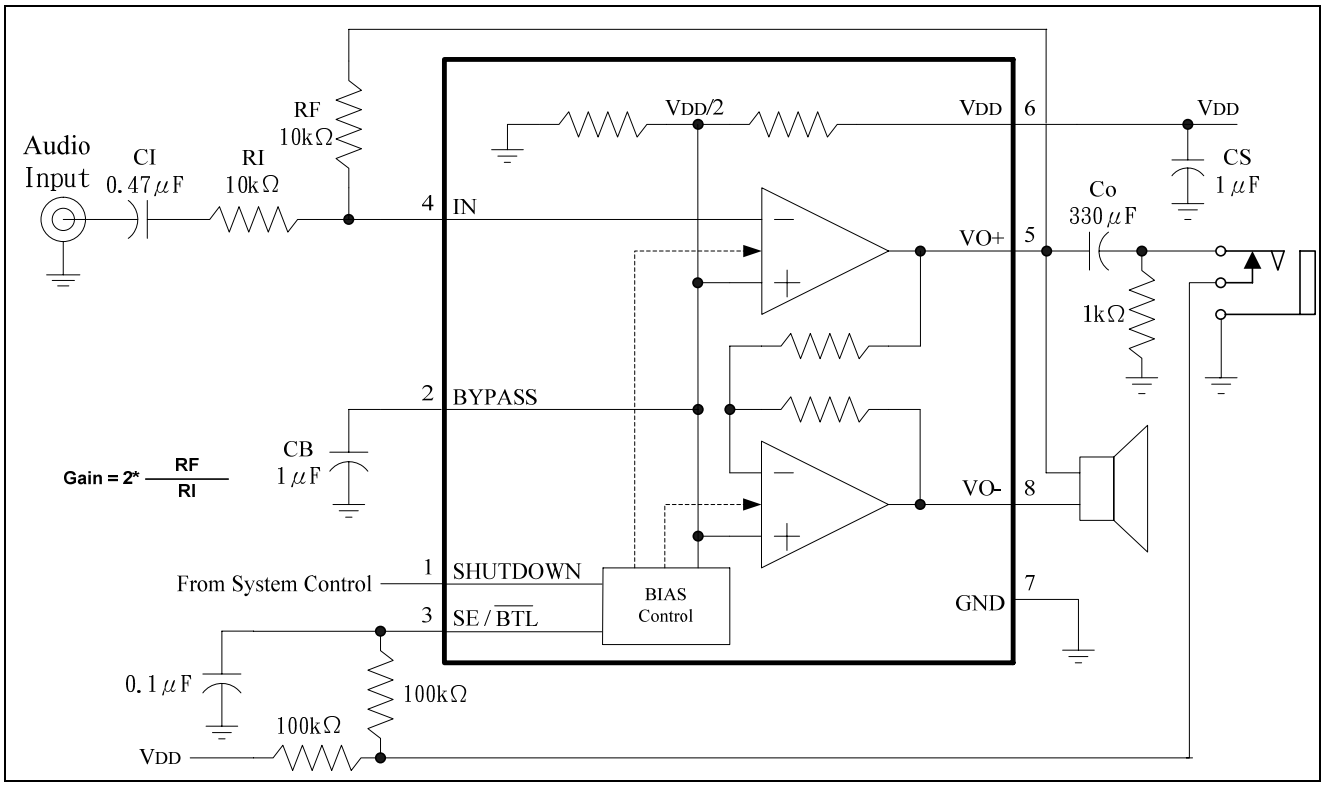
6.1. GPY0031A Typical Application Circuit



6.2. GPY0031A Differential Input Application Circuit



6.3. GPY0032A Typical Application Circuit



6.4. BTL Amplifier Efficiency

The following equations are basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{\text{Output Power}}{\text{Input Power}} = \frac{P_{OUT}}{P_{SUP}} \quad (1)$$

Where

$$P_{OUT} = \frac{V_{O.RMS}^2}{R_L} = \frac{V_P^2}{2R_L} \quad (2)$$

$$V_{O.RMS} = \frac{V_P^2}{\sqrt{2}} \quad (3)$$

$$P_{SUP} = V_{DD} \times I_{DD.AVG} = V_{DD} \times \frac{2V_P}{\pi R_L} \quad (4)$$

Efficiency of a BTL configuration:

$$\frac{P_{OUT}}{P_{SUP}} = \frac{\pi V_P}{4V_{DD}} \quad (5)$$

$$P_D = P_{SUP} - P_{OUT} \quad (6)$$

Table-1 Efficiency vs. Output Power in 3.3V 8Ω BTL System

P_{OUT} (W)	Efficiency (%)	V_P (V)	P_D (W)
0.125	33.6	1.41	0.26
0.250	47.6	2.00	0.29
0.375	58.3	2.45*	0.28

* High-peak voltage values cause the THD to increase.

6.5. Power Dissipation

Power Dissipation is major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. Equation 7 states the maximum power dissipation point for a single-ended mode operating at a given supply voltage and driving a specified output load.

$$P_{D.MAX} = (V_{DD})^2/(2\pi^2 R_L) \quad \text{Single-Ended (7)}$$

However, a direct consequence of the increased power delivered to the load by bridge amplifier is an increment in internal power dissipation point for a bridge amplifier operating at the same conditions.

$$P_{D.MAX} = 4(V_{DD})^2/(2\pi^2 R_L) \quad \text{Bridge-Mode (8)}$$

Since the GPY0031A/32A has two operational amplifiers in one package, the maximum internal power dissipation is four times

that of a single-end amplifier. The maximum power dissipation from equation 8 must not be greater than the power dissipation that results from the equation 9.

$$P_{D.MAX} = (T_{J.MAX}-T_J) /\theta_{JA} \quad (9)$$

For SOP-8 package with and without thermal pad, the thermal resistance (θ_{JA}) is equal to 60°C/W and 160°C/W, respectively.

Since the maximum junction temperature ($T_{J.MAX}$) of GPY0031A/32A is 150°C and ambient temperature (T_A) is defined by the power system design, the maximum power dissipation which the IC package is able to handle from equation 9. Once the power dissipation is greater than the maximum limit ($P_{D.MAX}$), either the supply voltage (V_{DD}) must be decreased, the load impedance (R_L) must be increased, or the θ_{JA} must be reduced with heat-sink.

Example: V_{DD}=6.0V, Load=8Ω, T_A=30°C, GPY0031A SOP-8 without thermal pad (θ_{JA}=160°C/W).

From equation 9:

$P_{D.MAX} = (150-30)/160 = 0.75W < 4(V_{DD})^2 /(2\pi^2 R_L) = 0.913W$

Decrease Power Voltage V_{DD} to 5V.

$P_{D.MAX} = (150-30)/160 = 0.75W > 4(V_{DD})^2 /(2\pi^2 R_L) = 0.634W$

6.6. Thermal Pad Considerations

The thermal pad must be connected to ground. The package with thermal pad of the GPY0031A/32A requires special attention on thermal design. If the thermal design issues are not properly addressed, the GPY0031A/32A will go into thermal shutdown when driving an 8Ω load.

Thermal pad on the bottom of the GPY0031A/32A should be soldered down to a copper pad on the circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. The copper plane used to conduct heat away from the thermal pad should be as large as practical.

If the ambient temperature is higher than 25°C, a larger copper plane or forced-air cooling will be required to keep the GPY0031A/32A junction temperature below thermal shutdown temperature (150°C).

In higher ambient temperature, higher airflow rate and/or larger copper area will be required to keep the IC out of thermal shutdown.

Table-2 Output Power vs. Junction Temperature in BTL System (T_A=25°C)

Output Power P_{OUT} (W)	Efficiency (%)	Internal Dissipation P_D (W)	Power From Supply P_{SUP} (W)	V_{OUT} Peak-to-Peak V_P (V)	Junction Temperature T_J – SOP-8 (°C)	Junction Temperature T_J – MSOP-8 (°C)	Junction Temperature T_J – SOP-8-P / MSOP-8-P (°C)
V_{DD} = 3.3V, Load=4Ω System							
0.5	47.6	0.55	1.05	2.00	113.0	135.0	58.0
0.8	60.2	0.53	1.33	2.53	109.8	131.0	56.8
1.1	70.7	0.46	1.56	2.97	98.6	117.0	52.6
V_{DD} = 5V, Load=4Ω System							
0.5	31.4	1.09	1.59	2.00	**199.4***	**243.0***	90.4
1	44.0	1.25	2.25	2.83	**225.0***	**275.0***	100.0
2	62.8	1.18	3.18	4.00	**213.8***	**261.0***	95.8
V_{DD} = 6V, Load=4Ω System							
0.5	26.2	1.41	1.91	2.00	**250.6***	**307.0***	109.6
1	37.0	1.70	2.70	2.83	**297.0***	**365.0***	127.0
2	52.3	1.82	3.82	4.00	**316.2***	**389.0***	134.2
V_{DD} = 3.3V, Load=8Ω System							
0.25	47.6	0.28	0.53	2.00	69.8	81.0	41.8
0.4	60.2	0.26	0.66	2.53	66.6	77.0	40.6
0.55	70.7	0.22	0.77	2.97	60.2	69.0	38.2
V_{DD} = 5V, Load=8Ω System							
0.5	44.4	0.63	1.13	2.83	125.8	**151.0***	62.8
1	62.8	0.59	1.59	4.00	119.4	143.0	60.4
1.27	70.7	0.52	1.79	4.50	108.2	129.0	56.2
V_{DD} = 6V, Load=8Ω System							
0.5	37.0	0.85	1.35	2.83	**161.0***	**195.0***	76.0
1	52.3	0.91	1.91	4.00	**170.6***	**207.0***	79.6
1.82	70.7	0.76	2.58	5.40	146.6	**177.0***	70.6

*** T_J must be less than $T_{J.MAX}$ (150°C).**

**** $T_J = \theta_{JA} \times P_D + T_A$; θ_{JA}(SOP-8) = 160°C/W ; θ_{JA}(MSOP-8) = 200°C/W; θ_{JA}(SOP-8-P or MSOP-8-P) = 60°C/W**

7. PACKAGE/PAD LOCATIONS

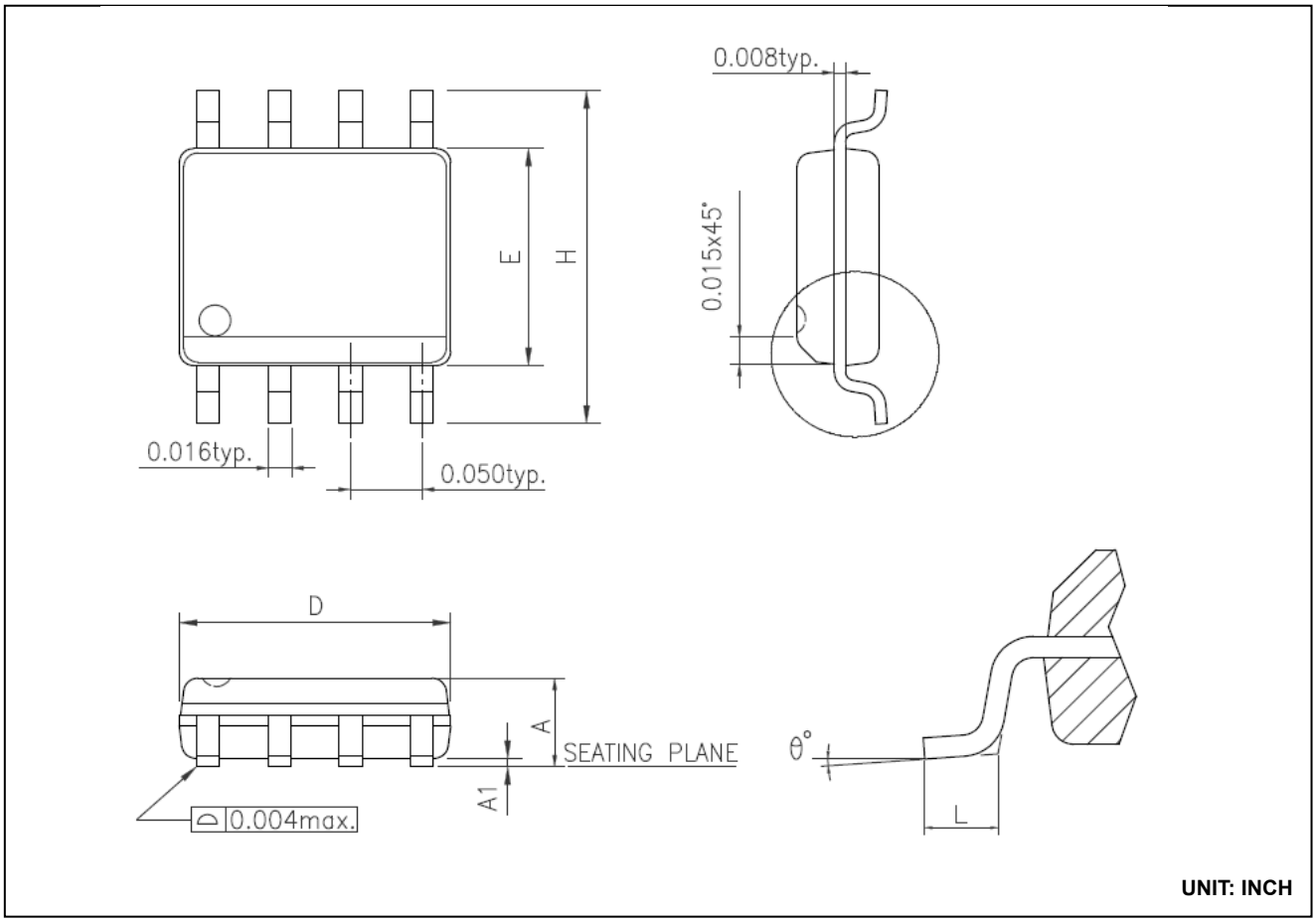
7.1. Ordering Information

Product Number	Package Type
GPY0031A – HS011	Green Package – SOP-8 (150mil)
GPY0031A – HS141	Green Package – SOP-8-P With Thermal PAD (150mil)
GPY0032A – HS01x	Green Package – SOP-8 (150mil)

Note: Package form number (x = 1 - 9, serial number).

7.2. Package Information

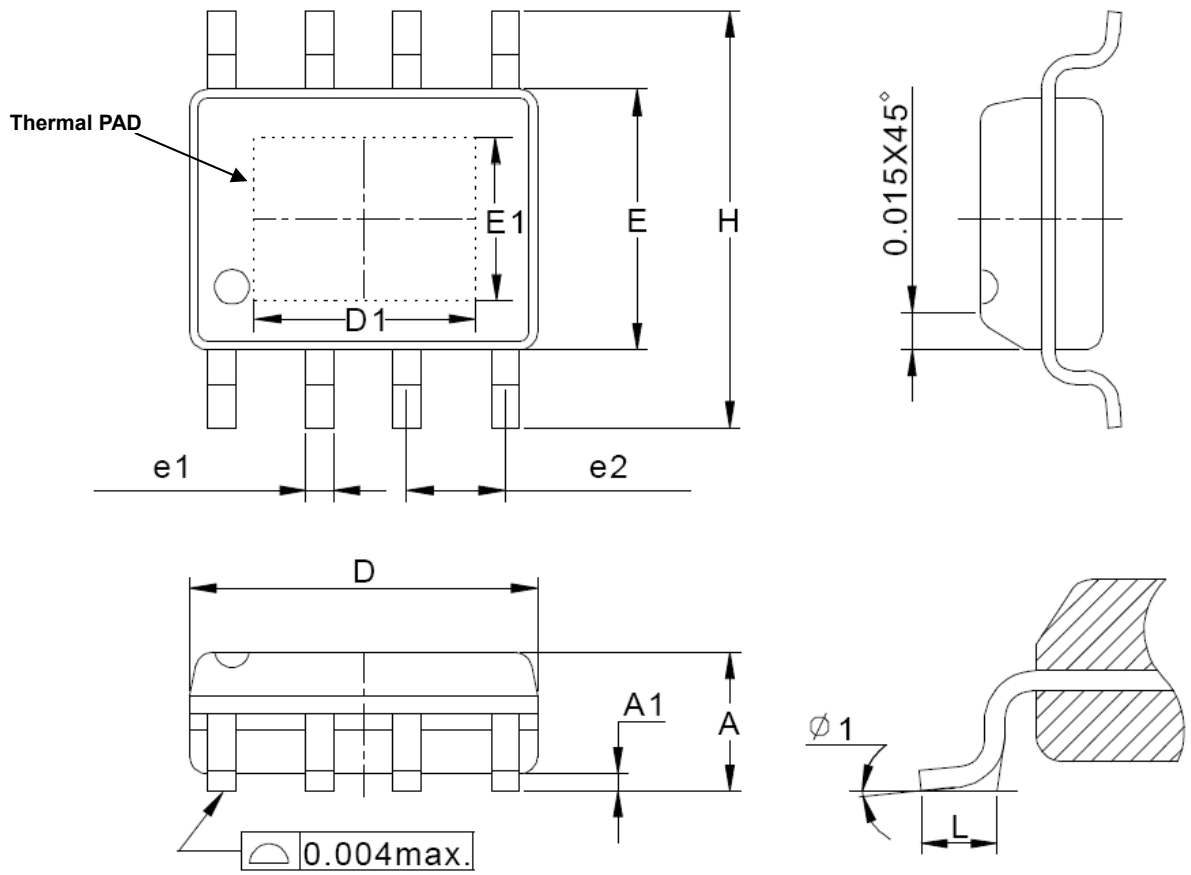
7.2.1. SOP-8



UNIT: INCH

Symbol	Dimension in inch		
	Min.	Typ.	Max.
A	0.053	-	0.069
A1	0.004	-	0.010
D	0.189	-	0.196
E	0.150	-	0.157
H	0.228	-	0.244
L	0.016	-	0.050
θº	0	-	8

7.2.2. SOP-8-P



UNIT: INCH

Symbol	Dimension in inch		
	Min.	Typ.	Max.
A	0.053	-	0.067
A1	0.000	-	0.006
D	0.189		0.196
D1	0.077	-	0.090
E	0.150	-	0.157
E1	0.077	-	0.090
H	0.228	-	0.244
L	0.016	-	0.050
e1	-	0.016	-
e2	-	0.050	-
Φ1	8°		

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9. REVISION HISTORY

Date	Revision #	Description	Page
MAR. 14, 2014	1.5	1. Modify Package Pin Assignment in section 4.1. 2. Modify Thermal Characteristics in section 5.2. 3. Modify Order Information in section 7.1. 4. Delete MSOP-8 and MSOP-8-P Package Information in section 7.2.3 and 7.2.4	6 7 24 26-27
JAN. 18, 2010	1.4	1. Modify Order Information in section 7.1.	25
SEP. 08, 2009	1.3	1. Modify Package Pin Assignment in section 4.1. 2. Modify Thermal Characteristics in section 5.2. 3. Add Current Limitation in section 5.3. 4. Add BTL Amplifier Efficiency in section 6.4. 5. Add Power Dissipation in section 6.5. 6. Add Thermal Pad Considerations in section 6.6. 7. Add Table 2. Output Power vs. Junction Temperature in BTL System in section 6. 8. Modify Ordering Information in section 7.1. 9. Add MSOP-8 Package Information in section 7.2.3. 10. Add MSOP-8-P Package Information in section 7.2.4.	6 7 7-8 21 21-22 22 23 24 26 27
JUL. 14, 2009	1.2	1. Modify Signal Description in section 4. 2. Modify Thermal Characteristics in section 5.2	5 7
MAY 06, 2009	1.1	1. Modify Feature in section 2. 2. Modify DC Characteristics in section 5.3.	3 7, 8
DEC. 19, 2008	1.0	1. Modify the title page for 2.0W Audio Power Amplifier. 2. Modify Package Pin Assignment in section 4.1. 3. Modify DC Characteristics in section 5.3. 4. Modify Typical Performance Characteristics in section 5.4. 5. Modify Ordering Information section 7.1. 6. Modify Package Information in section 7.2.	1 6 7 9 22 22
AUG. 20, 2008	0.1	Original	16