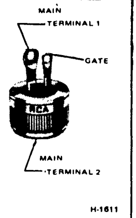
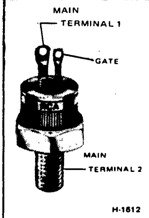
RCA
Solid State
Division

Thyristors
T4103 T4104 T4105
T4113 T4114 T4115
Series



T4103 Series
T4104 Series
T4105 Series

PRESS-FIT



T4113 Series
T4114 Series
T4115 Series

STUD

400-Hz, 6,10, & 15-A Silicon Triacs

For Control-Systems Application in Airborne and Ground-Support Type Equipment

Features:

- di/dt capability = 150 A/μs
- Shorted-emitter center-gate design
- Commutating dv/dt capability characterized at 400 Hz

Package / Voltage	Press-fit Types			Stud Types		
200 V Types	T4103B (40783)	T4104B (40779)	T4105B (40775)	T4113B (40785)	T4114B (40781)	T4115B (40777)
400 V Types	T4103D (40784)	T4104D (40780)	T4105D (40776)	T4113D (40786)	T4114D (40782)	T4115D (40778)

Numbers in parentheses are former RCA type numbers.

These RCA triacs are gate-controlled full-wave silicon ac switches.

The devices are designed to switch from an off-state to an on-state for either polarity of applied voltage with positive or negative gate triggering voltages.

They are intended for operation up to 400 Hz with resistive or inductive loads and nominal line voltages of 115 and 208 V RMS sine wave and repetitive peak off-state voltages of 200 V and 400 V.

These triacs exhibit commutating voltage (dv/dt) capability at high commutating current (di/dt). They can also be used in 60-Hz applications where high commutating capability is required.

MAXIMUM RATINGS, *Absolute-Maximum Values:*
For Operation with Sinusoidal Supply Voltage at Frequencies up to 400 Hz and with Resistive or Inductive Load.

		T4103B T4113B T4104B T4114B T4105B T4115B	T4103D T4113D T4104D T4114D T4105D T4115D	
REPETITIVE PEAK OFF-STATE VOLTAGE:*	V_{DROM}			
Gate open, T_J = −50 to 100°C		200	400	V
RMS ON-STATE CURRENT (Conduction angle = 360°):	$I_{T(RMS)}$			
Case temperature				
T_C = 90°C (T4105B, T4105D, T4115B, T4115D)		6		A
= 85°C (T4104B, T4104D, T4114B, T4114D)		10		A
= 80°C (T4103B, T4103D, T4113B, T4113D)		15		A
For other conditions		*See Fig. 3*		
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT:	I_{TSM}			
For one cycle of applied principal voltage, T_C as above				
400 Hz (sinusoidal)		200		A
60 Hz (sinusoidal)		100		A
50 Hz (sinusoidal)		85		A
For more than one cycle of applied principal voltage		*See Fig. 4*		
RATE-OF-CHANGE OF ON-STATE CURRENT:	di/dt			
V_{DM} = V_{DROM}, I_{GT} = 160 mA, t_r = 0.1 μs *(See Fig. 13)*		150		A/μs
FUSING CURRENT (for triac protection):				
T_J = −50 to 100°C, t = 1.25 to 10 ms	I^2t	30		A^2s
PEAK GATE-TRIGGER CURRENT:■	I_{GTM}			
For 1 μs max., *(See Fig. 7)*		4		A
GATE POWER DISSIPATION:				
PEAK (For 1 μs max., I_{GTM} ≤4 A, *See Fig. 7)*	P_{GM}	16		W
AVERAGE	$P_{G(AV)}$	0.2		W
TEMPERATURE RANGE:▲				
Storage	T_{stg}	-50 to 150		°C
Operating (Case)	T_C	-50 to 100		°C
TERMINAL TEMPERATURE (During soldering):				
For 10 s max. (terminals and case)	T_T	225		°C

* For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
■ For either polarity of gate voltage (V_G) with reference to main terminal 1.
▲ For temperature measurement reference point, see Dimensional Outline.

MAXIMUM RATINGS, *Absolute-Maximum Values:*
For Operation with Sinusoidal Supply Voltage at Frequencies up to 400 Hz and with Resistive or Inductive Load. (Cont'd.).

	T4103B T4104B T4105B	T4113B T4114B T4115B	T4103D T4104D T4105D	T4113D T4114D T4115D	
STUD TORQUE: τ_S					
Recommended			35		in-1b
Maximum (DO NOT EXCEED).....................			50		in-1b

ELECTRICAL CHARACTERISTICS
At Maximum Ratings and at Indicated Case Temperature (T_C) Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	LIMITS ALL TYPES Min.	Typ.	Max.	UNITS
Peak Off-State Current:♦ Gate open, T_J = 100°C, V_{DROM} = Max. rated value	I_{DROM}	–	0.1	2	mA
Maximum On-State Voltage:♦ For i_T = 21 A (peak), T_C = 25 °C.	V_{TM}	–	1.4	1.8	V
DC Holding Current:♦ Gate open, Initial principal current = 500 mA (DC), v_D = 12 V, T_C = 25° C.	I_{HO}	–	20	75	mA
For other case temperatures		See Fig. 6			
Critical Rate-of-Rise of Commutation Voltage:♦ For v_D = V_{DROM}, $I_{T(RMS)}$ = rated value, gate unenergized, (See Fig. 14):					
Commutating di/dt = 21.4 A/ms, T_C = 90° C T4105B, T4105D, T4115B, T4115D	dv/dt	5	10	–	V/μs
Commutating di/dt = 36 A/ms, T_C = 85° C T4104B, T4104D, T4114B, T4114D	dv/dt	5	10	–	V/μs
Commutating di/dt = 53.3 A/ms, T_C = 80° C T4103B, T4103D, T4113B, T4113D	dv/dt	5	10	–	V/μs
Critical Rate-of-Rise of Off-State Voltage:♦ For v_D = V_{DROM}, exponential voltage rise, gate open, T_C = 100° C.	dv/dt	30	150	–	V/μs
DC Gate-Trigger Current:♦† For v_D = 12 V (DC), R_L = 30 Ω, and T_C = 25 °C — Mode I+, V_{MT2} positive, V_G positive	I_{GT}	–	20	50	mA
Mode III−, V_{MT2} negative, V_G negative	I_{GT}	–	20	50	mA
Mode I−, V_{MT2} positive, V_G negative	I_{GT}	–	35	80	mA
Mode III+, V_{MT2} negative, V_G positive	I_{GT}	–	35	80	mA
For other case temperatures.		See Figs. 8 & 9			
DC Gate-Trigger Voltage:♦† For v_D = 12 V(DC), R_L = 30Ω, T_C = 25°C.	V_{GT}	–	1	2.5	V
For other case temperatures.		See Fig. 10			
For v_D = V_{DROM}, R_L = 125Ω, T_C = 100°C	V_{GT}	0.2	–	–	V
Gate-Controlled Turn-On Time: (Delay Time + Rise Time) For v_D = V_{DROM}, I_{GT} = 160mA, t_r = 0.1 μs, i_T = 25A (peak), T_C = 25°C, (See Figs. 11 & 15)	t_{gt}	–	1.6	2.5	μs
Thermal Resistance Steady-State (Junction-to-Case)	$\theta_{J\text{-}C}$	–	–	1	°C/W
Transient (Junction-to-Case).		See Fig. 12			
Steady-State (Junction-to-Ambient).	$\theta_{J\text{-}A}$	–	–	33	°C/W

♦ For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.

† For either polarity of gate voltage (V_G) with reference to main terminal 1.

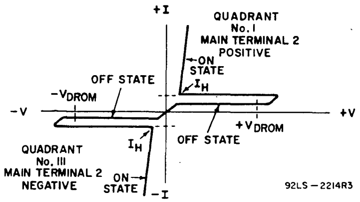


Fig. 1 — Principal voltage-current characteristic.

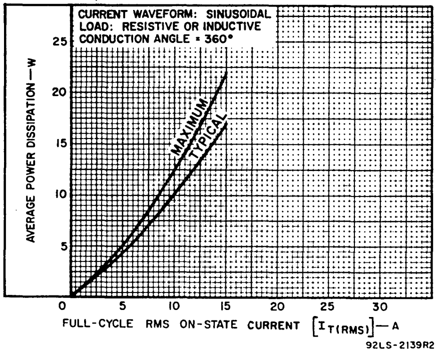


Fig. 2 — Power dissipation vs. on-state current.

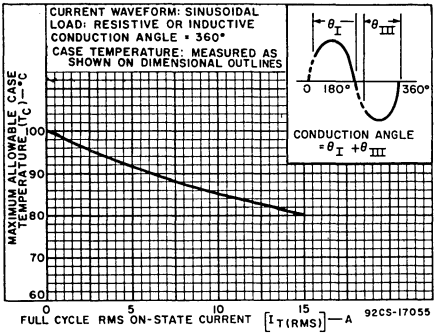


Fig. 3 — Maximum allowable case temperature vs. on-state current.

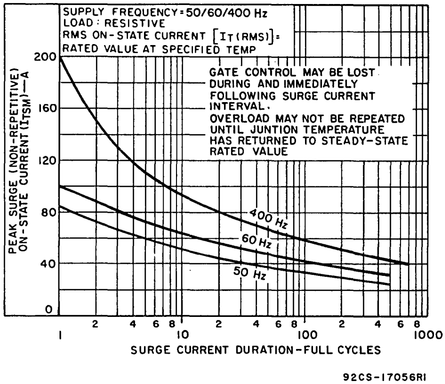


Fig. 4 — Peak surge on-state current vs. surge-current duration.

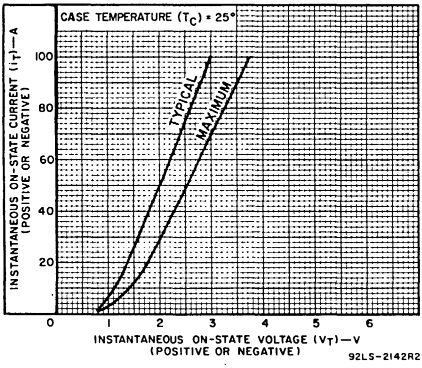


Fig. 5 — On-state current vs. on-state voltage.

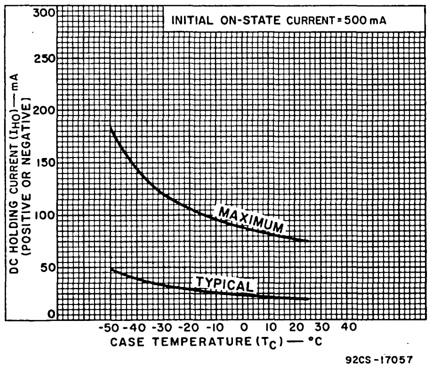


Fig. 6 — DC holding current vs. case temperature.

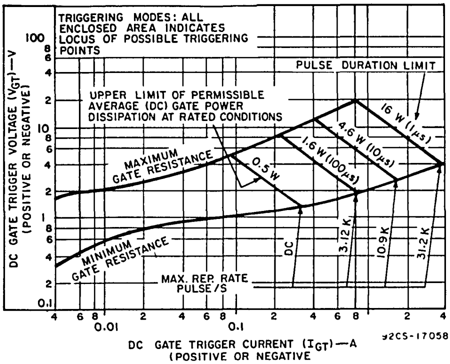


Fig. 7 – Gate trigger characteristics and limiting conditions for determination of permissible gate trigger pulses.

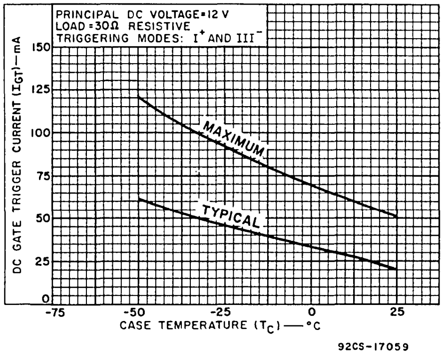


Fig. 8 – DC gate-trigger current vs. case temperature. (I^+ & III^- modes).

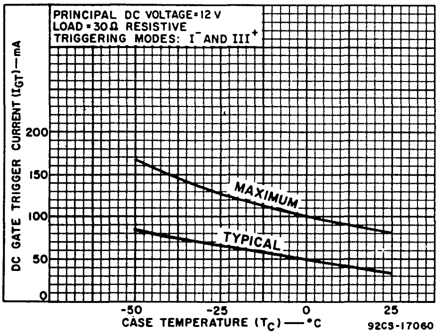


Fig. 9 – DC gate-trigger current vs. case temperature. (I^- & III^+ modes).

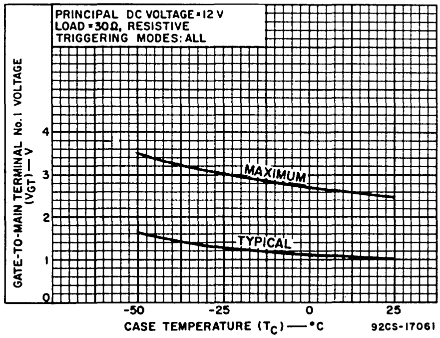


Fig. 10 – DC gate-trigger voltage vs. case temperature.

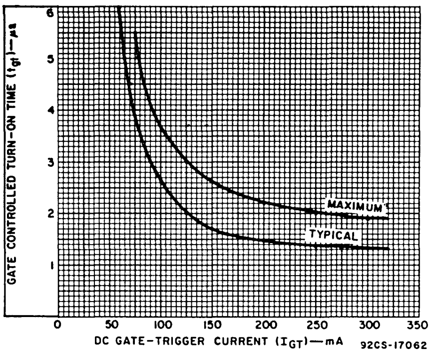


Fig. 11 – Turn-on time vs. gate trigger current.

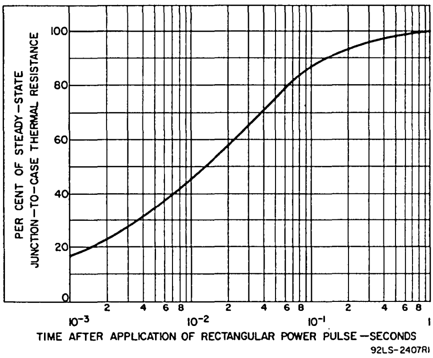


Fig. 12 – Transient thermal resistance vs. time (junction-to-case).

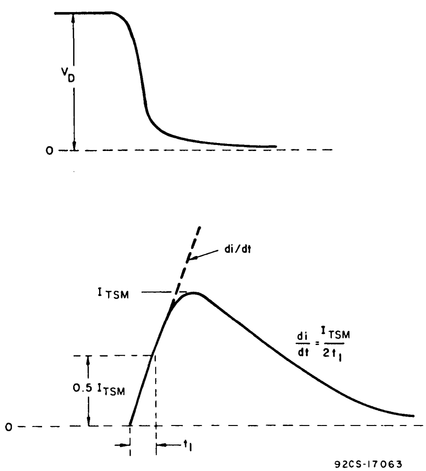


Fig. 13 — Rate of change of on-state current with time (defining di/dt).

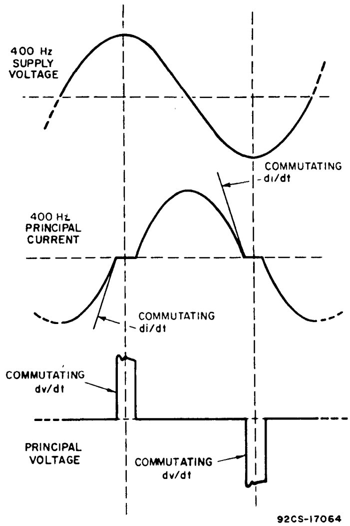


Fig. 14 — Relationship between supply voltage and principal current (inductive load) showing reference points for definition of commutating voltage (dv/dt).

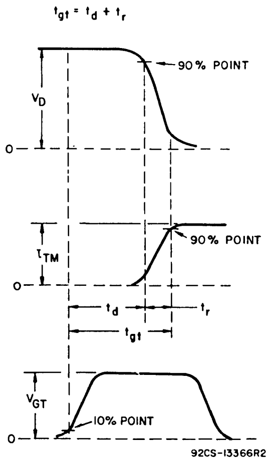


Fig. 15 — Relationship between off-state voltage, on-state current, and gate-trigger voltage showing reference points for definition of turn-on time (t_{gt}).

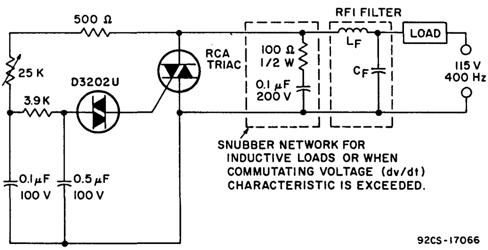


Fig. 16 — Typical phase-control circuit for operation at 400 Hz.

TERMINAL CONNECTIONS

No. 1—Gate
No. 2—Main Terminal 1
Case, No. 3—Main Terminal 2