

# 3N140 (SILICON)

## N-CHANNEL DUAL-GATE SILICON-NITRIDE PASSIVATED MOS FIELD-EFFECT TRANSISTOR

Depletion mode (Type B) dual-gate transistor designed for VHF amplifier and mixer applications.

- Silicon-Nitride Passivation for Excellent Long Term Stability
- High Common-Source Power Gain —  
 $G_{ps} = 16 \text{ dB (Min) @ } f = 200 \text{ MHz}$
- Low Reverse Transfer Capacitance —  
 $C_{rss} = 0.02 \text{ pF (Typ) @ } V_{DS} = 13 \text{ Vdc}$

## N-CHANNEL DUAL-GATE MOS FIELD-EFFECT TRANSISTOR

Type B



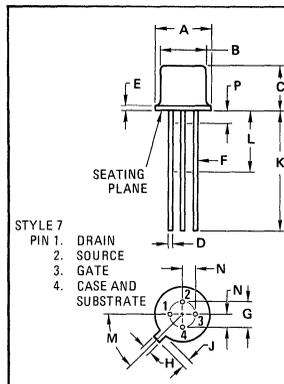
### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	0 to +20	Vdc
Drain-Gate 1 Voltage	$V_{DG1}$	20	Vdc
Drain-Gate 2 Voltage	$V_{DG2}$	20	Vdc
Reverse Gate 1-Source Voltage	$V_{GS1(r)}$	-8.0	Vdc
Reverse Gate 2-Source Voltage	$V_{GS2(r)}$	-8.0 to $0.4 V_{DS}$	Vdc
Forward Gate 1-Source Voltage	$V_{GS1(f)}$	+1.0	Vdc
Forward Gate 2-Source Voltage	$V_{GS2(f)}$	$0.4 V_{DS}$	Vdc
Drain Current	$I_D$	50	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	400 2.67	mW mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +175	$^\circ\text{C}$

### HANDLING PRECAUTIONS:

MOS field-effect transistors have extremely high input resistance. They can be damaged by the accumulation of excess static charge. Avoid possible damage to the devices while handling, testing, or in actual operation, by following the procedures outlined below:

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on because transient voltages may cause permanent damage to the devices.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	—	0.76	—	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC	—	0.100 BSC	—
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	—	0.500	—
L	6.35	—	0.250	—
M	45 $^\circ$ BSC	—	45 $^\circ$ BSC	—
N	1.27 BSC	—	0.050 BSC	—
P	—	1.27	—	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03  
TO-72

ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Gate 1-Source Cutoff Voltage (V <sub>DS</sub> = +16 Vdc, I <sub>D</sub> = 200 μA, V <sub>G2S</sub> = +4.0 Vdc)	V <sub>G1S(off)</sub>	-0.5	-4.0	Vdc
Gate 2-Source Cutoff Voltage (V <sub>DS</sub> = +16 Vdc, I <sub>D</sub> = 200 μA, V <sub>G1S</sub> = 0)	V <sub>G2S(off)</sub>	-0.5	-4.0	Vdc
Gate 1-Reverse Current (V <sub>G1S</sub> = 20 Vdc, V <sub>G2S</sub> = 0, V <sub>DS</sub> = 0) (V <sub>G1S</sub> = 20 Vdc, V <sub>DS</sub> = 0, V <sub>G2S</sub> = 0, T <sub>A</sub> = 125 °C)	I <sub>G1SS</sub>	-	1.0	nA μA
Gate 2-Reverse Current (V <sub>G2S</sub> = 20 Vdc, V <sub>G1S</sub> = 0, V <sub>DS</sub> = 0) (V <sub>G2S</sub> = 20 Vdc, V <sub>DS</sub> = 0, V <sub>G1S</sub> = 0, T <sub>A</sub> = 125 °C)	I <sub>G2SS</sub>	-	1.0	nA μA

ON CHARACTERISTICS

Zero-Gate Voltage Drain Current (V <sub>DD</sub> = +14 Vdc, V <sub>G1S</sub> = 0, V <sub>G2S</sub> = +14 Vdc)	I <sub>DSS</sub>	5.0	30	mA
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SMALL-SIGNAL CHARACTERISTICS

Forward Transconductance (V <sub>DD</sub> = +14 Vdc, I <sub>D</sub> = 10 mA, V <sub>G2S</sub> = +4.0 Vdc, f = 1.0 kHz)	Re(y <sub>fs</sub> )**	6000	18,000	μmhos
Input Capacitance (V <sub>DS</sub> = +13 Vdc, I <sub>D</sub> = 10 mA, V <sub>G2S</sub> = +4.0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	3.0	7.0	pF
Reverse Transfer Capacitance (V <sub>DS</sub> = +13 Vdc, I <sub>D</sub> = 10 mA, V <sub>G2S</sub> = +4.0 Vdc, f = 1.0 MHz)	C <sub>rss</sub> *	0.01	0.03	pF
Common-Source Noise Figure (See Figure 1) (V <sub>DD</sub> = +15 Vdc, R <sub>S</sub> = 275 Ohms, R <sub>G</sub> = 50 Ohms, f = 200 MHz)	NF	-	4.5	dB
Power Gain (See Figure 1) (f = 200 MHz)	G <sub>ps</sub>	16	22	dB
Bandwidth (See Figure 1) (f = 200 MHz)	BW	9.5	14.5	MHz

\*Drain-to-Gate 1

\*\*Gate 1-to-Drain

FIGURE 1 — 200 MHz POWER GAIN AND NOISE FIGURE TEST CIRCUIT

