

MM54C200/MM74C200 256-Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C200/MM74C200 is a 256-bit random access read/write memory. Inputs consist of eight address lines and three chip enables. The eight binary address inputs are decoded internally to select each of the 256 locations. The internal address register, latches, and address information are on the positive to negative edge of \overline{CE}_3 . The TRI-STATE data output line, working in conjunction with \overline{CE}_1 or \overline{CE}_2 inputs, provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of \overline{CE}_3 . It is therefore unnecessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition).

Note: The timing is different from the DM74200 in that a positive to negative transition of the \overline{CE}_3 must occur for the memory to be selected.

Read Operation: The data is read out by selecting the proper address and bringing \overline{CE}_3 low and WE high.

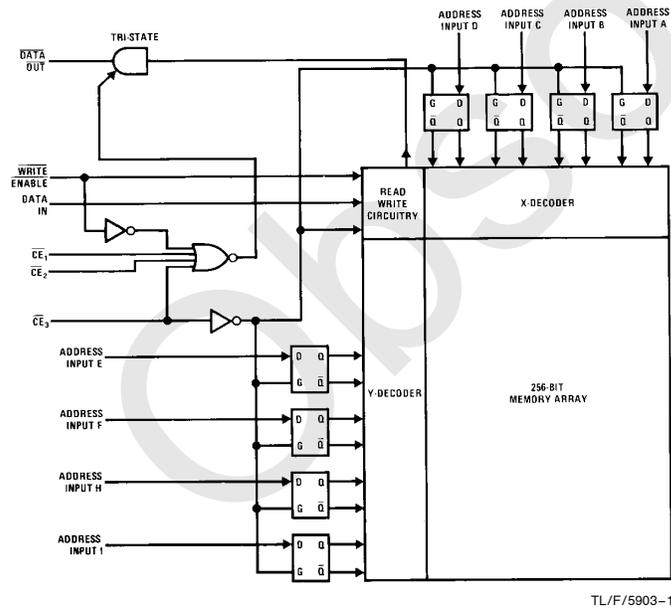
Holding either \overline{CE}_1 , \overline{CE}_2 , or \overline{CE}_3 at a high level forces the output into TRI-STATE. When used in bus-organized systems, \overline{CE}_1 , or \overline{CE}_2 , a TRI-STATE control provides for fast access times by not totally disabling the chip.

Write Operation: Data is written into the memory with \overline{CE}_3 low and WE low. The state of \overline{CE}_1 or \overline{CE}_2 has no effect on the write cycle. The output assumes TRI-STATE with \overline{WE} low.

Features

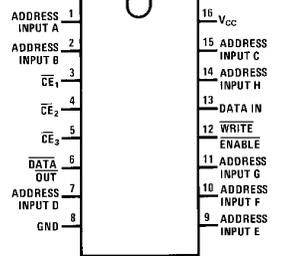
- Wide supply voltage range 3V to 15V
- Guaranteed noise margin 1V
- High noise immunity 0.45 V_{CC} (typ.)
- TTL compatibility Fan out of 1 driving standard TTL
- Low power 500 nW (typ.)
- Internal address register

Logic and Connection Diagrams



TL/F/5903-1

Dual-In-Line Package



TL/F/5903-2

Top View

Order Number MM54C200 or
MM74C200

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	-0.3V to $V_{CC} + 0.3V$
Operating Temperature Range (T_A)	-55°C to +125°C
MM54C200	-40°C to +85°C
MM74C200	-65°C to +150°C
Storage Temperature Range (T_S)	-65°C to +150°C

Power Dissipation (P_D)	700 mW
Dual-In-Line	500 mW
Small Outline	3V to 15V
Operating V_{CC} Range	18V
Absolute Maximum V_{CC}	260°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V, I_O = -10 \mu A$ $V_{CC} = 10V, I_O = -10 \mu A$	4.5 9			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V, I_O = +10 \mu A$ $V_{CC} = 10V, I_O = +10 \mu A$			0.5 1	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.1	600	μA
CMOS/TTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5V, I_O = -1.6 mA$ 74C $V_{CC} = 4.75V, I_O = -1.6 mA$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5V, I_O = 1.6 mA$ 74C $V_{CC} = 4.75V, I_O = 1.6 mA$			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5V, V_{OUT} = 0V$ $T_A = 25^\circ C$	-4 -1.8	-6		mA mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V, V_{OUT} = 0V$ $T_A = 25^\circ C$	-16 -1.5	-25		mA mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$	5	8		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$	20	30		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{ACC}	Access Time from Address	$V_{\text{CC}} = 5\text{V}$		450	900	ns
		$V_{\text{CC}} = 10\text{V}$		200	400	ns
t_{pd}	Propagation Delay from $\overline{\text{CE}}_3$	$V_{\text{CC}} = 5\text{V}$		360	700	ns
		$V_{\text{CC}} = 10\text{V}$		120	300	ns
t_{pCE1}	Propagation Delay from $\overline{\text{CE}}_1$ or $\overline{\text{CE}}_2$	$V_{\text{CC}} = 5\text{V}$		250	700	ns
		$V_{\text{CC}} = 10\text{V}$		85	200	ns
t_{SA}	Address Setup Time	$V_{\text{CC}} = 5\text{V}$	200	80		ns
		$V_{\text{CC}} = 10\text{V}$	100	30		ns
t_{HA}	Address Hold Time	$V_{\text{CC}} = 5\text{V}$	50	15		ns
		$V_{\text{CC}} = 10\text{V}$	25	5.0		ns
t_{WE}	Write Enable Pulse Width	$V_{\text{CC}} = 5\text{V}$	300	160		ns
		$V_{\text{CC}} = 10\text{V}$	150	70		ns
t_{CE}	$\overline{\text{CE}}_3$ Pulse Widths	$V_{\text{CC}} = 5\text{V}$	400	200		ns
		$V_{\text{CC}} = 10\text{V}$	160	80		ns
C_{IN}	Input Capacity	Any Input (Note 2)		5.0		pF
C_{OUT}	Output Capacity in TRI-STATE	(Note 2)		9.0		pF
C_{PD}	Power Dissipation Capacity	(Note 3)		400		pF

AC Electrical Characteristics* $C_L = 50\text{ pF}$

Symbol	Parameter	Conditions	MM54C200		MM74C200		Units
			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		
			Min	Max	Min	Max	
t_{ACC}	Access Time from Address	$V_{\text{CC}} = 5\text{V}$		1200		1100	ns
		$V_{\text{CC}} = 10\text{V}$		520		480	ns
t_{pd}	Propagation Delay from $\overline{\text{CE}}_3$	$V_{\text{CC}} = 5\text{V}$		950		850	ns
		$V_{\text{CC}} = 10\text{V}$		400		360	ns
t_{pdCE1}	Propagation Delay from $\overline{\text{CE}}_1$ or $\overline{\text{CE}}_2$	$V_{\text{CC}} = 5\text{V}$		650		600	ns
		$V_{\text{CC}} = 10\text{V}$		300		275	ns
t_{SA}	Address Setup Time	$V_{\text{CC}} = 5\text{V}$	250		250		ns
		$V_{\text{CC}} = 10\text{V}$	120		120		ns
t_{HA}	Address Hold Time	$V_{\text{CC}} = 5\text{V}$	100		100		ns
		$V_{\text{CC}} = 10\text{V}$	50		50		ns
t_{WE}	Write Enable Pulse Width	$V_{\text{CC}} = 5\text{V}$	450		400		ns
		$V_{\text{CC}} = 10\text{V}$	225		200		ns
t_{CE}	Disable Pulse Width	$V_{\text{CC}} = 5\text{V}$	500		460		ns
		$V_{\text{CC}} = 10\text{V}$	250		230		ns
t_{HD}	Data Hold Time	$V_{\text{CC}} = 5\text{V}$	50		50		ns
		$V_{\text{CC}} = 10\text{V}$	25		25		ns

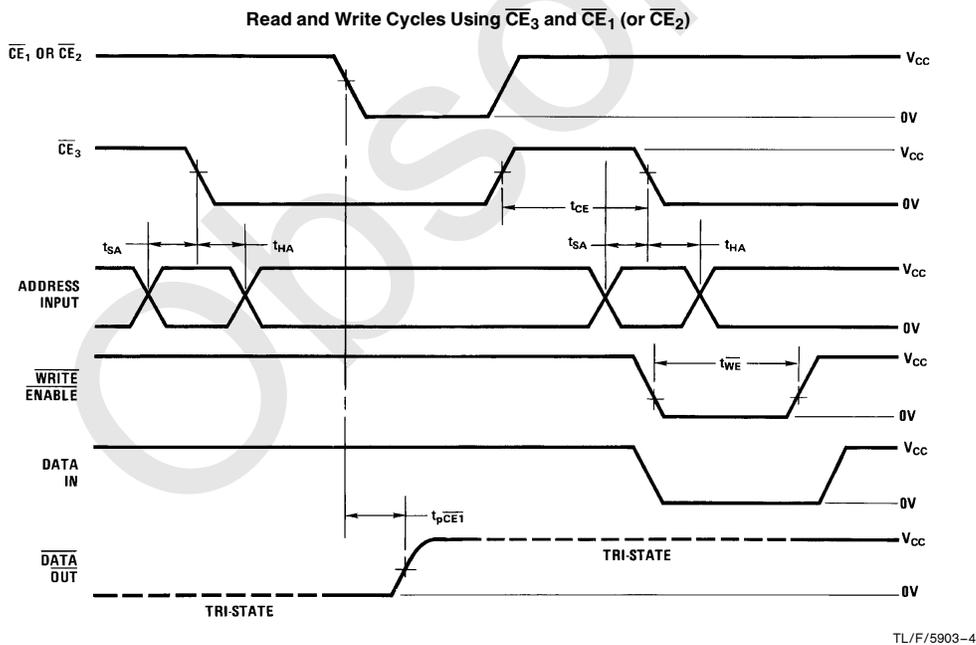
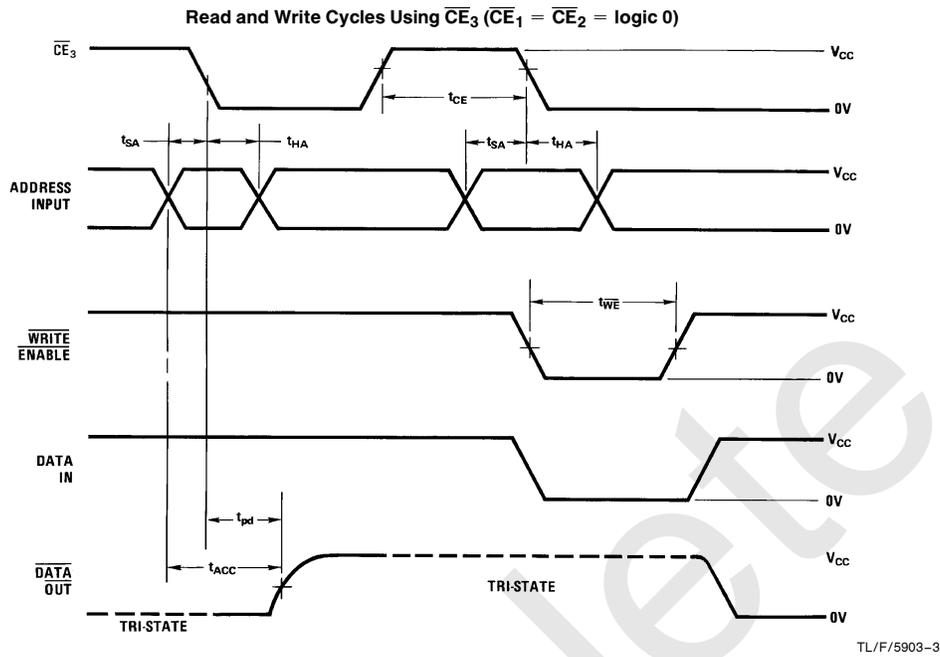
*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

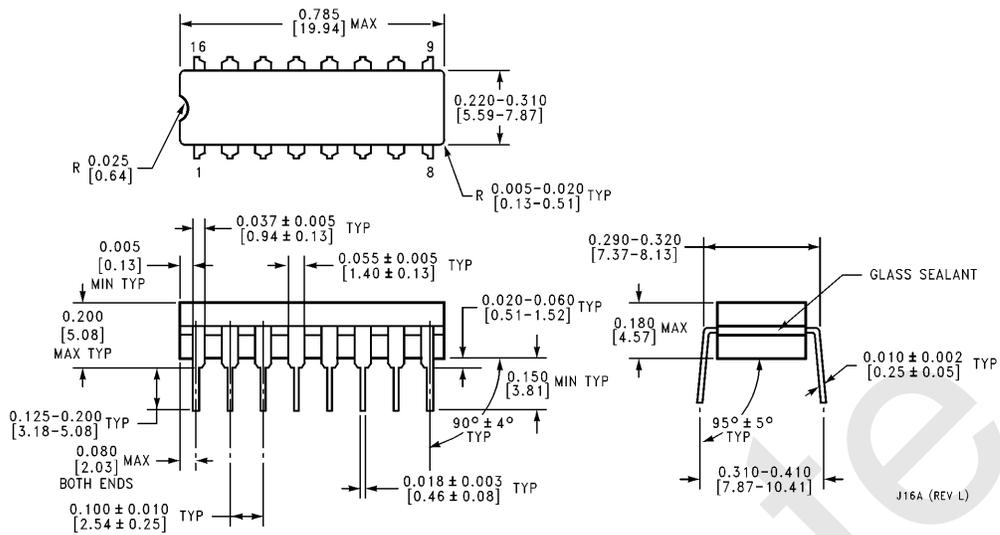
Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Switching Time Waveforms



Note: Used for fast access time in bused systems.

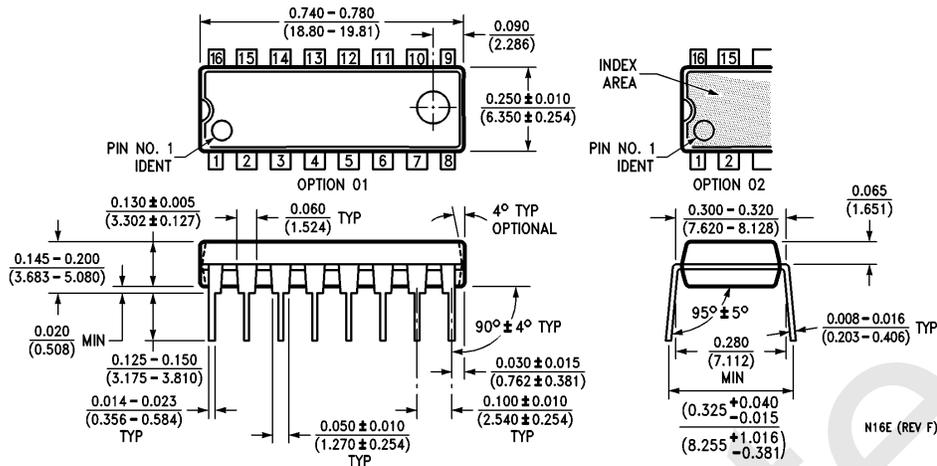
Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54C200J or MM74C200J
NS Package Number J16A

J16A (REV L)

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number MM54C200N or MM74C200N
NS Package Number N16E

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