Integrated Device Technology, Inc.

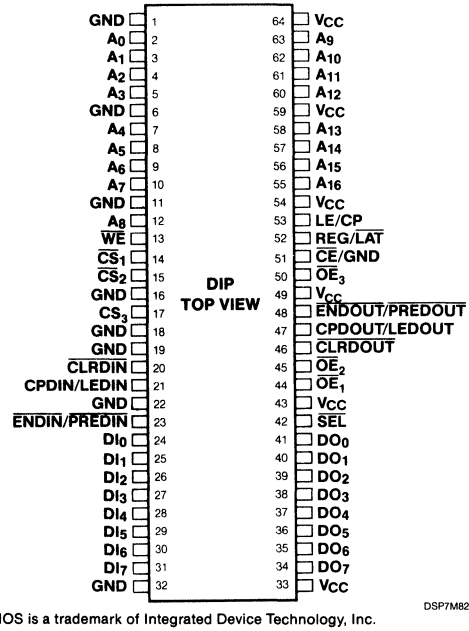
1 MEGABIT REGISTERED/ BUFFERED/LATCHED CMOS STATIC RAM MODULES

ADVANCE INFORMATION IDT7M824S FAMILY

FEATURES:

- High-density 1024K-bit (128K x 8-bit) CMOS static RAM modules with registered/buffered/latched addresses and I/Os
- Fast access times: 75ns max. commercial and military
- Low-power consumption (typ.): active 980mW; standby 150mW; full-standby 1.6mW
- Low input capacitance (typ.): input 20pF; output 25pF
- High output drive (min.): I_{OL} = 32mA; I_{OH} = −15mA
- 64-pin, 900 mil center sidebraze DIP with LCCs on both sides, achieving very high memory density
- Module select output
- Separate inputs and outputs
- Clear data and clock enables on all registers
- Addresses, inputs and outputs on separate clocks or latch enables
- Registered write enable
- Internal bypass capacitors for minimizing power supply noise
- TTL compatible; single 5V (±10%) power supply
- Five GND pins for maximum noise immunity, 5 V_{CC} pins
- Military grade module available with semiconductor components 100% manufactured and screened to MIL-STD-883, Class B

PIN CONFIGURATION



DSP7M824S-002

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DESCRIPTION:

The IDT7M824 family is a set of 1024K-bit (128K x 8-bit) high-speed CMOS static RAM modules with registered/buffered/latched addresses and I/Os. They are constructed on co-fired, multi-layered ceramic substrates with sidebrazed leads using 16 IDT71981 (16K x 4) static RAMs, IDT logic devices, and decoupling capacitors. Devices in leadless chip carriers are mounted top and bottom for maximum density.

Extremely high speeds are achievable by the use of IDT71981s and logic devices fabricated in IDT's high-performance, high-reliability technology, CEMOS™. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest circuits possible. The IDT7M824 has access times of 75ns (max.) over commercial and military temperature ranges, but it can be operated with cycle times as fast as 50ns if skewed clocks are used.

Designing with this device can be very flexible because of such features as module select output and clock enables on all registers, registered write enable and 8-bit separate inputs and outputs. Because of the proprietary IDT49C801, the modules are cascadable in terms of depth. The write enable can be turned off when the module is de-selected. Immunity to noise has been extended with such features as 8-bit separate inputs and outputs; addresses, inputs, and outputs on separate clocks; internal decoupling capacitors; five ground pins; and five V_{CC} pins.

The semiconductor components used on all IDT military modules are 100% processed to the test methods of MIL-STD-883, Class B. In addition IDT military modules are qualified to requirements patterned after MIL-STD-883, Method 5005 making them ideally suited to applications demanding the highest level of performance and reliability.

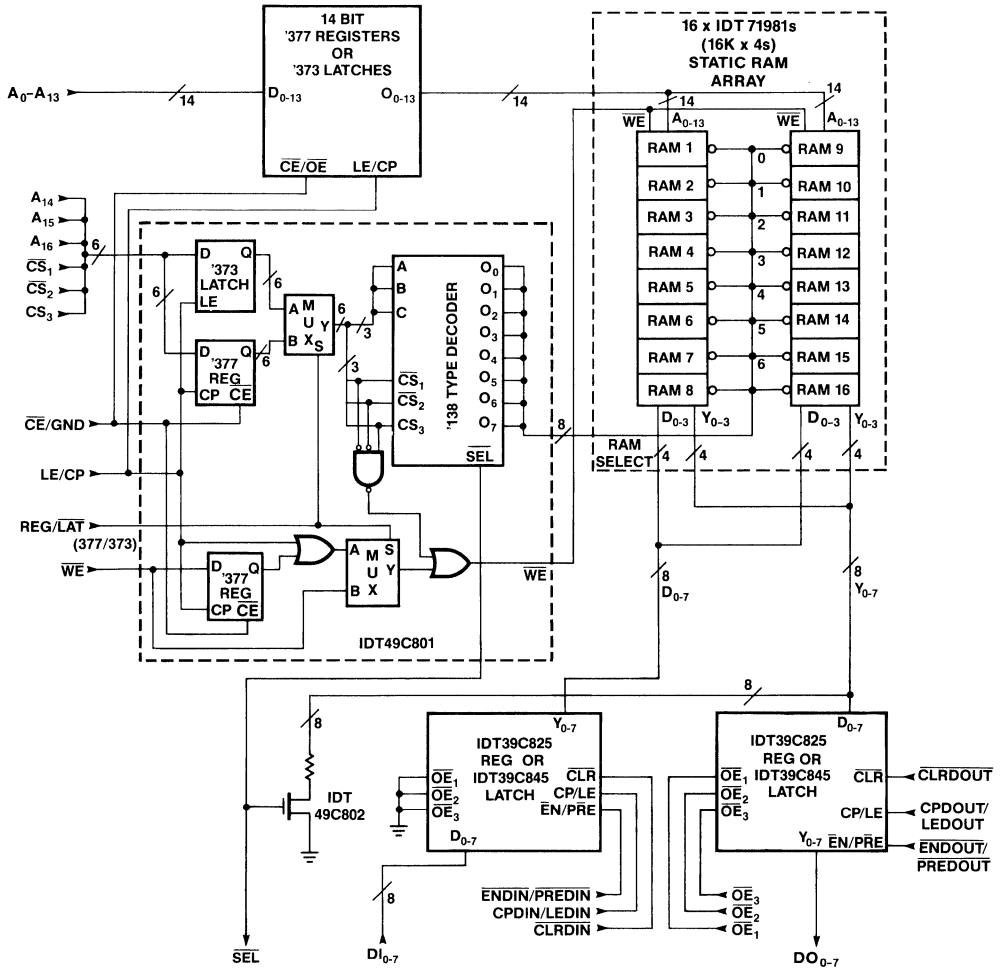
PRODUCT SELECTOR GUIDE

DATA INPUT & OUTPUT FEATURE	ADDRESS	
	REGISTERED	LATCHED
Input — Registered Output — Registered	IDT7M824SA	IDT7M824SE
Input — Registered Output — Latched	IDT7M824SB	IDT7M824SF
Input — Latched Output — Registered	IDT7M824SC	IDT7M824SG
Input — Latched Output — Latched	IDT7M824SD	IDT7M824SH

NOTE:

All V_{CC} pins (33, 43, 49, 54, 59 and 64) need to be connected to the 5V supply. and all GND pins (1, 6, 11, 16, 18, 19, 22, and 32) need to be grounded for proper operation.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

$A_0 - A_{16}$	Addresses
$DI_0 - DI_7$	Data input
$DO_0 - DO_7$	Data output
$\overline{CLRDIN}$	Data input latch/register clear
CPDIN/LEDIN	Data input register clock/latch enable
$\overline{ENDIN}/\overline{PREDIN}$	Data input register clock enable/ latch preset
$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$	Output enable
CPDOUT/LEDOUT	Data output register clock/latch enable
$\overline{ENDOUT}/\overline{PREDOUT}$	Data output register clock enable/ latch preset
$\overline{CS}_1$, $\overline{CS}_2$ & CS_3	Chip select
$\overline{WE}$	Write enable
$\overline{SEL}$	Select output
LE/CP	Latch enable/clock pulse control input
$\overline{CE}$/GND	Clock enable/ground
REG/$\overline{LAT}$	Register/latch (low active) input control
V_{CC}	Power
GND	Ground