

ILI2113A

Capacitive Touch Controller

Datasheet

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V1.01	2012/08/14	Jay Lee	Added Reference circuit
V1.02	2012/8/20	Jay Lee	Modified Reference Circuit
V1.03	2012/8/23	Jay Lee	Modified Typing Error
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V1.09	2013/03/06	Louis Lee	Modified Pin Configuration

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1 Description

ILI2113A is a single chip capacitive touch controller optimized for mobile phone touch panel design. It is a powerful SOC with specialized 32-bit MCU and 34-channel CDC (capacitance to digital converter). ILI2113A supports true 10-point touch with 100Hz report rate enabling the best human touch performance.

2 Feature

- 34 capacitive driving and sensing channels.
- 2.6V to 3.6V operating voltage.
- 1.62V to 1.98V IO operating voltage.
- Support 10-point touch
- I²C wire serial interface
- 48 pin QFN 6x6x0.8 package.

3 Block Diagram

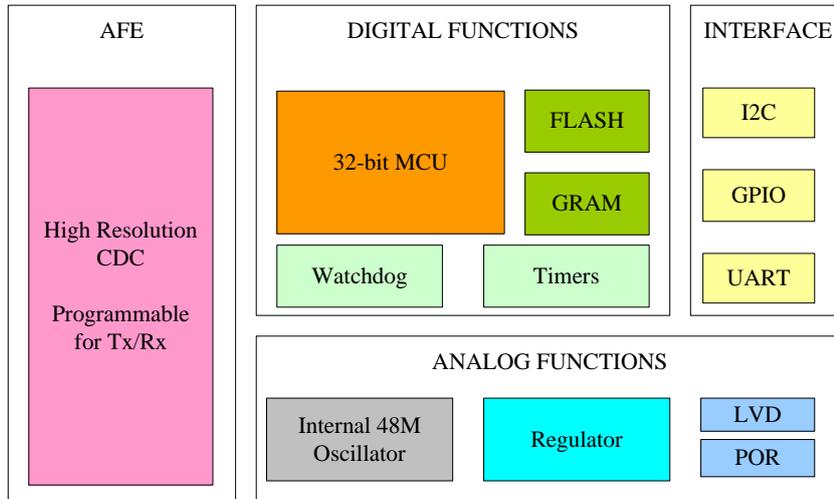


Figure 3-1 ILI2113A Block Diagram

4 Pin Configuration

4.1 ILI2113A (6X6X0.8, QFN48)

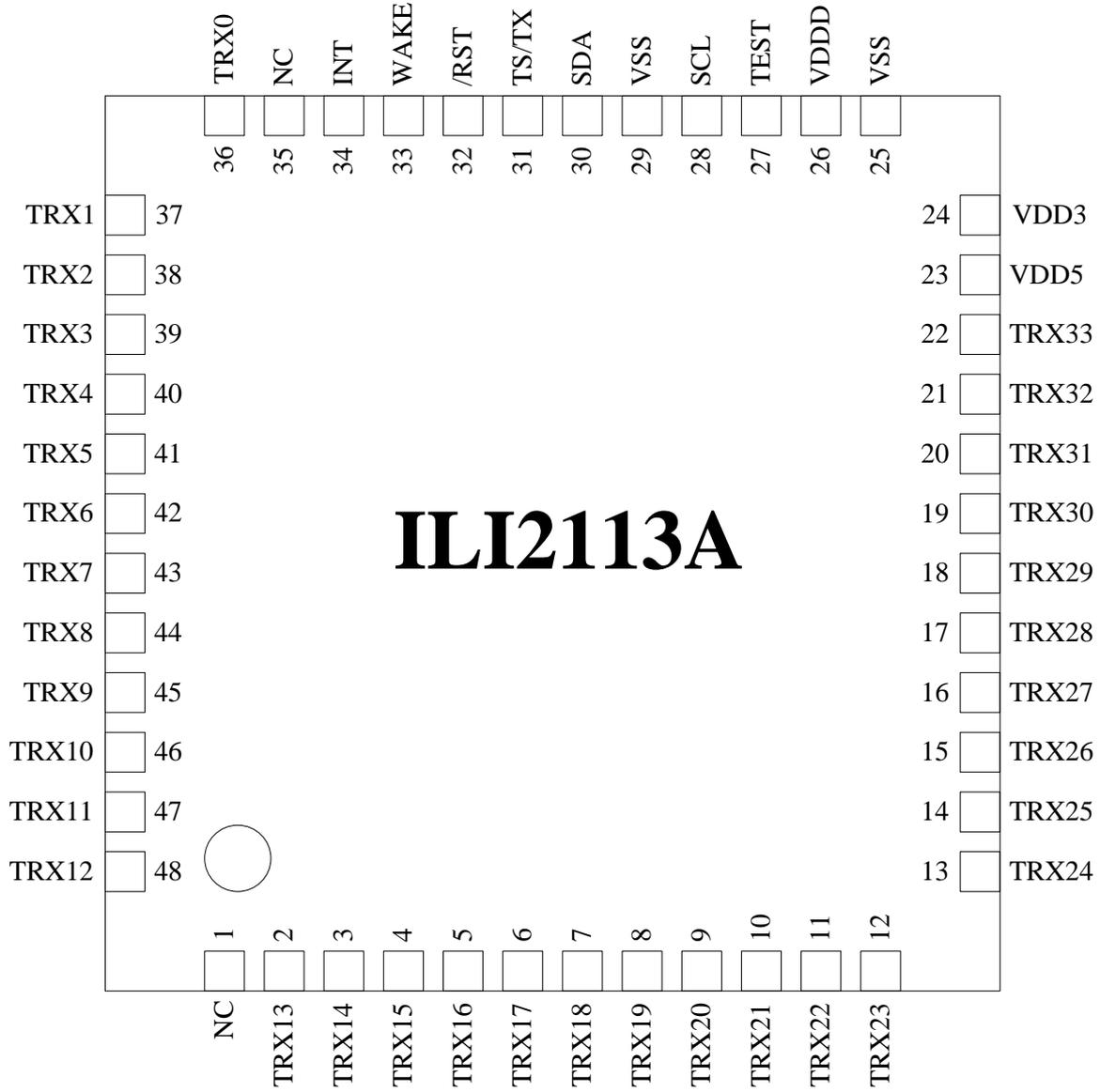


Figure 4-1: ILI2113A (QFN48) Package Diagram

4.2 Pinout Description

Table 4-1: Type Define

Symbol	Description
(A)	analog pad
(D)	Digital pad
(P)	Power pad
I	input pad
O	output pad
IO	input / output pad

Table 4-2: ILI2113A Pin Assignments

Pin Out	Name	Type	Description
1	NC	—	Not Connection.
2	TRX13	IO(A)	Transmit output or receive input channel for CTP.
3	TRX14	IO(A)	Transmit output or receive input channel for CTP.
4	TRX15	IO(A)	Transmit output or receive input channel for CTP.
5	TRX16	IO(A)	Transmit output or receive input channel for CTP.
6	TRX17	IO(A)	Transmit output or receive input channel for CTP.
7	TRX18	IO(A)	Transmit output or receive input channel for CTP.
8	TRX19	IO(A)	Transmit output or receive input channel for CTP.
9	TRX20	IO(A)	Transmit output or receive input channel for CTP.
10	TRX21	IO(A)	Transmit output or receive input channel for CTP.
11	TRX22	IO(A)	Transmit output or receive input channel for CTP.
12	TRX23	IO(A)	Transmit output or receive input channel for CTP.
13	TRX24	IO(A)	Transmit output or receive input channel for CTP.
14	TRX25	IO(A)	Transmit output or receive input channel for CTP.
15	TRX26	IO(A)	Transmit output or receive input channel for CTP.
16	TRX27	IO(A)	Transmit output or receive input channel for CTP.
17	TRX28	IO(A)	Transmit output or receive input channel for CTP.
18	TRX29	IO(A)	Transmit output or receive input channel for CTP.
19	TRX30	IO(A)	Transmit output or receive input channel for CTP.
20	TRX31	IO(A)	Transmit output or receive input channel for CTP.
21	TRX32	IO(A)	Transmit output or receive input channel for CTP.
22	TRX33	IO(A)	Transmit output or receive input channel for CTP.
23	VDD5	VDD(P)	Internal Generated 5V power supply. A 0.1μF ceramic capacitor to GND is required.

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24	VDD3	VDD(P)	Analog power supply.
25	VSS	GND(P)	Analog and digital ground.
26	VDDD	VDD(P)	Internal Generated 1.8V power supply. A 1μF ceramic capacitor to GND is required.
27	TEST	O(D)	Test mode output pin and floating in normal mode.
28	SCL	IO(D)	A serial clock pin for I ² C interface
29	VSS	GND(P)	Analog and digital ground.
30	SDA	IO(D)	A serial data pin for I ² C interface
31	TS/TX	O(D)	UART data transmitter pin.
32	/RST	I(D)	Hardware reset pin. Active low.
33	WAKE	I(D)	External interrupt pin from host.
34	INT	O(D)	External interrupt pin to host.
35	NC	—	Not Connection
36	TRX0	IO(A)	Transmit output or receive input channel for CTP.
37	TRX1	IO(A)	Transmit output or receive input channel for CTP.
38	TRX2	IO(A)	Transmit output or receive input channel for CTP.
39	TRX3	IO(A)	Transmit output or receive input channel for CTP.
40	TRX4	IO(A)	Transmit output or receive input channel for CTP.
41	TRX5	IO(A)	Transmit output or receive input channel for CTP.
42	TRX6	IO(A)	Transmit output or receive input channel for CTP.
43	TRX7	IO(A)	Transmit output or receive input channel for CTP.
44	TRX8	IO(A)	Transmit output or receive input channel for CTP.
45	TRX9	IO(A)	Transmit output or receive input channel for CTP.
46	TRX10	IO(A)	Transmit output or receive input channel for CTP.
47	TRX11	IO(A)	Transmit output or receive input channel for CTP.
48	TRX12	IO(A)	Transmit output or receive input channel for CTP.

5 Electrical Character

5.1 Absolute Maximum Ratings

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or under any other conditions above those indicated in the operational sections of this specification are not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5-1: Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit
System power supply voltage	VDD3	-0.3	3.6	V
HV power supply voltage	VDD5	-0.3	TBD	V
Digital power supply voltage	VDDD	-0.3	1.98	V
I/O power supply Voltage	VDDIO	-0.3	1.98	V
Operating temperature	T _{opr}	-40	+85	°C
Storage temperature	T _{stg}	-55	+125	°C

5.2 DC Characteristics

Table 5-2: Power Supply

Item	Symbol	Min	Typ.	Max	Unit
System power supply voltage	VDD3	2.6	3.3	3.6	V
HV power supply voltage	VDD5	—	TBD	—	V
Digital power supply voltage	VDDD	1.62	1.8	1.98	V
I/O power supply Voltage	VDDIO	—	VDDD	—	V

Table 5-3: DC Characteristics

(VDD = 3.3, GND = 0V, T_{opr} = 25°C)

Item	Symbol	Min	Typ.	Max	Unit	Condition
Input high voltage	V _{IH}	0.7*VDDIO	—	VDDIO	V	
Input low voltage	V _{IL}	-0.3	—	0.3*VDDIO	V	
Output high voltage	V _{OH}	—	VDDIO	—	V	
Output low voltage	V _{OL}	—	0.3	—	V	
Input leakage current	I _I	—	—	1	μA	
Pull-high/low impedance	R _{IN}	—	4.7K	—	Ω	
Operation mode current	I _{Op}	—	—	TBD	mA	
Standby current	I _{idle}	—	—	100	uA	

5.3 AC Characteristics of the SDA and SCL on I²C interface

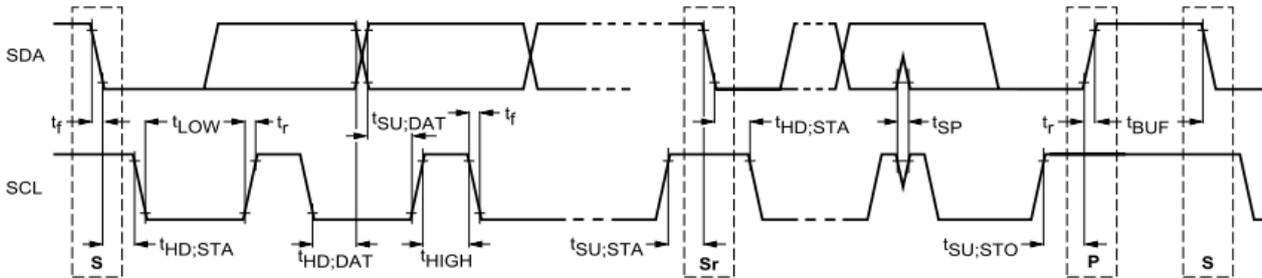


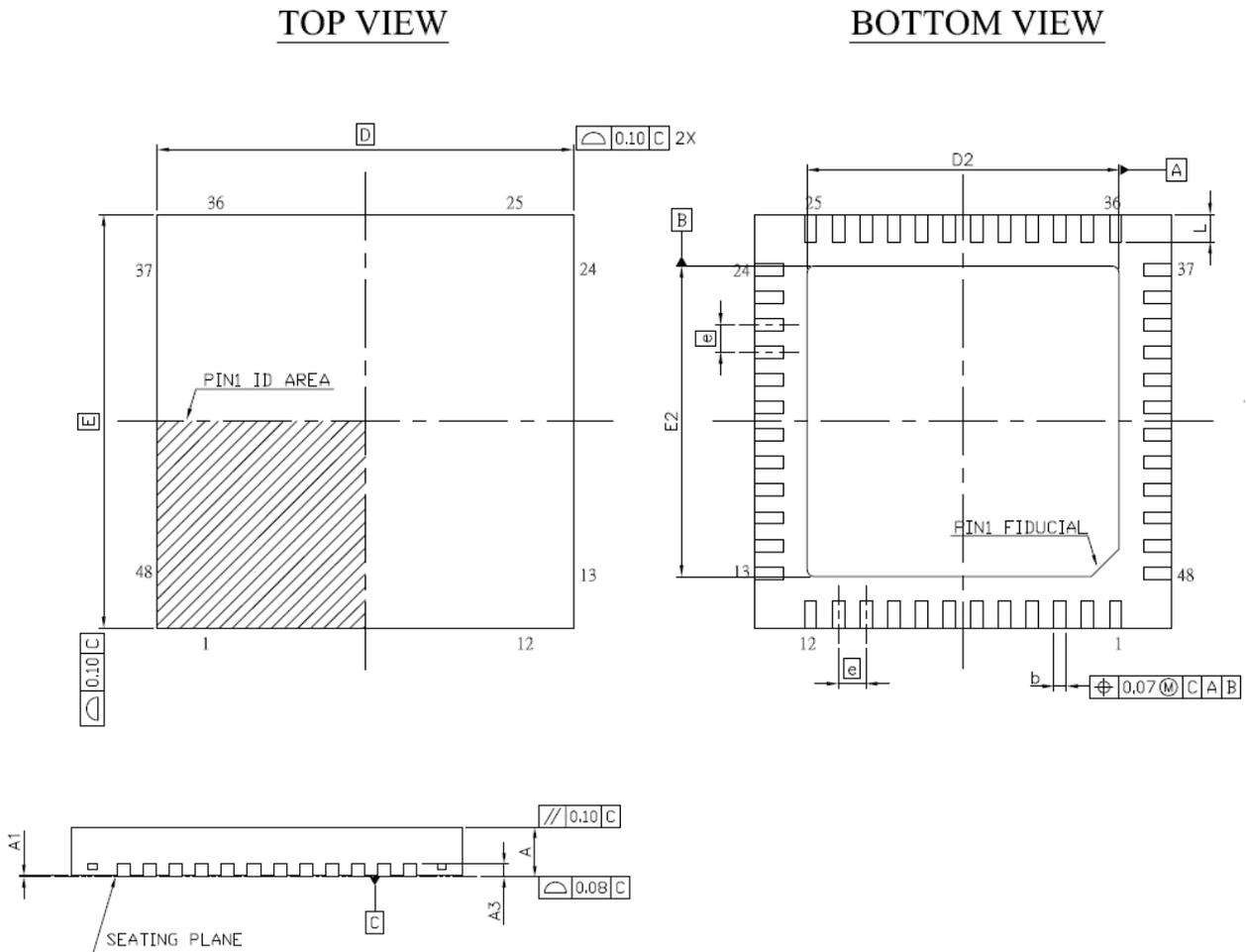
Figure 5-1: The timing of I²C Interface

Table 5-4: Characteristics of the SDA and SCL bus lines

Symbol	Parameter	100KHz			400KHz		
		Min	Max	Unit	Min	Max	Unit
f _{SCL}	SCL clock frequency	0	100	kHz	0	400	kHz
t _{HD;STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	μs	0.6	–	μs
t _{LOW}	LOW period of the SCL clock	4.7	–	μs	1.3	–	μs
t _{HIGH}	HIGH period of the SCL clock	4.0	–	μs	0.6	–	μs
t _{SU;STA}	Set-up time for a repeated START condition	4.7	–	μs	0.6	–	μs
t _{HD;DAT}	Data hold time	5.0	–	μs	0	0.9	μs
t _{SU;DAT}	Data set-up time	250	–	ns	100	–	ns
t _r	Rise time of both SDA and SCL signals	–	1000	ns	–	300	ns
t _f	Fall time of both SDA and SCL signals	–	300	ns	–	300	ns
t _{SU;STO}	Set-up time for STOP condition	4.0	–	μs	0.6	–	μs
t _{BUF}	Bus free time between a STOP and START condition	4.7	–	μs	1.3	–	μs

6 Package Information

6.1 QFN48 6x6x0.8mm



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	28	30	32
A1	0	0.02	0.05	0	0.8	2.0
A3	0.203 REF			8 REF		
b	0.15	0.20	0.25	6	8	10
D	5.90	6.00	6.10	232	236	240
D2	4.40	4.50	4.60	173	177	181
E	5.90	6.00	6.10	232	236	240
E2	4.40	4.50	4.60	173	177	181
e	0.40 BSC			16 REF		
L	0.30	0.40	0.50	12	16	20

Figure 6-1: Package Information of QFN48 6x6x0.8mm

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7 Application Circuit

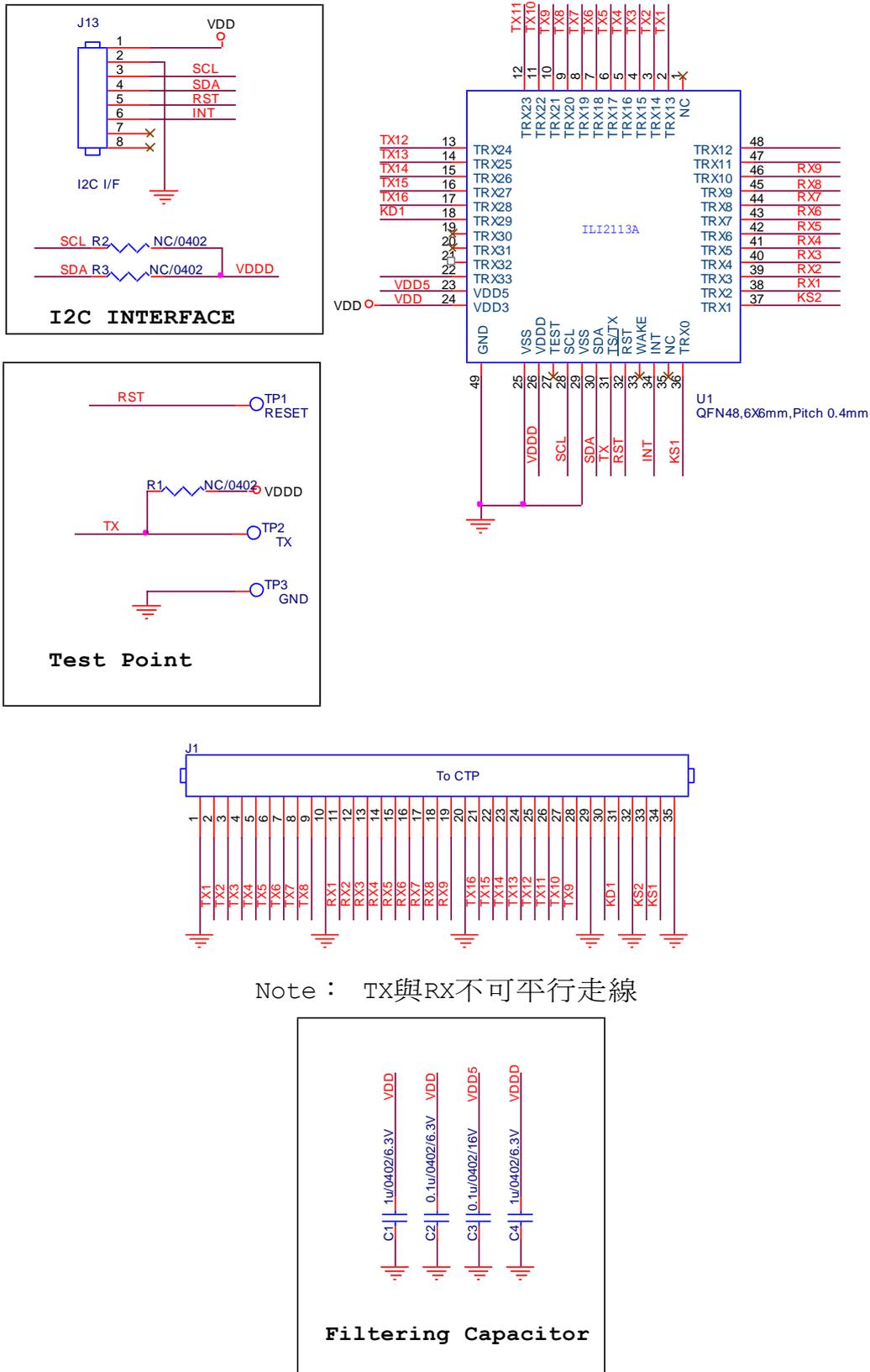


Figure 7-1: ILI2113A reference circuit

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