

## FEATURES

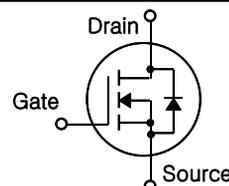
- ❑ Originative New Design
- ❑ 100% EAS Test
- ❑ Rugged Gate Oxide Technology
- ❑ Extremely Low Intrinsic Capacitances
- ❑ Remarkable Switching Characteristics
- ❑ Unequalled Gate Charge : 10 nC (Typ.)
- ❑ Extended Safe Operating Area
- ❑ Lower  $R_{DS(ON)}$  : 2.45  $\Omega$  (Typ.) @ $V_{GS}=10V$
- ❑ Halogen Free

## APPLICATION

- ❑ Low power battery chargers
- ❑ Switch mode power supply (SMPS)
- ❑ DC-AC converters.

## PFP4N70E / PFF4N70E 650V N-Channel MOSFET

**$BV_{DSS} = 700\text{ V}$**   
 **$R_{DS(on)} = 2.45\ \Omega$**   
 **$I_D = 4.0\text{ A}$**



**TO-220**



1.Gate 2. Drain 3. Source

**TO-220F**



1.Gate 2. Drain 3. Source

## Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	PFP4N70E	PFF4N70E	Units
$V_{DSS}$	Drain-Source Voltage	700		V
$I_D$	Drain Current – Continuous ( $T_C = 25^\circ\text{C}$ )	4.0	4.0*	A
	Drain Current – Continuous ( $T_C = 100^\circ\text{C}$ )	2.6	2.6*	A
$I_{DM}$	Drain Current – Pulsed (Note 1)	16.1	16.1*	A
$V_{GS}$	Gate-Source Voltage	$\pm 30$		V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	240		mJ
$I_{AR}$	Avalanche Current (Note 1)	4.0		A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	10.0		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5		V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	100	33	W
		0.80	0.26	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

## Thermal Resistance Characteristics

Symbol	Parameter	PFP4N70E	PFF4N70E	Units
$R_{\theta JC}$	Junction-to-Case	1.25	3.79	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient	62.5	62.5	

\* When mounted on the minimum pad size recommended (PCB Mount)

**Electrical Characteristics**  $T_C=25\text{ }^\circ\text{C}$  unless otherwise specified

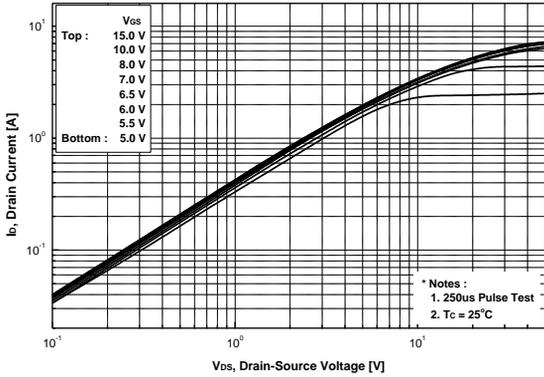
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>On Characteristics</b>						
$V_{GS}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.5	--	4.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 2.0\text{ A}$	--	2.45	2.8	$\Omega$
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	700	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25\text{ }^\circ\text{C}$	--	0.6	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 700\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	$\mu\text{A}$
		$V_{DS} = 560\text{ V}, T_C = 125\text{ }^\circ\text{C}$	--	--	100	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	585	760	pF
$C_{oss}$	Output Capacitance		--	63	82	pF
$C_{rss}$	Reverse Transfer Capacitance		--	4	6	pF
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Time	$V_{DS} = 350\text{ V}, I_D = 4.0\text{ A},$ $R_G = 25\text{ }\Omega$	--	14	28	ns
$t_r$	Turn-On Rise Time		--	7.5	15	ns
$t_{d(off)}$	Turn-Off Delay Time		--	28	56	ns
$t_f$	Turn-Off Fall Time		(Note 4,5)	--	6.5	13
$Q_g$	Total Gate Charge	$V_{DS} = 560\text{ V}, I_D = 4.0\text{ A},$ $V_{GS} = 10\text{ V}$	--	10	15	nC
$Q_{gs}$	Gate-Source Charge		--	3.2	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4,5)	--	3.8	--
<b>Source-Drain Diode Maximum Ratings and Characteristics</b>						
$I_S$	Continuous Source-Drain Diode Forward Current		--	--	4.0	A
$I_{SM}$	Pulsed Source-Drain Diode Forward Current		--	--	16.1	
$V_{SD}$	Source-Drain Diode Forward Voltage	$I_S = 4.0\text{ A}, V_{GS} = 0\text{ V}$	--	--	1.5	V
$t_{rr}$	Reverse Recovery Time	$I_S = 4.0\text{ A}, V_{GS} = 0\text{ V}$ $di_F/dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	290	--	ns
$Q_{RR}$	Reverse Recovery Charge		--	1.8	--	$\mu\text{C}$

**Notes ;**

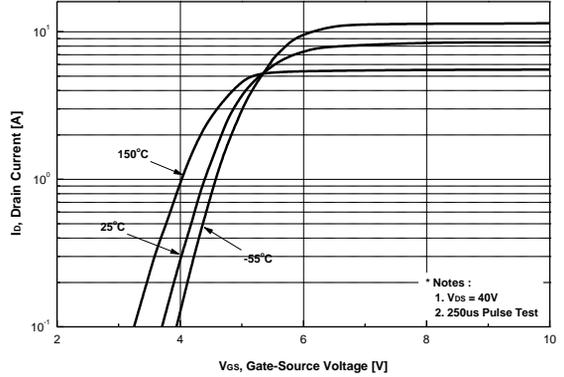
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $I_{AS}=4.0\text{ A}, V_{DD}=50\text{ V}, R_G=25\text{ }\Omega$ , Starting  $T_J=25\text{ }^\circ\text{C}$
3.  $I_{SD}\leq 4.0\text{ A}, di/dt\leq 300\text{ A}/\mu\text{s}, V_{DD}\leq BV_{DSS}$ , Starting  $T_J=25\text{ }^\circ\text{C}$
4. Pulse Test : Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2\%$
5. Essentially Independent of Operating Temperature

# Typical Characteristics

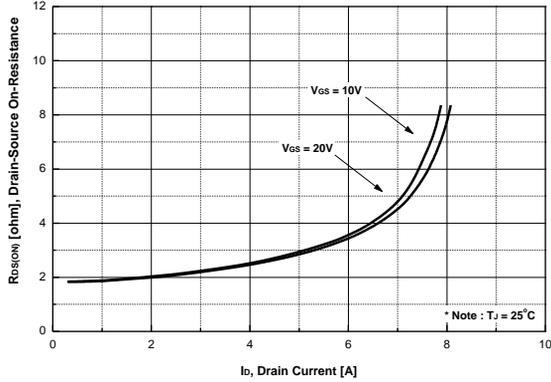
**Fig 1. Output Characteristics**



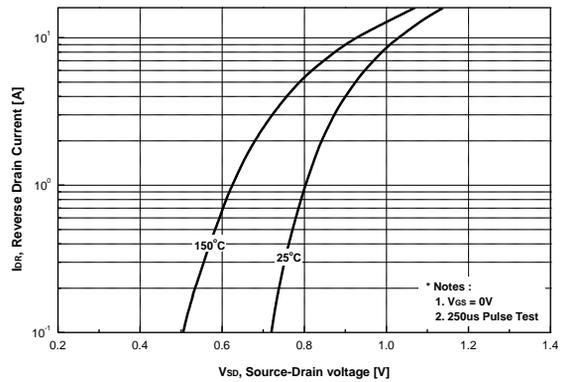
**Fig 2. Transfer Characteristics**



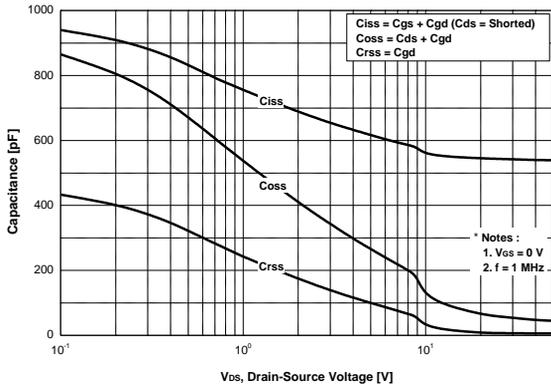
**Fig 3. Static Drain-Source On Resistance**



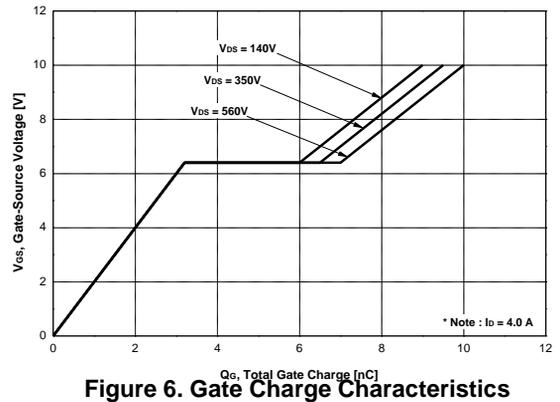
**Fig 4. Source-Drain Diode Forward Voltage**



**Fig 5. Capacitance Characteristics**



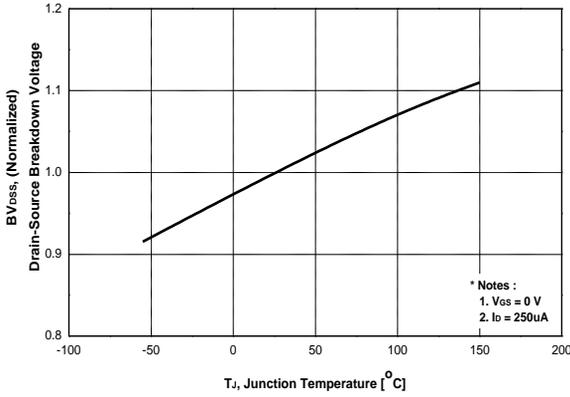
**Fig 6. Gate Charge Characteristics**



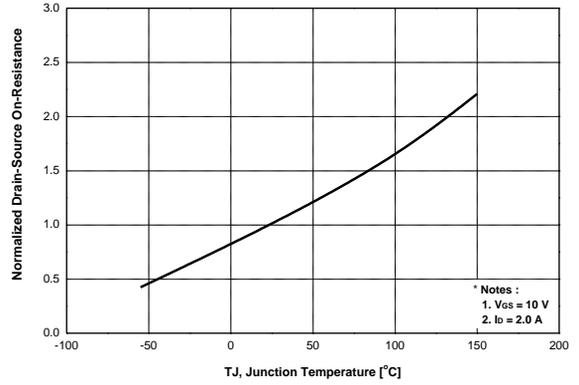
**Figure 6. Gate Charge Characteristics**

# Typical Characteristics

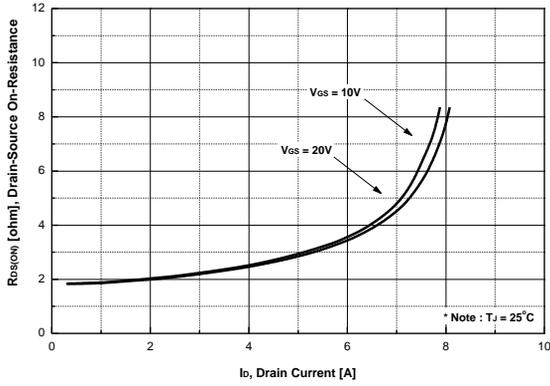
**Fig 7.  $BV_{DSS}$  vs. Junction Temperature**



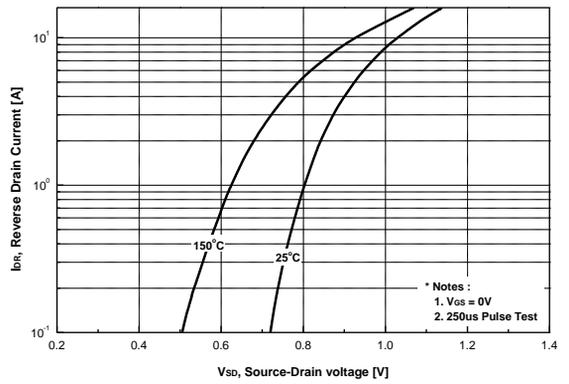
**Fig 8.  $R_{DS(ON)}$  vs. Junction Temperature**



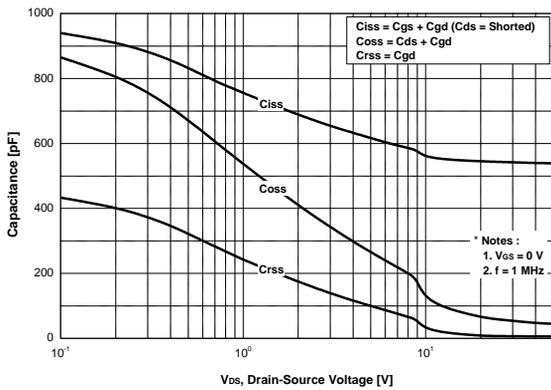
**Fig 3. Static Drain-Source On Resistance**



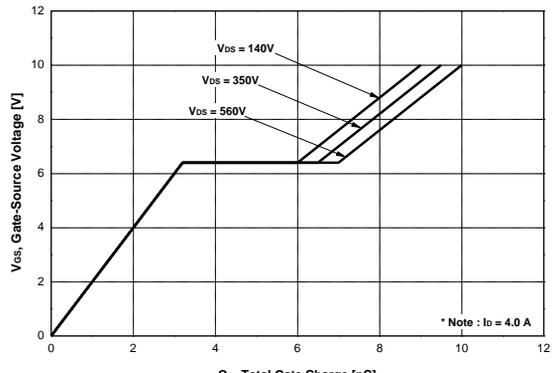
**Fig 4. Source-Drain Diode Forward Voltage**



**Fig 5. Capacitance Characteristics**



**Fig 6. Gate Charge Characteristics**



**Figure 6. Gate Charge Characteristics**

Typical Characteristics (continued)

Figure 7. Breakdown Voltage Variation vs Temperature

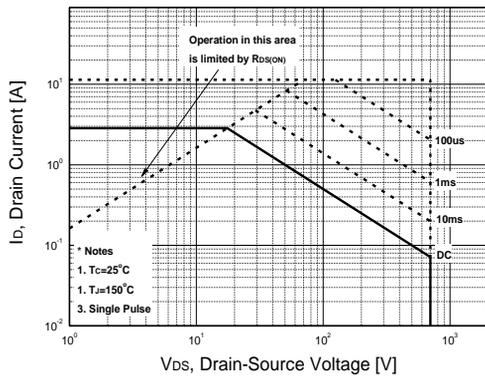


Figure 9. Maximum Safe Operating Area

Figure 8. On-Resistance Variation vs Temperature

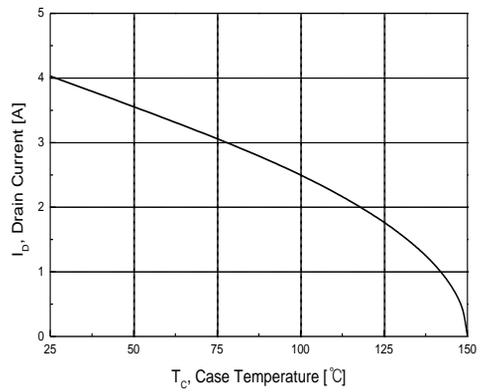


Figure 10. Maximum Drain Current vs Case Temperature

Figure 11. Transient Thermal Response Curve

Characteristics Test Circuit & Waveform

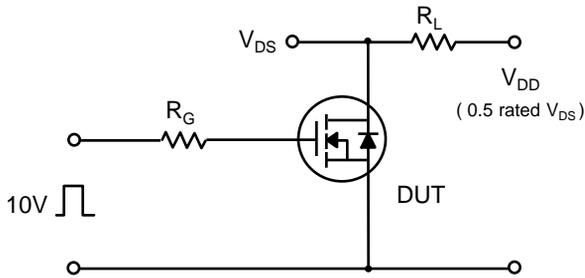


Fig 14. Resistive Switching Test Circuit & Waveforms

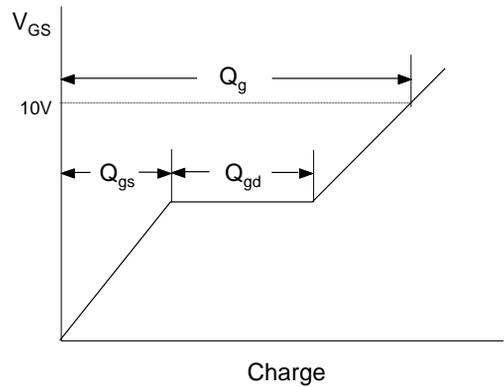
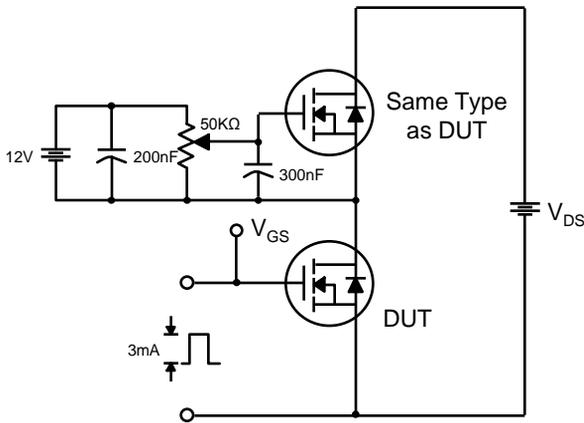


Fig 15. Gate Charge Test Circuit & Waveform

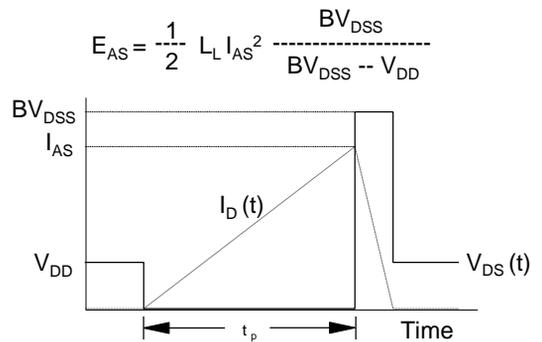
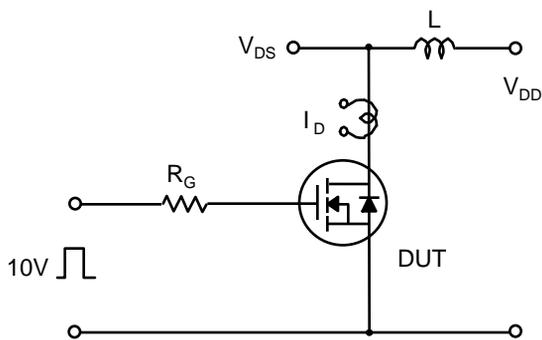


Fig 16. Unclamped Inductive Switching Test Circuit & Waveforms

Characteristics Test Circuit & Waveform (continued)

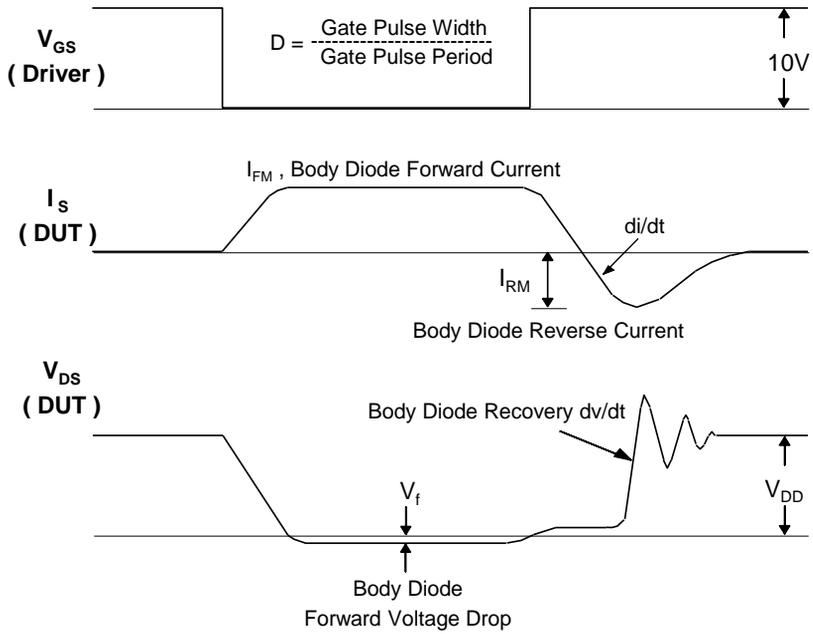
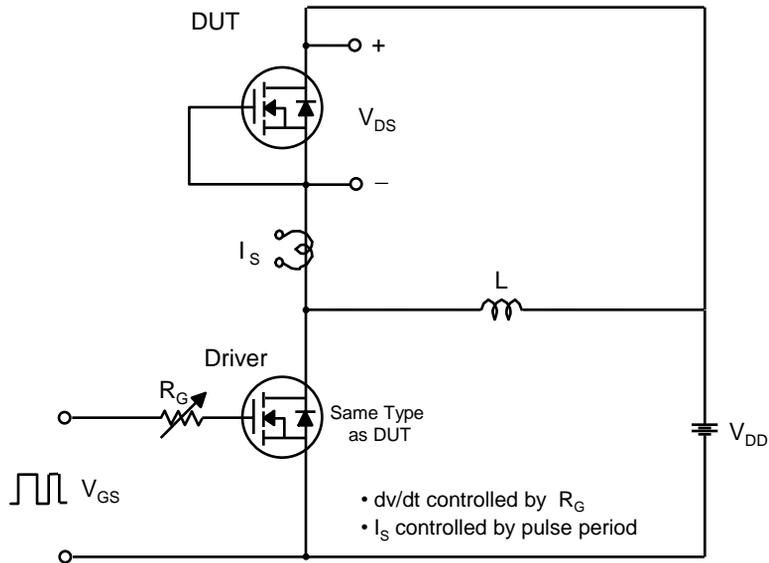
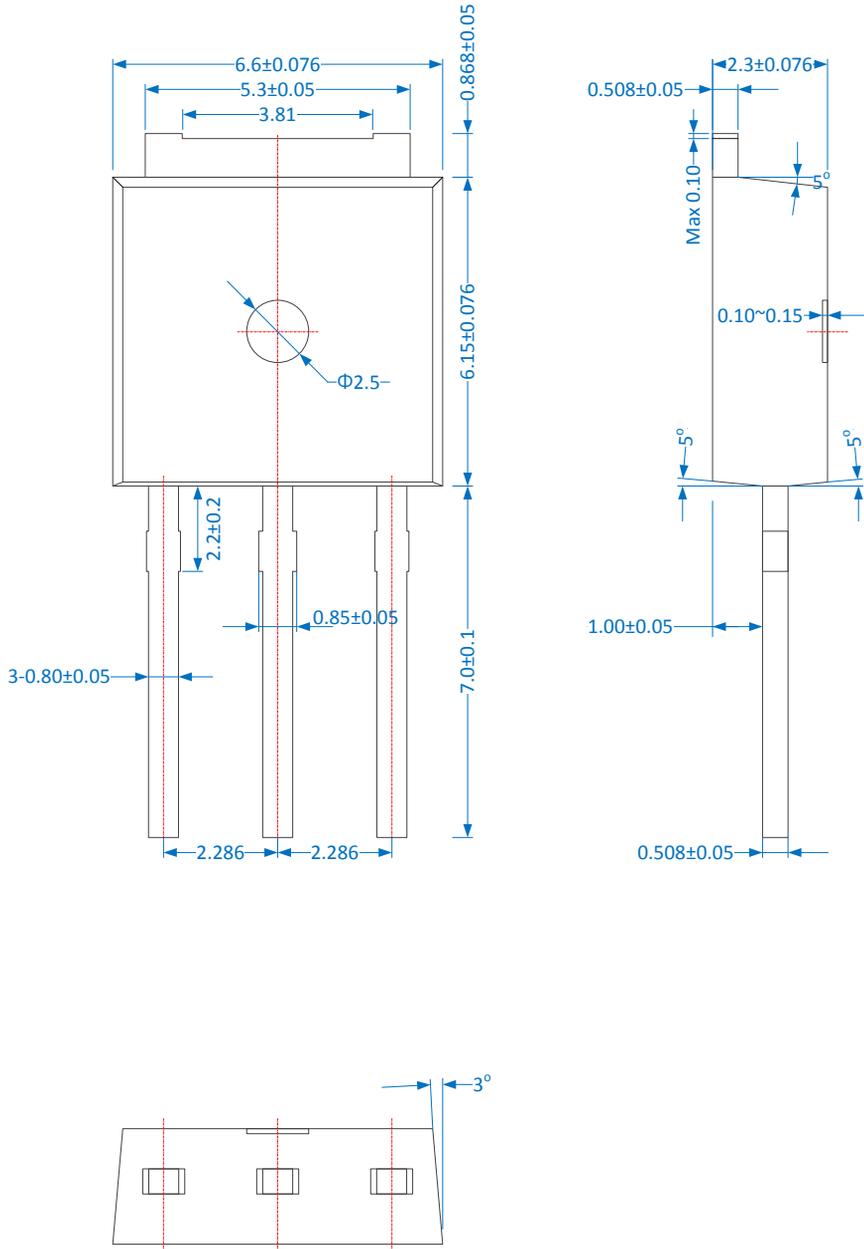


Fig 17. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

Package Dimension

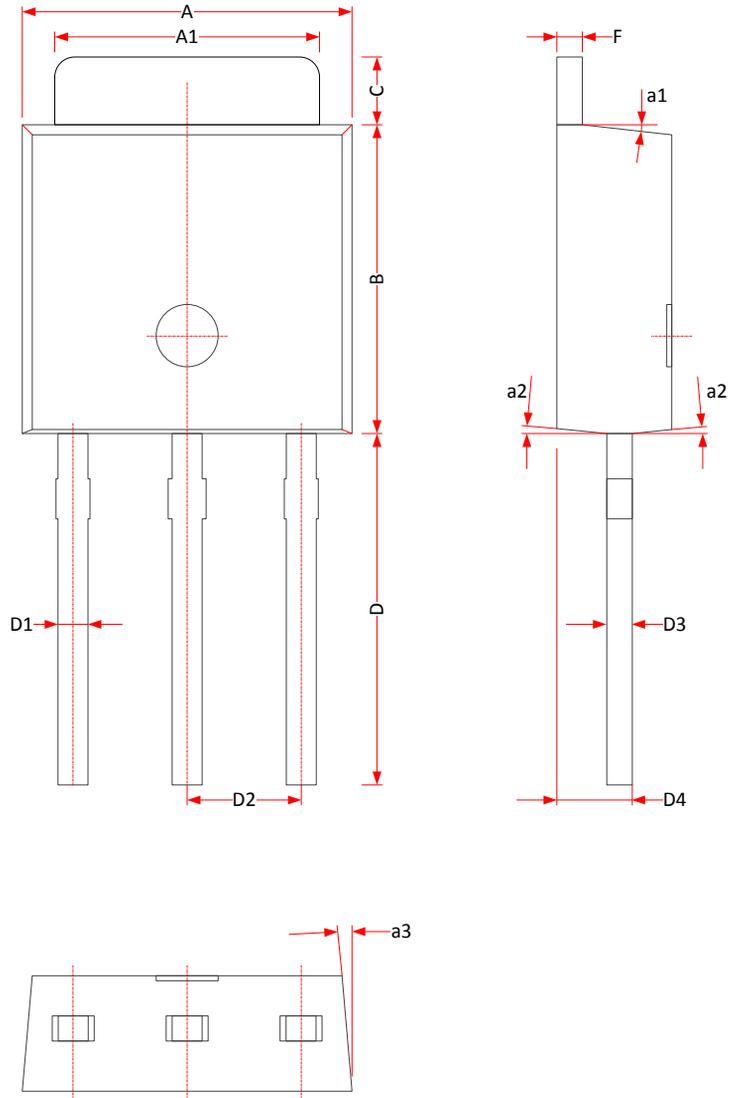
I-PAK(TO-251) (Z)



Package Dimension

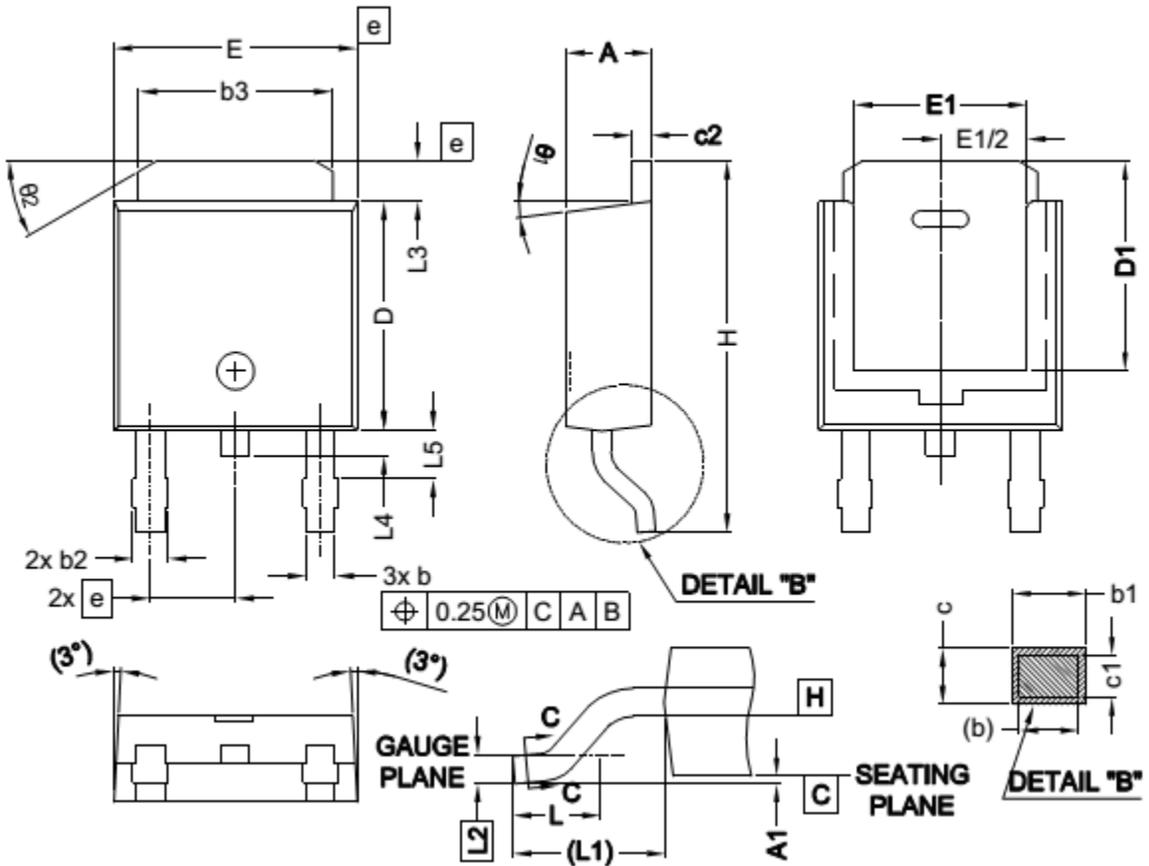
I-PAK(TO-251) (h)

Symbol	Millimeters
A	6.40 ~ 6.60
A1	5.30 ~ 5.50
B	5.40 ~ 5.70
C	1.35 ~ 1.65
D	7.40 ~ 8.00
D1	0.60 ~ 0.75
D2	2.30
D3	0.49 ~ 0.59
D4	1.72 ~ 1.82
E	2.20 ~ 2.40
F	0.55 ~ 0.65
a1	5 deg
a2	5 deg
a3	2 deg



Package Dimension

D-PAK(TO-252) (a)



SYMBOL	MIN.	MAX.	SYMBOL	MIN.	MAX.	SYMBOL	MIN.	MAX.
A	2.18	2.39	E	6.35	6.73	$\phi 1$	0°	15°
A1	-	0.13	E1	4.32	-	$\phi 2$	25°	35°
b	0.640	0.884	e	2.29 BSC				
b1	0.65	0.79	H	9.94	10.34			
b2	0.760	1.124	L	1.50	1.78			
b3	4.95	5.46	L1	2.74 REF				
c	0.46	0.61	L2	0.51 BSC				
c1	0.41	0.56	L3	0.89	1.27			
c2	0.40	0.60	L4	-	1.02			
D	5.97	6.22	L5	1.140	1.492			
D1	5.21	-	$\phi$	0°	10°			

Package Dimension

D-PAK(TO-252) (Z)

