



PFP10N40 / PFF10N40

400V N-Channel MOSFET

FEATURES

- ❑ Originative New Design
- ❑ 100% EAS Test
- ❑ Rugged Gate Oxide Technology
- ❑ Extremely Low Intrinsic Capacitances
- ❑ Remarkable Switching Characteristics
- ❑ Unequalled Gate Charge : 23 nC (Typ.)
- ❑ Extended Safe Operating Area
- ❑ Lower $R_{DS(ON)}$: 0.44 Ω (Typ.) @ $V_{GS}=10V$

APPLICATION

- ❑ Electronic lamp ballasts based on half bridge topology
- ❑ PFC (Power Factor Correction)
- ❑ SMPS (Switched Mode Power Supplies)

<p>$BV_{DSS} = 400\text{ V}$</p> <p>$R_{DS(on)} = 0.55\ \Omega$</p> <p>$I_D = 10\text{ A}$</p>	
<p>TO-220</p> <p>1.Gate 2. Drain 3. Source</p>	<p>TO-220F</p> <p>1.Gate 2. Drain 3. Source</p>

Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	PFP10N40	PFF10N40	Units
V_{DSS}	Drain-Source Voltage	400		V
I_D	Drain Current – Continuous ($T_C = 25^\circ\text{C}$)	10	10*	A
	Drain Current – Continuous ($T_C = 100^\circ\text{C}$)	6.3	6.3*	A
I_{DM}	Drain Current – Pulsed (Note 1)	40	40*	A
V_{GS}	Gate-Source Voltage	± 30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	450		mJ
I_{AR}	Avalanche Current (Note 1)	10.0		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	13.4		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5		V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	134	44	W
	– Derate above 25°C	1.08	0.35	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

* Drain current limited by maximum junction temperature

Thermal Resistance Characteristics

Symbol	Parameter	PFP10N40	PFF10N40	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.93	2.86	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink	0.5	--	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	

Electrical Characteristics $T_C=25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
V_{GS}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	--	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\ \text{V}, I_D = 5.0\ \text{A}$	--	0.44	0.55	Ω
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\ \text{V}, I_D = 250\ \mu\text{A}$	400	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to $25\text{ }^\circ\text{C}$	--	0.5	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 400\ \text{V}, V_{GS} = 0\ \text{V}$	--	--	1	μA
		$V_{DS} = 320\ \text{V}, T_C = 125\text{ }^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\ \text{V}, V_{DS} = 0\ \text{V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\ \text{V}, V_{DS} = 0\ \text{V}$	--	--	-100	nA
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25\ \text{V}, V_{GS} = 0\ \text{V},$ $f = 1.0\ \text{MHz}$	--	815	1060	pF
C_{oss}	Output Capacitance		--	133	175	pF
C_{rss}	Reverse Transfer Capacitance		--	18	23	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	$V_{DS} = 200\ \text{V}, I_D = 10\ \text{A},$ $R_G = 25\ \Omega$ (Note 4,5)	--	15	30	ns
t_r	Turn-On Rise Time		--	22	50	ns
$t_{d(off)}$	Turn-Off Delay Time		--	55	110	ns
t_f	Turn-Off Fall Time		--	22	50	ns
Q_g	Total Gate Charge	$V_{DS} = 320\ \text{V}, I_D = 10\ \text{A},$ $V_{GS} = 10\ \text{V}$ (Note 4,5)	--	23	30	nC
Q_{gs}	Gate-Source Charge		--	3.5	--	nC
Q_{gd}	Gate-Drain Charge		--	9.0	--	nC
Source-Drain Diode Maximum Ratings and Characteristics						
I_S	Continuous Source-Drain Diode Forward Current		--	--	10	A
I_{SM}	Pulsed Source-Drain Diode Forward Current		--	--	40	
V_{SD}	Source-Drain Diode Forward Voltage	$I_S = 10.0\ \text{A}, V_{GS} = 0\ \text{V}$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$I_S = 10.0\ \text{A}, V_{GS} = 0\ \text{V}$ $di_f/dt = 100\ \text{A}/\mu\text{s}$ (Note 4)	--	250	--	ns
Q_{rr}	Reverse Recovery Charge		--	2.3	--	μC

Notes ;

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $I_{AS}=10\text{A}, V_{DD}=50\text{V}, R_G=25\Omega$, Starting $T_J=25\text{ }^\circ\text{C}$
3. $I_{SD}\leq 10\text{A}, di/dt\leq 300\text{A}/\mu\text{s}, V_{DD}\leq BV_{DSS}$, Starting $T_J=25\text{ }^\circ\text{C}$
4. Pulse Test : Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
5. Essentially Independent of Operating Temperature

Typical Characteristics

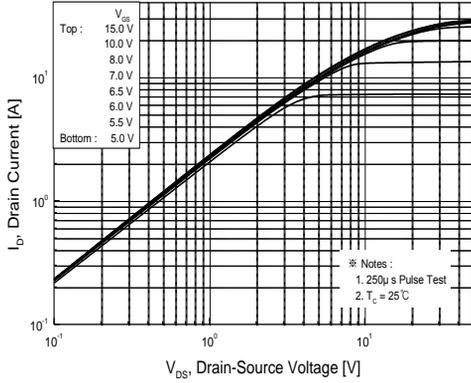


Figure 1. On Region Characteristics

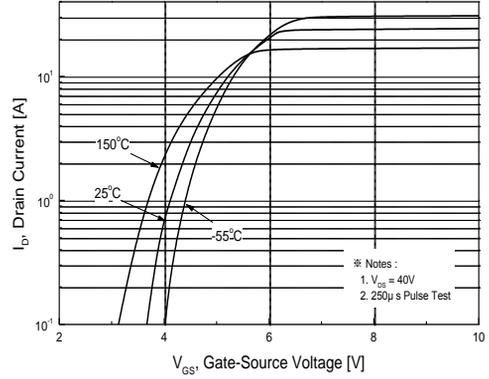


Figure 2. Transfer Characteristics

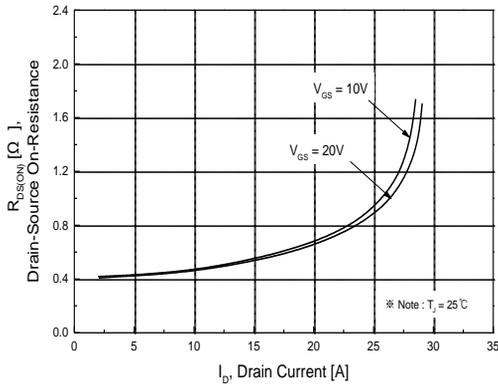


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

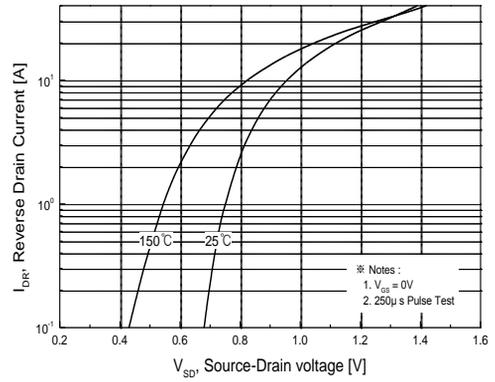


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

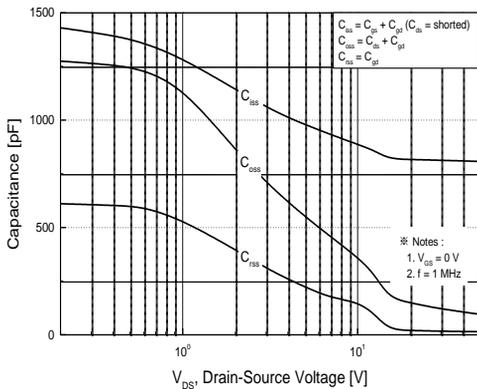


Figure 5. Capacitance Characteristics

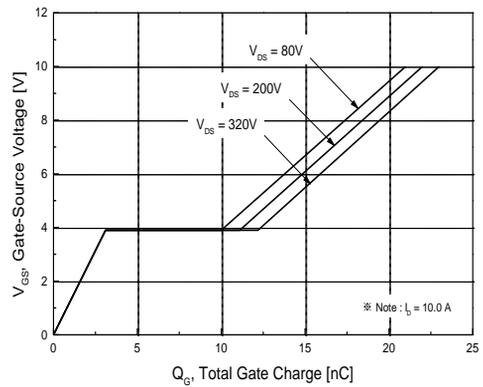


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

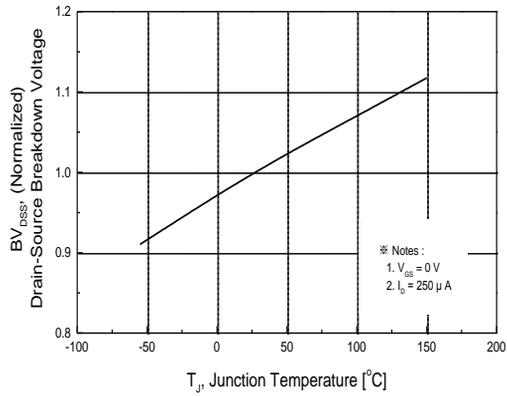


Figure 7. Breakdown Voltage Variation vs Temperature

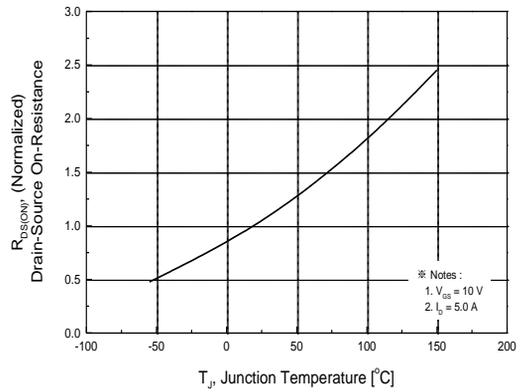


Figure 8. On-Resistance Variation vs Temperature

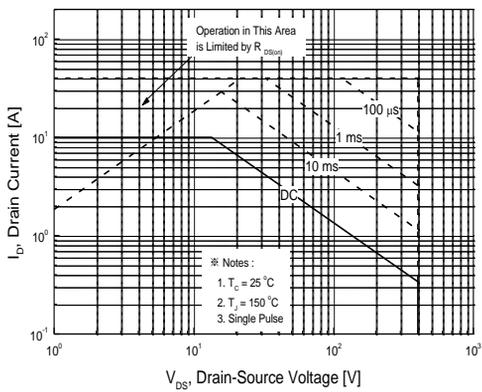


Figure 9. Maximum Safe Operating Area for PFP10N40

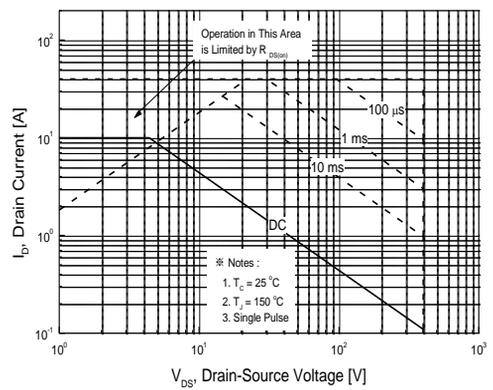


Figure 10. Maximum Safe Operating Area for PFF10N40

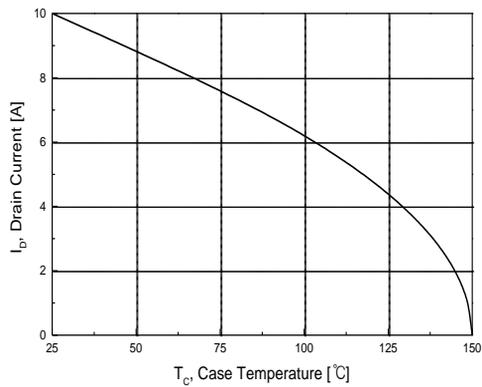


Figure 11. Maximum Drain Current vs Case Temperature

Typical Characteristics (continued)

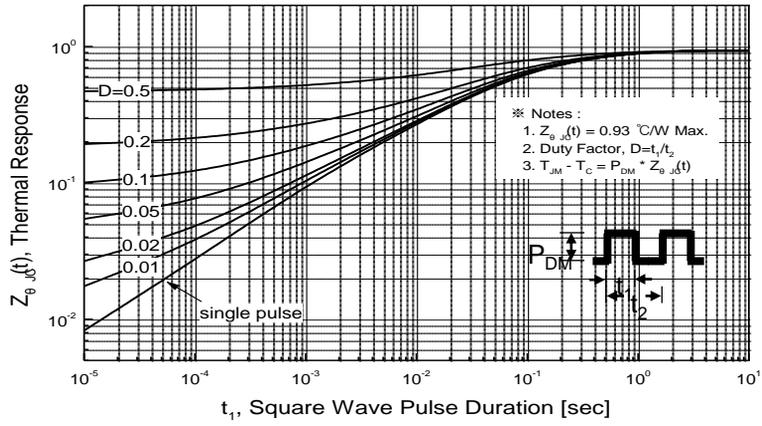


Figure 12. Transient Thermal Response Curve for PFP10N40

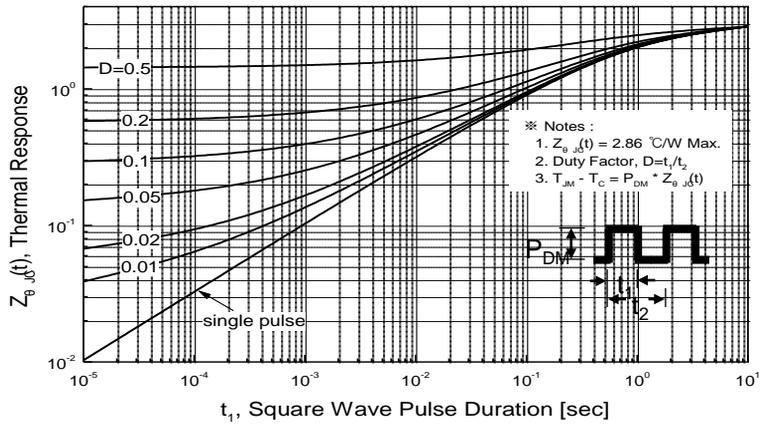


Figure 13. Transient Thermal Response Curve for PFF10N40

Characteristics Test Circuit & Waveform

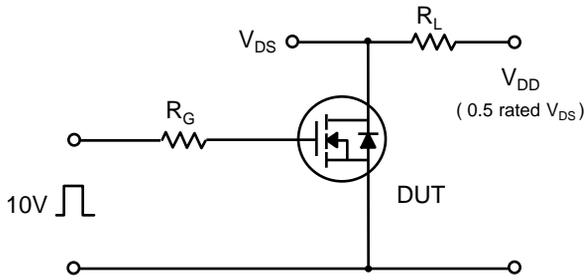


Fig 14. Resistive Switching Test Circuit & Waveforms

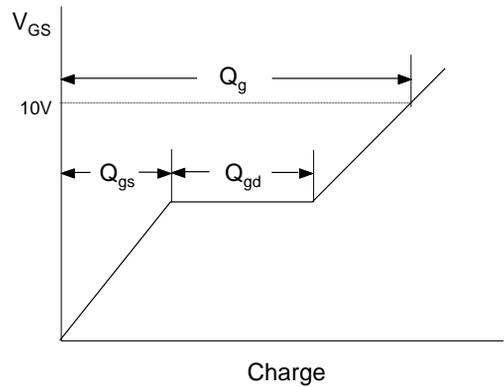
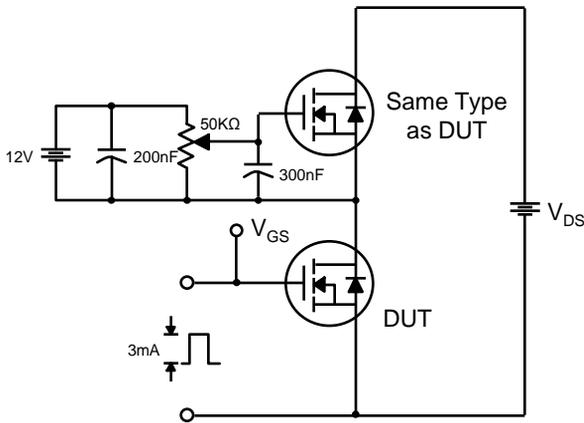


Fig 15. Gate Charge Test Circuit & Waveform

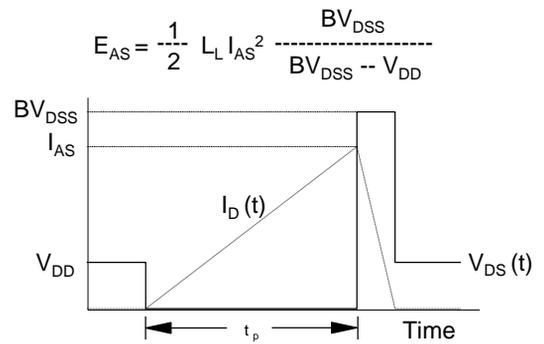
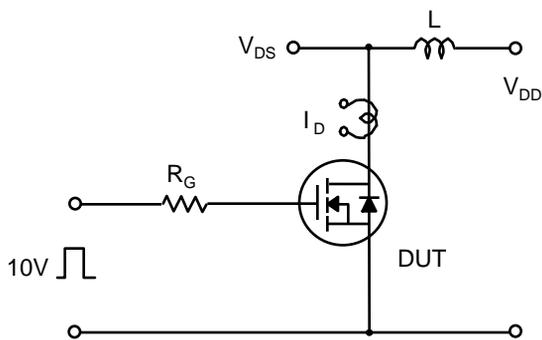


Fig 16. Unclamped Inductive Switching Test Circuit & Waveforms

Characteristics Test Circuit & Waveform (continued)

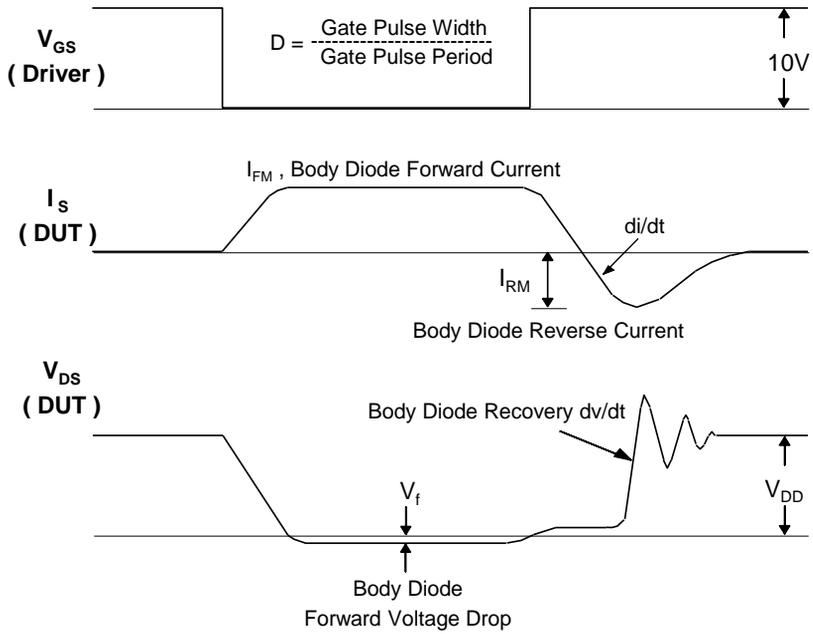
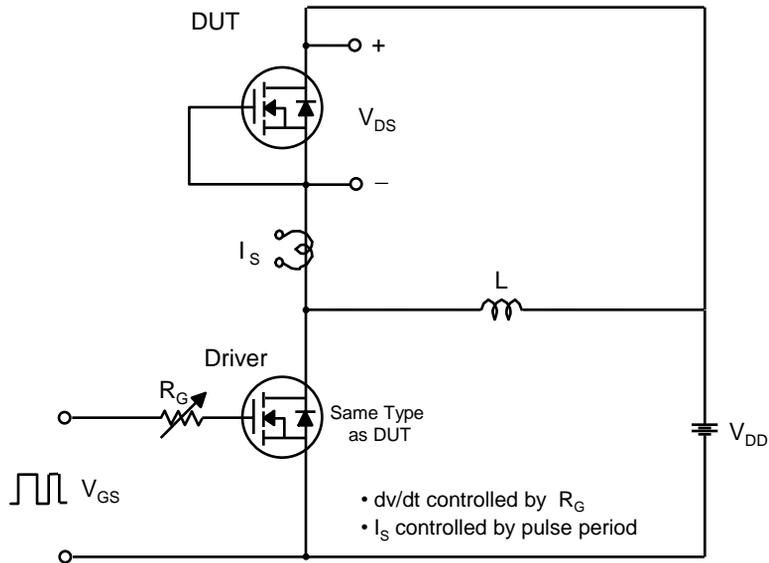
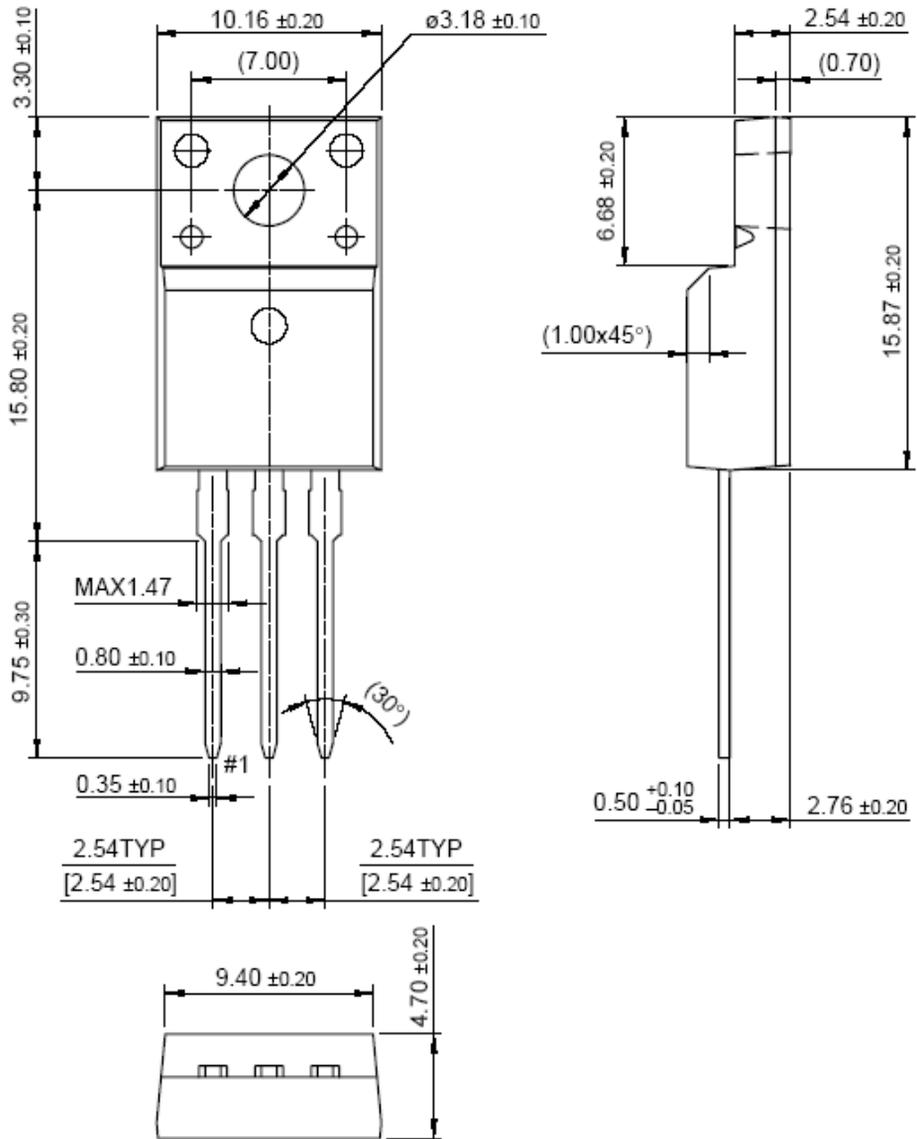


Fig 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Package Dimension

TO-220F



Reliability Qualification

A. High Temperature Reverse Bias (HTRB)

The purpose of this test is to determine the sensitivity of the product to mobile ion contamination and related failure mechanisms.

Conditions: MIL-STD-750C 1038, JIS C 7021 B-3

$T_A=150\text{ }^{\circ}\text{C}$ $V_{DS}=80\%$ max rated V_{DS}

Sample Size	#of Fail	Cum. Fail%	168hrs	300hrs
45	0	0.0%	0	0

B. High Temperature Gate Bias (HTGB)

The purpose of this test is to determine the sensitivity of the product to mobile ion contamination between gate and source and related failure mechanisms.

Conditions: MIL-STD-750C 1038, JIS C 7021 B-3

$T_A=150\text{ }^{\circ}\text{C}$ $V_{DS}=V_{GSS}$ max

Sample Size	#of Fail	Cum. Fail%	168hrs	300hrs
45	0	0.0%	0	0

C. Temperature Humidity Bias (THB)

The purpose of this test is to evaluate the moisture resistance of non-hermetic components.

The addition of voltage bias accelerates the corrosive effect after moisture penetration has taken place. with time, this is a catastrophically destructive test.

Conditions: JESD22-A101, JIS C 7021 B-11

$T_A=85\text{ }^{\circ}\text{C}$ $\text{RH}=85\%$ $V_{DS}=80\%$ max rated V_{DS}

Sample Size	#of Fail	Cum. Fail%	168hrs	300hrs
45	0	0.0%	0	0

Reliability Qualification (Continued)

D. High Temperature Storage (HTS)

The purpose of this test is to expose time/temperature failure mechanisms and to evaluate long-term strong stability.

Conditions: MIL-STD-750C 1031.4, JIS C 7021 B-10

$T_A = T_{stg}(\max) 150\text{ }^\circ\text{C}$

Sample Size	#of Fail	Cum. Fail%	168hrs	300hrs
45	0	0.0%	0	0

E. Pressure Cooker Test (PCT)

Autoclave (ACLV)

The purpose of this test is to evaluate the moisture resistance of non-hermetic components under pressure/temperature conditions.

Conditions: MIL-STD-750C 1071.2, JIS C 7021 A-6

$T_A = 121\text{ }^\circ\text{C} \pm 2\text{ }^\circ\text{C}$ RH=100% P=1 atmosphere (15psig)

Sample Size	#of Fail	Cum. Fail%	48hrs
22	0	0.0%	0

F. Temperature Cycle Air-to Air (T/C)

The purpose of this test is to evaluate the ability of the device to withstand both exposure to extreme temperature and the transition between temperature extreme, and to exposure excessive thermal mismatch between materials.

Conditions: JESD22-A104, JIS C 7021 A-4

Air to air, $-65\text{ }^\circ\text{C} \sim 150\text{ }^\circ\text{C}$, 10 minutes dwell time at each temperature

Sample Size	#of Fail	Cum. Fail%	100cycles	200cycles
22	0	0.0%	0	0