



PFP8N50/PFF8N50

500V N-Channel MOSFET

FEATURES

- ❑ Originative New Design
- ❑ 100% EAS Test
- ❑ Rugged Gate Oxide Technology
- ❑ Extremely Low Intrinsic Capacitances
- ❑ Remarkable Switching Characteristics
- ❑ Unequalled Gate Charge : 25 nC (Typ.)
- ❑ Extended Safe Operating Area
- ❑ Lower $R_{DS(ON)}$: 0.7 Ω (Typ.) @ $V_{GS}=10V$

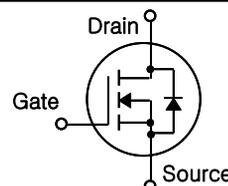
APPLICATION

- ❑ Electronic lamp ballasts based on half bridge topology
- ❑ PFC (Power Factor Correction)
- ❑ SMPS (Switched Mode Power Supplies)

$$BV_{DSS} = 500 \text{ V}$$

$$R_{DS(on)} = 0.85 \Omega$$

$$I_D = 8.0 \text{ A}$$

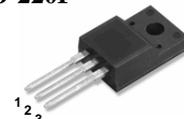


TO-220



1.Gate 2. Drain 3. Source

TO-220F



1.Gate 2. Drain 3. Source

Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	PFP8N50	PFF8N50	Units
V_{DSS}	Drain-Source Voltage	500		V
I_D	Drain Current – Continuous ($T_C = 25^\circ\text{C}$)	8.0	8.0*	A
	Drain Current – Continuous ($T_C = 100^\circ\text{C}$)	5.1	5.1*	A
I_{DM}	Drain Current – Pulsed (Note 1)	32	32*	A
V_{GS}	Gate-Source Voltage	± 30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	320		mJ
I_{AR}	Avalanche Current (Note 1)	8.0		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	13.4		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5		V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) – Derate above 25°C	134	44	W
		1.08	0.35	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

* Drain current limited by maximum junction temperature

Thermal Resistance Characteristics

Symbol	Parameter	PFP8N50	PFF8N50	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.93	2.86	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink	0.5	--	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	

Electrical Characteristics $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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On Characteristics

V_{GS}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2.0	--	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 4.0 \text{ A}$	--	0.7	0.85	Ω

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	500	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	--	0.5	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500 \text{ V}, V_{GS} = 0 \text{ V}$	--	--	1	μA
		$V_{DS} = 400 \text{ V}, T_C = 125^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30 \text{ V}, V_{DS} = 0 \text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30 \text{ V}, V_{DS} = 0 \text{ V}$	--	--	-100	nA

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1.0 \text{ MHz}$	--	850	1110	pF
C_{oss}	Output Capacitance		--	150	195	pF
C_{rss}	Reverse Transfer Capacitance		--	20	26	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Time	$V_{DS} = 250 \text{ V}, I_D = 8.0 \text{ A},$ $R_G = 25 \Omega$	--	15	30	ns	
t_r	Turn-On Rise Time		--	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4,5)	--	60	120	ns
t_f	Turn-Off Fall Time			--	25	50	ns
Q_g	Total Gate Charge	$V_{DS} = 400\text{V}, I_D = 8.0 \text{ A},$ $V_{GS} = 10 \text{ V}$	--	25	33	nC	
Q_{gs}	Gate-Source Charge		(Note 4,5)	--	4	--	nC
Q_{gd}	Gate-Drain Charge			--	10	--	nC

Source-Drain Diode Maximum Ratings and Characteristics

I_S	Continuous Source-Drain Diode Forward Current	--	--	8.0	A	
I_{SM}	Pulsed Source-Drain Diode Forward Current	--	--	32		
V_{SD}	Source-Drain Diode Forward Voltage	$I_S = 8.0 \text{ A}, V_{GS} = 0 \text{ V}$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$I_S = 8.0 \text{ A}, V_{GS} = 0 \text{ V}$ $di_f/dt = 100 \text{ A}/\mu\text{s}$ (Note 4)	--	310	--	ns
Q_{rr}	Reverse Recovery Charge		--	2.3	--	μC

Notes ;

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $I_{AS}=8.0\text{A}, V_{DD}=50\text{V}, R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
3. $I_{SD}\leq 8.0\text{A}, di/dt\leq 300\text{A}/\mu\text{s}, V_{DD}\leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$
4. Pulse Test : Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
5. Essentially Independent of Operating Temperature

Typical Characteristics

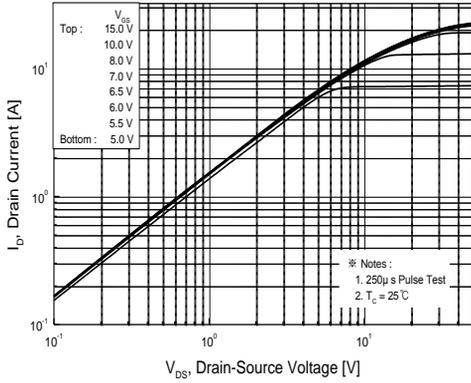


Figure 1. On Region Characteristics

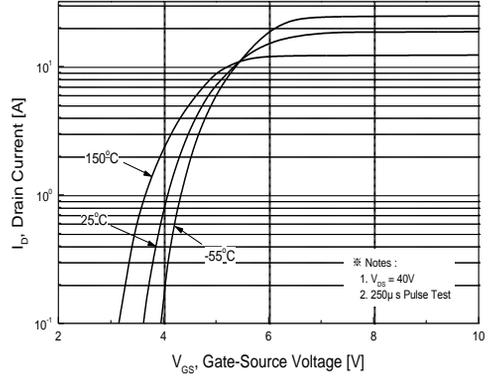


Figure 2. Transfer Characteristics

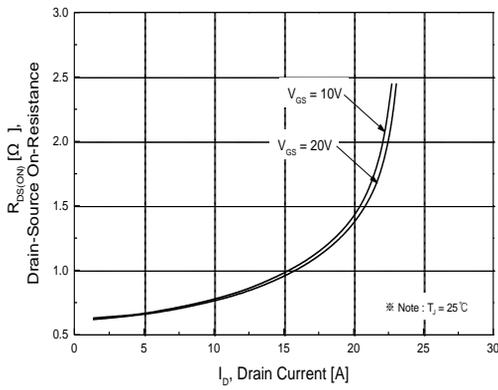


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

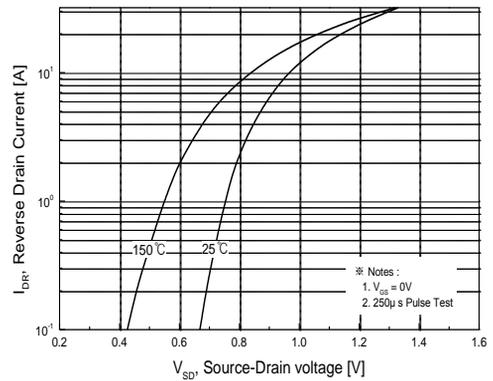


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

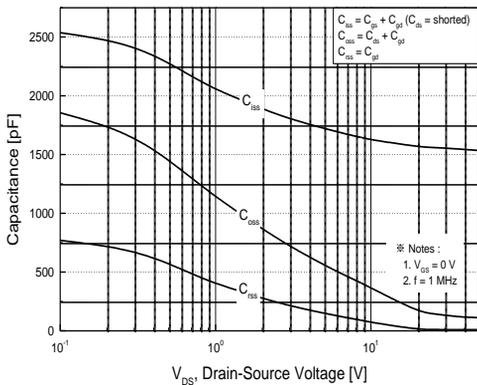


Figure 5. Capacitance Characteristics

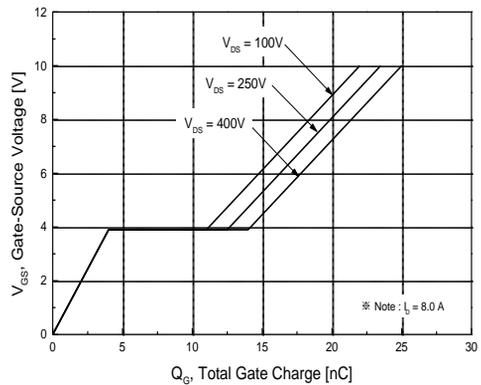


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

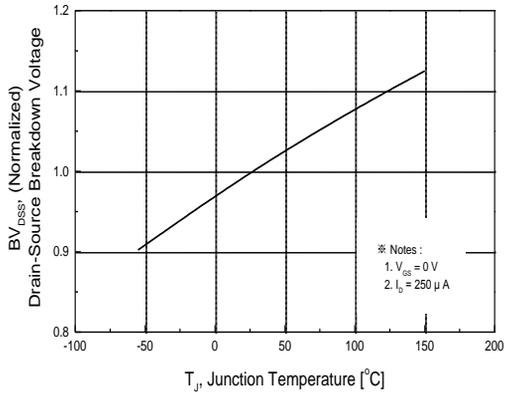


Figure 7. Breakdown Voltage Variation vs Temperature

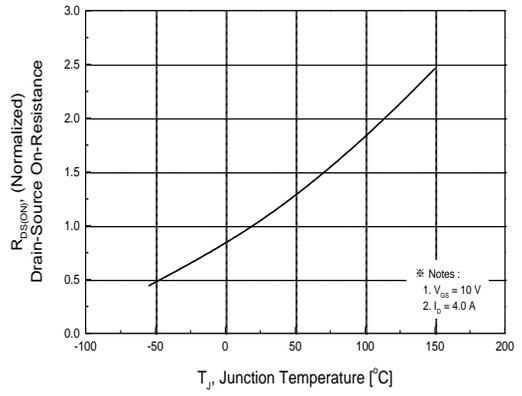


Figure 8. On-Resistance Variation vs Temperature

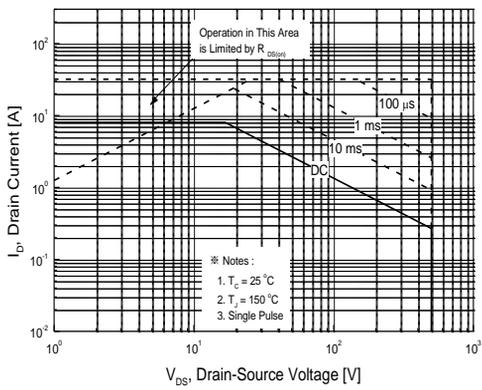


Figure 9. Maximum Safe Operating Area for PFP8N50

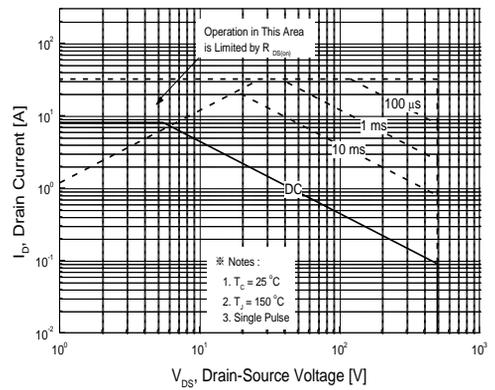


Figure 10. Maximum Safe Operating Area for PFF8N50

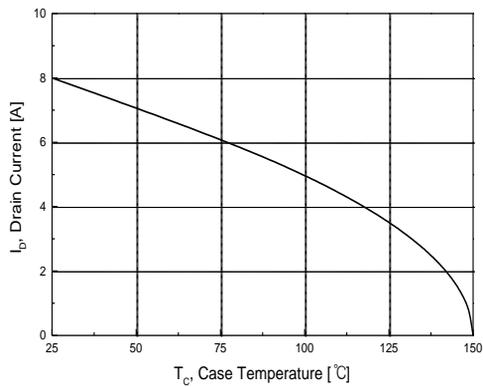


Figure 11. Maximum Drain Current vs Case Temperature

Typical Characteristics (continued)

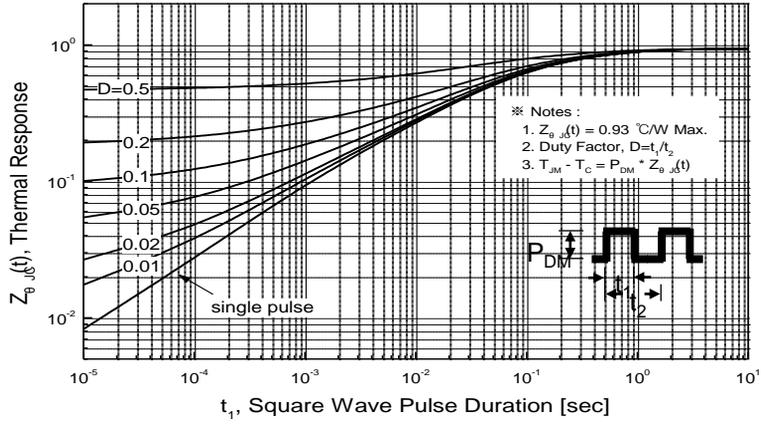


Figure 12. Transient Thermal Response Curve for PFP8N50

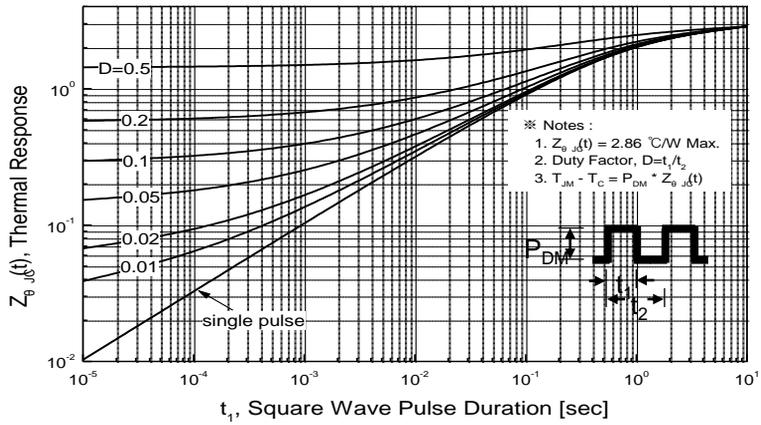


Figure 13. Transient Thermal Response Curve for PFF8N50

Characteristics Test Circuit & Waveform

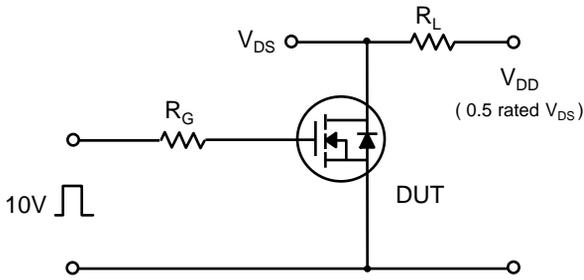


Fig 14. Resistive Switching Test Circuit & Waveforms

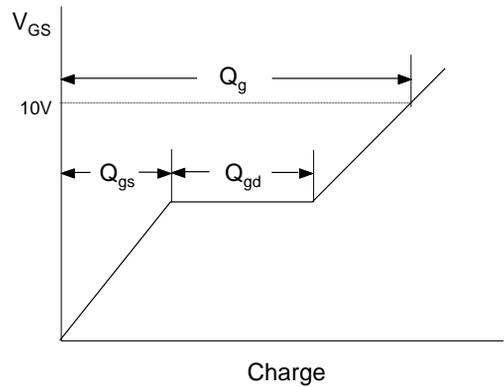
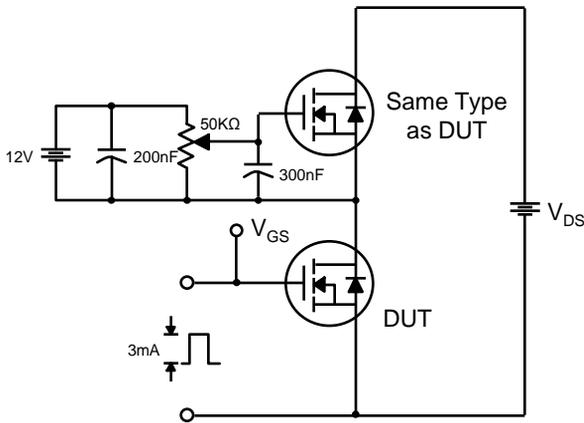


Fig 15. Gate Charge Test Circuit & Waveform

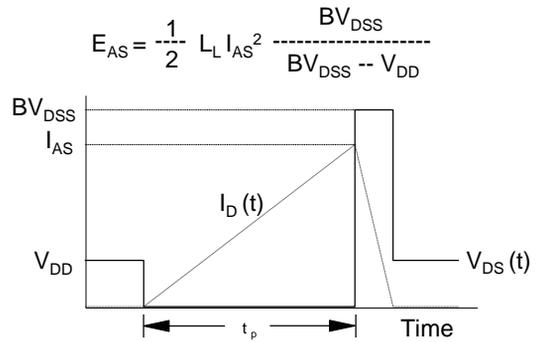
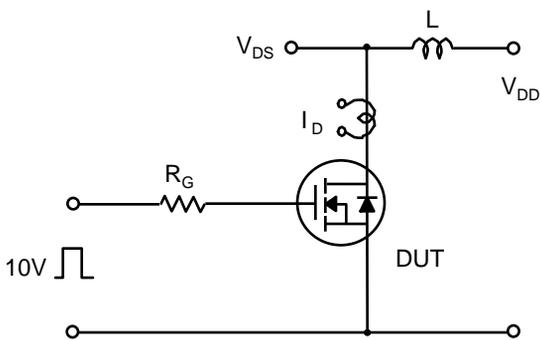


Fig 16. Unclamped Inductive Switching Test Circuit & Waveforms

Characteristics Test Circuit & Waveform (continued)

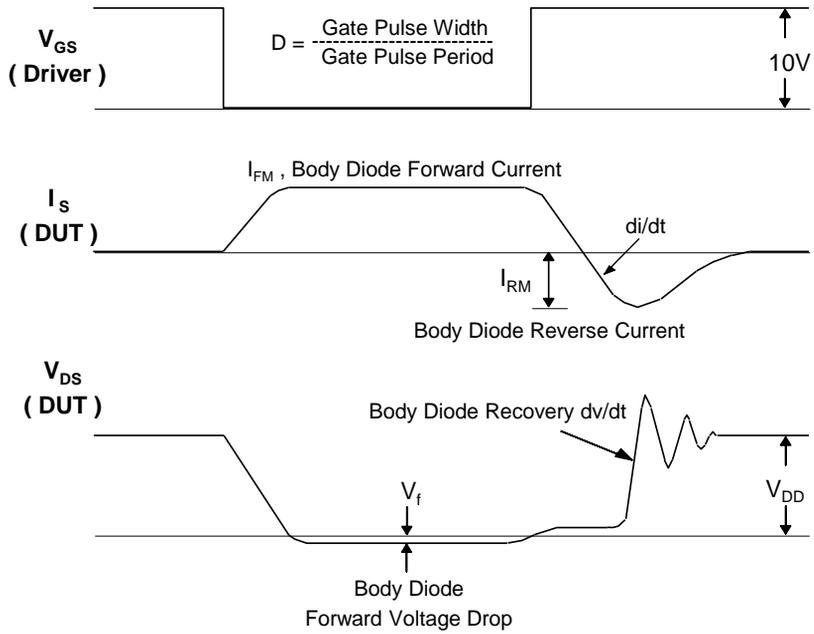
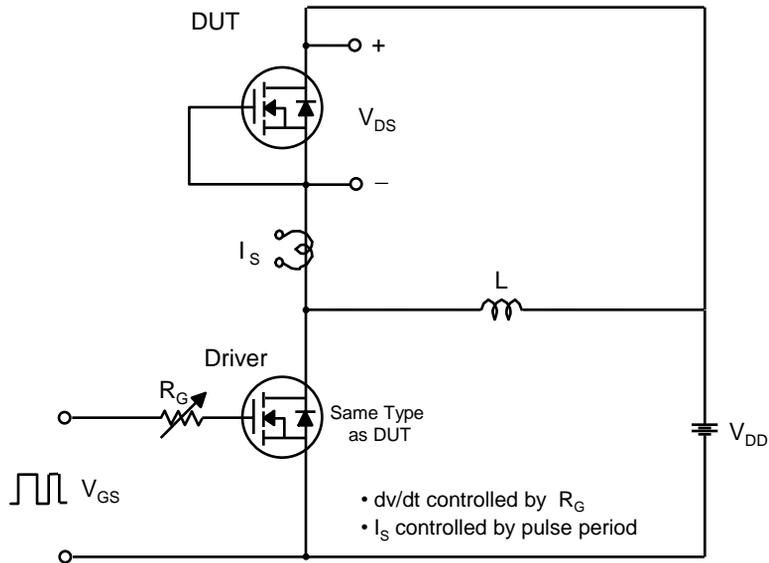
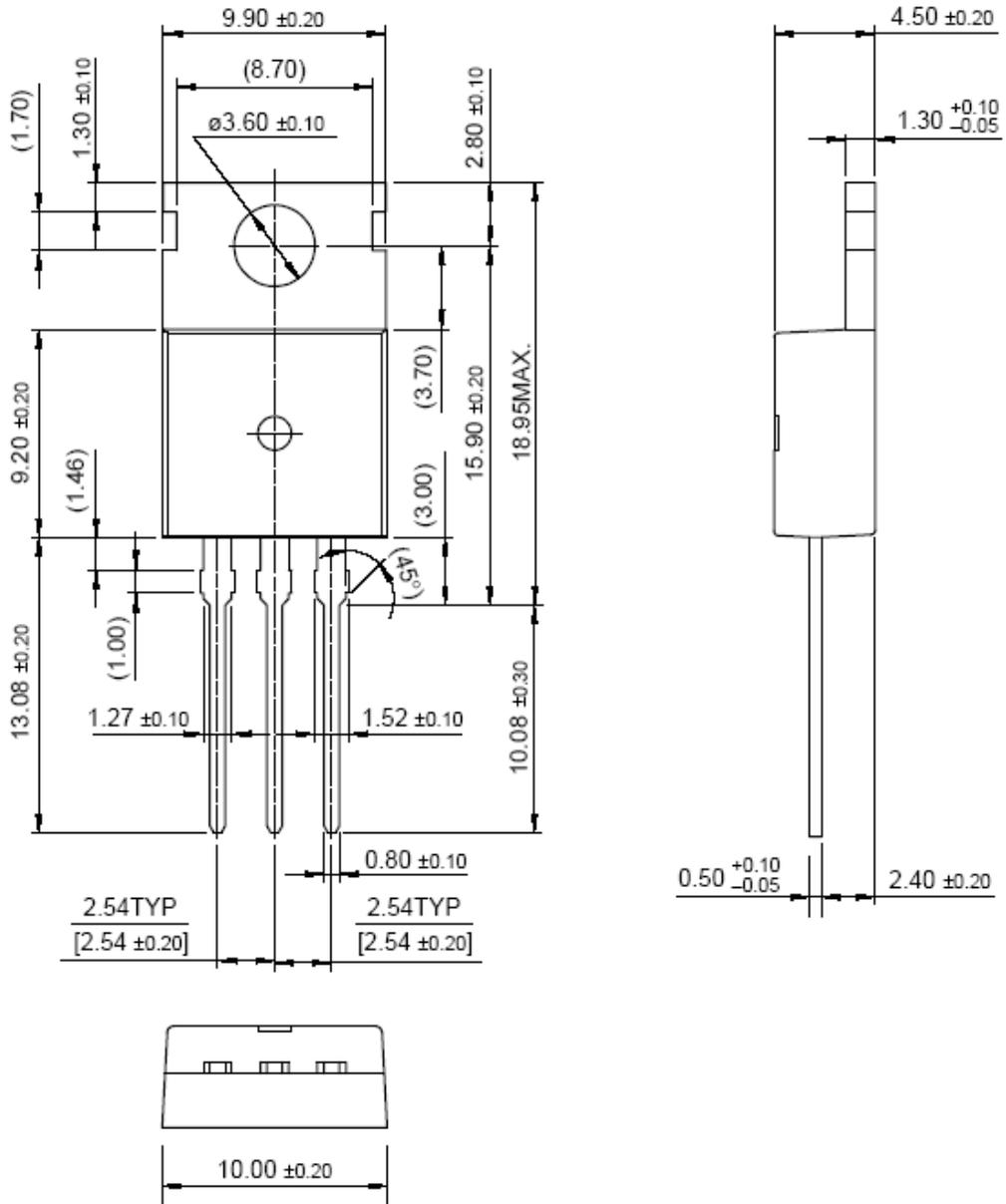


Fig 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

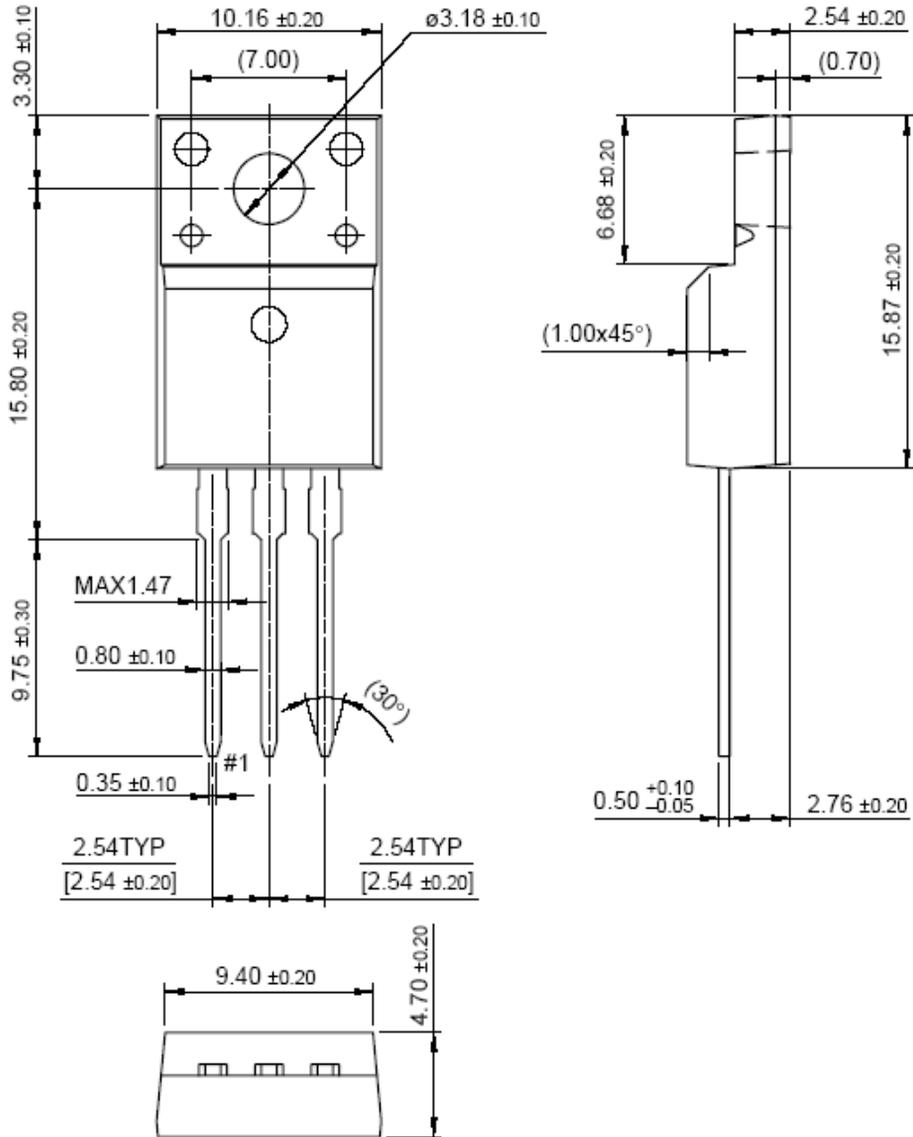
Package Dimension

TO-220



Package Dimension

TO-220F (1)



Package Dimension

TO-220F (2)

