POWER™

PFP13N50 / PFF13N50

500V N-Channel MOSFET

FEATURES

- Originative New Design
- 100% EAS Test
- Rugged Gate Oxide Technology
- Extremely Low Intrinsic Capacitances
- Remarkable Switching Characteristics
- Unequalled Gate Charge : 28 nC (Typ.)
- Extended Safe Operating Area
- Lower $R_{DS(ON)}$: 0.46 Ω (Typ.) @V_{GS}=10V

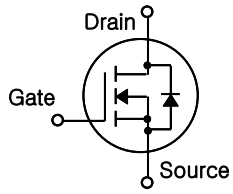
APPLICATION

- Electronic lamp ballasts based on half bridge topology
- PFC (Power Factor Correction)
- SMPS (Switched Mode Power Supplies)

BV_{DSS} = 500 V

$R_{DS(on)typ}$ = 0.46 Ω

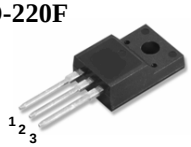
I_D = 12.5 A



TO-220

1.Gate 2. Drain 3. Source

TO-220F



1.Gate 2. Drain 3. Source

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	PFP13N50	PFF13N50	Units
V_{DSS}	Drain-Source Voltage	500		V
I_D	Drain Current – Continuous (T_C = 25℃)	12.5	12.5*	A
	Drain Current – Continuous (T_C = 100℃)	7.9	7.9*	A
I_{DM}	Drain Current – Pulsed (Note 1)	50	50*	A
V_{GS}	Gate-Source Voltage	±30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	810		mJ
I_{AR}	Avalanche Current (Note 1)	12.5		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	17		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5		V/ns
P_D	Power Dissipation (T_C = 25℃)	170	56	W
	– Derate above 25℃	1.35	0.45	W/℃
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		℃
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		℃

* Drain current limited by maximum junction temperature

Thermal Resistance Characteristics

Symbol	Parameter	PFP13N50	PFF13N50	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.74	2.23	℃/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink	0.5	--	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	

Electrical Characteristics T_C=25 °C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
V_{GS}	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.0	--	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 6.25 A	--	0.46	0.57	Ω
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	500	--	--	V
ΔBV_{DSS} /ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to25℃	--	0.5	--	V/℃
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	10	μA
		V_{DS} = 400 V, T_C = 125℃	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	1140	1480	pF
C_{oss}	Output Capacitance		--	155	200	pF
C_{rss}	Reverse Transfer Capacitance		--	18	25	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	V_{DS} = 250 V, I_D = 12.5 A, R_G = 25 Ω (Note 4,5)	--	15	30	ns
t_r	Turn-On Rise Time		--	30	60	ns
$t_{d(off)}$	Turn-Off Delay Time		--	70	140	ns
t_f	Turn-Off Fall Time		--	30	60	ns
Q_g	Total Gate Charge	V_{DS} = 400V, I_D = 12.5 A, V_{GS} = 10 V (Note 4,5)	--	28	35	nC
Q_{gs}	Gate-Source Charge		--	6.5	--	nC
Q_{gd}	Gate-Drain Charge		--	12	--	nC
Source-Drain Diode Maximum Ratings and Characteristics						
I_S	Continuous Source-Drain Diode Forward Current		--	--	12.5	A
I_{SM}	Pulsed Source-Drain Diode Forward Current		--	--	50	
V_{SD}	Source-Drain Diode Forward Voltage	I_S = 12.5 A, V_{GS} = 0 V	--	--	1.5	V
trr	Reverse Recovery Time	I_S = 12.5 A, V_{GS} = 0 V di_F/dt = 100 A/μs (Note 4)	--	380	--	ns
Qrr	Reverse Recovery Charge		--	3.0	--	μC

Notes ;

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. I_{AS}=12.5A, V_{DD}=50V, R_G=25Ω, Starting T_J=25°C
3. I_{SD}≤12.5A, di/dt≤300A/μs, V_{DD}≤BV_{DSS}, Starting T_J=25 °C
4. Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature

Typical Characteristics

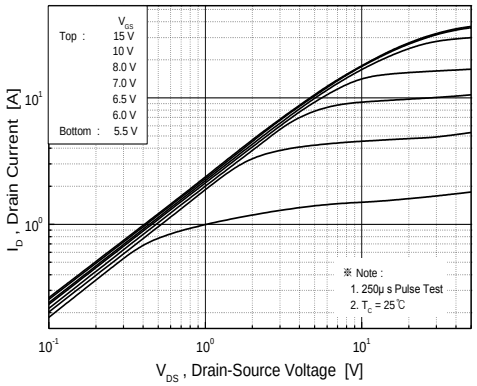


Figure 1. On Region Characteristics

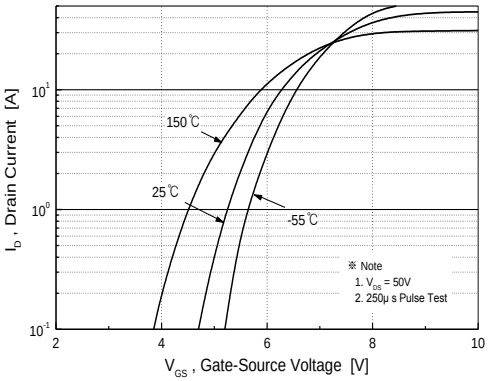


Figure 2. Transfer Characteristics

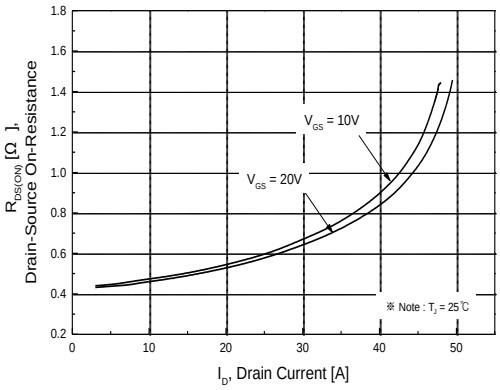


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

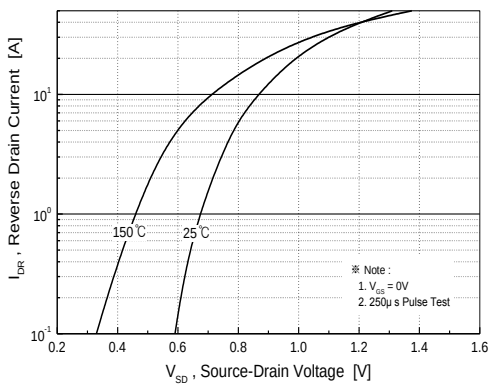


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

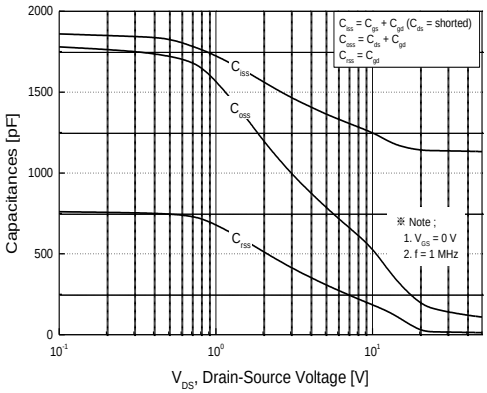


Figure 5. Capacitance Characteristics

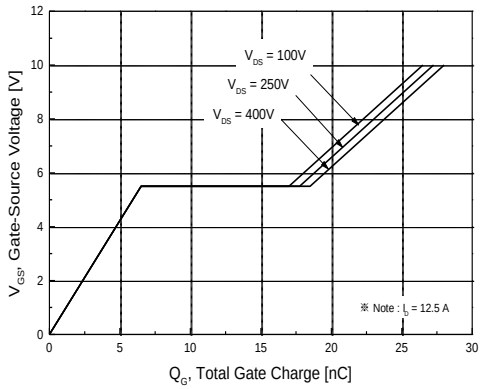


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

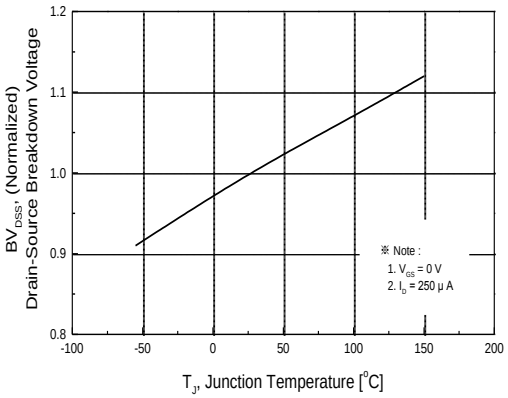


Figure 7. Breakdown Voltage Variation vs Temperature

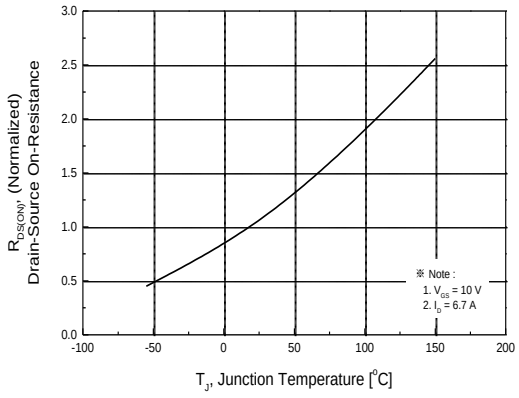


Figure 8. On-Resistance Variation vs Temperature

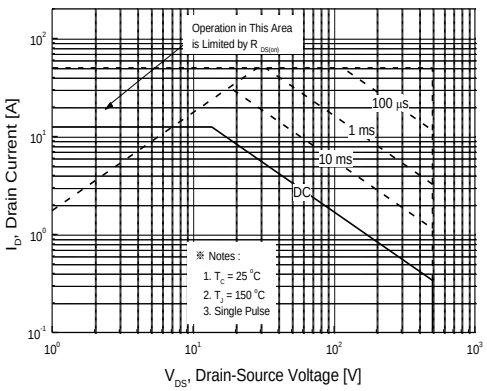


Figure 9. Maximum Safe Operating Area for PFP13N50

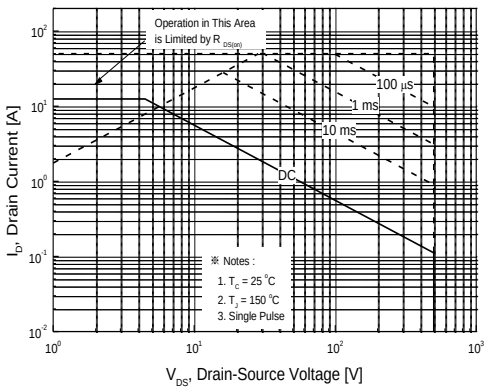


Figure 10. Maximum Safe Operating Area for PFF13N50

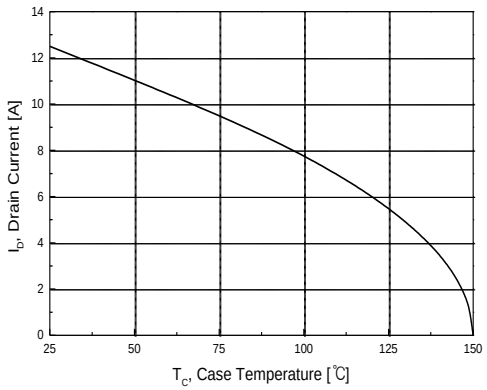


Figure 11. Maximum Drain Current vs Case Temperature

Typical Characteristics (continued)

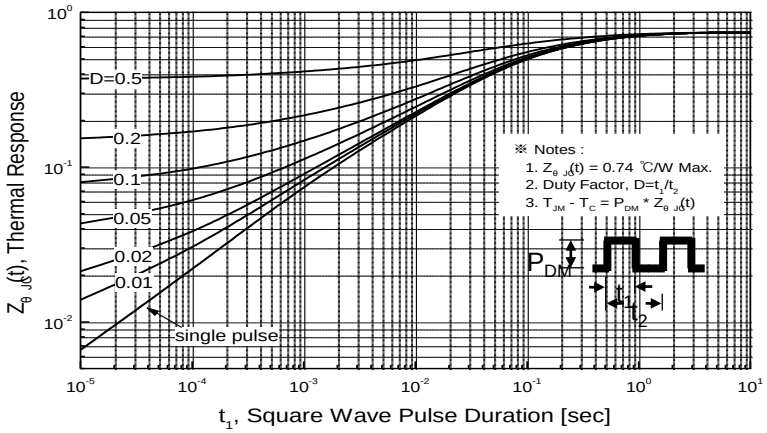


Figure 12. Transient Thermal Response Curve for PFP13N50

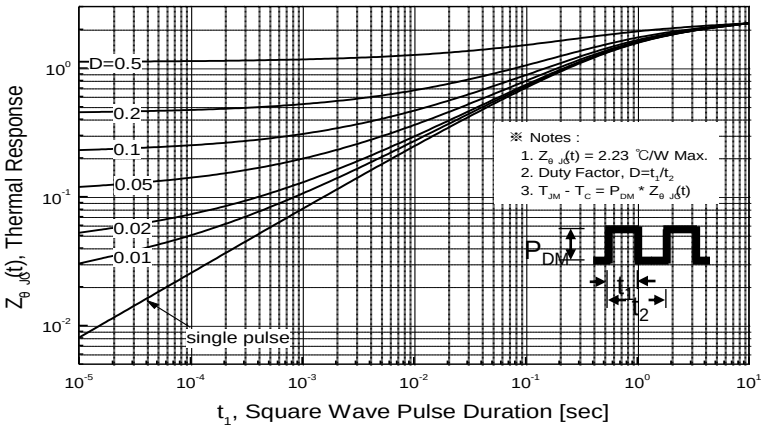


Figure 13. Transient Thermal Response Curve for PFF13N50

Characteristics Test Circuit & Waveform

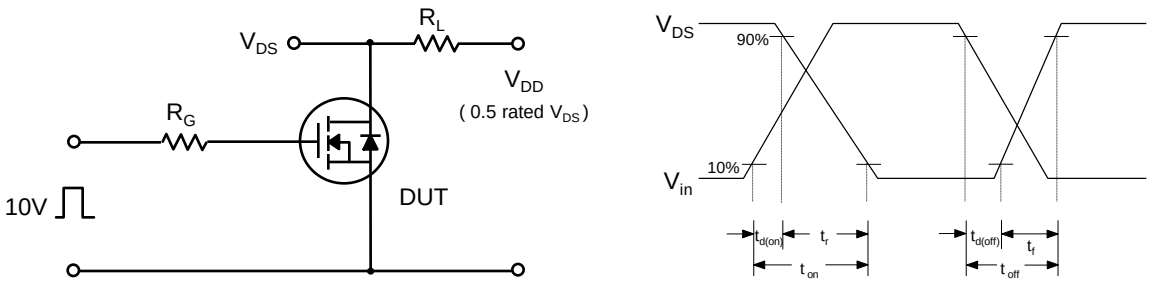


Fig 14. Resistive Switching Test Circuit & Waveforms

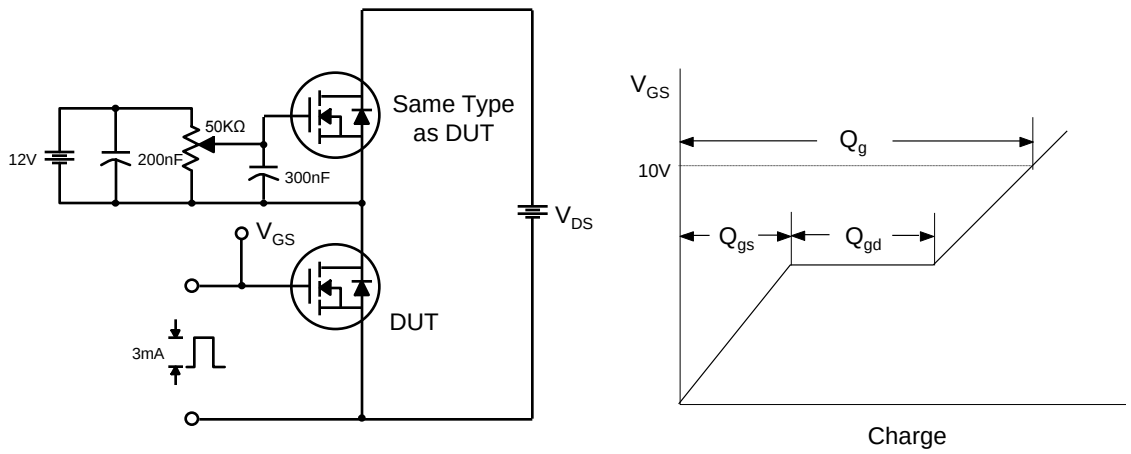


Fig 15. Gate Charge Test Circuit & Waveform

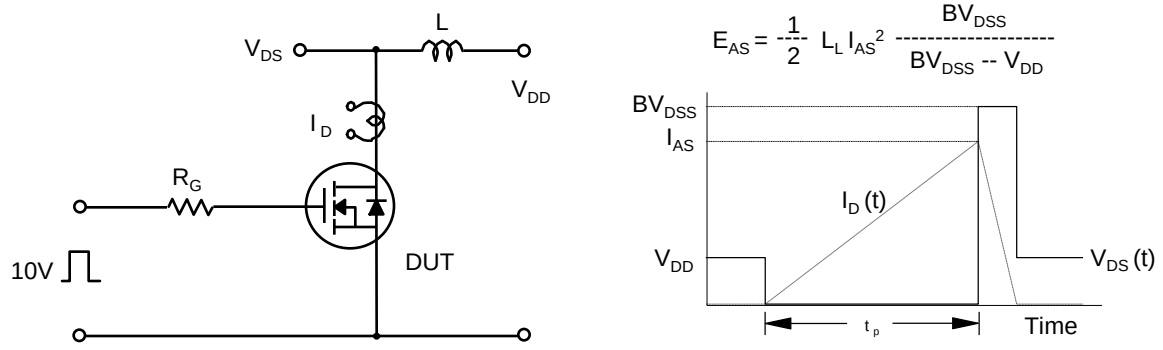
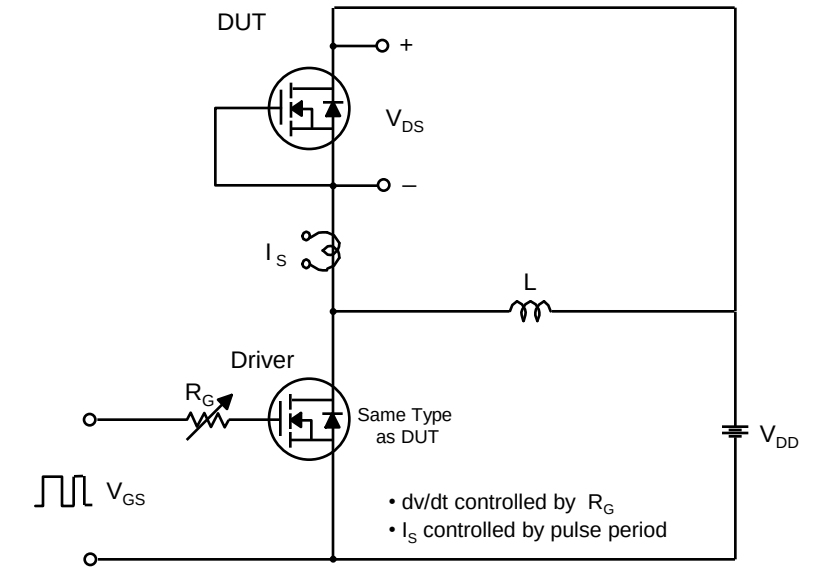


Fig 16. Unclamped Inductive Switching Test Circuit & Waveforms

Characteristics Test Circuit & Waveform (continued)



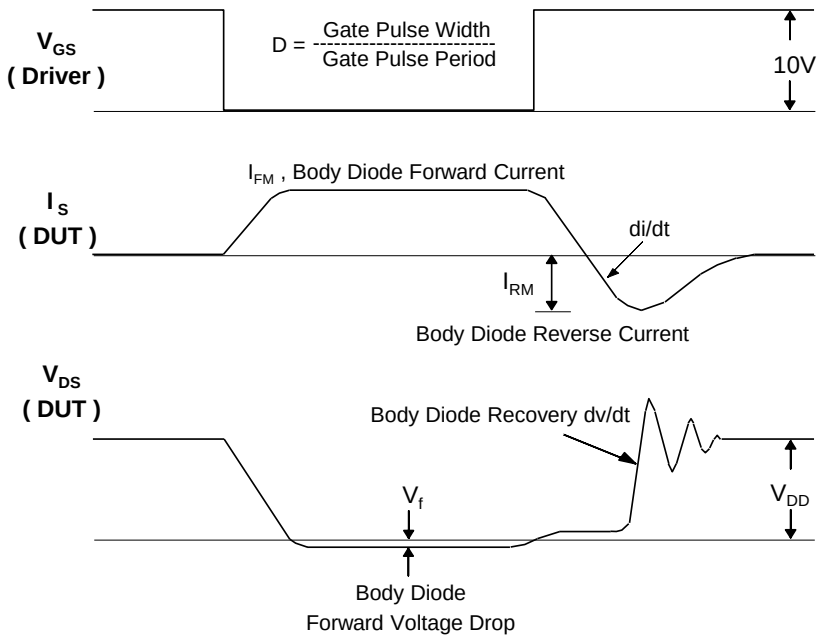
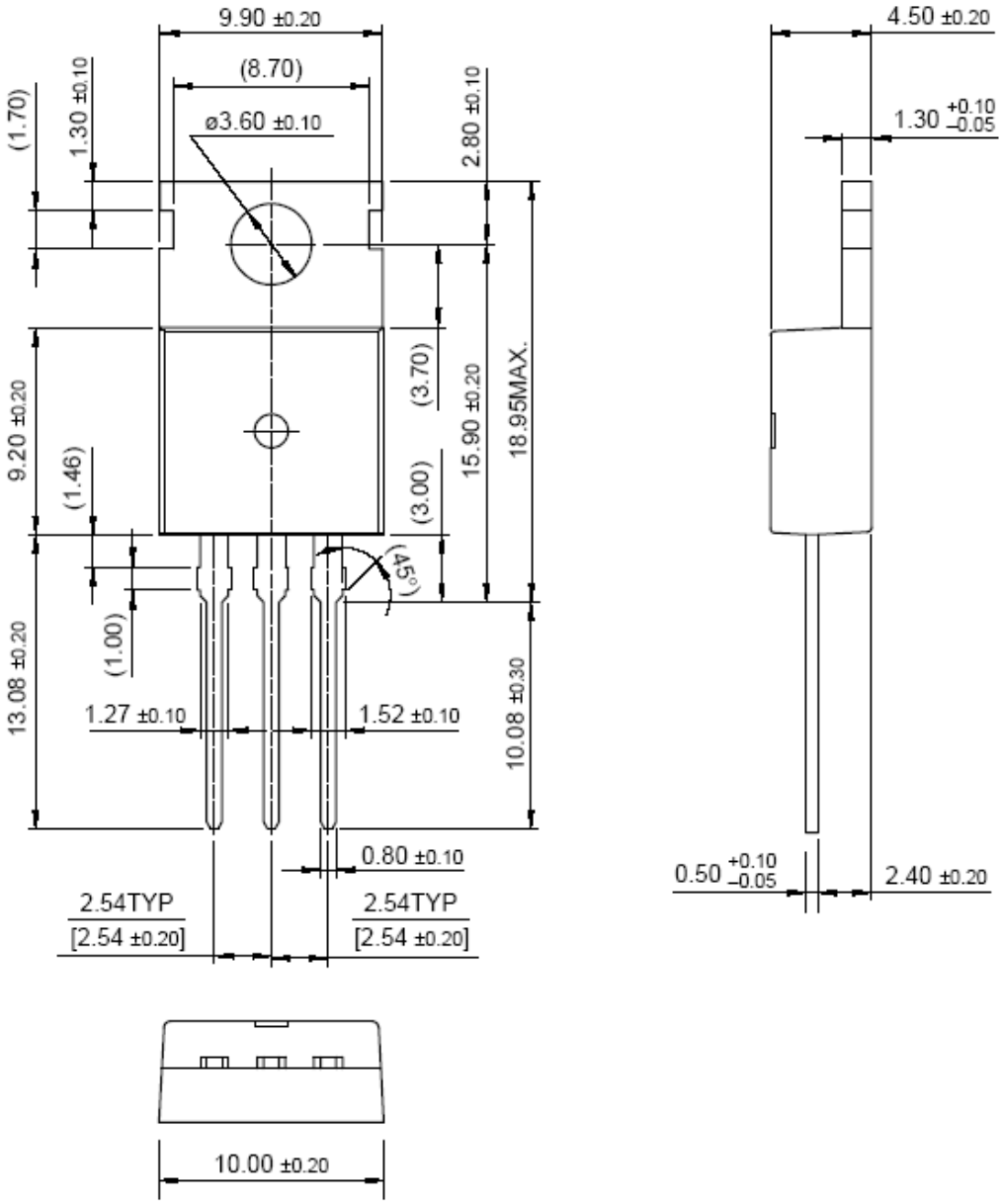


Fig 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Package Dimension

TO-220



Package Dimension

TO-220F