# STSPIN840

## Compact dual brushed DC motor driver

**QFN 4 x 4 - 24 lead**

## Features

- Operating voltage from 7 to 45 V
- Maximum output current 1.5 $A_{rms}$
- $R_{DSon}$ HS + LS = 1 $\Omega$ typ.
- Current control with adjustable OFF time
- Current sensing based on external shunt resistors
- Full protections set
  - Non-dissipative overcurrent protection
  - Short-circuit protection
  - Undervoltage lockout
  - Thermal shutdown
- Parallel operation mode achieving single full-bridge configuration with output $I_{RMS}$ = 3 $A_{rms}$ and $R_{DSon}$ HS + LS = 500 m$\Omega$ typ.
- Low standby current consumption

## Applications

- Industrial automation and service robots
- Medical and health care
- ATM and money handling machines
- Stage lighting
- Thermal printers
- Textile and sewing machines
- Vending machines
- Office and home automation

## Description

The STSPIN840 is a compact brushed DC motor driver able to drive two bi-directional brushed DC motors simultaneously. It integrates, in a very small 4 x 4 mm QFN package, both the control logic and a fully protected low $R_{DSon}$ dual full-bridge power stage.

Thanks to a dedicated PARALLEL input pin the parallel mode function can be enabled, transforming the device in an equivalent and more powerful single full-bridge able to deliver up to 3$A_{rms}$ current at an equivalent HS + LS $R_{DSon}$ of 500 m$\Omega$.

The STSPIN840 embeds two independent PWM current controllers (one for each full bridge) based on user settable values of reference voltage and OFF time.

The devices can be forced in a low consumption state reducing the total current consumption down to less than 45 $\mu$A.

As with all other devices from the STSPIN family, the STSPIN840 integrates a complete set of protections for the power stages (non-dissipative overcurrent, thermal shutdown, short-circuit and undervoltage lockout) making it a bulletproof solution for the new wave of demanding industrial applications.

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**Figure 1. Block diagram (general)**

# 2 Electrical data

## 2.1 Absolute maximum ratings

**Table 1. Absolute maximum ratings**

| Symbol | Parameter | Test condition | Value | Unit |
|--------|-----------|:-:|:-:|:-:|
| $V_S$ | Supply voltage | - | -0.3 to 48 | V |
| $V_{IN}$ | Logic input voltage | - | -0.3 to 5.5 | V |
| $V_{OUT,diff}$ | Differential voltage between VSx, OUT1x, OUT2x and SENSEx pins | - | up to 48 | V |
| $V_{SENSE}$ | Sense pins voltage[1] | - | -2 to 2 | V |
| $V_{REFX}$ | Reference voltage input | - | -0.3 to 2 | V |
| $I_{OUT,RMS}$ | Continuous power stage output current (each full bridge) | - | 1.5 | $A_{rms}$ |
| $T_j$ | Junction temperature | - | -40 to 150 | °C |
| $T_{stg}$ | Storage temperature | - | -55 to 150 | °C |

1. SENSEA1, SENSEA2, SNSA, SENSEB1, SENSEB2, SNSB.

## 2.2 Recommended operating conditions

**Table 2. Recommended operating conditions**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------|-----------|:-:|:-:|:-:|:-:|
| $V_S$ | Supply voltage | 7 | - | 45 | V |
| $V_{IN}$ | Logic input voltage | | - | 5 | V |
| $V_{SENSE}$ | Sense pins voltage | -1 | - | +1 | V |
| $V_{REFX}$ | Reference voltage input | 0.1 | - | 1 | V |

## 2.3 Thermal data

**Table 3. Thermal data**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| $R_{thJA}$ | Junction to ambient thermal resistance | Natural convection, according to JESD51-2a[1] | 36.5 | °C/W |
| $R_{thJCtop}$ | Junction to case thermal resistance (top side) | Cold plate on top package, according to JESD51-12[1] | 27.6 | °C/W |
| $R_{thJCbot}$ | Junction to case thermal resistance (bottom side) | Cold plate on exposed pad, according to JESD51-12[1] | 5.9 | °C/W |
| $R_{thJB}$ | Junction to board thermal resistance | According to JESD51-8[1] | 13.6 | °C/W |
| $\Psi_{JT}$ | Junction to top characterization | According to JESD51-2a[1] | 1 | °C/W |
| $\Psi_{JB}$ | Junction to board characterization | According to JESD51-2a[1] | 13.7 | °C/W |

1. Simulated on a 76.2 x 114.3 x 1.6 mm, with vias underneath the component, 2s2p board as per standard JEDEC (JESD51-7) in natural convection.

## 2.4 ESD protection ratings

**Table 4. ESD protection ratings**

| Symbol | Parameter | Conditions | Class | Value | Unit |
|---|---|---|---|---|---|
| HBM | Human body model | Conforming to ANSI/ESDA/JEDEC JS001 | H2 | 2 | kV |
| CDM | Charge device model | Conforming to ANSI/ESDA/JEDEC JS002 All pins | C2a | 500 | V |
| | | Conforming to ANSI/ESDA/JEDEC JS002 Corner pins only (1, 6, 7, 12, 13, 18, 19, 24) | - | 750 | V |
| MM | Machine model | Conforming to EIA/JESD22-A115-C | NC | 200 | V |

# 3 Electrical characteristics

Testing conditions: $V_S$ = 36 V, $T_j$ = 25 °C unless otherwise specified.

**Table 5. Electrical characteristics**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **General** | | | | | | |
| $V_{Sth(ON)}$ | $V_S$ turn-on threshold | $V_S$ rising from 0 V | - | 6.0 | 6.5 | V |
| $V_{Sth(HYST)}$ | $V_S$ turn-off threshold hysteresis | $V_S$ falling from 7 V | - | 0.4 | - | V |
| $I_S$ | $V_S$ supply current | No commutations ENx = '0' $R_{TOFF}$ = 10 kΩ | - | 2.3 | 2.7 | mA |
| | | No commutations ENx = '1' $R_{TOFF}$ = 10 kΩ | - | 2.7 | 3 | mA |
| $V_{STBYL}$ | Standby low voltage | - | - | - | 0.8 | V |
| $V_{STBYH}$ | Standby high voltage | - | 2 | - | - | V |
| $I_{S, STBY}$ | $V_S$ supply standby current | STBY = '0' | - | - | 45 | µA |
| **Power stage** | | | | | | |
| $R_{DSon\ HS+LS}$ | Total on resistance HS + LS | $V_S$ = 21 V $I_{OUT}$ = 1 A | - | 1 | 1.3 | Ω |
| | | $V_S$ = 21 V $I_{OUT}$ = 1 A Tj = 150 °C[1] | - | 1.4 | 1.6 | |
| $I_{DSS}$ | Output leakage current | OUTx = $V_S$ = 48 V | - | - | 20 | µA |
| | | OUTx = -0.3 V | -1 | - | - | |
| $V_{DF}$ | Freewheeling diode forward voltage | $I_D$ = 1.5 A | - | 1 | - | V |
| $t_{rise}$ | Rise time | $V_S$ = 21 V | - | 120 | - | ns |
| $t_{fall}$ | Fall time | $V_S$ = 21 V | - | 60 | - | ns |
| **Logic IO** | | | | | | |
| $V_{IH}$ | High logic level input voltage | - | 2 | - | - | V |
| $V_{IL}$ | Low logic level input voltage | - | - | - | 0.8 | V |
| $V_{OL}$ | Low logic level output voltage | $I_{OL}$ = 4 mA | - | - | 0.3 | V |
| $V_{RELEASE}$ | FAULT open drain release voltage | - | - | - | 0.6 | V |
| $R_{STBY}$ | STBY pull-down resistance | - | - | 60 | - | kΩ |
| $I_{ENx}$ | Enable pull-down current | - | - | 5 | - | µA |
| $t_{ENxd}$ | Enable input propagation delay | From ENx falling edge to OUTx high impedance | - | 400 | - | ns |
| $t_{PWM,d(ON)}$ | PWM turn-on propagation delay | [2] | - | 450 | - | ns |

**Table 5. Electrical characteristics (continued)**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--------|-----------|----------------|------|------|------|------|
| $t_{PWM,d(OFF)}$ | PWMx turn-off propagation delay | (2) | - | 250 | - | ns |
| $t_{PH,d}$ | PHx propagation delay | (2) | - | 450 | - | ns |
| **PWM current control** | | | | | | |
| $V_{SNS,OFFSET}$ | Current control offset | - | -15 | - | 15 | mV |
| $t_{BLANK}$ | Blanking time | - | - | 1.5 | - | µs |
| $t_{OFF}$ | Total OFF time | $R_{OFF}$ = 10 kΩ | - | 13 | - | µs |
| | | $R_{OFF}$ = 160 kΩ | - | 146 | - | µs |
| $\Delta_{tOFF}$ | OFF time precision | Full temperature range(1) | -20 | - | +20 | % |
| $t_{OFF,jitter}$ | Total OFF time jittering | - | - | ±2 | - | |
| **Protections** | | | | | | |
| $T_{jSD}$ | Thermal shutdown threshold | - | - | 160 | - | °C |
| $T_{jSD,Hyst}$ | Thermal shutdown hysteresis | - | - | 40 | - | °C |
| $I_{OC}$ | Overcurrent protection threshold | - | - | 3 | 3.5 | A |

1. Based on characterization data on a limited number of samples, not tested during production.

2. See *Figure 4*.

# 4    Pin connection

Figure 2. Pin connection (top view)
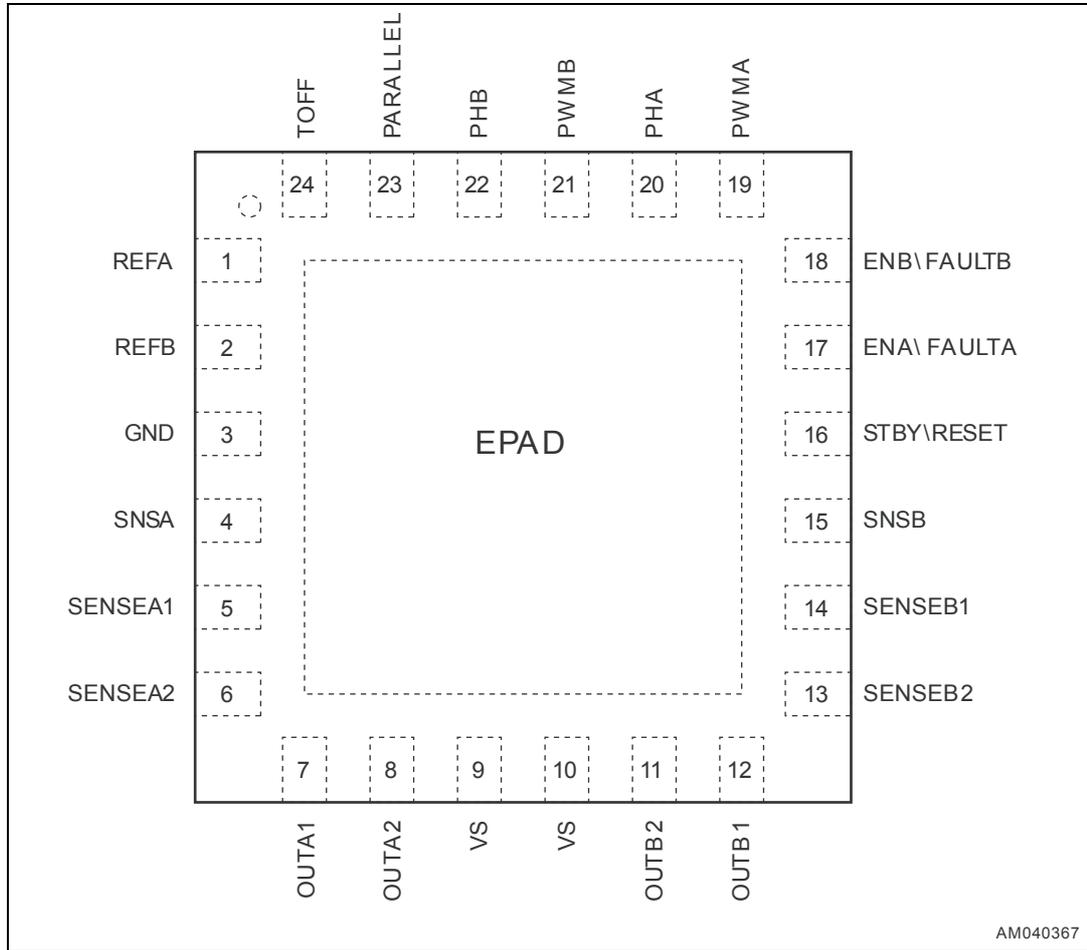


*Note:    The exposed pad must be connected to ground.*

Table 6. Pin description

| No. | Name | Type | Function |
|---|---|---|---|
| 1 | REFA | Analog input | Reference voltage for the PWM current control circuitry (side A) |
| 2 | REFB | Analog input | Reference voltage for the PWM current control circuitry (side B) |
| 3, EPAD | GND | Ground | Device ground |
| 4 | SNSA | Analog input | Full bridge A current regulator sense input |
| 5 | SENSEA1 | Power output | Sense output of the bridge A |
| 6 | SENSEA2 | Power output | Sense output of the bridge A |
| 7 | OUTA1 | Power output | Power bridge output side A1 |
| 8 | OUTA2 | Power output | Power bridge output side A2 |

**Table 6. Pin description (continued)**

| No. | Name | Type | Function |
|-----|------|------|----------|
| 9 | VS | Supply | Device supply voltage |
| 10 | VS | Supply | Device supply voltage |
| 11 | OUTB2 | Power output | Power bridge output side B2 |
| 12 | OUTB1 | Power output | Power bridge output side B1 |
| 13 | SENSEB2 | Power output | Sense output of the bridge B |
| 14 | SENSEB1 | Power output | Sense output of the bridge B |
| 15 | SNSB | Analog input | Full bridge B current regulator sense input |
| 16 | STBY\ RESET | Logic input | Standby\Reset input.<br>When forced low the device enter in low consumption mode |
| 17 | ENA\ FAULTA | Logic input\ open drain output | Logic input 5 V compliant with open drain output.<br>This is the full bridge A enable (when low, the power stage is turned off) and is forced low through the integrated open-drain MOSFET when a failure occurs. |
| 18 | ENB\ FAULTB | Logic input\ open drain output | Logic input 5 V compliant with open drain output.<br>This is the full bridge B enable (when low, the power stage is turned off) and is forced low through the integrated open-drain MOSFET when a failure occurs. |
| 19 | PWMA | Logic input | Full bridge A PWM input |
| 20 | PHA | Logic input | Full bridge A current direction input |
| 21 | PWMB | Logic input | Full bridge B PWM input |
| 22 | PHB | Logic input | Full bridge B current direction input |
| 23 | PARALLEL | Logic input | Parallel mode input (see paragraph PARALLEL mode) |
| 24 | TOFF | Analog input | Internal oscillator frequency adjustment. |

# 5 Detailed description

The STSPIN840 is a dual brush DC motor driver integrating two PWM current controllers and a power stage composed of two fully-protected full-bridges.

## 5.1 Power supply and standby

The device is supplied through the VS pins, the two pins must be at the same voltage.

At power-up the power stage is disabled and the FAULT pins are forced low until the $V_S$ voltage rise above the $V_{Sth(ON)}$ threshold.

If the $V_S$ falls below the $V_{Sth(ON)}$ - $V_{Sth(HYST)}$ value power stage is immediately disabled and the FAULT pins are forced low.

**Figure 3. UVLO protection management**
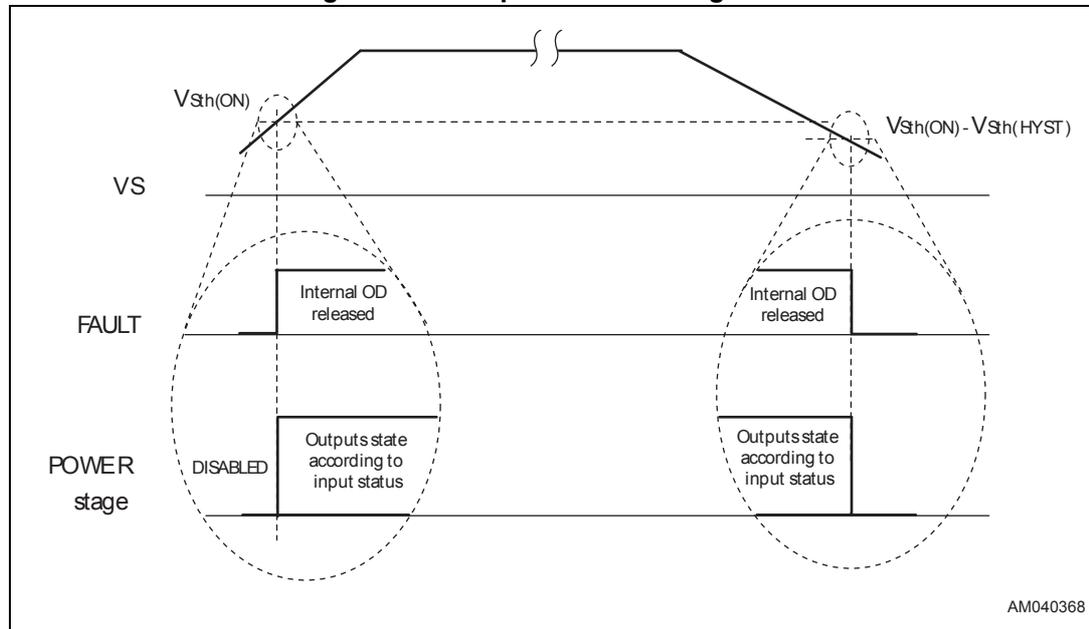


The device provides a low consumption mode, which is set by forcing the STBY\RESET input below the $V_{STBYL}$ threshold.

When the device is in standby status the power stage is disabled (outputs are at high impedance) and the supply to the integrated control circuitry is strongly reduced. When the device leaves the standby status, all the control circuitry is reset to the power-up condition.

## 5.2    Logic inputs

The outputs of each full bridge are controlled by the respective PWMx and PHx inputs. The status of the power bridge is also determined by the PWM current controller as indicated in *Section 5.3*.

**Table 7. Truth table**

| ENx | PHx | PWMx | OUTx1 | OUTx2 | Full bridge condition |
|-----|-----|------|-------|-------|-----------------------|
| 0 | X[1] | X[1] | High Z[2] | High Z[2] | Disabled |
| 1 | 0 | 0 | GND | GND | Both LS on |
| 1 | 0 | 1 | GND | VS | HS2 and LS1 on (current OUTx1 → OUTx2) |
| 1 | 1 | 0 | GND | GND | Both LS on |
| 1 | 1 | 1 | VS | GND | HS1 and LS2 on (current OUTx1 → OUTx2) |

1.  X: don't care.

2.  High Z: high impedance.

**Figure 4. Dual brush DC motor driver time diagram**
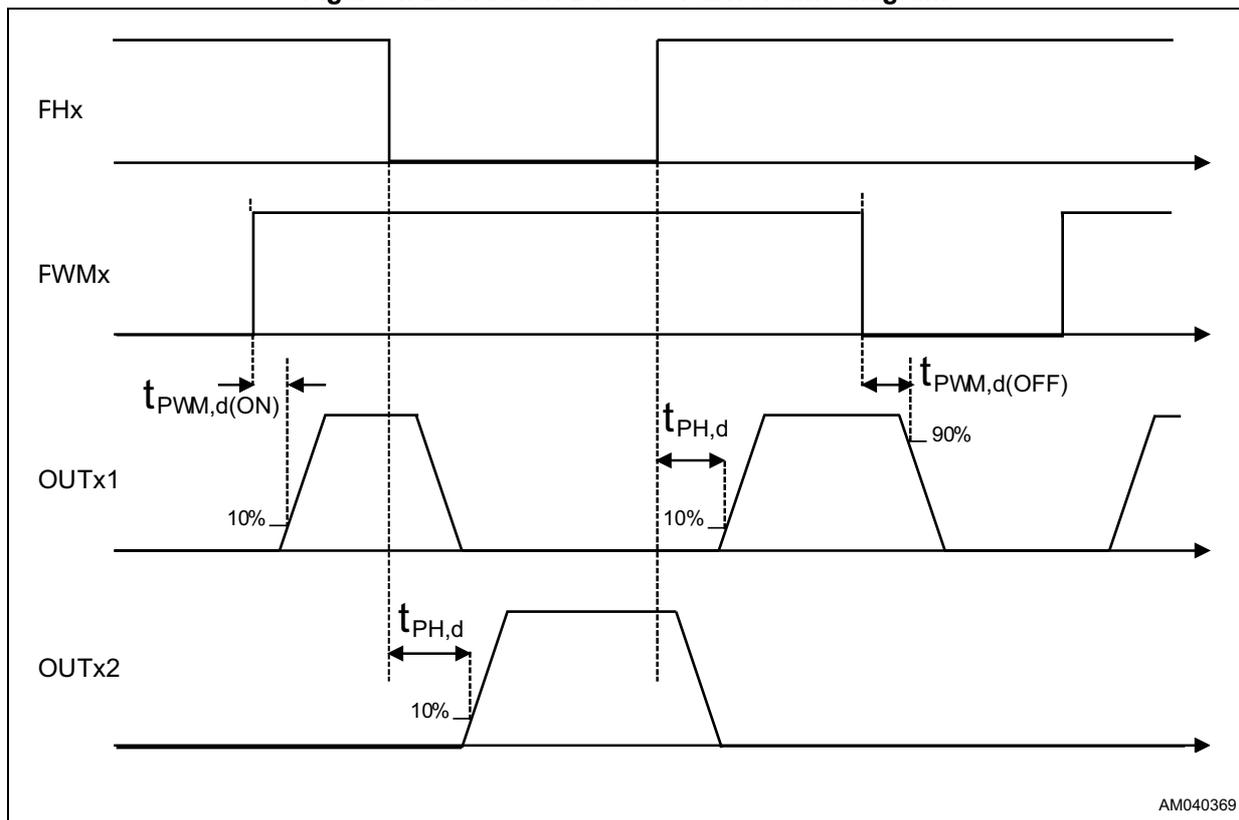
## PARALLEL mode

The device can operate in parallel mode by forcing the PARALLEL input pin high.

In this operation mode both the full bridges are driven by the ENA, PWMA and PHA inputs. The PWM current control comparator of the bridge B is disabled, and bridge A one drives both the power stages.

The resulting single full-bridge power stage allows an increase in the output current capability and reduce the device power dissipation. The outputs and sense pins configuration must be:

- OUT1A connected with OUT1B
- OUT2A connected with OUT2B
- All SENSE and SNS pins connected together as shown in *Figure 5*.

The ENA\FAULTA pin is also used as FAULT indication through the integrated open-drain MOSFETs as described in *Section 5.4* and *Section 5.4.3 on page 21*.

*Note:* *In parallel mode the ENB\FAULTB pin is forced low.*

**Figure 5. PARALLEL mode typical application**
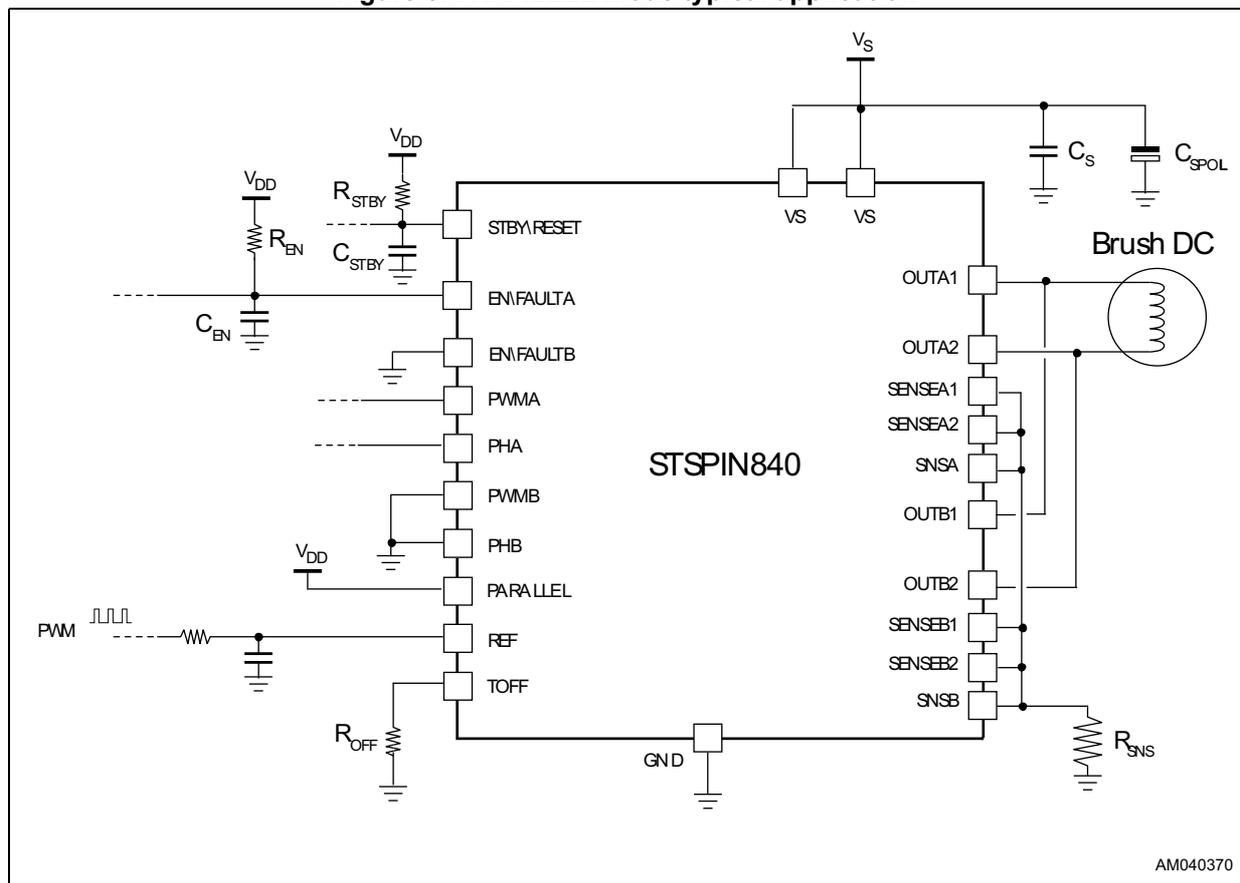
## 5.3 PWM current control

The device implements two independent PWM current controllers, one for each full bridge.

The bridge current is sensed through the SNS pins monitoring the voltage drop across an external resistor connected between the source of the low side power MOSFET (SENSE pins) and ground.

The voltage of the SNS pins ($V_{SNSA}$ and $V_{SNSB}$) is compared to the respective reference voltage pin ($V_{REFA}$ and $V_{REFB}$).

When $V_{SNSX} > V_{REFX}$ the current limiter is triggered, the OFF time counter is started and the low sides of the full bridge are turned on (slow decay) until the end of count of the timer.

During current decays the inputs values are ignored until the system returns to ON condition (decay time expired).

**Table 8. ON and slow decay states**

| PHx[1] | PWMx[1] | ON | Slow decay |
|:---:|:---:|:---:|:---:|
| 0 | 0 | HSx1 = OFF<br>**LSx1 = ON**<br>HSx2 = OFF<br>**LSx2 = ON** | HSx1 = OFF<br>**LSx1 = ON**<br>HSx2 = OFF<br>**LSx2 = ON** |
| 0 | 1 | HSx1 = OFF<br>**LSx1 = ON**<br>**HSx2 = ON**<br>LSx2 = OFF | HSx1 = OFF<br>**LSx1 = ON**<br>HSx2 = OFF<br>**LSx2 = ON** |
| 1 | 0 | HSx1 = OFF<br>**LSx1 = ON**<br>HSx2 = OFF<br>**LSx2 = ON** | HSx1 = OFF<br>**LSx1 = ON**<br>HSx2 = OFF<br>**LSx2 = ON** |
| 1 | 1 | **HSx1 = ON**<br>LSx1 = OFF<br>HSx2 = OFF<br>**LSx2 = ON** | HSx1 = OFF<br>**LSx1 = ON**<br>HSx2 = OFF<br>**LSx2 = ON** |

1. When the device works in parallel mode the PHA and PWMA inputs drive both Full bridge A and B.

The reference voltage value, $V_{REF}$, has to be selected according the load current target value (peak value) and sense resistors value.

**Equation 1**

$$V_{REF} = R_{SENSE} \times I_{LOAD,peak}$$

The choice of sense resistors value must be take into account two main issues:

- The sensing resistor dissipates energy and provides dangerous negative voltages on the SENSE pins during the current recirculation. For this reason the resistance of this component should be kept low (using multiple resistors in parallel will help obtaining the required power rating with standard resistors).

- The lower is the RSENSE value, the higher is the peak current error due to noise on $V_{REF}$ pin and to the input offset of the current sense comparator: too small values of RSENSE must be avoided.

**Figure 6. PWM current control sequence example**
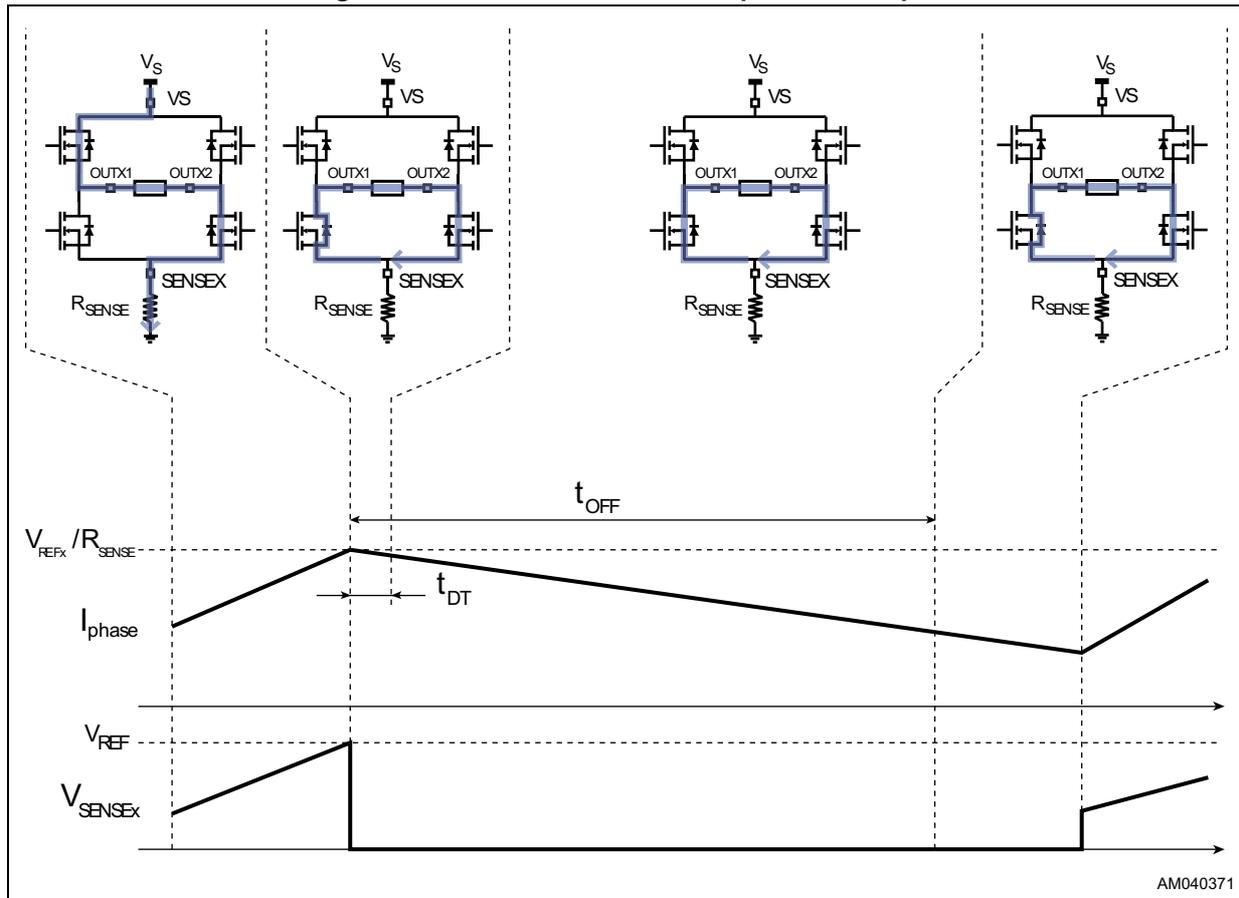


*Note:* *When the voltage on the SNSx pin exceeds the absolute ratings, a fault condition is triggered and the respective ENx\FAULTx output is forced low.*

## TOFF adjustment

The OFF time is adjusted through an external resistor connected between the TOFF pin and ground as shown in *Figure 7*.

**Figure 7. OFF time regulation circuit**
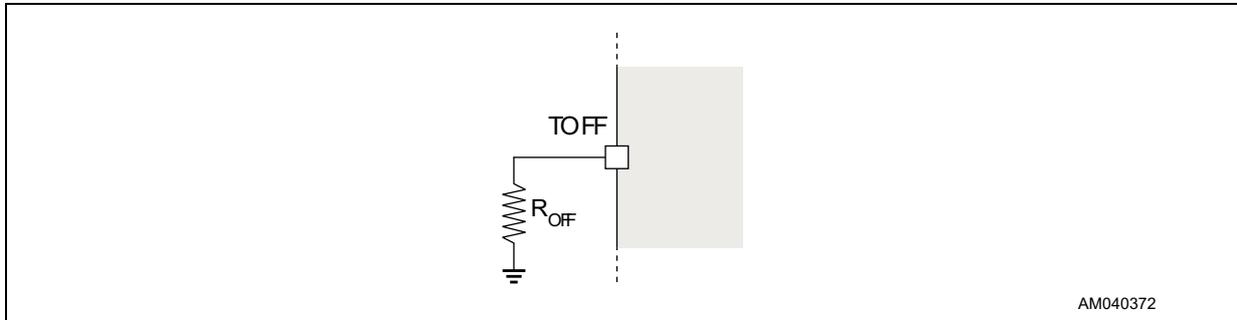


The relation between the OFF time and the external resistor value is shown in the graph of *Figure 8*. The value typically ranges from 10 µs to 150 µs.

The recommended value for $R_{OFF}$ is in the range between 5 k$\Omega$ and 180 k$\Omega$.

**Figure 8. OFF time vs $R_{OFF}$ value**
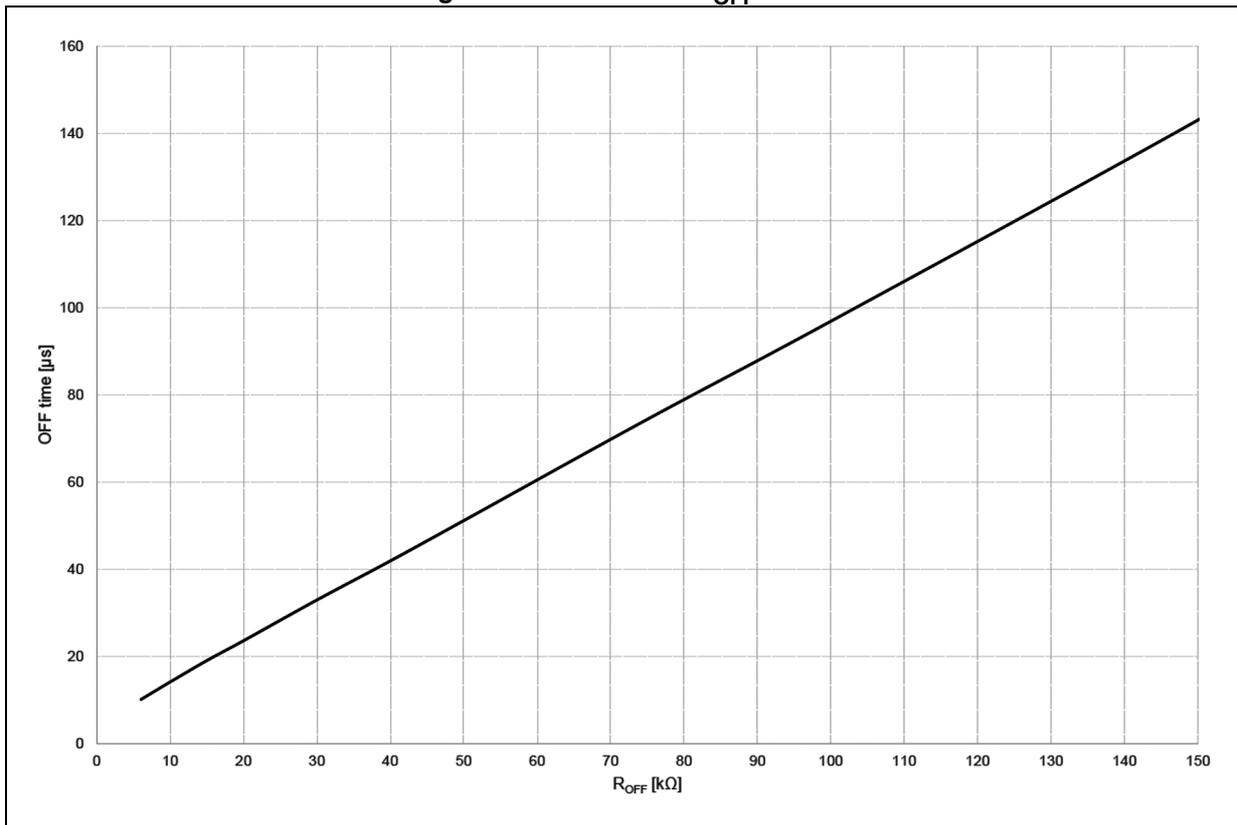
## 5.4 Device protections

### 5.4.1 Overcurrent and short-circuit protections

The device has circuitry embedded to protect each power MOSFET against the overload and short-circuit conditions (short-circuit to ground, short-circuit to VS and short-circuit between outputs).

When the overcurrent or the short-circuit protection is triggered the respective power stage is disabled and the relative EN\FAULT input is forced low through the integrated open-drain MOSFET discharging the external $C_{EN}$ capacitor (refer to *Figure 9*).

The power stage is kept disabled and the open-drain MOSFET is kept ON until the EN\FAULT input falls below the $V_{RELEASE}$ threshold, then the $C_{EN}$ capacitor is charged through the external $R_{EN}$ resistor.

**Figure 9. Overcurrent and short-circuit protections management**
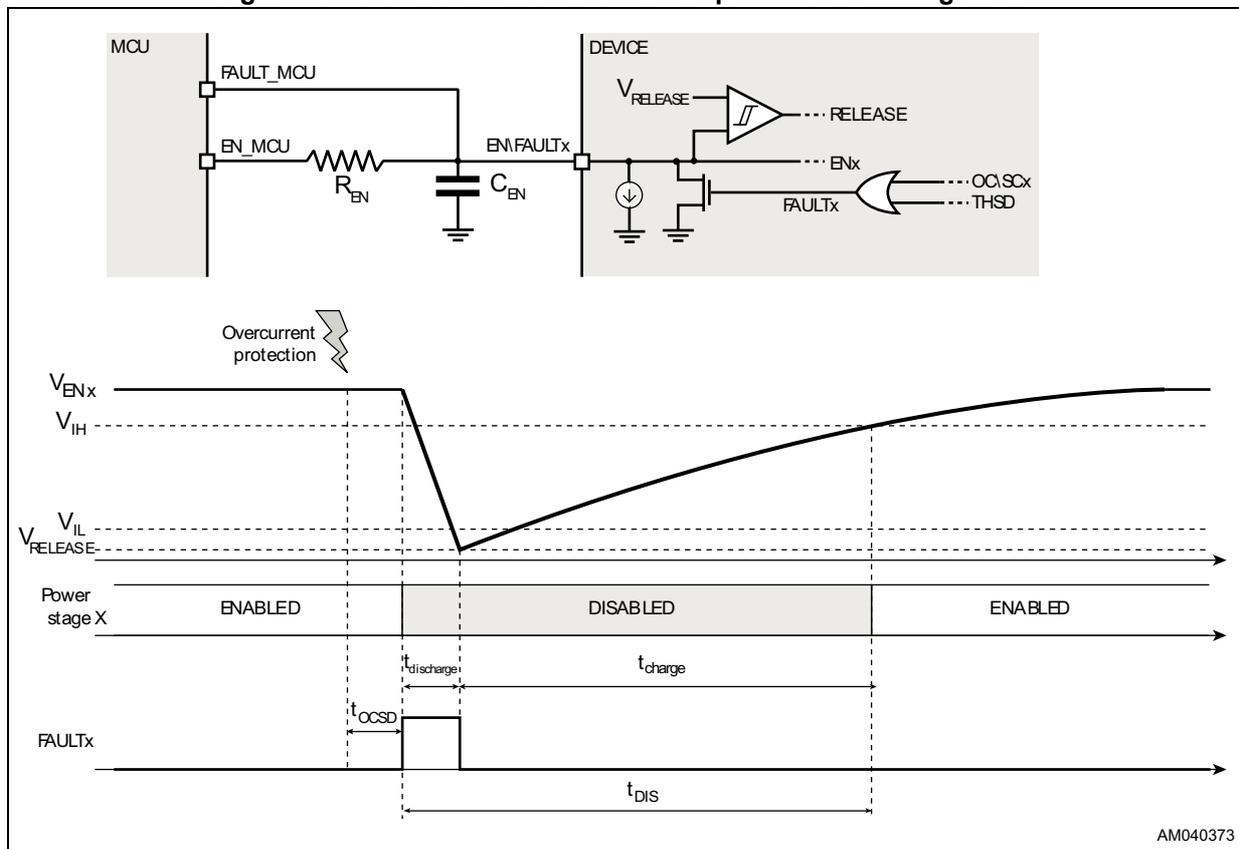


The total disable time after an overcurrent event is set sizing properly the external network connected to EN\FAULT pins (refer to *Figure 10*) and it is the sum of the discharging and charging time of the $C_{EN}$ capacitor:

**Equation 2**

$$t_{DIS} = t_{discharge} + t_{charge}$$

Considering $t_{discharge}$ is normally significantly lower than $t_{charge}$, its contribution is negligible and the disable time is almost equal to $t_{charge}$ only:

**Equation 3**

$$t_{DIS} \cong R_{EN} \times C_{EN} \times I_n \frac{(V_{DD} - R_{EN} \times I_{PD}) - V_{RELEASE}}{(V_{DD} - R_{EN} \times I_{PD}) - V_{IH}}$$

Where $V_{DD}$ is the pull-up voltage of $R_{EN}$ resistor.

The recommended value for $R_{EN}$ and $C_{EN}$ are respectively 39 k$\Omega$ and 10 nF that allow obtaining 300 µs disable time.

**Figure 10. Disable time versus $R_{EN}$ and $C_{EN}$ values (VDD = 3.3 V)**
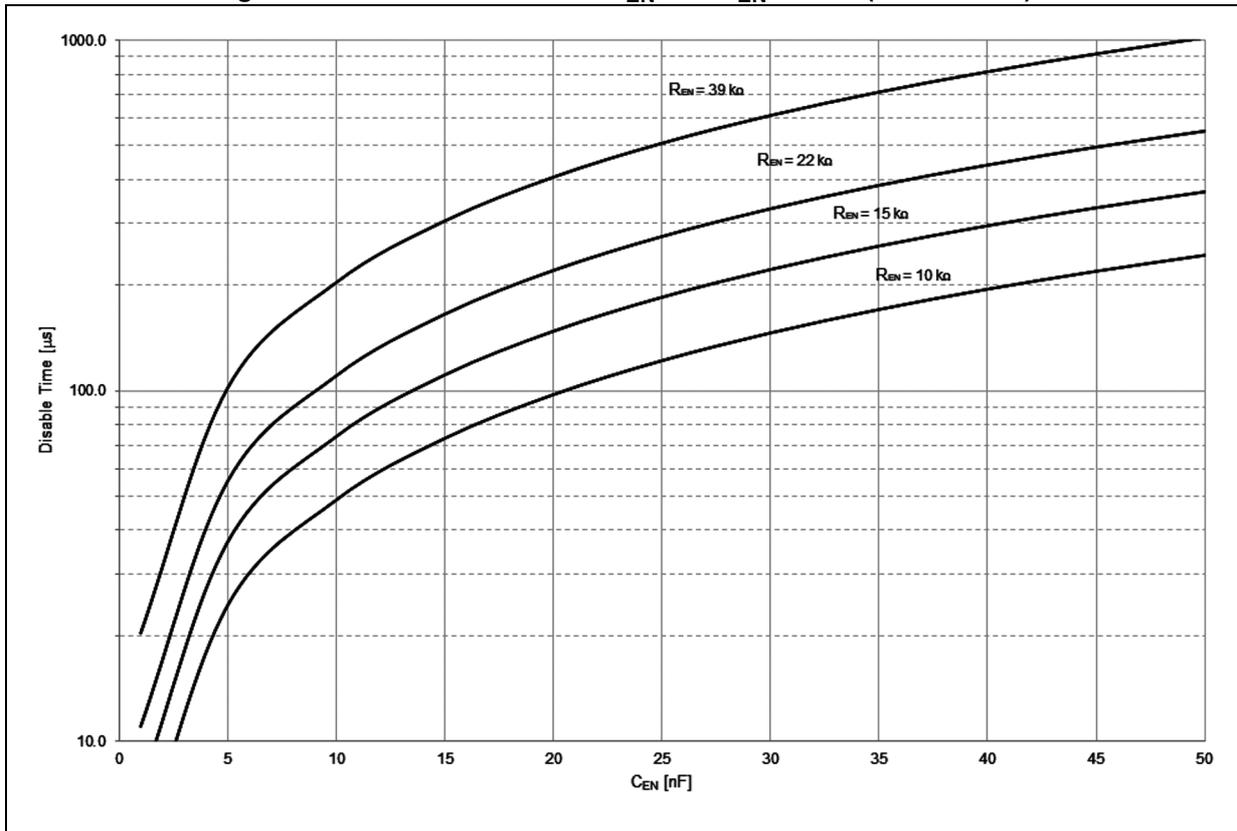
**Figure 11. Overcurrent threshold versus temperature (normalized at 25 °C)**
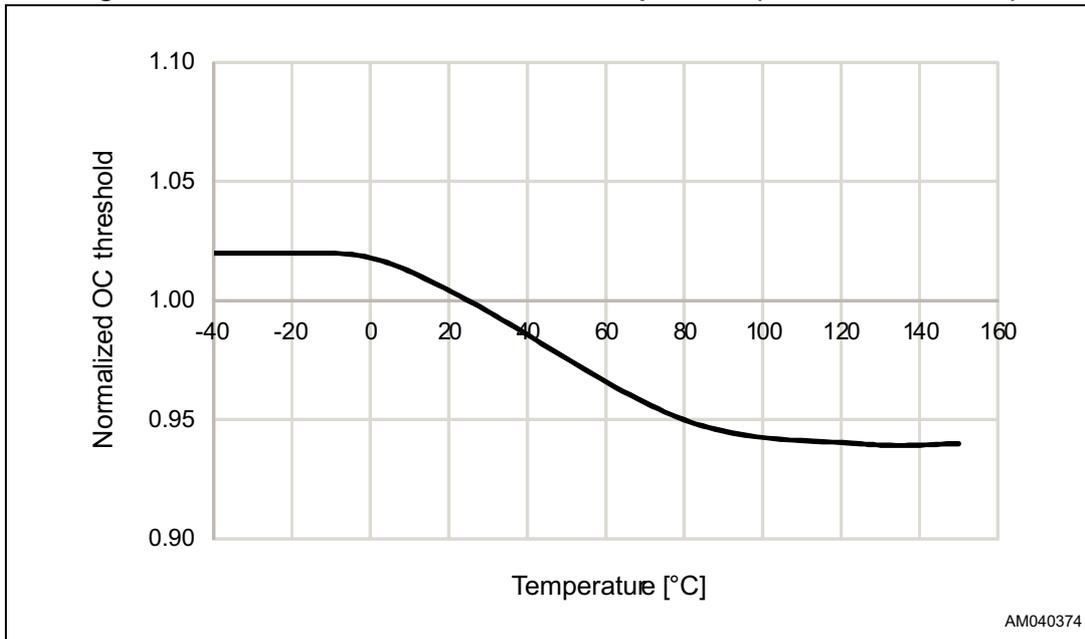


### 5.4.2 Thermal shutdown

The device has circuitry embedded to protect it from overtemperature conditions.

When the thermal shutdown temperature is reached both the power bridge are disabled and both the EN\FAULT inputs are forced low through the integrated open-drain MOSFETs (refer to *Figure 12*).

The protection and the EN\FAULT outputs are released when the IC temperature returns below a safe operating value ($T_{jSD}$ - $T_{jSD,Hyst}$).

**Figure 12. Thermal shutdown management**
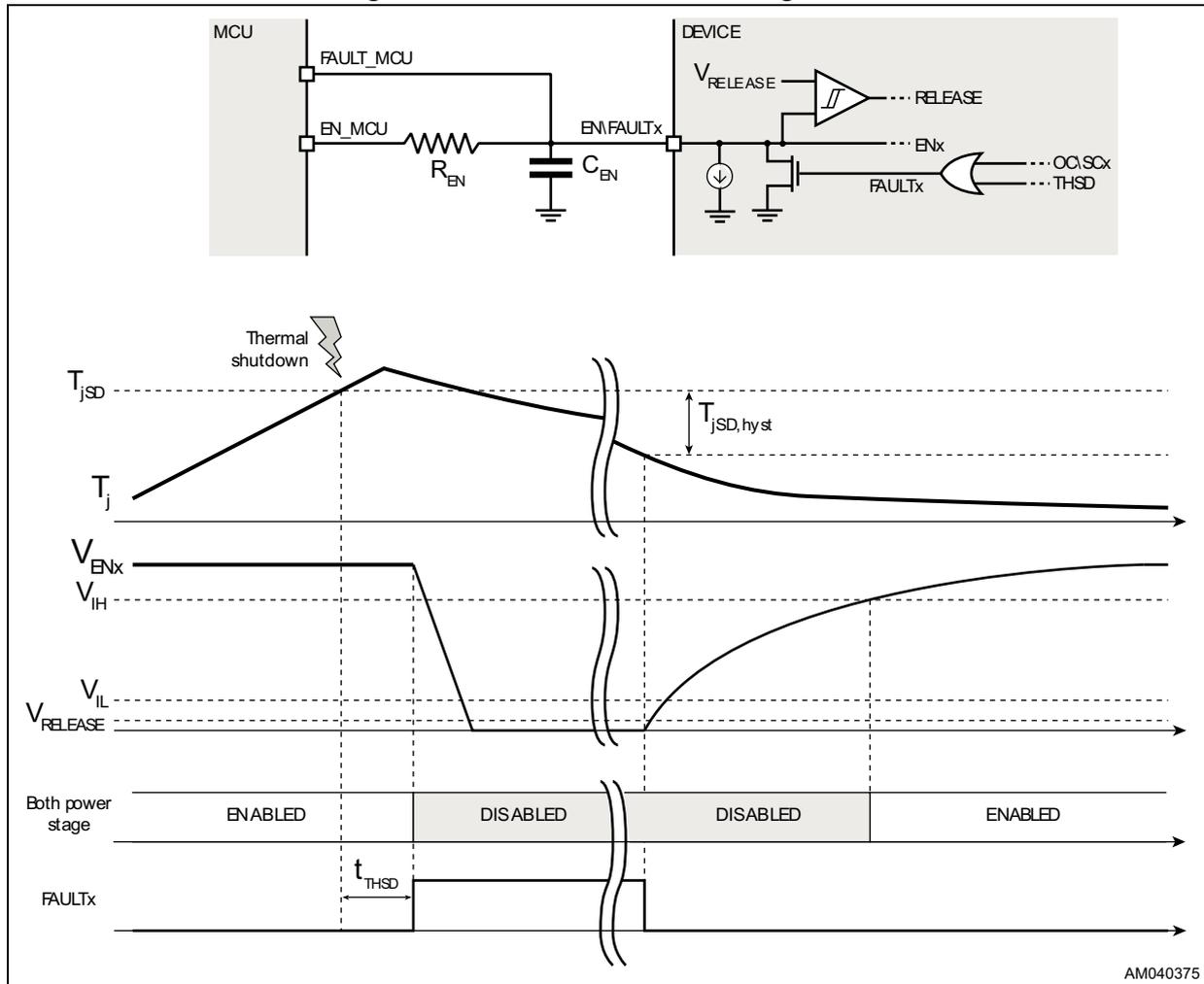


## 5.4.3 Blanking time

The device provides a blanking time $t_{BLANK}$ after each power MOSFET commutation to prevent false triggering of protections and current control.

During blanking time the following circuits are inhibited:

- Overcurrent and short-circuit protections of commutating power stage
- Current control comparator of the commutating power stage
- Thermal protection of the commutating power stage.

## 5.5 ESD protection strategy

**Figure 13. ESD protection strategy**
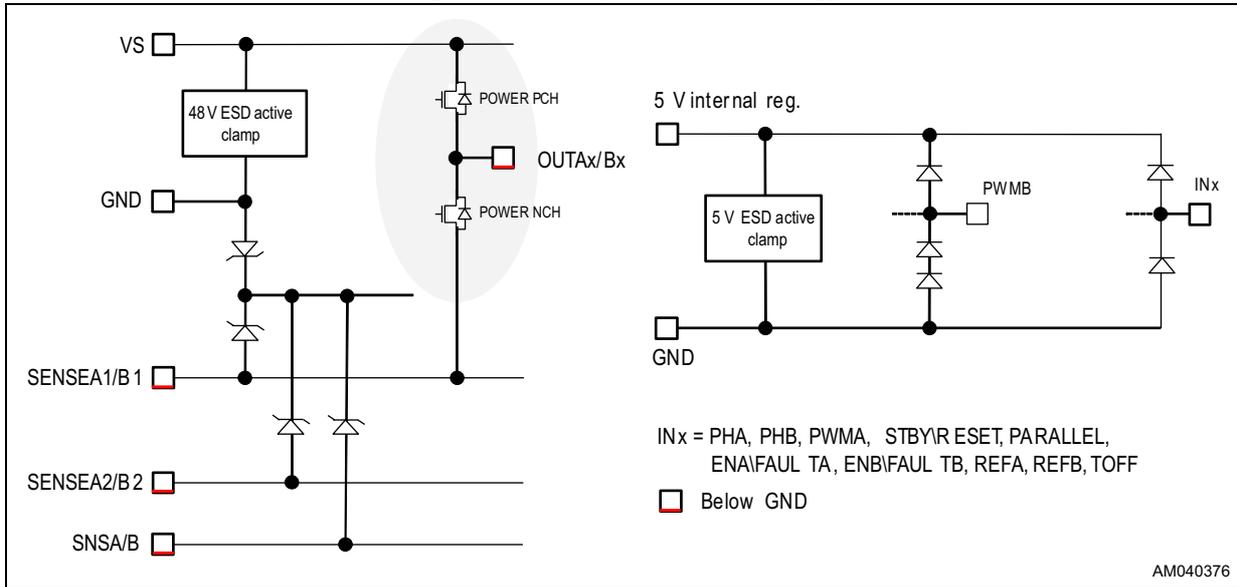
# 6        Typical applications

Table 9. Typical application values

| Name | Value |
|------|-------|
| $C_S$ | 330 nF |
| $C_{SPOL}$ | 33 µF |
| $R_{SNSA}$, $R_{SNSB}$ | 330 mΩ / 1 W |
| $C_{ENA}$, $C_{ENB}$ | 10 nF |
| $R_{ENA}$, $R_{ENB}$ | 39 kΩ |
| $C_{STBY}$ | 1 nF |
| $R_{STBY}$ | 18 kΩ |
| $R_{OFF}$ | 10 kΩ ($T_{OFF} \cong 13$ µs) |

Figure 14. Typical application schematic
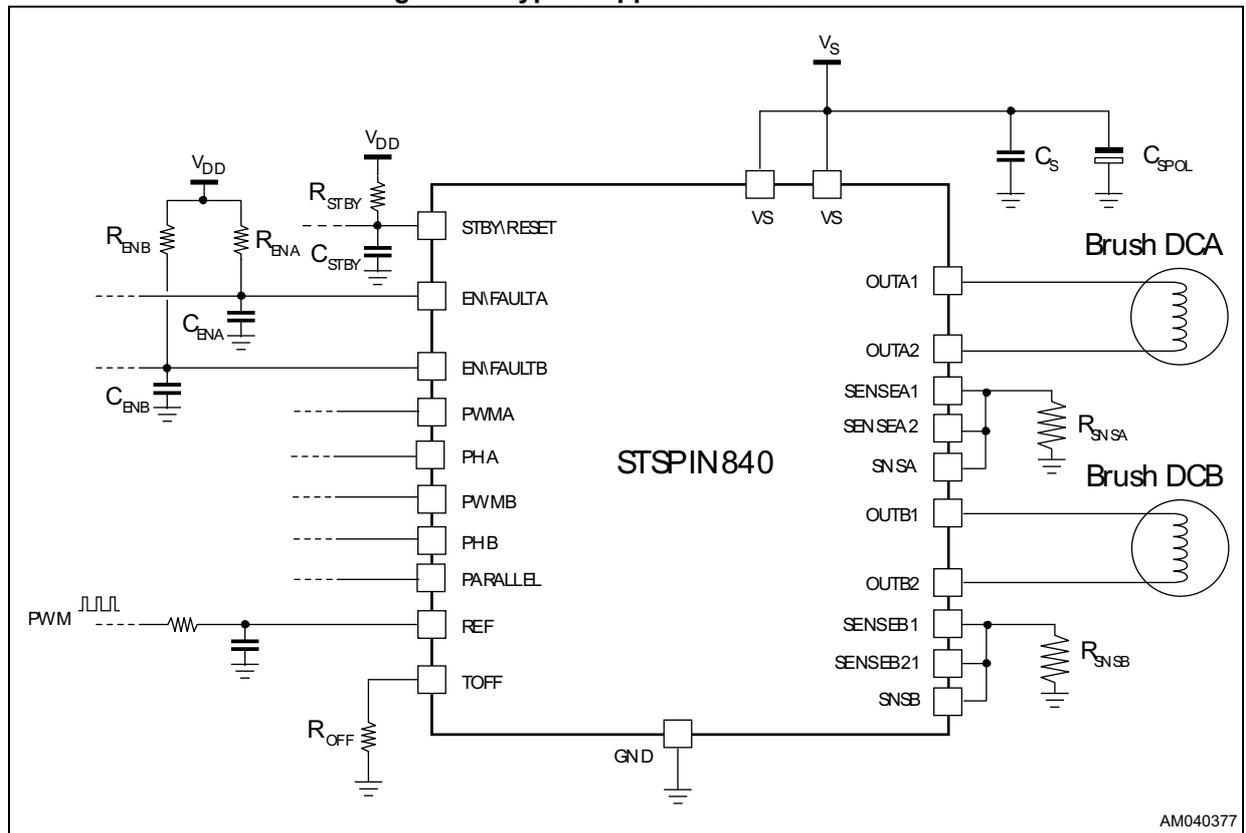
# 7 Layout recommendations

The STSPIN840 device integrates the power stage; in order to improve the thermal dissipation, the exposed pad must be connected to the ground plane on the bottom layer using multiple vias equally spaced. This ground plane acts as a heatsink, for this reason it should be as wide as possible.

The voltage supply $V_S$ must be stabilized and filtered with a ceramic bypass capacitor, typically 330 nF. It must be placed on the same side and as close as possible to the $V_S$ pin in order to reject high frequency noise components on the supply. A bulk capacitor could also be required (typically a 33 $\mu$F). The connection between the power supply connector and the $V_S$ pins must be as short as possible using wide traces.

In order to ensure the best ground connection between the STSPIN840 and the other components, a GND plane surrounding the device is recommended.

A capacitor between REF pins and ground should be positioned as near as possible to the device in order to filter the noise and stabilize the reference voltage.

Several vias should be positioned as near as possible each sense resistor connecting them to the ground plane on the bottom layer. In this way, both the GND planes provide a path for the current flowing into the power stage.

The path between the ground of the shunt resistors and the ceramic bypass capacitor of the device is critical; for this reason it must be as short as possible minimizing parasitic inductances that can cause voltage spikes on SENSE and OUT pins.

The OUT pins and the VS nets can be routed using the bottom layer, it is recommended to use two vias for output connections.

**Figure 15. PCB layout example (top layer)**
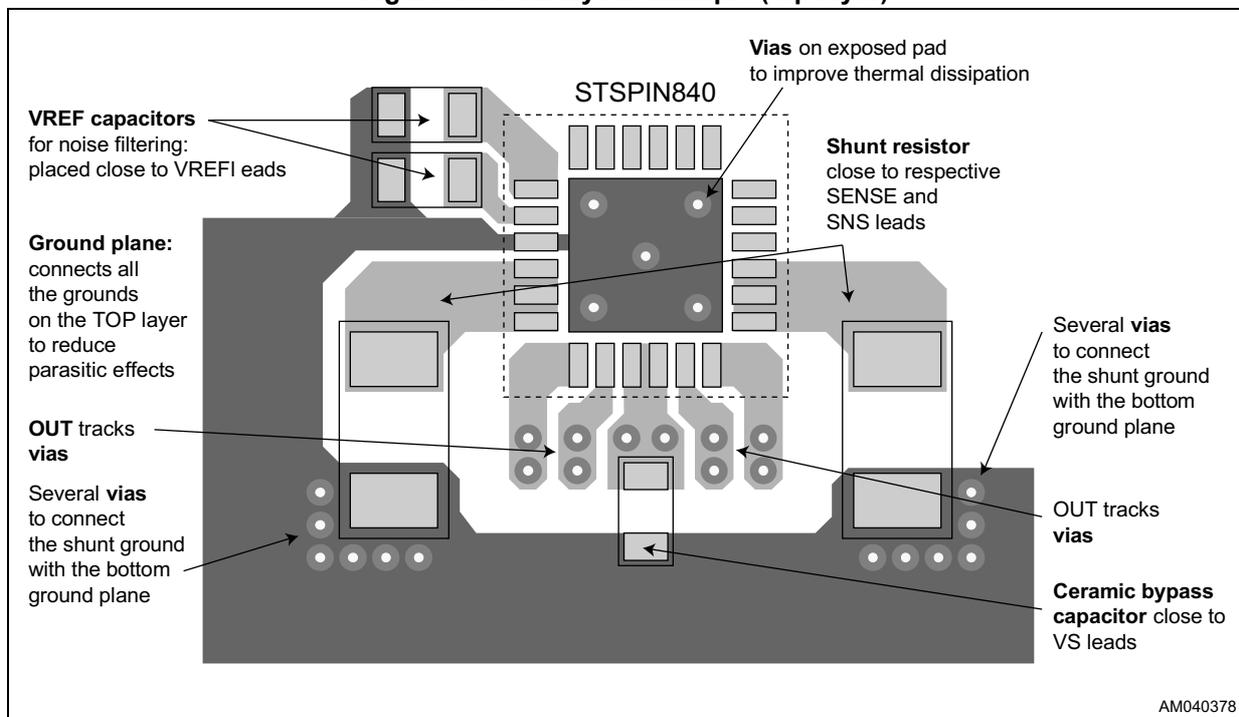
# 8       Package information

In order to meet environmental requirements, ST offers these devices in different grades of
ECOPACK® packages, depending on their level of environmental compliance. ECOPACK®
specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

## 8.1      TFQFPN TFQFPN 4 x 4 x 1.05 - 24 L package information
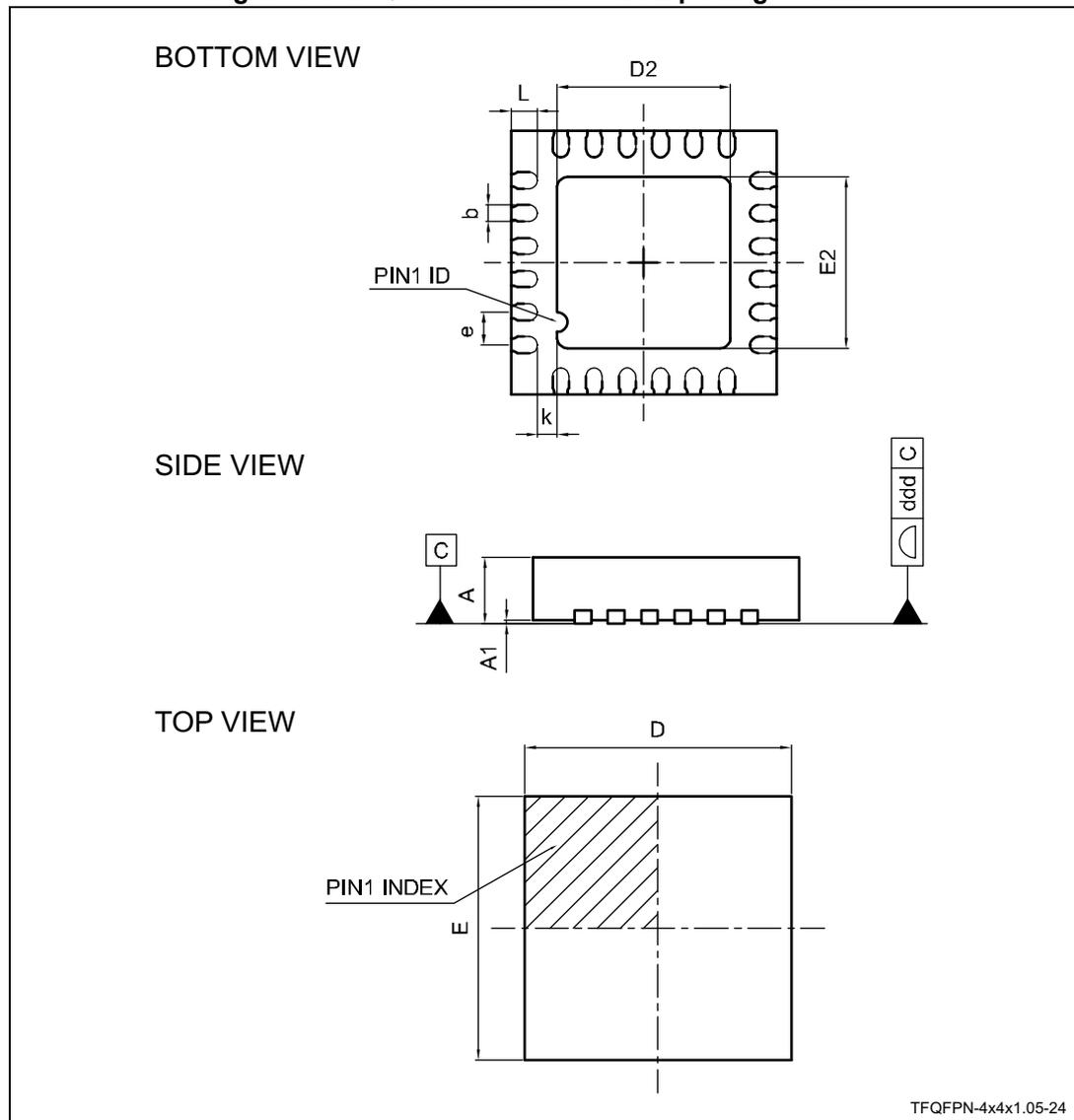
**Figure 16. TFQFPN 4 x 4 x 1.05 - 24 L package outline**

**Table 10. TFQFPN 4 x 4 x 1.05 - 24 L package mechanical data**

| Symbol | Dimensions (mm) | | | Note |
|--------|------|------|------|------|
| | Min. | Typ. | Max. | |
| A | 0.90 | 1.00 | 1.10 | - |
| A1 | 0.00 | 0.02 | 0.05 | - |
| b | 0.20 | 0.25 | 0.30 | (1) |
| D | 3.90 | 4.00 | 4.10 | - |
| D2 | 2.55 | 2.60 | 2.65 | - |
| E | 3.90 | 4.00 | 4.10 | - |
| E2 | 2.55 | 2.60 | 2.65 | - |
| e | - | 0.50 | - | - |
| L | 0.35 | 0.40 | 0.45 | |
| k | - | 0.30 | - | - |
| ddd | - | 0.05 | - | - |

1. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" dimension by more than 0.08 mm.

**Figure 17. TFQFPN 4 x 4 x 1.05 - 24 L suggested footprint**
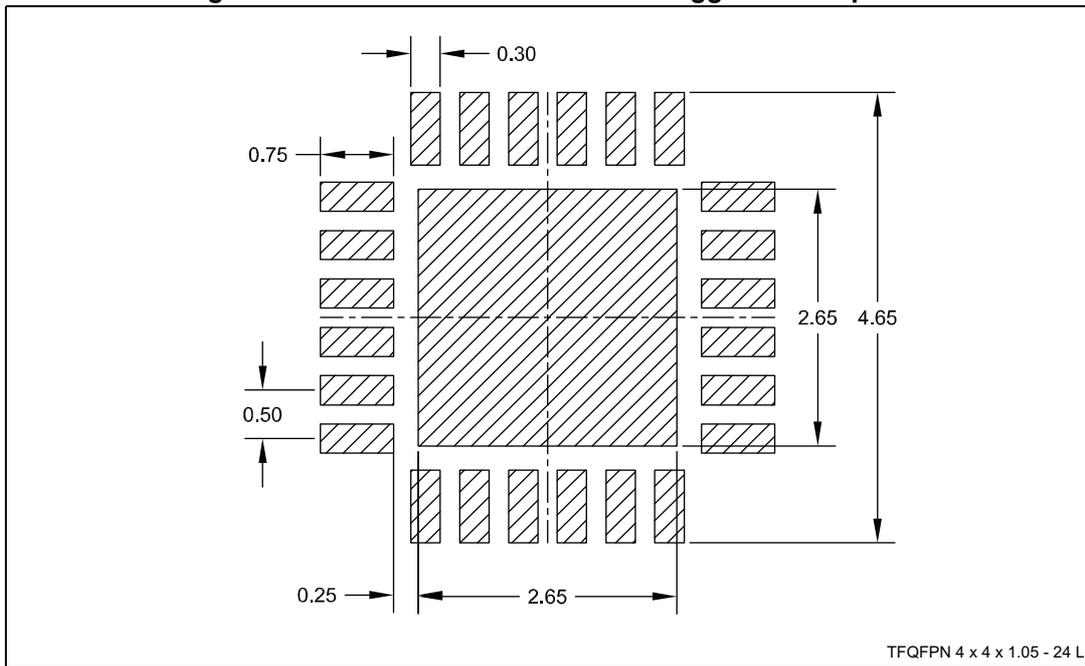
# 9     Ordering information

**Table 11. Device summary**

| Order code | Package | Packaging |
|------------|---------|-----------|
| STSPIN840 | TFQFPN 4 x 4 x 1.05 - 24 L | Tape and reel |

# 10     Revision history

**Table 12. Document revision history**

| Date | Revision | Changes |
|------|----------|---------|
| 18-May-2018 | 1 | Initial release. |

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**