

M5M5408AFP,TP,RT-55L, -70L,-10L -55LL,-70LL,-10LL

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5408A is a 4,194,304-bit CMOS Static RAM organized as 524,288-word by 8-bit. This device is fabricated using Mitsubishi's high-performance silicon-gate CMOS technology. This state-of-the-art process technology, combined with innovative circuit design techniques, yields high-density and low-power devices. The M5M5408A is suitable for memory applications where high reliability, large storage, simple interfacing and battery back-up are important design objectives.

The M5M5408A is available in 32-pin plastic SOP (M5M5408AFP), 32-pin plastic normal-lead-bend TSOP (M5M5408ATP) and 32-pin plastic reverse-lead-bend TSOP (M5M5408ART) packages. Two types of TSOP's are suitable for Surface Mounting on double-sided printed circuit boards.

FEATURES

Type name	Access time (max.)	Power supply current	
		Active (max.)	Stand-by (max.)
M5M5408AFP, TP, RT -55L	55ns		100μA
M5M5408AFP, TP, RT -70L	70ns	30mA	(V _{cc} =5.5V*)
M5M5408AFP, TP, RT -10L	100ns	(1MHz)	
M5M5408AFP, TP, RT -55LL	55ns		20μA
M5M5408AFP, TP, RT -70LL	70ns	30mA	(V _{cc} =5.5V*)
M5M5408AFP, TP, RT -10LL	100ns	(1MHz)	0.4μA
			(V _{cc} =3V**)

* at 70°C / **at 25°C

- Single +5V power supply
- No clocks, No refresh
- All inputs and outputs are TTL compatible.
- Easy memory expansion and power down by S
- Data retention supply voltage=2.0V to 5.5V
- Three-state outputs: OR-tie capability
- OE prevents data contention in the I/O bus
- Common Data I/O
- Battery backup capability
- Small stand-by current.....0.4μA (typical)
- Package

M5M5408AFP : 32 pin 525 mil SOP

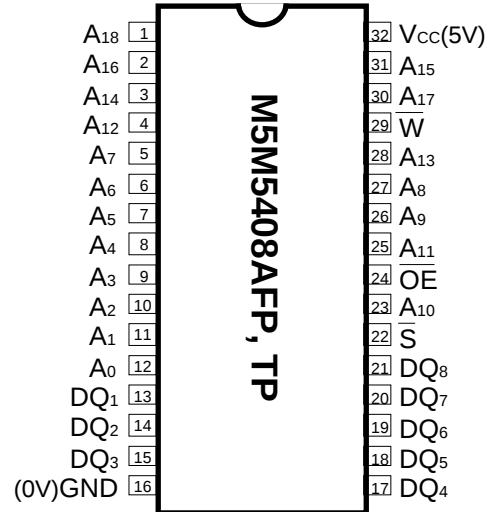
M5M5408ATP : 32 pin 400 mil TSOP(II)

M5M5408ART : 32 pin 400 mil TSOP(II)

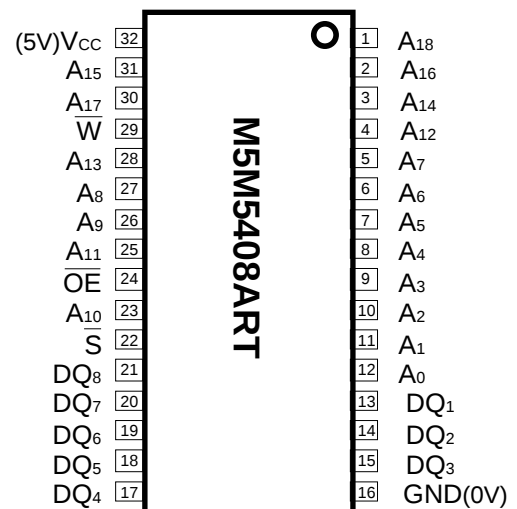
APPLICATION

Small capacity memory units
IC card
Battery operating system

PIN CONFIGURATION (TOP VIEW)



Outline 32P2M-A (AFP)
32P3Y-H (ATP)



Outline 32P3Y-J (ART)

PIN DISCRIPTION

A0 A18: ADDRESS INPUTS
DQ1..... DQ8: DATA INPUTS & OUTPUTS
S: CHIP SELECT INPUT
W: WRITE ENABLE INPUT
OE: OUTPUT ENABLE INPUT
V_{cc}: Power supply
GND: Ground

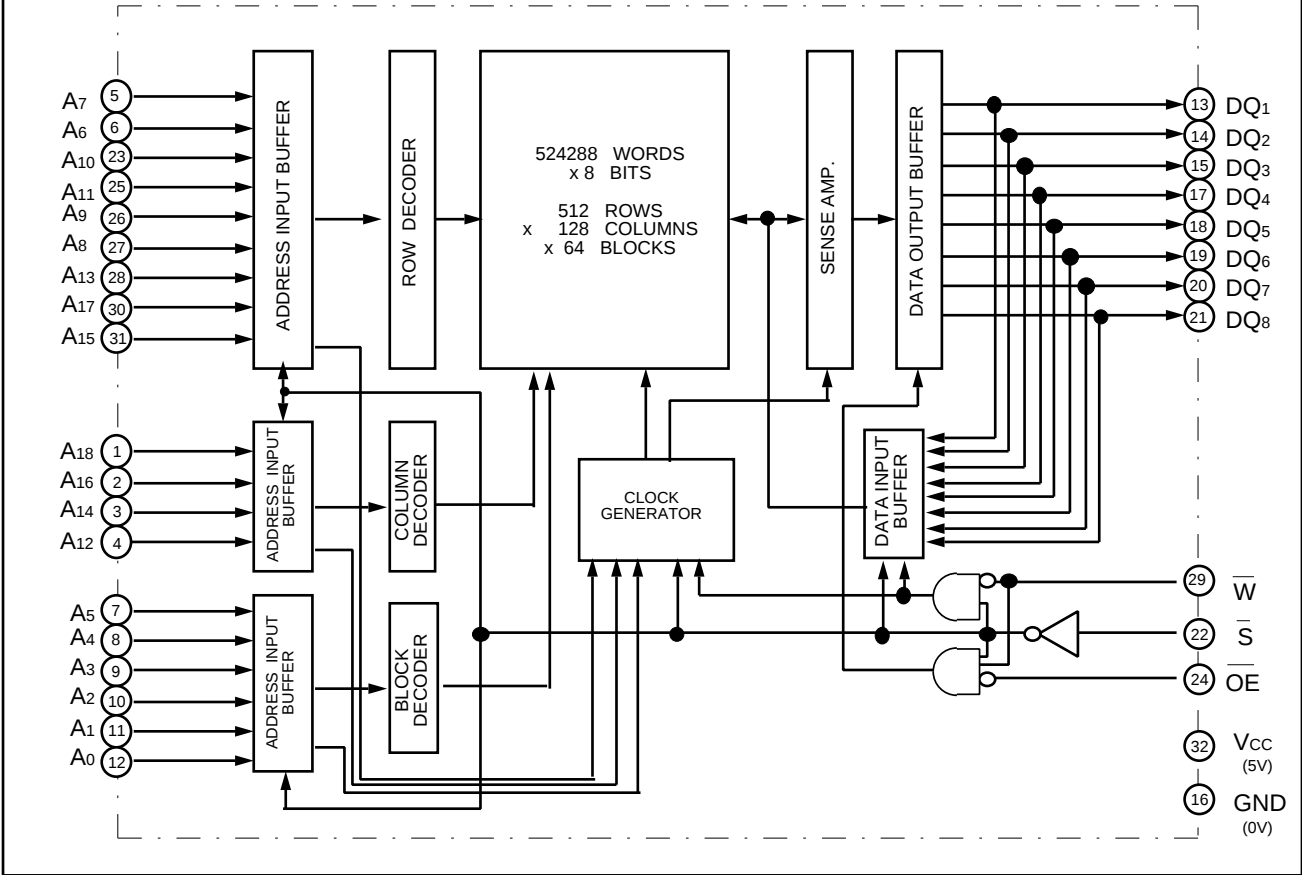


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BLOCK DIAGRAM



FUNCTION

The operation mode of the M5M5408A is determined by a combination of the device control inputs S, W and OE. Each mode is summarized in the truth table.

A write cycle is executed whenever the low level W overlaps with the low level S. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of W or S, whichever occurs first, requiring the set-up and hold time relative to these edges to be maintained. The output enable OE directly controls the output stage. Setting the OE at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting W at a high level and OE at a low level while S is in an active state (S=L).

When setting S at a high level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by S. The power supply current is reduced as low as the stand-by current which is specified as I_{cc3} or I_{cc4}, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

TRUTH TABLE

S	W	OE	Mode	DQ	I _{cc}
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	Data input	Active
L	H	L	Read	Data output	Active
L	H	H	Read	High-impedance	Active



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage	With respect to GND	- 0.3 ~ 7	V
V _i	Input voltage		- 0.3* ~ V _{cc} + 0.3	V
V _o	Output voltage		0 ~ V _{cc}	V
P _d	Power dissipation	T _a =25°C	700	mW
T _{opr}	Operating temperature		0 ~ 70	°C
T _{stg}	Storage temperature		-65 ~ 150	°C

* -3.0V in case of AC (Pulse width £ 50ns)

DC ELECTRICAL CHARACTERISTICS (T_a=0 - 70°C, V_{cc}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{IH}	High-level input voltage		2.2		V _{cc} +0.3	V
V _{IL}	Low-level input voltage		-0.3*		0.8	V
V _{OH}	High-level output voltage	I _{OH} = - 1mA	2.4			V
		I _{OH} = - 0.1mA	V _{cc} -0.5			V
V _{OL}	Low-level output voltage	I _{OL} = 2 mA			0.4	V
I _i	Input leakage current	Inputs = 0 ~ V _{cc}			±1	µA
I _o	Output leakage current	$\bar{S}$ = V _{IH} $\overline{OE}$ = V _{IH} , DQ=0 ~ V _{cc}			±1	µA
I _{cc1}	Active supply current (AC, MOS-level)	$\bar{S}$ £ 0.2 Other inputs £ 0.2V or ≥V _{cc} -0.2V DQ = open (duty 100%)	minimum cycle	50	80	mA
			1MHz	25	30	
I _{cc2}	Active supply current (AC, TTL-level)	$\bar{S}$ = V _{IL} Other inputs = V _{IH} or V _{IL} DQ = open (duty 100%)	minimum cycle	60	90	mA
			1MHz	30	40	
I _{cc3}	Stand-by current	$\bar{S}$ V _{cc} - 0.2V, Other inputs = 0 ~ V _{cc}	-L version		100	µA
			-LL version	1	20	µA
I _{cc4}	Stand-by current	$\bar{S}$ = V _{IH} , other inputs=0 ~ V _{cc}			3	mA

* -3.0V in case of AC (Pulse width £ 50ns)

CAPACITANCE (T_a=0 - 70°C, V_{cc}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
C _i	Input capacitance	V _i = GND, V _i = 25mV rms, f = 1MHz			6	pF
C _o	Output capacitance	V _o = GND, V _o = 25mV rms, f = 1MHz			8	pF

Note1. Direction for current flowing into IC is indicated as positive value.

2. Typical value is for T_a=25°C and V_{cc}=5.0V

3. C_i and C_o are random samples ,not production tested.



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AC ELECTRICAL CHARACTERISTICS (Ta=0 - 70°C, Vcc=5V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse $V_{IH}=2.4V$, $V_{IL}=0.6V$ (AFP,TP,RT-70L,-10L,-70LL,-10LL)
 $V_{IH}=3.0V$, $V_{IL}=0V$ (AFP,TP,RT-55L,-55LL)

Input rise and fall time5ns

Output reference level $V_{OH}=V_{OL}=1.5V$

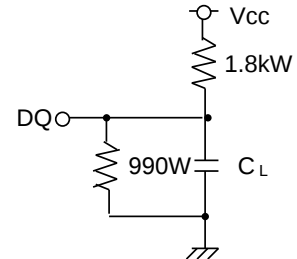
For t_{en} and t_{dis} , transition is measured ±500mV from steady state voltage

Output loads Show in Fig. 1;

$C_L=100pF$ (AFP,TP,RT-70L,-10L,-70LL,-10LL)

$C_L=30pF$ (AFP,TP,RT-55L,-55LL)

$C_L=5pF$ (for t_{en}, t_{dis})



C_L Includes jig and scope capacitance

Fig.1 Output load

(2) READ CYCLE

Symbol	Parameter	Limits						Unit
		M5M5408AFP,TP,RT		M5M5408AFP,TP,RT		M5M5408AFP,TP,RT		
		-55L, -55LL		-70L, -70LL		-10L, -10LL		
		Min.	Max.	Min.	Max.	Min.	Max.	
tCR	Read cycle time	55		70		100		ns
ta(A)	Address access time		55		70		100	ns
ta(S)	Chip select access time		55		70		100	ns
ta(OE)	Output enable access time		25		35		50	ns
tdis(S)	Output disable time after S high		20		25		35	ns
tdis(OE)	Output disable time after OE high		20		25		35	ns
ten(S)	Output enable time after S low	10		10		10		ns
ten(OE)	Output enable time after OE low	5		5		5		ns
tv(A)	Data valid time after address change	10		10		10		ns

Symbol	Parameter	Limits						Unit
		M5M5408AFP,TP,RT		M5M5408AFP,TP,RT		M5M5408AFP,TP,RT		
		-55L, -55LL		-70L, -70LL		-10L, -10LL		
		Min.	Max.	Min.	Max.	Min.	Max.	
tCW	Write cycle time	55		70		100		ns
tw(W)	Write pulse width	40		50		60		ns
tsu(A)	Address set up time	0		0		0		ns
tsu(A-WH)	Address set up time with respect to W high	50		60		80		ns
tsu(S)	Chip select set up time	50		60		80		ns
tsu(D)	Data set up time	25		30		35		ns
th(D)	Data hold time	0		0		0		ns
trec(W)	Write recovery time	0		0		0		ns
tdis(W)	Output disable time after W low		20		25		35	ns
tdis(OE)	Output disable time after OE high		20		25		35	ns
ten(W)	Output enable time after W high	5		5		5		ns
ten(OE)	Output enable time after OE low	5		5		5		ns



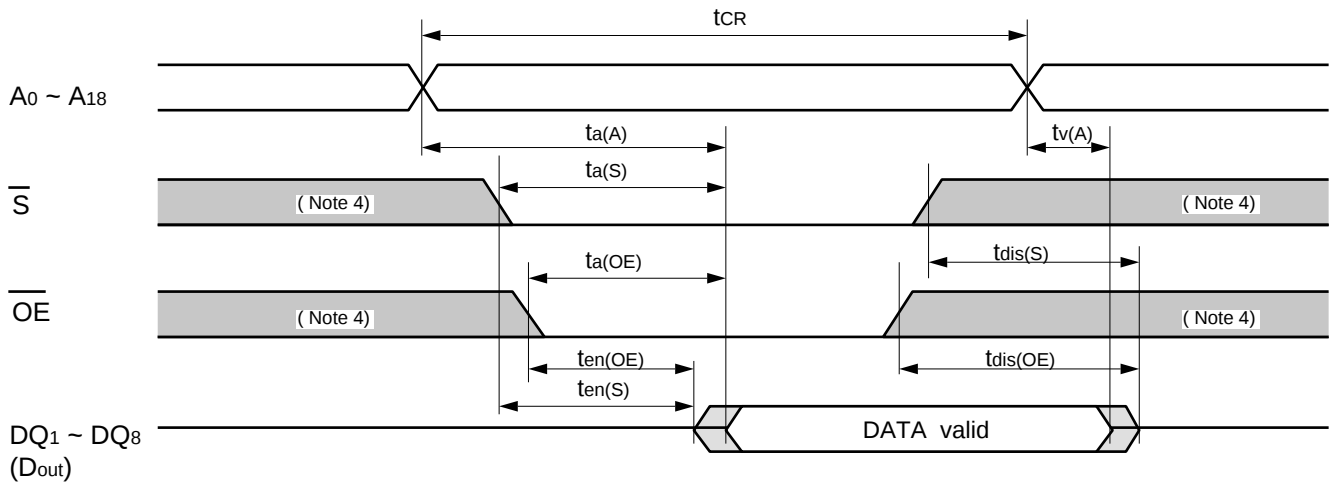
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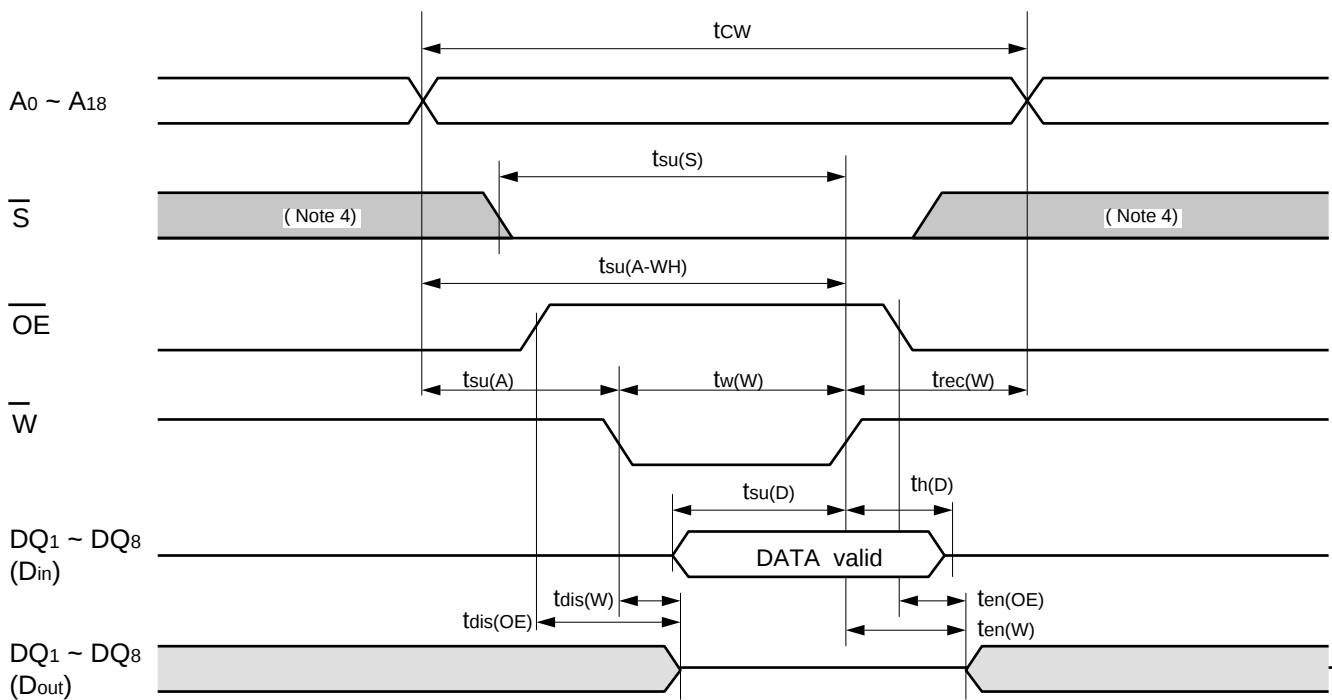
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(4) TIMING DIAGRAMS

Read cycle



Write cycle (WE control mode)

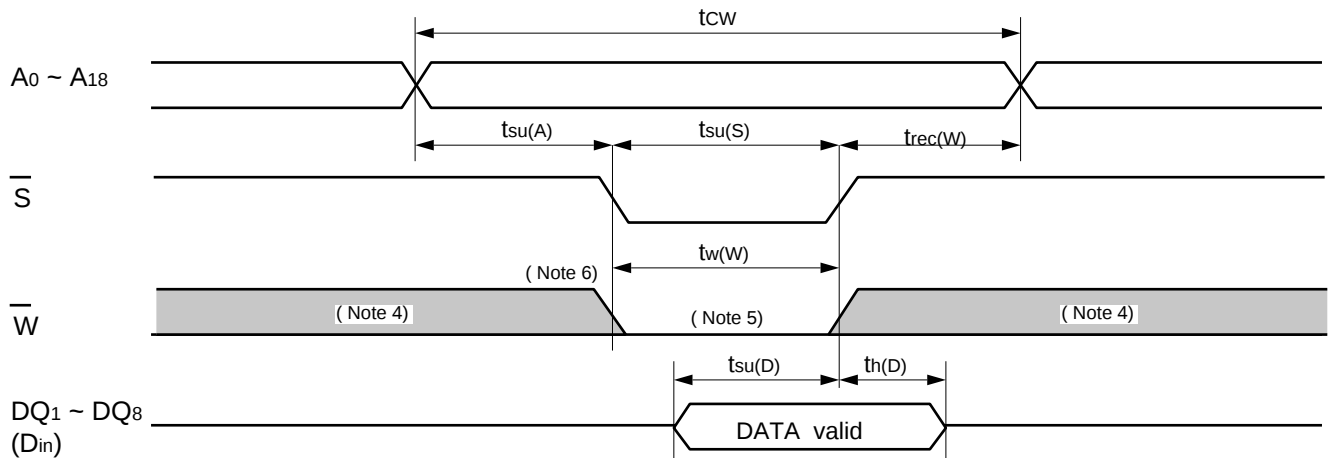


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Write cycle ($\overline{S}$ control mode)



Note 4: Hatching indicates the state is "don't care".

5: A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.

6: If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high-impedance state.

7: Don't apply inverted phase signal externally when DQ pin is in output mode.



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POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{cc} (PD)	Power down supply voltage		2			V
V _i (S)	Chip select input S	V _{cc} (PD) ≥ 2.2V	2.2			V
		2.2V ≥ V _{cc} (PD) ≥ 2.0V		V _{cc} (PD)		V
I _{cc} (PD)	Power down supply current	V _{cc} =3V, S ≥ V _{cc} -0.2V, other inputs = 0 ~ 3V	-L version		50	μA
			-LL version	0.4	10*	μA

* I_{cc} (PD) = 1μA at Ta=25°C

(2) TIMING REQUIREMENTS (Ta=0 - 70°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
t _{su} (PD)	Power down set up time		0			ms
t _{rec} (PD)	Power down recovery time		5			ms

(3) TIMING DIAGRAM

$\bar{S}$ control mode

