



NOVATEK
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Data Sheet

NT35410

One-chip Driver IC with internal GRAM
for 16.77M colors 360 RGB x 640 dot TFT LCD
with CPU / RGB / MIPI / MDDI interface

V2.0

2011/10/06

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REVISION HISTORY

Version	Contents	Prepared by	Checked by	Approved by	Date
1.0	Original	Steven Chen	Eric Tsai	Dennis Kuo	2011/09/02
2.0	-Add MDDI application reference circuit (page447) -Modify the power on sequence, power up/down can be any order (page226-228)	Steven Chen	Eric Tsai	Dennis Kuo	2011/10/6

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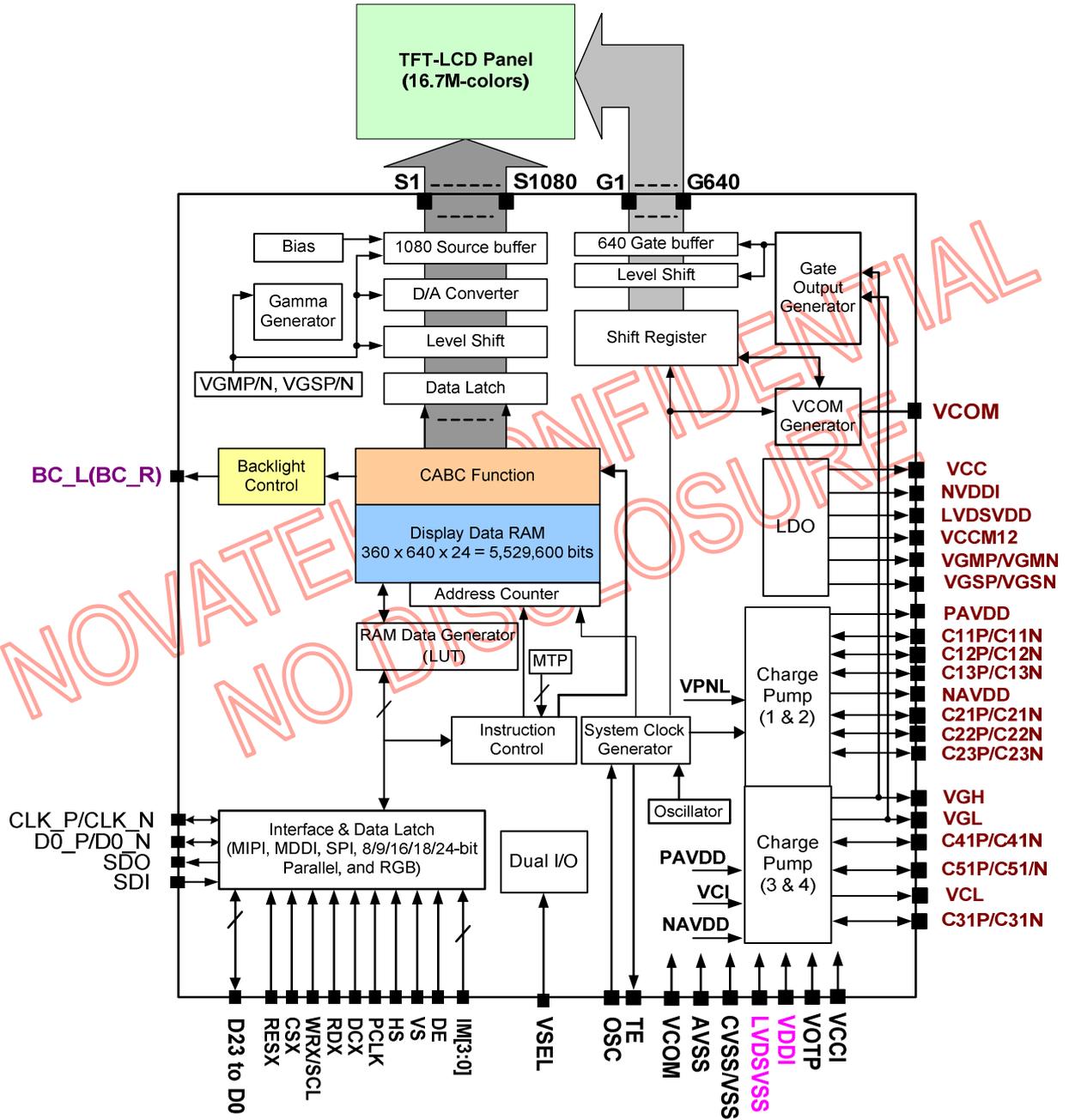
1 DESCRIPTION

NT35410 is a single chip low power CMOS LCD controller/driver for color TFT-LCD displays of 640 gates and 360xRGB columns. It has a 5.52M-bit (360 x 24bit x 640) display RAM and a full set of control functions. NT35410 offers 16 kinds microprocessor interfaces: 8080-system (8-bit, 9-bit, 16-bit, 18-bit, 24-bit), MIPI interface, MDDI interface, serial (3-pin or 4-pin) and RGB (16-bit, 18-bit, 24-bit) mode1, 2 interface.

2 FEATURES

- ◆ Single chip AM-TFT-LCD Controller/ driver with Display RAM.
- ◆ Display resolution : (programmable and s/w setting)
 - 320*RGB (H) *480(V)
 - 360*RGB (H) *480(V)
 - 360*RGB (H) *640(V)
- ◆ Operation Frequency:
 - MIPI interface: 500Mbps/Channel
 - MDDI interface: 400Mbps/Channel
 - 80-series MPU interface (WRX): 27MHz
 - RGB interface (PCLK): 30Mhz
 - SPI (SCL): 27MHz
- ◆ Display data RAM (frame memory): 360 x 640 x 24-bit = 5,529,600bit
- ◆ Output:
 - 1080ch source outputs (360xRGB)
 - 640 gate outputs
 - Common electrode output
- ◆ Display mode (Color mode)
 - Full color mode (Idle mode off): 16.7M-colors, 262k-colors, 65k-colors
 - Reduce color mode (Idle mode on): 8-colors (3-bit binary mode)
- ◆ Color modes on the display host interface:
 - 16-bit/Pixel: RGB= (565) using the 2488k-bit frame memory
 - 18-bit/Pixel: RGB= (666) using the 2488k-bit frame memory
 - 24-bit/Pixel: RGB= (888) using the 2488k-bit frame memory
- ◆ Interface:
 - 3-pin / 4-pin serial interface
 - 8-bit, 9-bit, 16-bit, 18-bit, 24-bit interface with 8080-series MCU
 - 16-bit, 18-bit, 24-bit RGB interface Mode 1 (DE + SYNC mode) and Mode 2 (SYNC only mode)
 - MIPI interface (1 clock and 1 data lane pairs, DSI V1.01 r11 and D-PHY V1.00.00)
 - Mobile Display Digital Interface (MDDI 1.2-Type1)
- ◆ Display features
 - Area scrolling
 - Partial display mode
 - Software programmable color depth mode
- ◆ Content Adaptive Backlight Control (CABC) Function
 - Histogram analysis & data process
 - Moving picture auto-detect mode.(UI or still picture mode decided by host)
 - Dimming control
 - 2 level PWM control line for the Display Backlight
- ◆ On chip
 - DC/DC converter
 - DC VCOM voltage generator

- Separate RGB gamma control
- Provide 4 times MTP to store VCOM and ID setting
- Oscillator for display clock generation
- ◆ NV Memory (4-times on each function)
 - 8-bits for User ID1
 - 8-bits for User ID2
 - 8-bits for User ID3
 - 8-bits for VCOM adjustment
- ◆ Driving Algorithm
 - 2 level gate drive with common electrode modulation drive
 - Support 1dot inversion , 2dot inversion, column inversion, zigzag inversion driving
- ◆ Supply voltage range
 - Analog supply voltage range for VPNL to AVSS: 2.3V to 4.8V
 - I/O supply voltage range for VDDI to VSS: 1.65V to 4.8V
 - MIPI supply voltage range for VCCL to VSS: 2.3 to 4.8V
- ◆ Output voltage levels
 - Positive Power supply for driver circuit range(PAVDD): $PAVDD-VSS = 5.9V$ to $6.5V$
 - Negative Power supply for driver circuit range(NAVDD): $NAVDD-VSS = -5.9V$ to $-6.5V$
 - Positive polarity Source output high voltage level: $VGMP = 3.5V$ to $5.9V$ ($PAVDD-VGMP > 0.25$)
 - Negative polarity Source output high voltage level: $VGMP = -3.5V$ to $-5.5V$ ($NAVDD-VGMP < -0.25$)
 - Positive polarity Source output low voltage level: $VGSP = 0.2V$ to $2.2V$ ($PAVDD-VGSP > 0.25$)
 - Negative polarity Source output low voltage level: $VGSP = -0.2V$ to $-2.2V$ ($NAVDD-VGSP < -0.25$)
 - Common electrode output voltage level: $VCOM = -0.2V$ to $-2.3V$ ($VCL-VCOM < -0.25$)
 - Positive gate driver output voltage level: $VGH-VSS = 7.0V$ to $15.0V$
 - Negative gate driver output voltage level: $VGL-AVSS = -15.0V$ to $-7.0V$
- ◆ Lower power consumption, suitable for battery operated systems
 - CMOS compatible inputs
 - Optimized layout for COG assembly
- ◆ HBM ESD (Handling body mode) $> \pm 3KV$, MM (machinery mode) $> \pm 300V$

3 BLOCK DIAGRAM


4 PIN DESCRIPTION

4.1 POWER SUPPLY PINS

Symbol	Name	Description
VPNL	Power	Power supply for Analog block, and booster
VPNL_DET	Power	Power supply for Analog block, and booster
VDDI	Power	Power supply for I/O Pad VDDI=1.65V~4.8V or 1.1V~1.3V, depends on VSEL and DSTB_SEL setting
DIOPWR	LDO Output	DIOPWR output is for 1.2V or 1.8V application. DIOPWR is controlled by VSEL.
VCC	LDO Output	Internal logic regulator output for logic circuit usage. Connect a capacitor for stabilization.
NVDDI	LDO Output	Negative Voltage level generated from VCC Connect a capacitor for stabilization.
VCCI	Input	Using to generate VCC, please connect to VPNL.
LVDSVDD	MIPI Voltage	Regulator output for internal MIPI / MDDI analog system (1.5V typical) Connect a capacitor for stabilization.
VCCM12	MIPI Voltage	Regulator output for internal MIPI low power system (1.2V typical) Connect a capacitor for stabilization.
VSS	Digital GND	System ground for digital system
CVSS	DC/DC GND	System ground for booster system
AVSS	Analog GND	System ground for Analog system
LVDSVSS	MIPI GND	System ground for internal MIPI analog system

4.2 MODE SELECTION PINS

Symbol	I/O	Description	
IM[3:0]	I	Interface type selection	
		IM[3:0]	Interface selection
		0000	80-series 8-bit MPU interface
		0001	80-series 9-bit MPU interface
		0010	80-series 16-bit MPU interface
		0011	80-series 18-bit MPU interface
		0100	80-series 24-bit MPU interface
		1100	3-SPI
		1101	4-SPI
		1001	RGB mode + 3-SPI
		1110	MIPI interface
		1111	MDDI interface with 3-SPI

NOTE: "1" = VDDI level, "0" = VSS level.

4.3 INTERFACE LOGIC PINS

Symbol	I/O	Description																																								
RESX	I	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low. The input voltage range for RESX pin is related to DSTB_SEL and VSEL pins.																																								
		<table border="1"> <thead> <tr> <th colspan="2">Input Voltage Level (DSTB_SEL="0")</th> <th>Min.</th> <th>Max.</th> <th>Unit</th> </tr> </thead> <tbody> <tr> <td rowspan="2">VDDI=1.65~4.8V</td> <td>Logic High level input voltage</td> <td>0.7xVDDI</td> <td>VDDI</td> <td>V</td> </tr> <tr> <td>Logic Low level input voltage</td> <td>VSS</td> <td>0.3xVDDI</td> <td>V</td> </tr> </tbody> </table>	Input Voltage Level (DSTB_SEL="0")		Min.	Max.	Unit	VDDI=1.65~4.8V	Logic High level input voltage	0.7xVDDI	VDDI	V	Logic Low level input voltage	VSS	0.3xVDDI	V																										
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			Logic Low level input voltage	VSS	0.3xVDDI	V																																				
		<table border="1"> <thead> <tr> <th colspan="2">Input Voltage Level (DSTB_SEL="1")</th> <th colspan="2">VDDI=1.65~4.8V</th> <th colspan="2">VDDIL=1.1~1.3V</th> <th>Unit</th> </tr> <tr> <th></th> <th></th> <th>Min.</th> <th>Max.</th> <th>Min.</th> <th>Max.</th> <th></th> </tr> </thead> <tbody> <tr> <td rowspan="2">VSEL =High</td> <td>Logic High level input voltage</td> <td>0.7xVDDI</td> <td>VDDI</td> <td>1.155</td> <td>1.95</td> <td>V</td> </tr> <tr> <td>Logic Low level input voltage</td> <td>VSSI</td> <td>0.3xVDDI</td> <td>VSSI</td> <td>0.585</td> <td>V</td> </tr> <tr> <td rowspan="2">VSEL =Low</td> <td>Logic High level input voltage</td> <td>0.88</td> <td>1.35V</td> <td>0.88</td> <td>1.35V</td> <td>V</td> </tr> <tr> <td>Logic Low level input voltage</td> <td>VSSI</td> <td>0.55</td> <td>VSSI</td> <td>0.55</td> <td>V</td> </tr> </tbody> </table>	Input Voltage Level (DSTB_SEL="1")		VDDI=1.65~4.8V		VDDIL=1.1~1.3V		Unit			Min.	Max.	Min.	Max.		VSEL =High	Logic High level input voltage	0.7xVDDI	VDDI	1.155	1.95	V	Logic Low level input voltage	VSSI	0.3xVDDI	VSSI	0.585	V	VSEL =Low	Logic High level input voltage	0.88	1.35V	0.88	1.35V	V	Logic Low level input voltage	VSSI	0.55	VSSI	0.55	V
		Input Voltage Level (DSTB_SEL="1")		VDDI=1.65~4.8V		VDDIL=1.1~1.3V		Unit																																		
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VSEL =Low	Logic High level input voltage	0.88	1.35V	0.88	1.35V	V																																				
	Logic Low level input voltage	VSSI	0.55	VSSI	0.55	V																																				
CSX	I	Chip select input pin ("Low" enable) in 80-series MPU I/F and SPI I/F. If this pin is not used, please connect to VDDI.																																								
WRX (SCL)	I	Writes strobe signal to write data when WRX is "Low" in 80-series MPU I/F. Serial interface clock in SPI I/F. If this pin is not used, please connect to VDDI.																																								
RDX	I	Reads strobe signal to write data when RDX is "Low" in 80-series MPU interface. If this pin is not used, please connect to VDDI.																																								
DCX	I	Display data / command selection in 80-series MPU I/F. DCX = "0" : Command DCX = "1" : Display data or Parameter If this pin is not used, please connect to VDDI.																																								
SDI	I	Serial input signal in SPI I/F. The data is input on the rising edge of the SCL signal. This pin is not used for 80-series MPU I/F and MIPI I/F, please connect to VSS this pin.																																								
SDO	O	Serial output signal in SPI I/F. The data is output on the rising edge of the SCL signal. This pin is not used for 80-series MPU I/F and MIPI I/F, please connect to VSS this pin.																																								
D[23:0]	I/O	24-bit bi-directional data bus for 80-series MPU I/F and RGB I/F. For 8080-series MPU I/F: 8-bit interface: D[7:0] are used, D[23:8] should be connected to VSS 16-bit interface: D[15:0] are used, D[23:16] should be connected to VSS 18-bit interface: D[17:0] are used, D[23:18] should be connected to VSS 24-bit interface: D[23:0] are used For RGB I/F: 16-bit/pixel: D[21:17]=R[4:0], D[13:8]=G[5:0] and D[5:1]=B[4:0], connect unused pins to VSS 18-bit/pixel: D[21:16]=R[5:0], D[13:8]=G[5:0] and D[5:0]=B[5:0], connect unused pins to VSS 24-bit/pixel: D[23:16]=R[7:0], D[15:8]=G[7:0] and D[7:0]=B[7:0] These pins are not used for MIPI I/F, please connect to VSS these pins.																																								
PCLK	I	Pixel clock signal in RGB I/F. This pin is not used for 80-series MPU I/F and MIPI I/F, please connect to VSS this pin.																																								

VS	I	Vertical sync. Signal in RGB I/F. This pin is not used for 80-series MPU I/F and MIPI I/F, please connect to VSS this pin.
HS	I	Horizontal sync. Signal in RGB I/F. This pin is not used for 80-series MPU I/F and MIPI I/F, please connect to VSS this pin.
DE	I	Data enable signal in RGB I/F mode 1. This pin is not used for RGB mode 2, 80-series MPU I/F and MIPI I/F, please connect to VSS this pin.
TE_L(TE_R)	O	Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is output low. If not used, please open this pin. - TE_L & TE_R can't connect together, choose one side for application.
ERR	O	CRC and ECC error output pin for MIPI interface, activated by S/W command. This pin is output low when it is not activated. When this pin is activated, it output high if CRC/ECC error found. If not used, please open this pin.

NOTE: "1" = VDDI level, "0" = VSS level.

4.4 MIPI / MDDI INTERFACE PINS

Symbol	I/O	Description
CLK_P CLK_N	I	-If MIPI interface is selected (IM[3:0] = "1110"), these two pins are positive/negative polarity of MIPI differential clock signal. -If MDDI interface is selected (IM[3:0] = "1111"), these two pins are positive/negative polarity of MDDI differential strobe signal. The polarity of these two pins can be changed by command for MIPI / MDDI interface only. -If not used, please connect these pins to LVDSVSS. -If not used, please connect these pins to LVDSVSS.
D0_P D0_N	I/O	-If MIPI interface is selected (IM[3:0] = "1110"), these two pins are positive/negative polarity of MIPI differential data signal. -If MDDI interface is selected (IM[3:0] = "1111"), these two pins are positive/negative polarity of MDDI differential data signal. -The polarity of these two pins can be changed by command for MIPI / MDDI interface only. -If not used, please connect these pins to LVDSVSS.

4.5 CABC Control Pins

Symbol	I/O	Description																																																																		
BC_L(BC_R)	O	<ul style="list-style-type: none"> - This pin is connected to the external driver. - PWM type control signal for brightness of the LED backlight. - The width of this PWM signal is set in 256 steps from 0%(Low) to 100%(High). - If not used, please open this pin. - BC_L & BC_R can't connect together, choose one side for application. 																																																																		
VSEL	I	<p>- This pin is used to select the output level of signal for BC, TE, RESX.</p> <table border="1"> <thead> <tr> <th rowspan="2">DSTB_SEL</th> <th rowspan="2">VDDI</th> <th rowspan="2">VSEL</th> <th rowspan="2">DIOPWR</th> <th rowspan="2">TE_PWR_SEL (0xC1 CMD)</th> <th colspan="2">Output Voltage Level</th> </tr> <tr> <th>TE</th> <th>BC</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1.65~4.8V</td> <td>X</td> <td>Off</td> <td>X</td> <td>VOH=VDDI VOL=VSSI</td> <td>VOH=VDDI VOL=VSSI</td> </tr> <tr> <td rowspan="4">1</td> <td rowspan="4">1.65~1.95V</td> <td rowspan="2">Low</td> <td rowspan="2">1.2V</td> <td>0</td> <td>VOH=VDDI VOL=VSSI</td> <td>VOH=VDDI VOL=VSSI</td> </tr> <tr> <td>1</td> <td>VOH=1.2V(DIOPWR) VOL=VSSI</td> <td>VOH=VDDI VOL=VSSI</td> </tr> <tr> <td rowspan="2">High</td> <td rowspan="2">1.8V</td> <td>0</td> <td>VOH=VDDI VOL=VSSI</td> <td>VOH=VDDI VOL=VSSI</td> </tr> <tr> <td>1</td> <td>VOH=1.8V(DIOPWR) VOL=VSSI</td> <td>VOH=VDDI VOL=VSSI</td> </tr> <tr> <td rowspan="2">1</td> <td rowspan="2">1.1~1.3V</td> <td rowspan="2">Low</td> <td rowspan="2">1.2V</td> <td>0</td> <td>VOH=VDDI VOL=VSSI</td> <td>VOH=VDDI VOL=VSSI</td> </tr> <tr> <td>1</td> <td>VOH=1.2V(DIOPWR) VOL=VSSI</td> <td>VOH=VDDI VOL=VSSI</td> </tr> <tr> <td rowspan="2">1</td> <td rowspan="2">1.1~1.3V</td> <td rowspan="2">High</td> <td rowspan="2">1.8V</td> <td>0</td> <td>VOH=VDDI VOL=VSSI</td> <td>VOH=VDDI VOL=VSSI</td> </tr> <tr> <td>1</td> <td>VOH=1.8V(DIOPWR) VOL=VSSI</td> <td>VOH=VDDI VOL=VSSI</td> </tr> </tbody> </table> <p>The input voltage range for VSEL pin:</p> <table border="1"> <thead> <tr> <th>Input Voltage Level</th> <th>Min.</th> <th>Max.</th> <th>Unit</th> </tr> </thead> <tbody> <tr> <td>Logic High level input voltage</td> <td>0.88</td> <td>VDDI</td> <td>V</td> </tr> <tr> <td>Logic Low level input voltage</td> <td>VSSI</td> <td>0.55</td> <td>V</td> </tr> </tbody> </table> <p>If not used, please connect to VDDI.</p>	DSTB_SEL	VDDI	VSEL	DIOPWR	TE_PWR_SEL (0xC1 CMD)	Output Voltage Level		TE	BC	0	1.65~4.8V	X	Off	X	VOH=VDDI VOL=VSSI	VOH=VDDI VOL=VSSI	1	1.65~1.95V	Low	1.2V	0	VOH=VDDI VOL=VSSI	VOH=VDDI VOL=VSSI	1	VOH=1.2V(DIOPWR) VOL=VSSI	VOH=VDDI VOL=VSSI	High	1.8V	0	VOH=VDDI VOL=VSSI	VOH=VDDI VOL=VSSI	1	VOH=1.8V(DIOPWR) VOL=VSSI	VOH=VDDI VOL=VSSI	1	1.1~1.3V	Low	1.2V	0	VOH=VDDI VOL=VSSI	VOH=VDDI VOL=VSSI	1	VOH=1.2V(DIOPWR) VOL=VSSI	VOH=VDDI VOL=VSSI	1	1.1~1.3V	High	1.8V	0	VOH=VDDI VOL=VSSI	VOH=VDDI VOL=VSSI	1	VOH=1.8V(DIOPWR) VOL=VSSI	VOH=VDDI VOL=VSSI	Input Voltage Level	Min.	Max.	Unit	Logic High level input voltage	0.88	VDDI	V	Logic Low level input voltage	VSSI	0.55	V
DSTB_SEL	VDDI	VSEL						DIOPWR	TE_PWR_SEL (0xC1 CMD)	Output Voltage Level																																																										
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1	1.65~1.95V	Low	1.2V	0	VOH=VDDI VOL=VSSI	VOH=VDDI VOL=VSSI																																																														
				1	VOH=1.2V(DIOPWR) VOL=VSSI	VOH=VDDI VOL=VSSI																																																														
		High	1.8V	0	VOH=VDDI VOL=VSSI	VOH=VDDI VOL=VSSI																																																														
				1	VOH=1.8V(DIOPWR) VOL=VSSI	VOH=VDDI VOL=VSSI																																																														
1	1.1~1.3V	Low	1.2V	0	VOH=VDDI VOL=VSSI	VOH=VDDI VOL=VSSI																																																														
				1	VOH=1.2V(DIOPWR) VOL=VSSI	VOH=VDDI VOL=VSSI																																																														
1	1.1~1.3V	High	1.8V	0	VOH=VDDI VOL=VSSI	VOH=VDDI VOL=VSSI																																																														
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Input Voltage Level	Min.	Max.	Unit																																																																	
Logic High level input voltage	0.88	VDDI	V																																																																	
Logic Low level input voltage	VSSI	0.55	V																																																																	
DSTB_SEL	I	<p>DSTB_SEL is used to select Dual power on/off in deep standby mode. DSTB_SEL=1(default), Dual IO power on(DIOPWR) DSTB_SEL=0, Dual IO power off(DIOPWR)</p>																																																																		

4.6 Others

Symbol	I/O	Description
VOTP	I	- MTP programming power pin. Normal Operation: Keep the pin floating or connect to GND. - MTP Programming: Apply external power 7.5V to this pin
TEST1~TEST16	I	- Internal Test pad. Please open this pin for normal operation.
VDDI_O	O	- VDDI voltage output level for control pin used.
VSS_O	O	- VSS voltage output level for control pin used
DUMMY_GND[0~1] DUMMY_GND[2~3] DUMMY_GND[4~6] DUMMY_GND[7~11] DUMMY_GND[12~14] DUMMY_GND[15~16]	O	- These pins are dummy (No function inside), internal pull to ground.

4.7 DRIVER OUTPUT PINS

Symbol	I/O	Description
SDUM0~SDUM3	O	Liquid crystal application voltage output lines for Zigzag drive method. The shift direction of the segment signal output can be reversed by setting the Register SMX.
S1 to S1080	O	- Source driver output pins.
G1 to G640	O	- Gate driver output pins.

4.8 DC/DC CONVERTER PINS

Symbol	I/O	Description
VCOM	O	VCOM output voltage for DC VCOM mode. Connect a capacitor to stabilize output voltage
PAVDD	Power output	Positive Power supply to the source and VCOM drive. Connect a stabilizing capacitor.
NAVDD	Power output	Negative Power supply to the source and VCOM drive. Connect a stabilizing capacitor.
VGH	Power output	Output voltage from the step-up circuit, generated from PAVDD. Connect a capacitor for stabilization.
VGL/VGLO	Power output	Output voltage from the step-up circuit, generated from NAVDD. Connect a capacitor for stabilization. VGL and VGLO must be connected together.
VCL	Power output	Output voltage from the step-up circuit, generated from VPNL. Connect a capacitor for stabilization. VCL = - VPNL
C11P/C11N C12P/C12N C13P/C13N	Power	Capacitor connection pins for the step-up circuit 1 which generate PAVDD. Connect capacitors as requirement.
C21P/C21N C22P/C22N C23P/C23N	Power	Capacitor connection pins for the step-up circuit 2 which generate NAVDD. Connect capacitors as requirement.
C31P/C31N	Power	Capacitor connection pins for the step-up circuit 3 which generate VCL. Connect capacitors as requirement.
C41P/C41N	Power	Capacitor connection pins for the step-up 4 circuit which generate VGH. Connect capacitors as requirement.
C51P/C51N	Power	Capacitor connection pins for the step-up 5 circuit which generate VGL. Connect capacitors as requirement.
VREF	LDO Output	Reference voltage output from the internal LDO reference voltage generating circuit. Connect a capacitor for stabilization.
VGMP	LDO Output	Positive voltage level generated from PAVDD. LDO output for gray scale high voltage generator.
VGMN	LDO Output	Negative voltage level generated from NAVDD. LDO output for gray scale high voltage generator.
VGSP	LDO Output	Positive voltage level generated from PAVDD. LDO output for gray scale low voltage generator.
VGSN	LDO Output	Negative voltage level generated from NAVDD. LDO output for gray scale low voltage generator.

5 FUNCTIONAL DESCRIPTION

5.1 MPU INTERFACE

NT35410 can interface with MPU at high speed. However, if the interface cycle time is faster than the limit, MPU needs to have dummy wait(s) to meet the cycle time limit.

5.1.1 Interface Type Selection

The selection of a given interfaces are done by setting IM3, IM2, IM1 and IM0 pins as show in **Table 5.1.1** and **Table 5.1.2**

Table 5.1.1 Interface Type Selection

IM3	IM2	IM1	IM0	Interface	Read back selection
0	0	0	0	8080 MCU 8-bit Parallel	RDX strobe (8-bit read data and 8-bit read parameter)
0	0	0	1	8080 MCU 9-bit Parallel	RDX strobe (9-bit read data and 8-bit read parameter)
0	0	1	0	8080 MCU 16-bit Parallel	RDX strobe (16-bit read data and 8-bit read parameter)
0	0	1	1	8080 MCU 18-bit Parallel	RDX strobe (18-bit read data and 8-bit read parameter)
0	1	0	0	8080 MCU 24-bit Parallel	RDX strobe (24-bit read data and 8-bit read parameter)
1	1	0	0	SPI 3-pins serial	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
1	1	0	1	SPI 4-pins serial	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
1	0	0	1	RGB mode 1/2	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
1	1	1	0	MIPI	Follow MIPI Read Back Sequence
1	1	1	1	MDDI	Follow MDDI Read Back Sequence

Table 5.1.2 Pin Connection according to the Interface Type

IM3	IM2	IM1	IM0	Interface	RDX	WRX	DCX	Read back selection
0	0	0	0	8080 MCU 8-bit Parallel	RDX	WRX	DCX	D[23:8]: Unused, D7-D0: 8-bit Data
0	0	0	1	8080 MCU 9-bit Parallel	RDX	WRX	DCX	D[23:9]: Unused, D8-D0: 9-bit Data
0	0	1	0	8080 MCU 16-bit Parallel	RDX	WRX	DCX	D[23:16]: Unused, D15-D0: 16-bit Data
0	0	1	1	8080 MCU 18-bit Parallel	RDX	WRX	DCX	D[23:18]: Unused, D17-D0: 18-bit Data
0	1	0	0	8080 MCU 24-bit Parallel	RDX	WRX	DCX	D[23:0] : 24-bit Data
1	1	0	0	SPI 3-pins serial	Note 1	SCL	Note 1	D[23:0]: Unused, SDI,SDO, WRX pad: SCL
1	1	0	1	SPI 4-pins serial	Note 1	SCL	Note 1	D[23:0]: Unused, SDI, SDO, WRX pad: SCL
1	0	0	1	RGB mode 1/2	Note 1	SCL	Note 1	- SDI, SDO, WRX pad: SCL RGB mode 1/2 is selected by command via SPI.
1	1	1	0	MIPI	Note 1	Note 1	Note 1	D[23:0]: Unused, CLK_P/CLK_N, D0_P/D0_N
1	1	1	1	MDDI	Note 1	Note 1	Note 1	D[23:0]: Unused, CLK_P/CLK_N, D0_P/D0_N

Note1: Unused pins connected to VDDI.

5.1.2 80-series MPU Interface

The MCU uses an 11-wires 8-data or 12-wires 9-data or 19-wires 16-data or 21-wires 18-data or 27-wires 24-data parallel interface.

The chip-select CSX (active low) enables and disables the parallel interface. WRX is the parallel data write, RDX is the parallel data read and D[23:0] is parallel data.

The Graphics Controller Chip reads the data at the rising edge of WRX signal. The DCX is the data/command flag. When DCX='1', D[23:0] bits are display RAM data or command parameters. When DCX='0', D[23:0] bits are commands.

The 8080-series bi-directional interface can be used for communication between the micro controller and LCD driver chip. Interface bus width can be selected with IM3, IM2, IM1 and IM0.

The interface functions of 80-series parallel interface are given in **Table 5.1.3**.

Table 5.1.3 Parallel interface function (80-Series).

IM3	IM2	IM1	IM0	Interface	DCX	RDX	WRX	Function
0	0	0	0	8-bit Parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 8-bit display data or 8-bit parameter (D7 to D0)
					1	↑	1	Read 8-bit display data (D7 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)
0	0	0	1	9-bit Parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 9-bit display data (D8 to D0) or 8-bit parameter (D7 to D0)
					1	↑	1	Read 9-bit display data (D8 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)
0	0	1	0	16-bit Parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 16-bit display data (D15 to D0) or 8-bit parameter (D7 to D0)
					1	↑	1	Read 16-bit display data (D15 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)
0	0	1	1	18-bit Parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 18-bit display data (D17 to D0) or 8-bit parameter (D7 to D0)
					1	↑	1	Read 18-bit display data (D17 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)
0	1	0	0	24-bit Parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 24-bit display data (D23 to D0) or 8-bit parameter (D7 to D0)
					1	↑	1	Read 24-bit display data (D23 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)

Note: applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, and 0Fh.

5.1.2.1 WRITE CYCLE SEQUENCE

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (DCX, RDX, WRX) and data signals (D[23:0]). DCX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (=‘0’) and vice versa it is data (=‘1’).

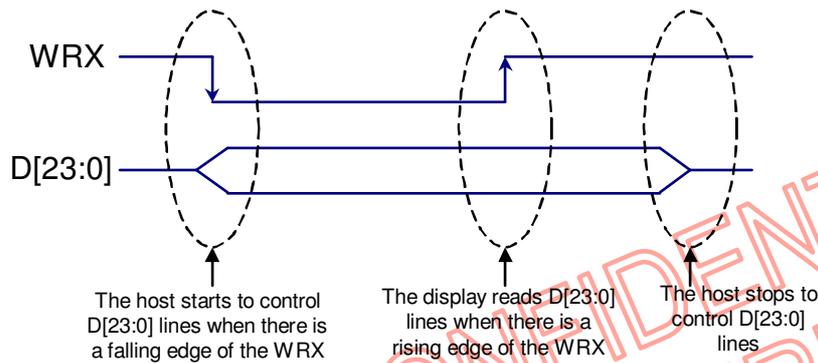


Fig. 5.1.1 80-Series WRX protocol

NOVATEK CONFIDENTIAL
NO DISCLOSURE

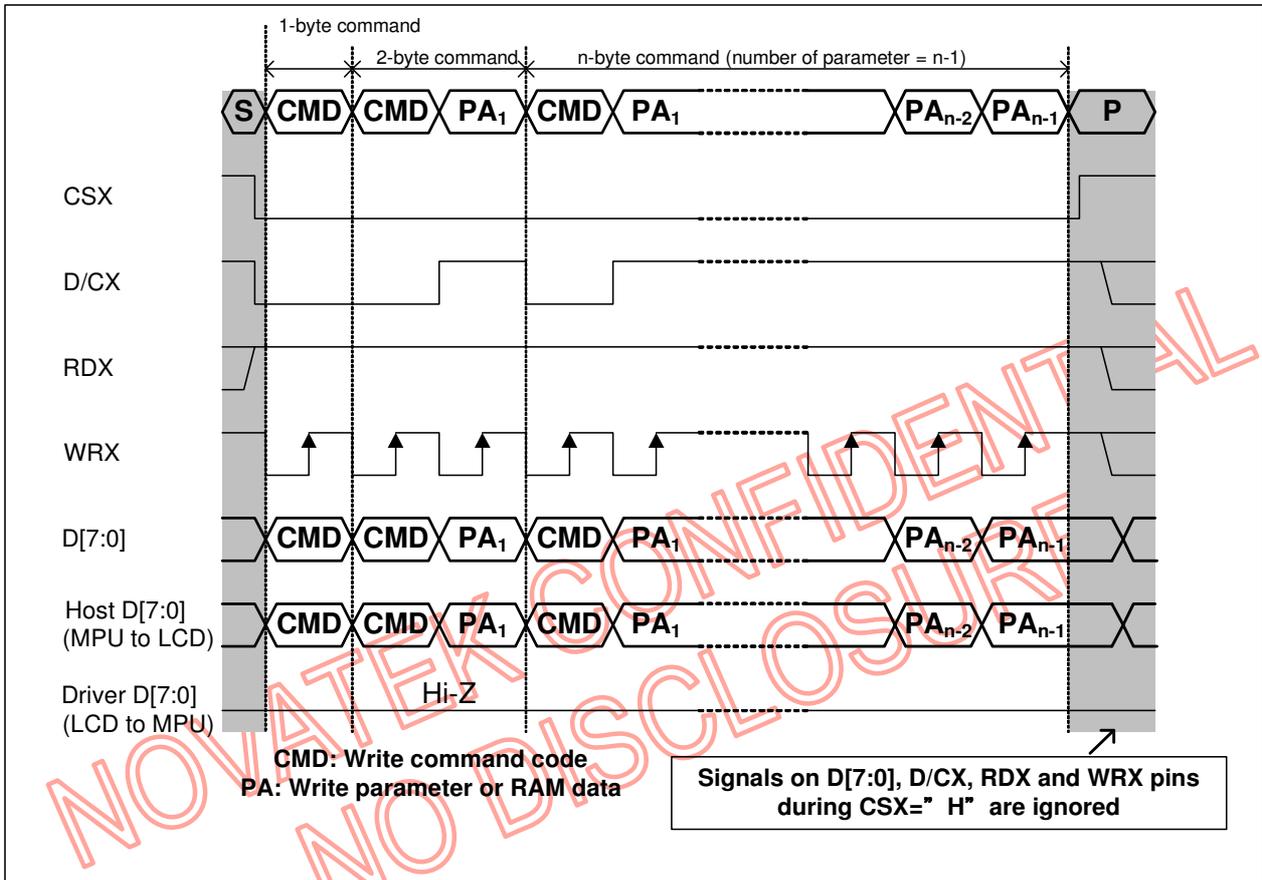


Fig. 5.1.2 80-Series parallel bus protocol, write to register or display RAM

5.1.2.2 Read cycle sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The display sends data (D[23:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

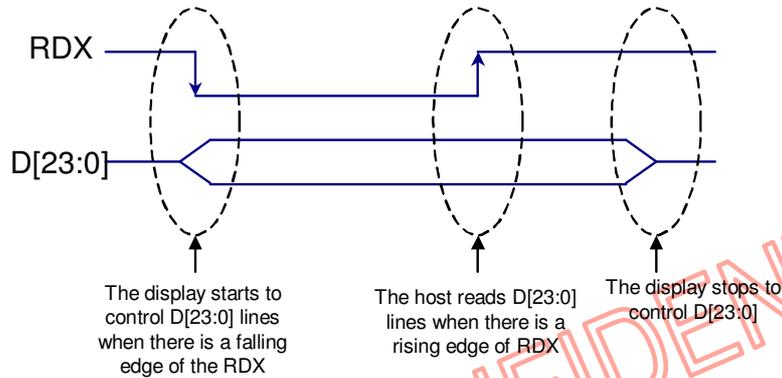


Fig. 5.1.3 80-Series RDX protocol

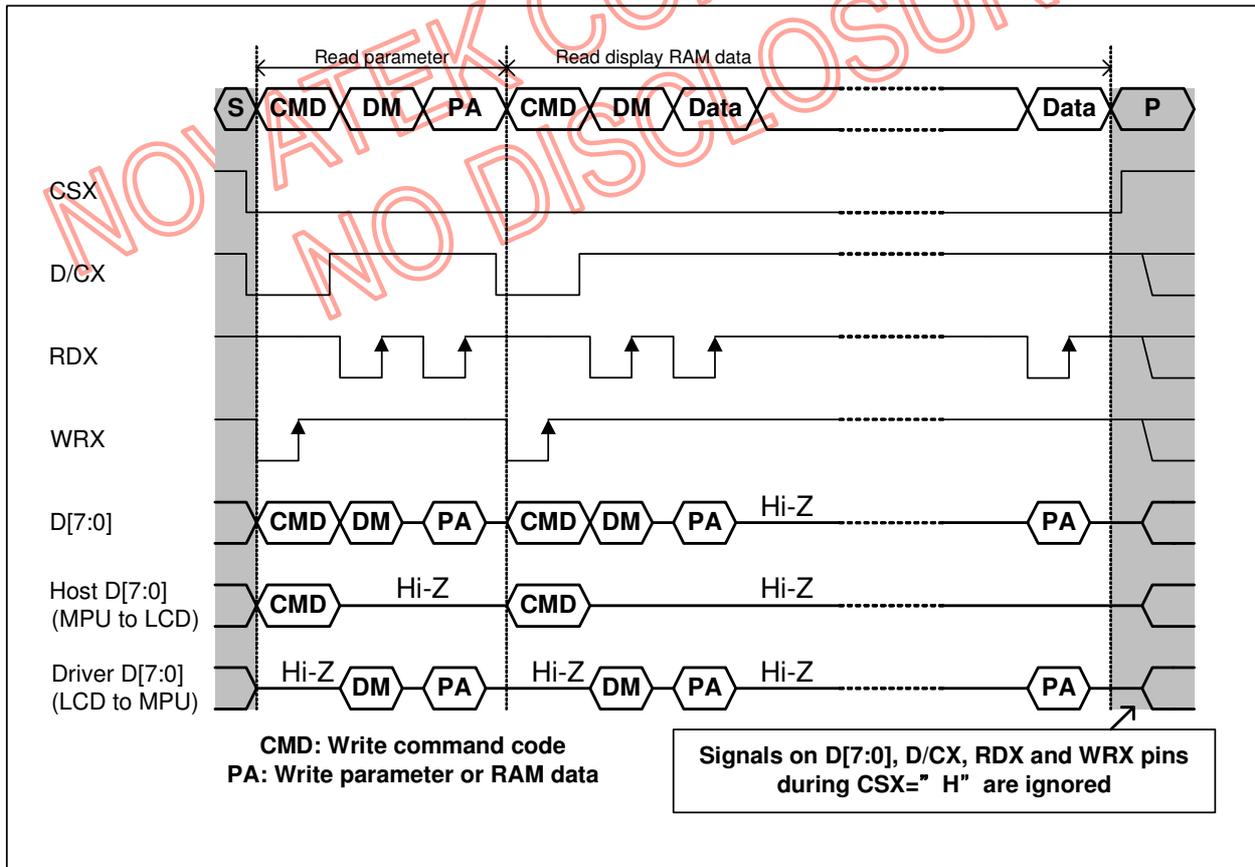


Fig. 5.1.4 80-Series parallel bus protocol, read from register or display RAM

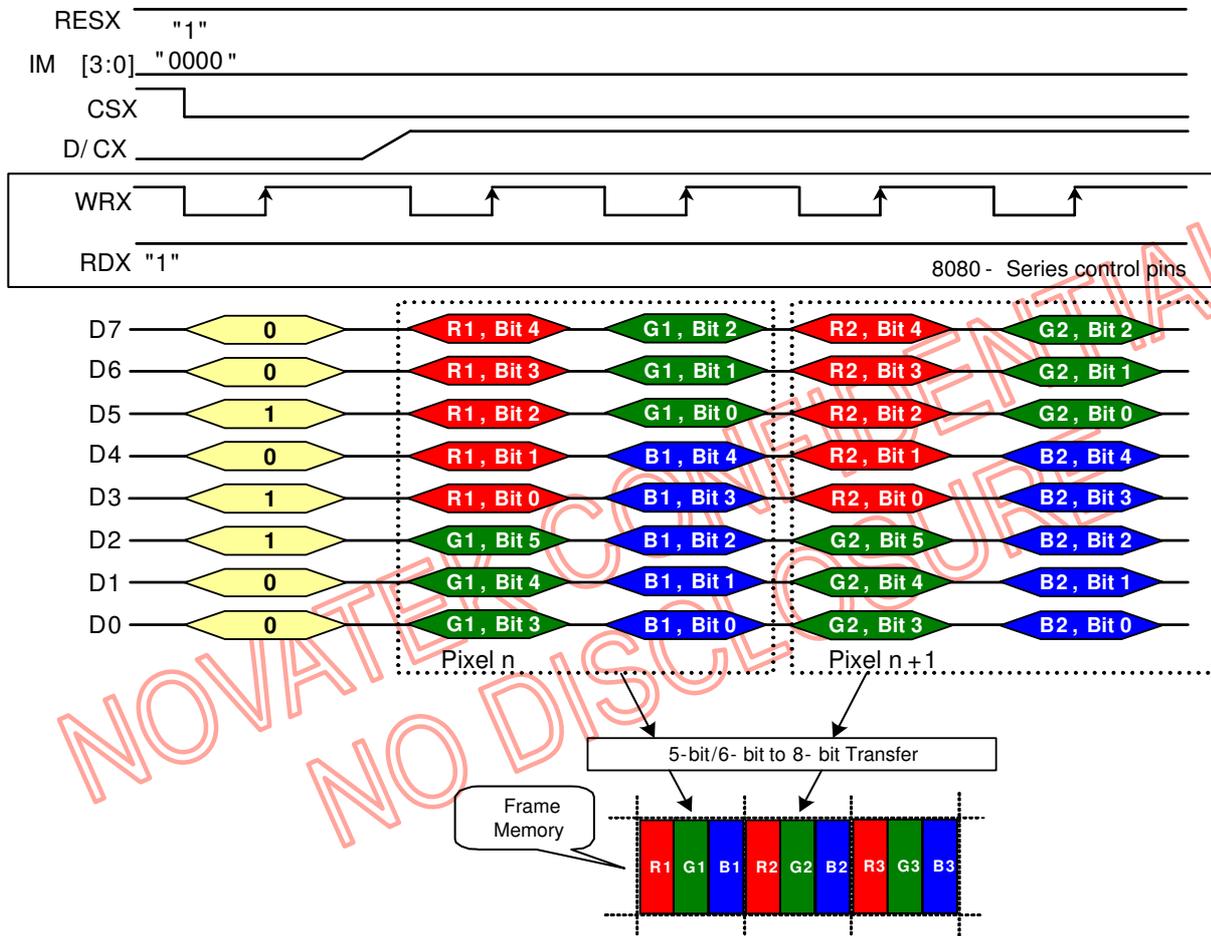
5.1.3 Display Data Format
5.1.3.1 8-BIT PARALLEL INTERFACE FOR DATA RAM WRITE

Different display data formats are available for three colors depth supported by the LCM listed below.

Register Command	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	2Ch
3Ah	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
05h	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	65K-Color (1-pixels/ 2-bytes)
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	G2	G1	G0	B4	B3	B2	B1	B0	
06h	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixels/ 3bytes)
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
07h	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	16.7M-Color (1-pixels/ 3bytes)
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	R2	R1	R0	
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	G7	G6	G5	G4	G3	G2	G1	G0	
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B7	B6	B5	B4	B3	B2	B1	B0	

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- 65K colors, RGB is 5-6-5-bit input



NOTE: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

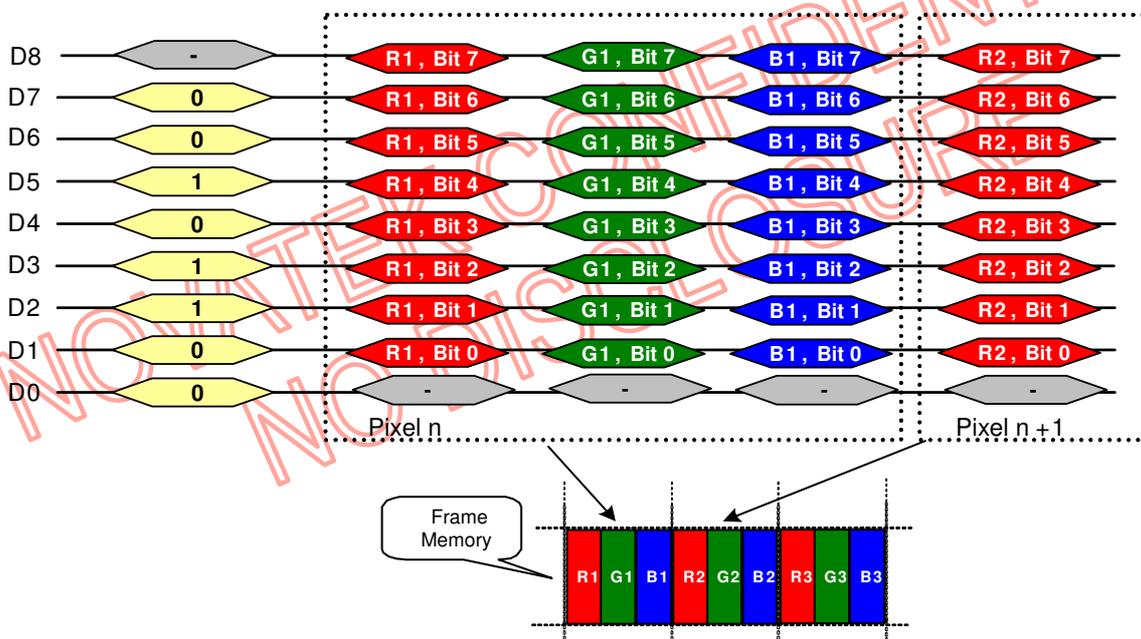
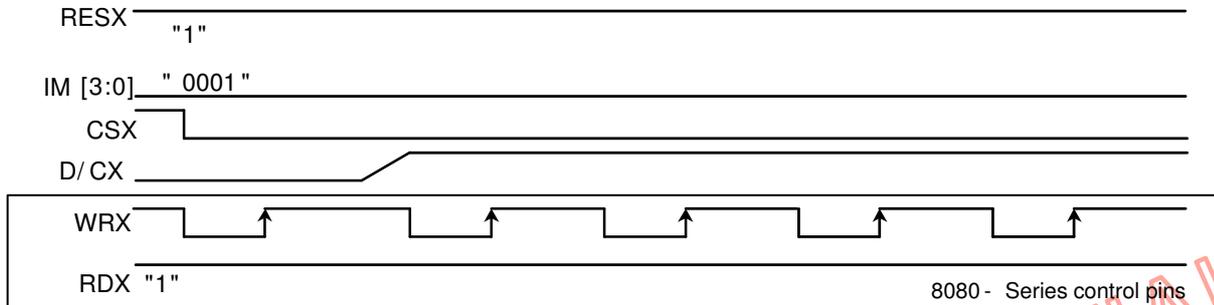
5.1.3.2 9-BIT PARALLEL INTERFACE FOR DATA RAM WRITE

Different display data formats are available for two colors depth supported by the LCM listed below.

Register Command	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
3Ah	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	2Ch
06h	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixels/ 2bytes)
07h	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	16.7M-Color (1-pixels/ 3bytes)

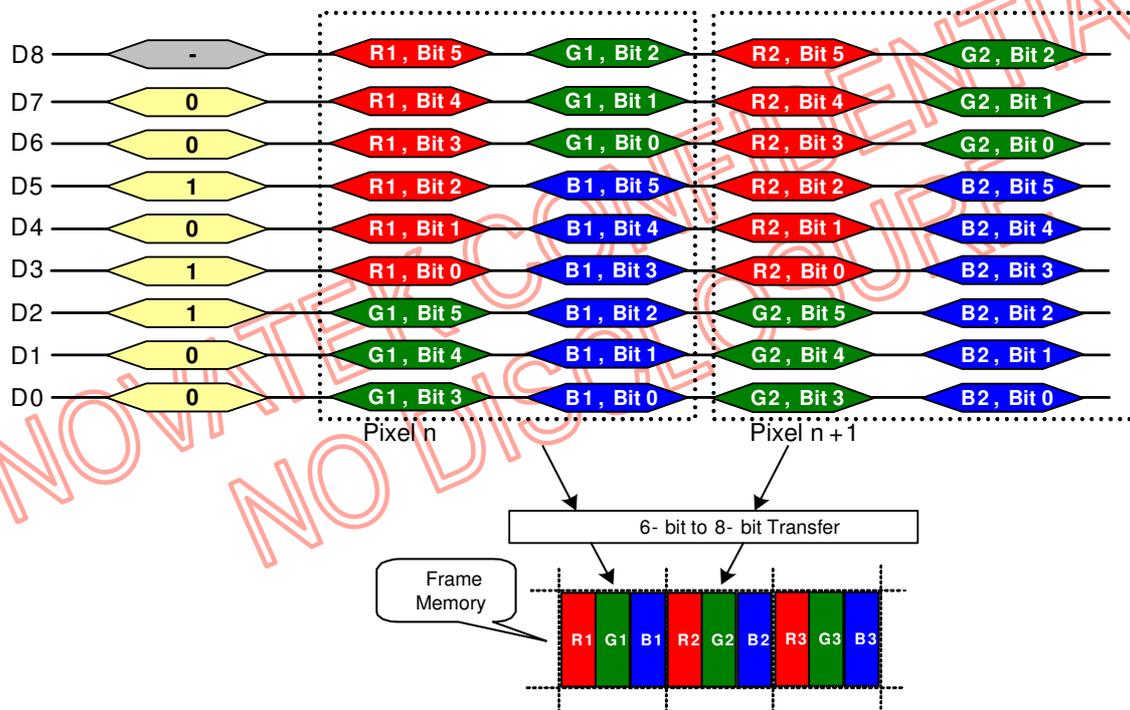
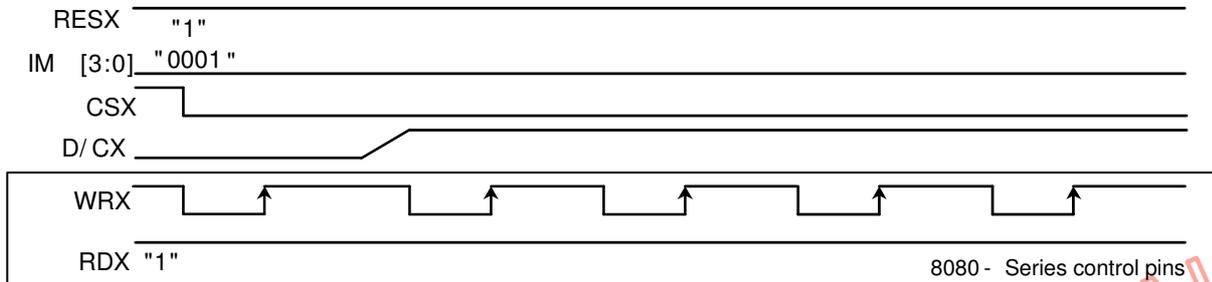
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- 16M colors, RGB is 8-8-8-bit input



NOTE: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 7, LSB=Bit 0 for Red, Green and Blue data.

- 262K colors, RGB is 6-6-6-bit input



NOTE: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

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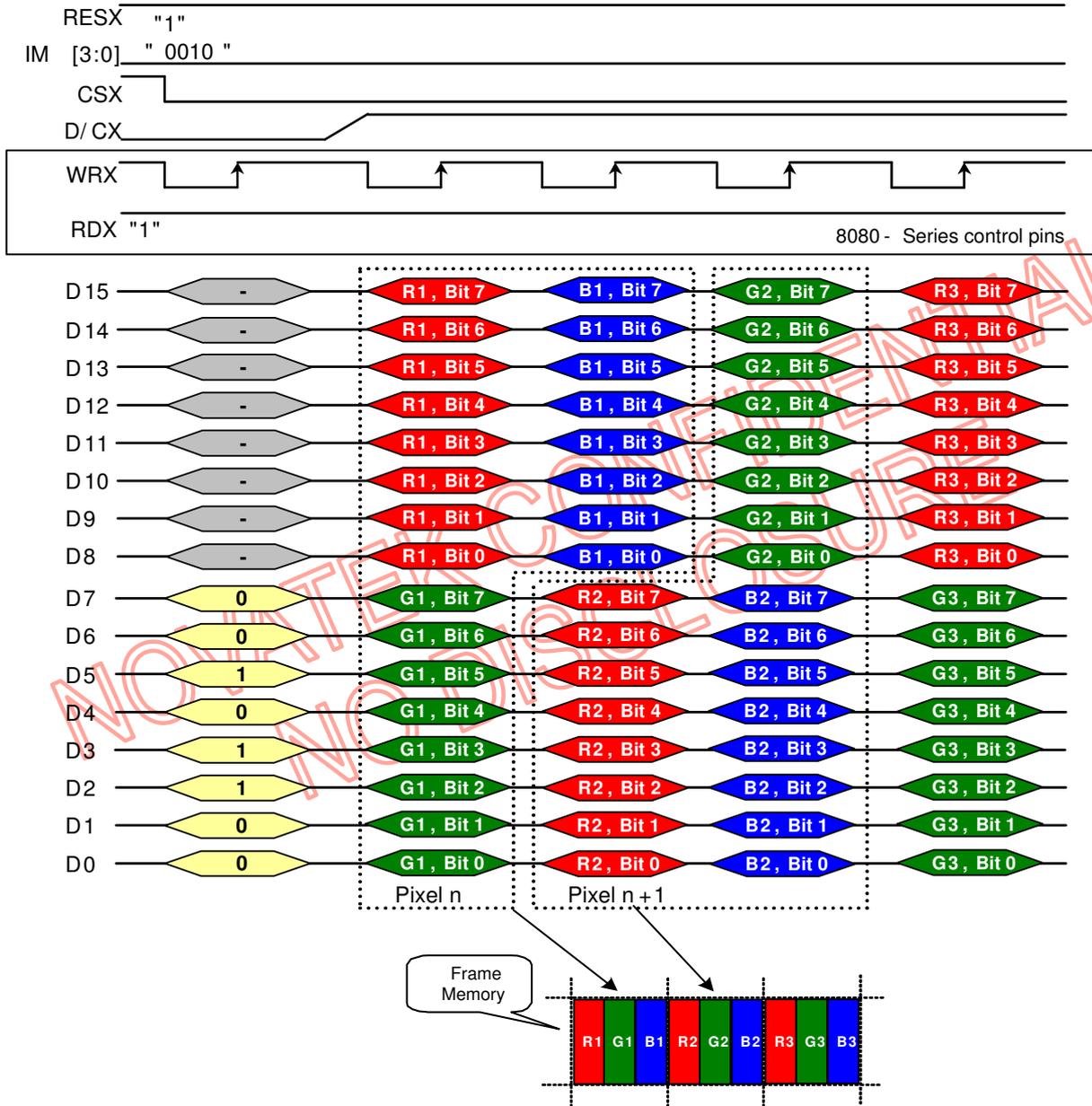
5.1.3.3 16-BIT PARALLEL INTERFACE FOR DATA RAM WRITE

Different display data formats are available for three colors depth supported by the LCM listed below.

Register Command	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
3Ah	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	2Ch
05h	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	65K-Color
06h	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Color (2-pixels/ 3bytes)
	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	
07h	x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	16.7M-Color (2-pixels/ 3bytes)
	x	x	x	x	x	x	x	x	B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0	
	x	x	x	x	x	x	x	x	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	

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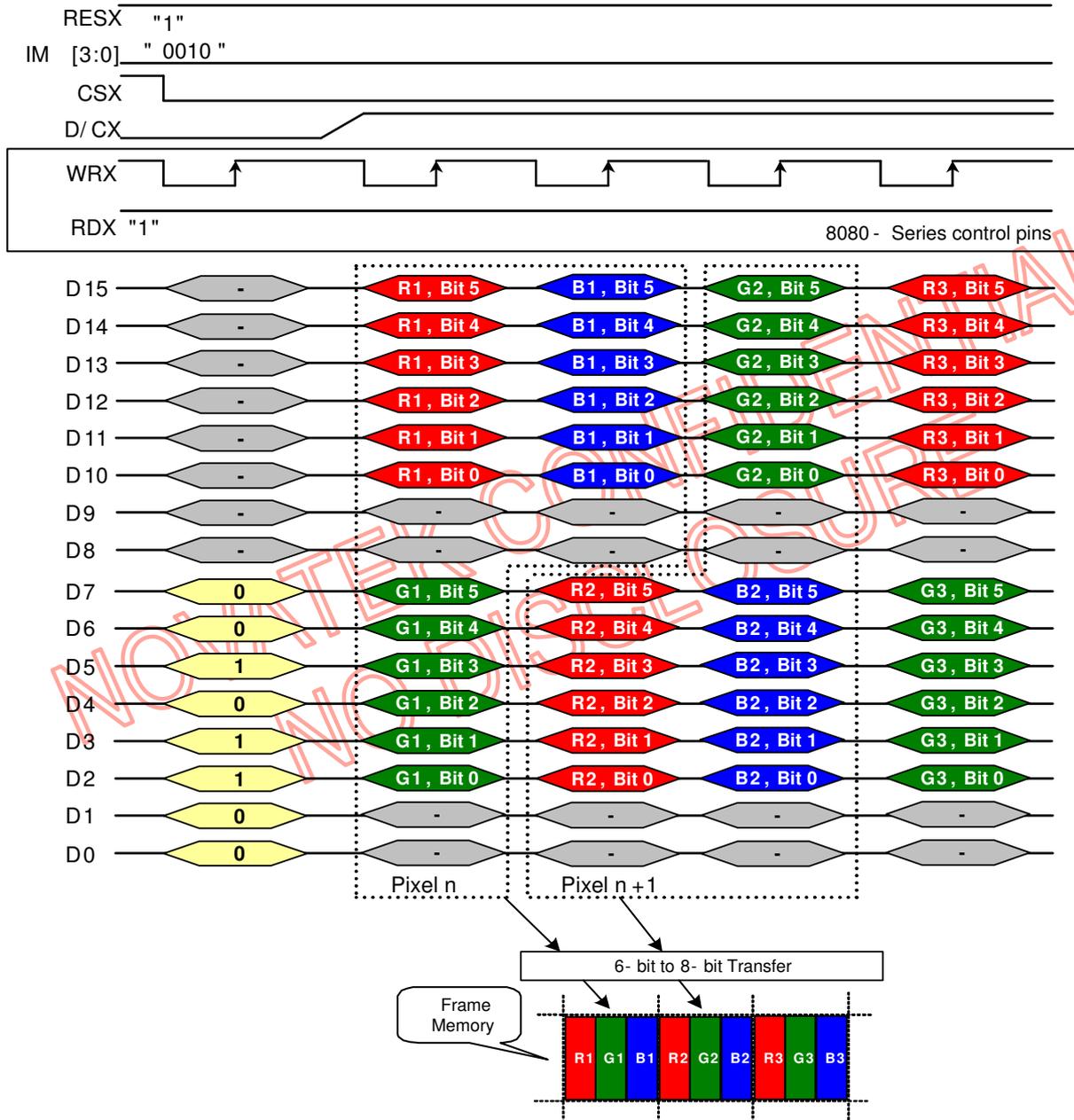
- 16M colors, RGB is 8-8-8-bit input



NOTE: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 7, LSB=Bit 0 for Red, Green and Blue data.

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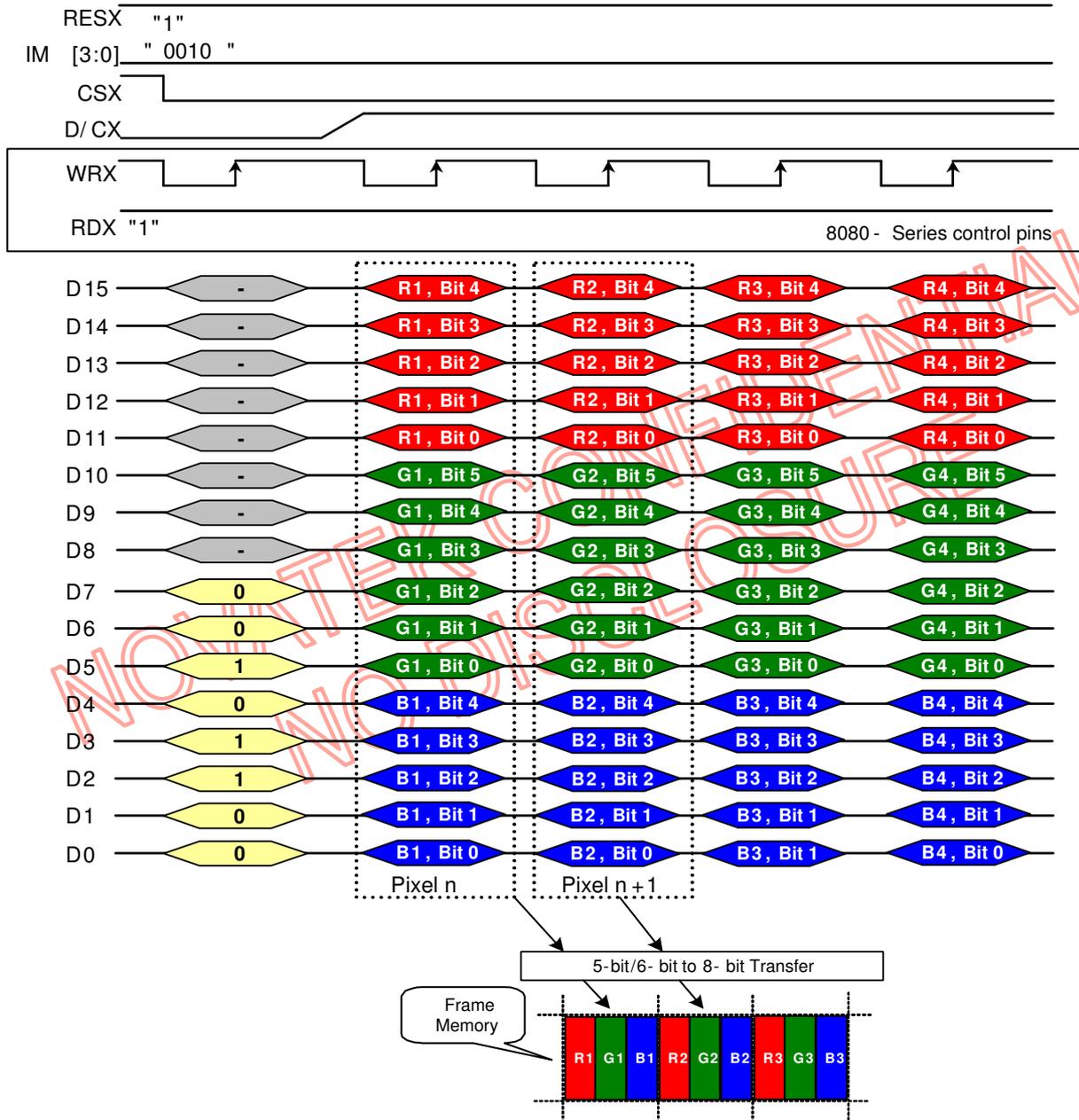
- 262K colors, RGB is 6-6-6-bit input



NOTE: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

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- 65K colors, RGB is 5-6-5-bit input



NOTE: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green data and MSB=Bit 4, LSB=Bit 0 for Red and Blue.

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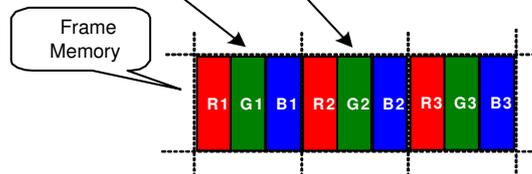
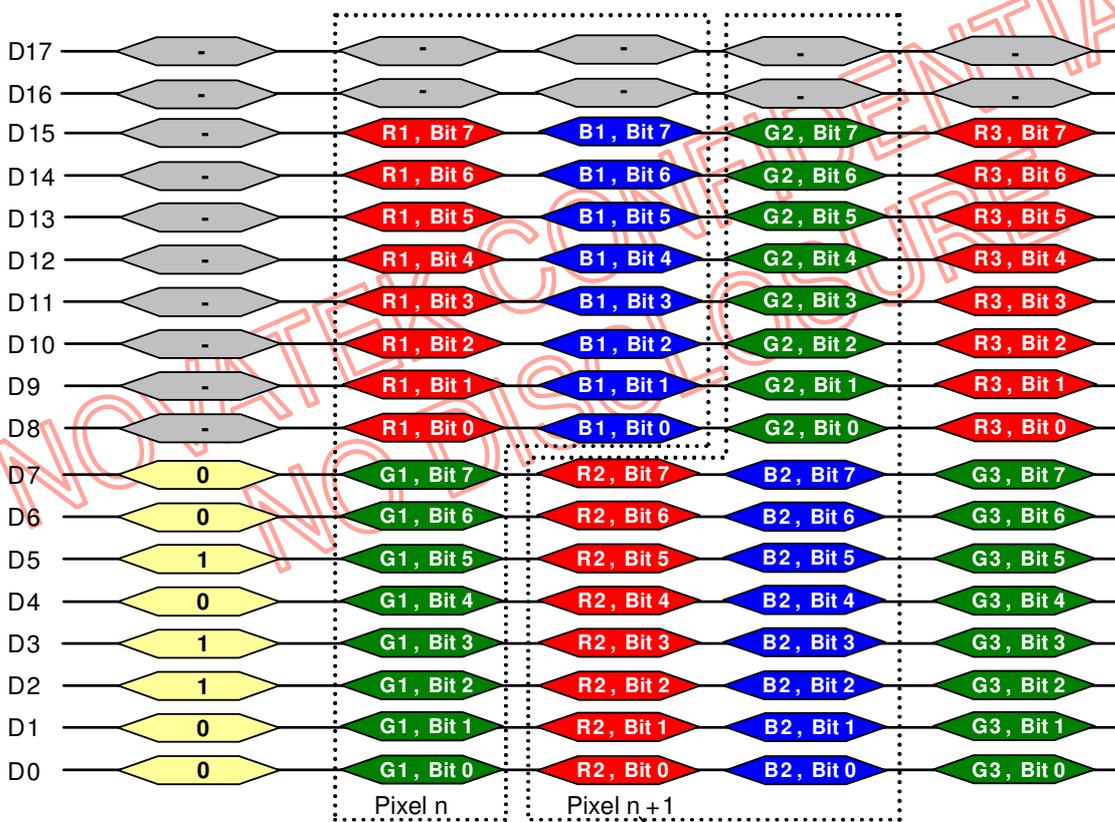
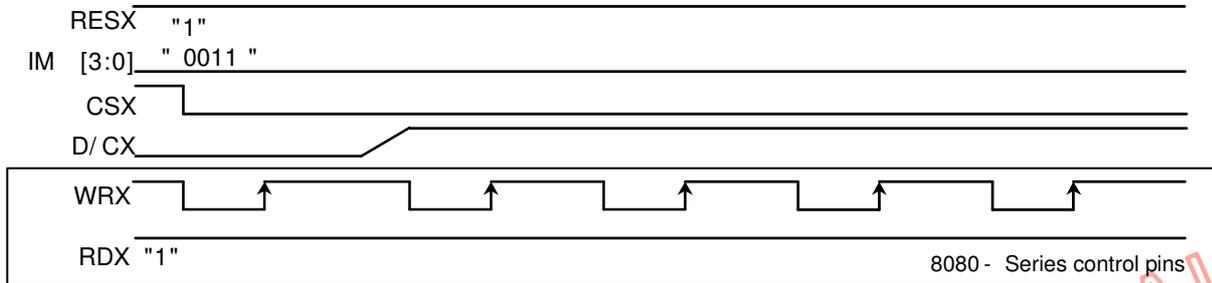
5.1.3.4 18-BIT PARALLEL INTERFACE FOR DATA RAM WRITE

Different display data formats are available for three colors depth supported by the LCM listed below.

Register Command	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
3Ah	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	2Ch
05h	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	65K-Color
06h	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color
07h	x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	16.7M-Color (2-pixels/ 3bytes)
	x	x	x	x	x	x	x	x	B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0	
	x	x	x	x	x	x	x	x	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	

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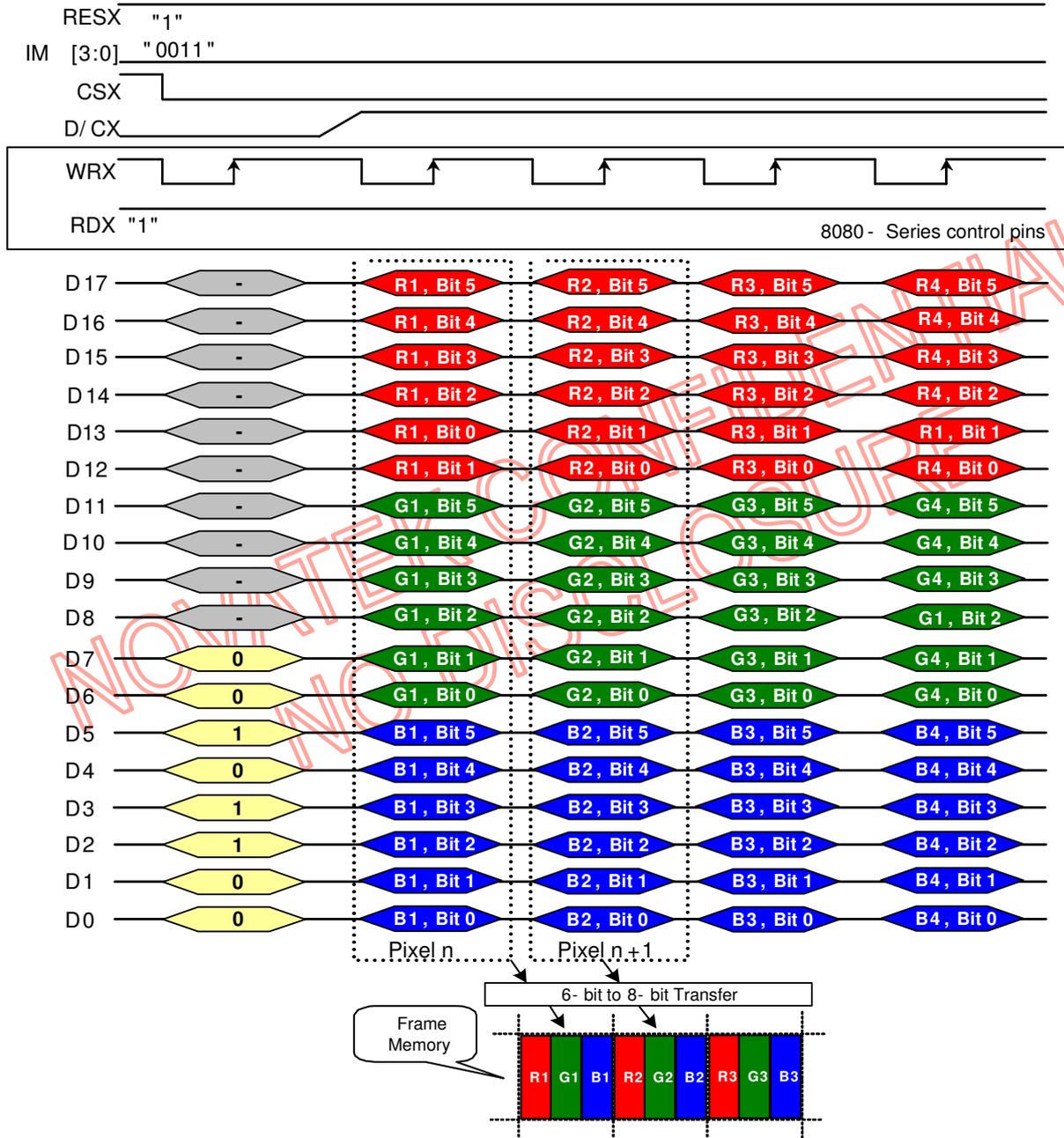
- 16M colors, RGB is 8-8-8-bit input



NOTE: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 7, LSB=Bit 0 for Red, Green and Blue data.

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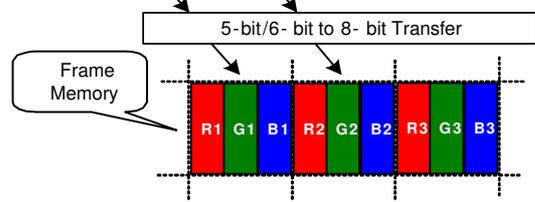
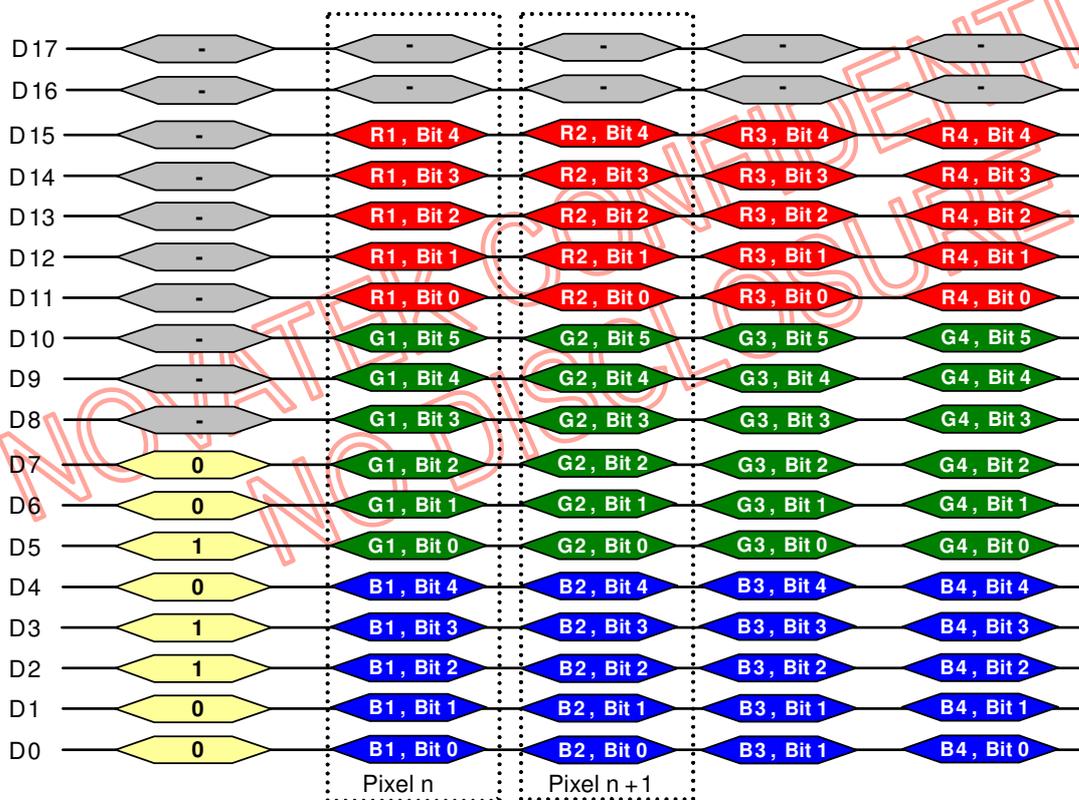
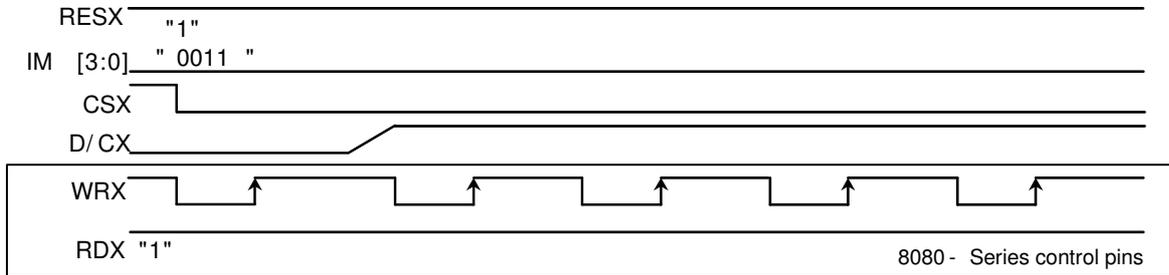
- 262K colors, RGB is 6-6-6-bit input



NOTE: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

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- 65K colors, RGB is 5-6-5-bit input



NOTE: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green and MSB=Bit 4, LSB=Bit 0 got Red and Blue data.

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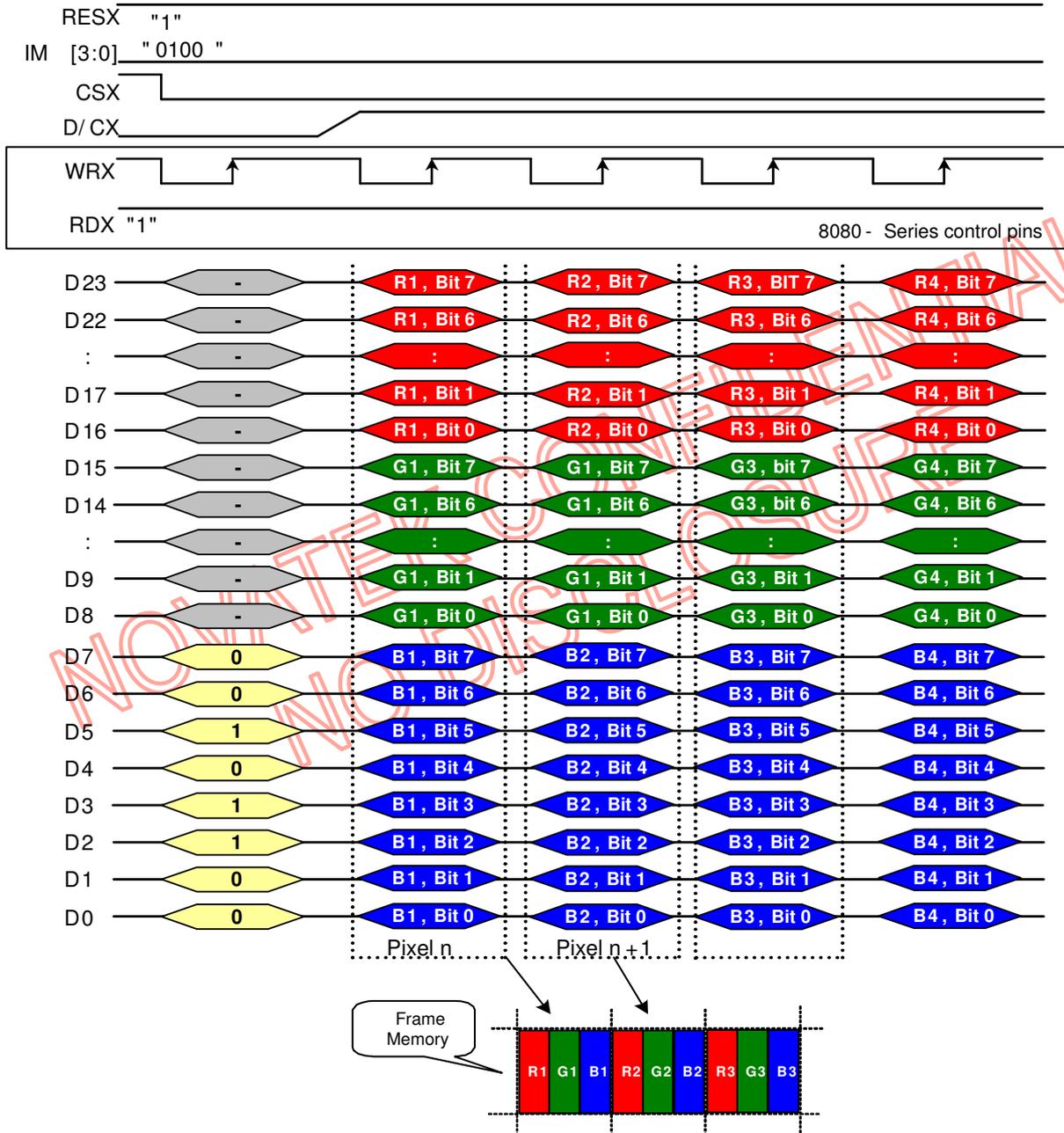
5.1.3.5 24-BIT PARALLEL INTERFACE FOR DATA RAM WRITE

Different display data formats are available for three colors depth supported by the LCM listed below.

Register Command	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
3Ah	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	0	2Ch
05h	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	65K-Color
06h	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color
07h	R7	R6	R5	R4	R3	R2	R1	G7	G6	G5	G4	G3	G2	G1	G0	R0	B7	B6	B5	B4	B3	B2	B1	B0	16.7M-Color

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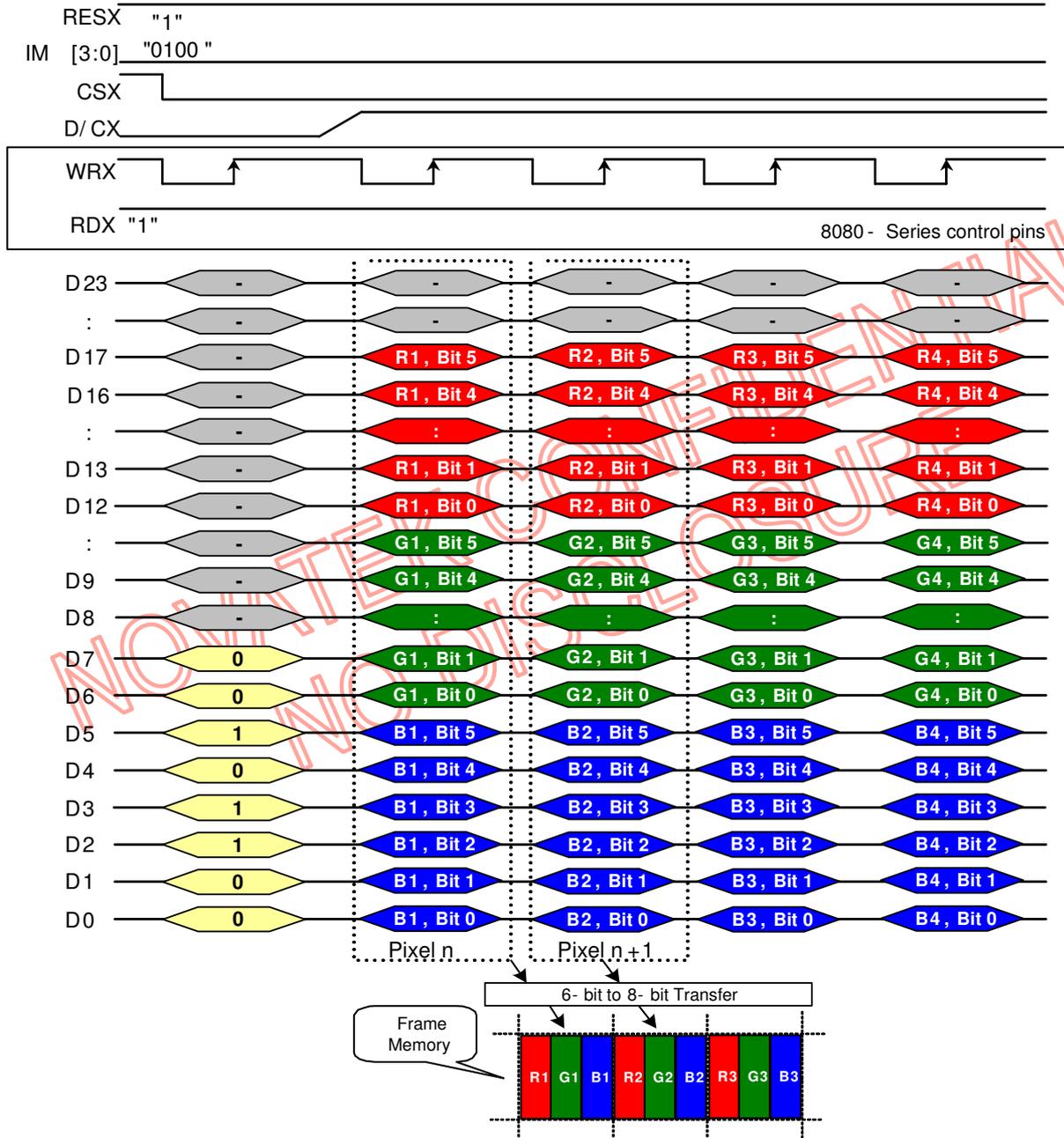
- 16M colors, RGB is 8-8-8-bit input



NOTE: The data order is as follows, MSB=D23, LSB=D0 and picture data is MSB=Bit 7, LSB=Bit 0 for Red, Green and Blue data.

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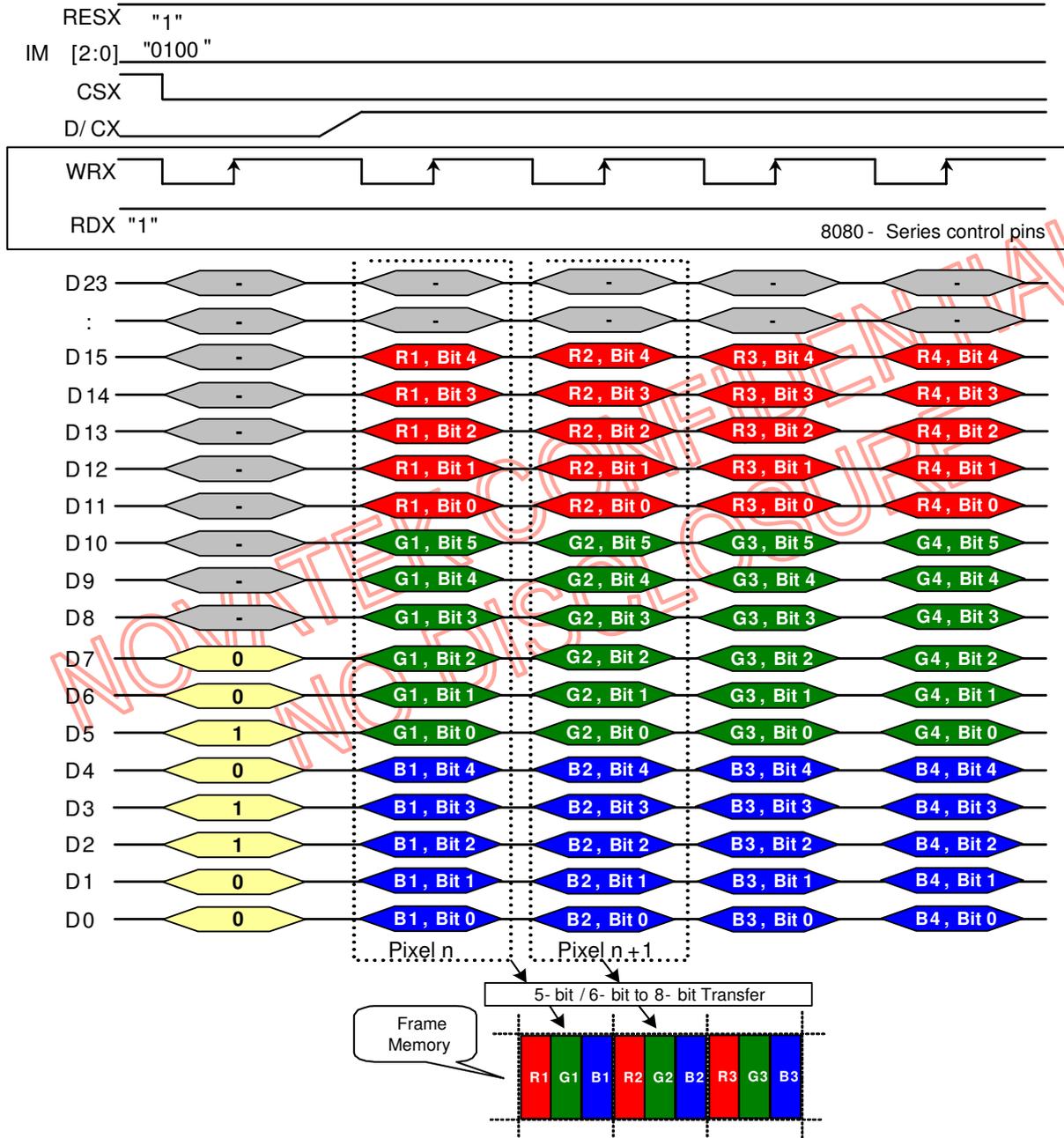
- 262K colors, RGB is 6-6-6-bit input



NOTE: The data order is as follows, MSB=D23, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

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- 65K colors, RGB is 5-6-5-bit input



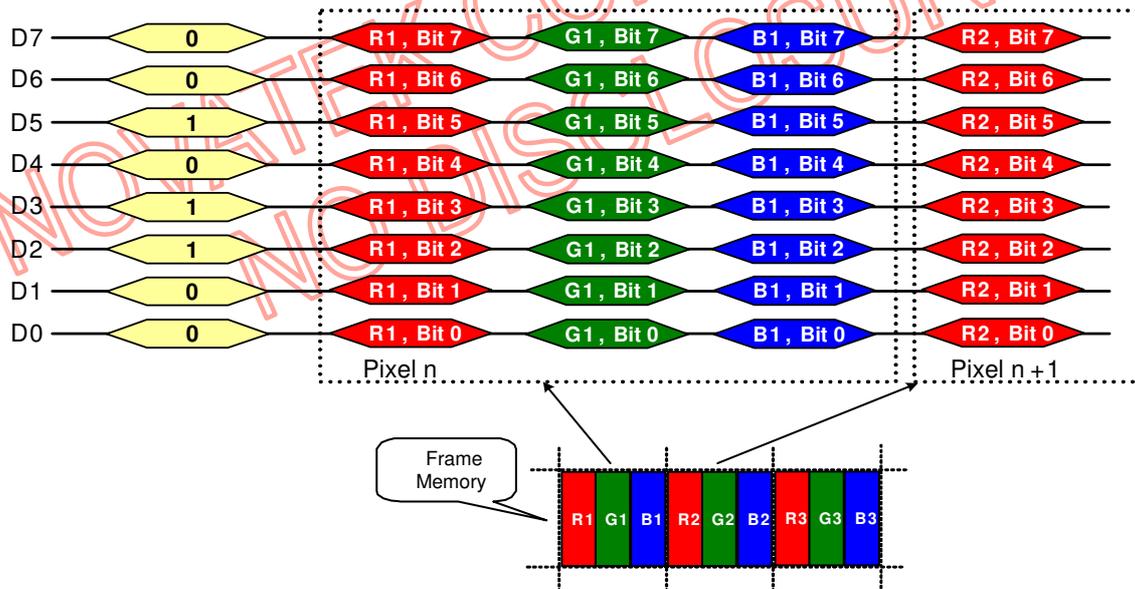
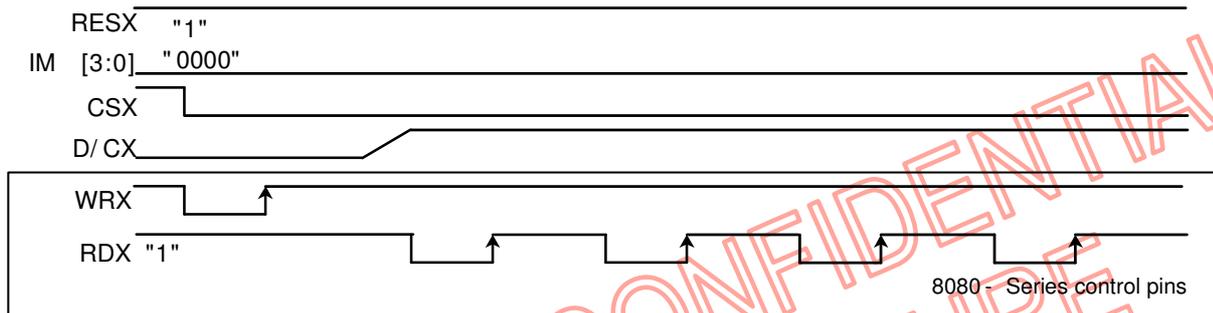
NOTE: The data order is as follows, MSB=D23, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

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5.1.3.6 8-BIT PARALLEL INTERFACE FOR DATA RAM READ

- Read data for RGB is 8-8-8-bit output

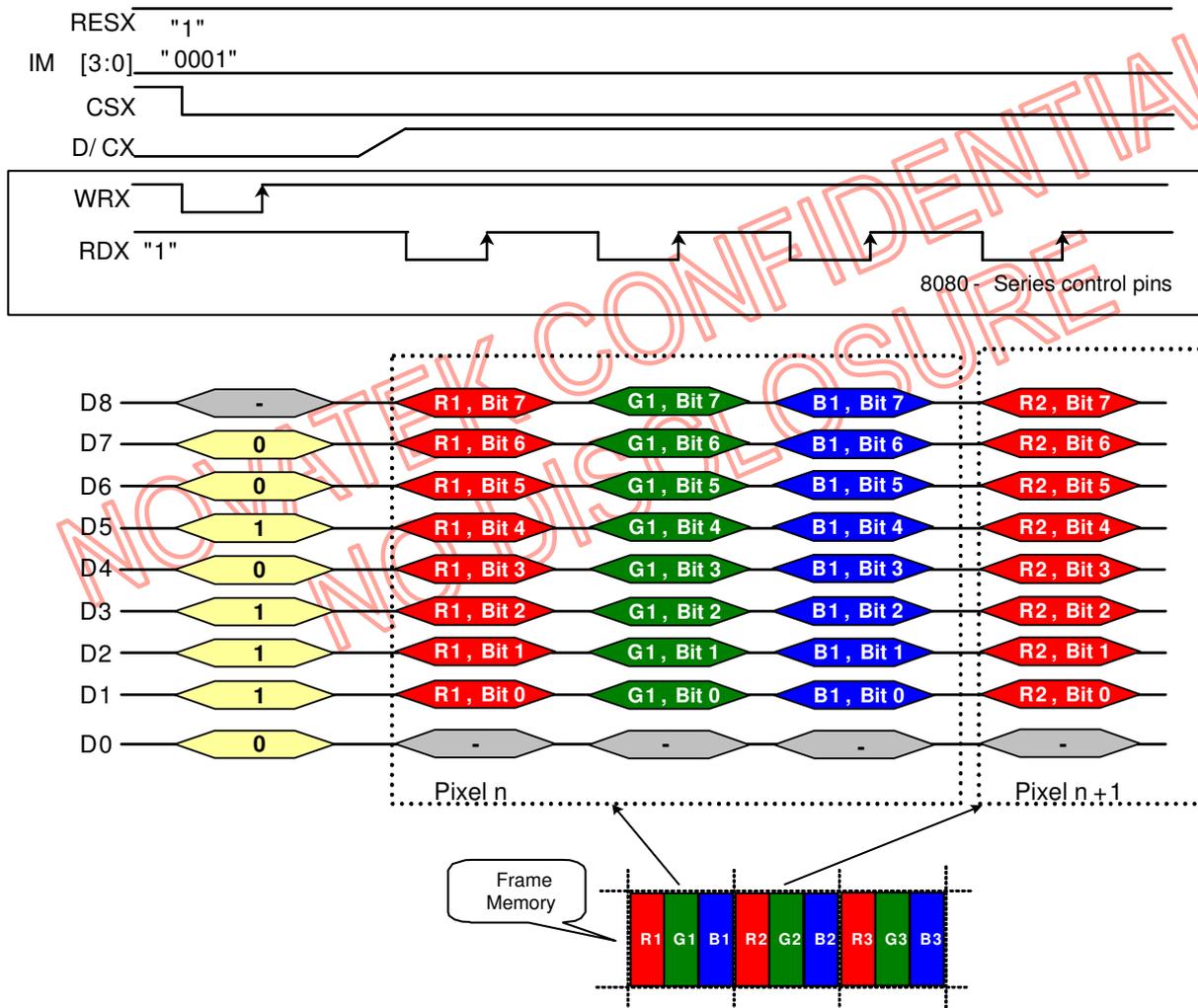
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	2Eh
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	R2	R1	R0	16.7M-Color (1-pixels/ 3bytes)
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	G7	G6	G5	G4	G3	G2	G1	G0	
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B7	B6	B5	B4	B3	B2	B1	B0	



5.1.3.7 9-BIT PARALLEL INTERFACE FOR DATA RAM READ

- Read data for RGB is 8-8-8-bit output

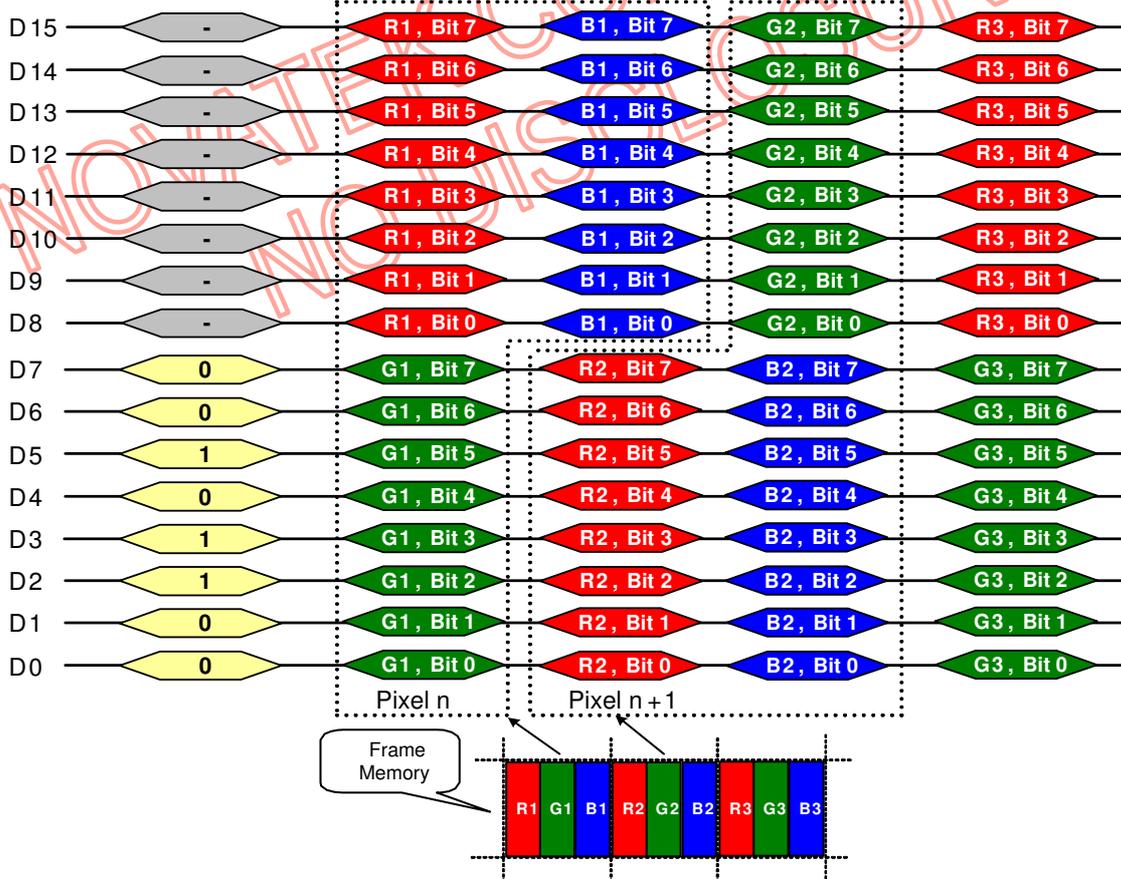
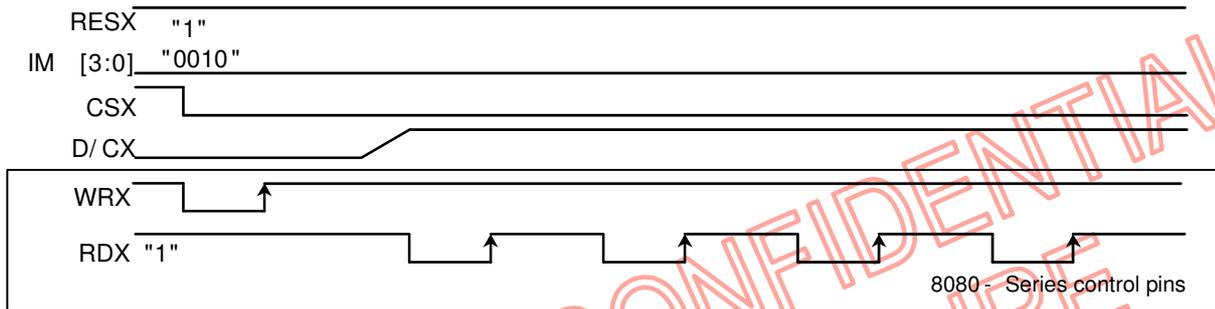
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	2Eh
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	R2	R1	R0	x	16.7M-Color (1-pixels/3bytes)
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	G7	G6	G5	G4	G3	G2	G1	G0	x	
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B7	B6	B5	B4	B3	B2	B1	B0	x	



5.1.3.8 16-BIT PARALLEL INTERFACE FOR DATA RAM READ

- Read data for RGB is 8-8-8-bit output

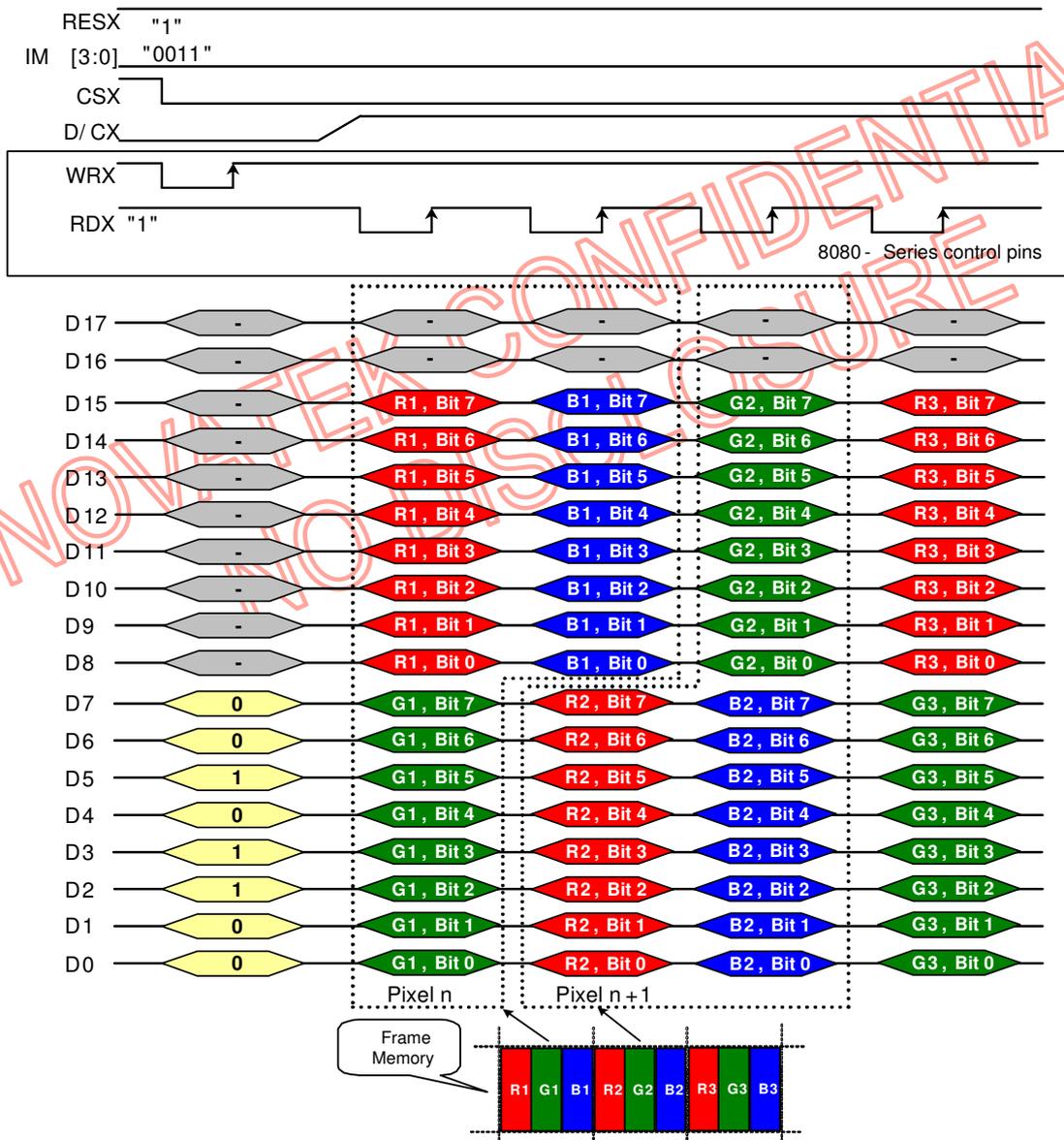
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	0	2Eh
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	16.7M-Color (1-pixels/ 3bytes)
x	x	x	x	x	x	x	x	B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0	
x	x	x	x	x	x	x	x	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	



5.1.3.9 18-BIT PARALLEL INTERFACE FOR DATA RAM READ

- Read data for RGB is 8-8-8-bit output

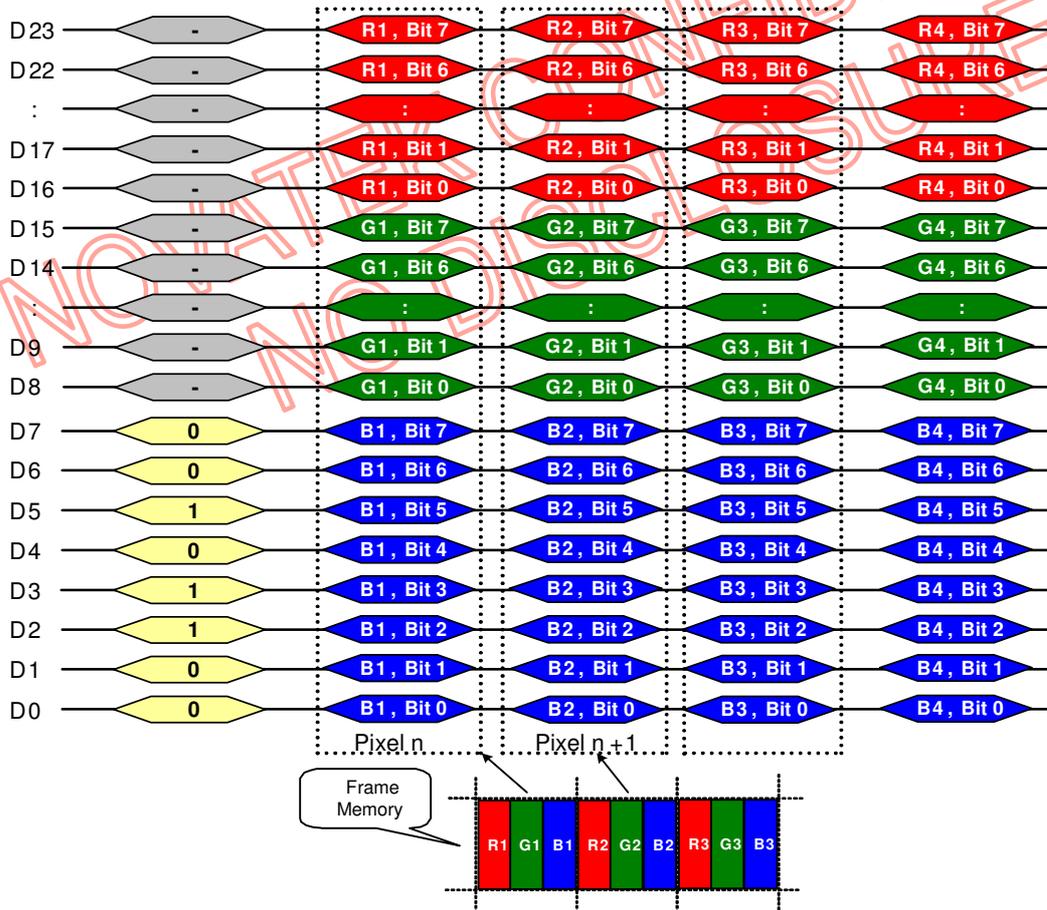
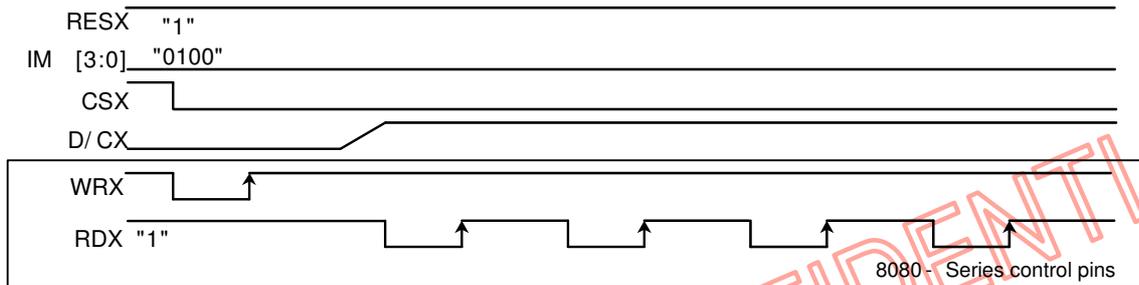
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0		2Eh
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	16.7M-Color (1-pixels/ 3bytes)
x	x	x	x	x	x	x	x	B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0	
x	x	x	x	x	x	x	x	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	



5.1.3.8 24-BIT PARALLEL INTERFACE FOR DATA RAM READ

- Read data for RGB is 8-8-8-bit output

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	2Eh
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
R7	R6	R5	R4	R3	R2	R1	G7	G6	G5	G4	G3	G2	G1	G0	R0	B7	B6	B5	B4	B3	B2	B1	B0	16.7M-Color



5.2 SERIAL INTERFACE

5.2.1 Interface Type Selection

The selection of a given interfaces are done by setting IM3, IM2, IM1 and IM0 pins as show in **Table 5.2.1**

Table 5.2.1 Interface Type Selection

IM3	IM2	IM1	IM0	Interface	Read back selection
0	0	0	0	8080 MCU 8-bit Parallel	RDX strobe (8-bit read data and 8-bit read parameter)
0	0	0	1	8080 MCU 9-bit Parallel	RDX strobe (9-bit read data and 8-bit read parameter)
0	0	1	0	8080 MCU 16-bit Parallel	RDX strobe (16-bit read data and 8-bit read parameter)
0	0	1	1	8080 MCU 18-bit Parallel	RDX strobe (18-bit read data and 8-bit read parameter)
0	1	0	0	8080 MCU 24-bit Parallel	RDX strobe (24-bit read data and 8-bit read parameter)
1	1	0	0	SPI 3-pins serial	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
1	1	0	1	SPI 4-pins serial	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
1	0	0	1	RGB mode 1/2	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
1	1	1	0	MIPI	Follow MIPI Read Back Sequence
1	1	1	1	MDDI	Follow MDDI Read Back Sequence

Table 5.2.2 Pin Connection according to the Interface Type

IM3	IM2	IM1	IM0	Interface	RDX	WRX	DCX	Read back selection
0	0	0	0	8080 MCU 8-bit Parallel	RDX	WRX	DCX	D[23:8]: Unused, D7-D0: 8-bit Data
0	0	0	1	8080 MCU 9-bit Parallel	RDX	WRX	DCX	D[23:9]: Unused, D8-D0: 9-bit Data
0	0	1	0	8080 MCU 16-bit Parallel	RDX	WRX	DCX	D[23:16]: Unused, D15-D0: 16-bit Data
0	0	1	1	8080 MCU 18-bit Parallel	RDX	WRX	DCX	D[23:18]: Unused, D17-D0: 18-bit Data
0	1	0	0	8080 MCU 24-bit Parallel	RDX	WRX	DCX	D[23:0] : 24-bit Data
1	1	0	0	SPI 3-pins serial	Note 1	SCL	Note 1	D[23:0]: Unused, SDI, SDO, WRX pad: SCL
1	1	0	1	SPI 4-pins serial	Note 1	SCL	Note1	D[23:0]: Unused, SDI, SDO, DCX WRX pad: SCL
1	0	0	1	RGB mode 1/2	Note 1	SCL	Note1	- SDI, SDO, WRX pad: SCL RGB mode 1/2 is selected by command via SPI.
1	1	1	0	MIPI	Note 1	Note 1	Note 1	D[23:0]: Unused, CLK_P/CLK_N, D0_P/D0_N
1	1	1	1	MDDI	Note 1	Note 1	Note 1	D[23:0]: Unused, CLK_P/CLK_N, D0_P/D0_N

Note1: Unused pins connected to VDDI.

5.2.2 Serial Interface

The selection of this interface is done by IM3, IM2, IM1 and IM0.

The serial interface is a 3-pin or 4-pin bi-directional interface for communication between the micro controller and the LCD driver chip. The 3-pin serial use: CSX (chip enable), SCL (serial clock) and SDI & SDO (serial data input/output) and 4-pin serial use: CSX (chip enable), DCX (data / command select), SCL (serial clock) and SDI & SDO (serial data input/output). Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary.

5.2.2.1 WRITE MODE

The write mode of the interface means the micro controller writes commands and data to the NT35410. 3-Pin serial data packet contains a control bit DCX and a transmission byte and in 4-pin serial case, data packet contains just transmission byte and control bit DCX is transferred by DCX pin. If DCX is low, the transmission byte is interpreted as command byte. If DCX is high, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to the NT35410. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDI/SDO data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

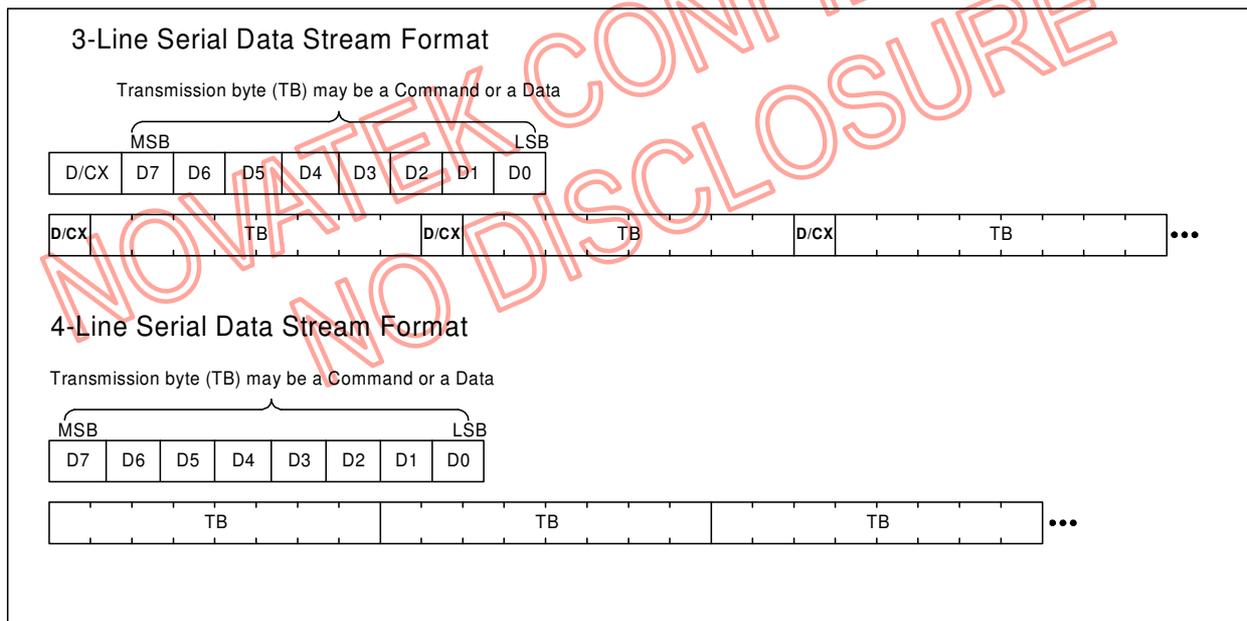


Fig. 5.2.1 Serial data stream, write mode

When CSX is high, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling CSX edge, SCL can be high or low (see **Fig. 5.2.2**). SDI, SDO is sampled at the rising edge of SCL. DCX indicates, whether the byte is command code (DCX=0) or parameter/RAM data (DCX=1). It is sampled when first rising SCL edge (3-line serial interface) or 8th rising SCL edge (4-line serial interface). If CSX stays low after the last bit of command/data byte, the serial interface expects the DCX bit (3-line serial interface) or D7 (4-line serial interface) of the next byte at the next rising edge of SCL.

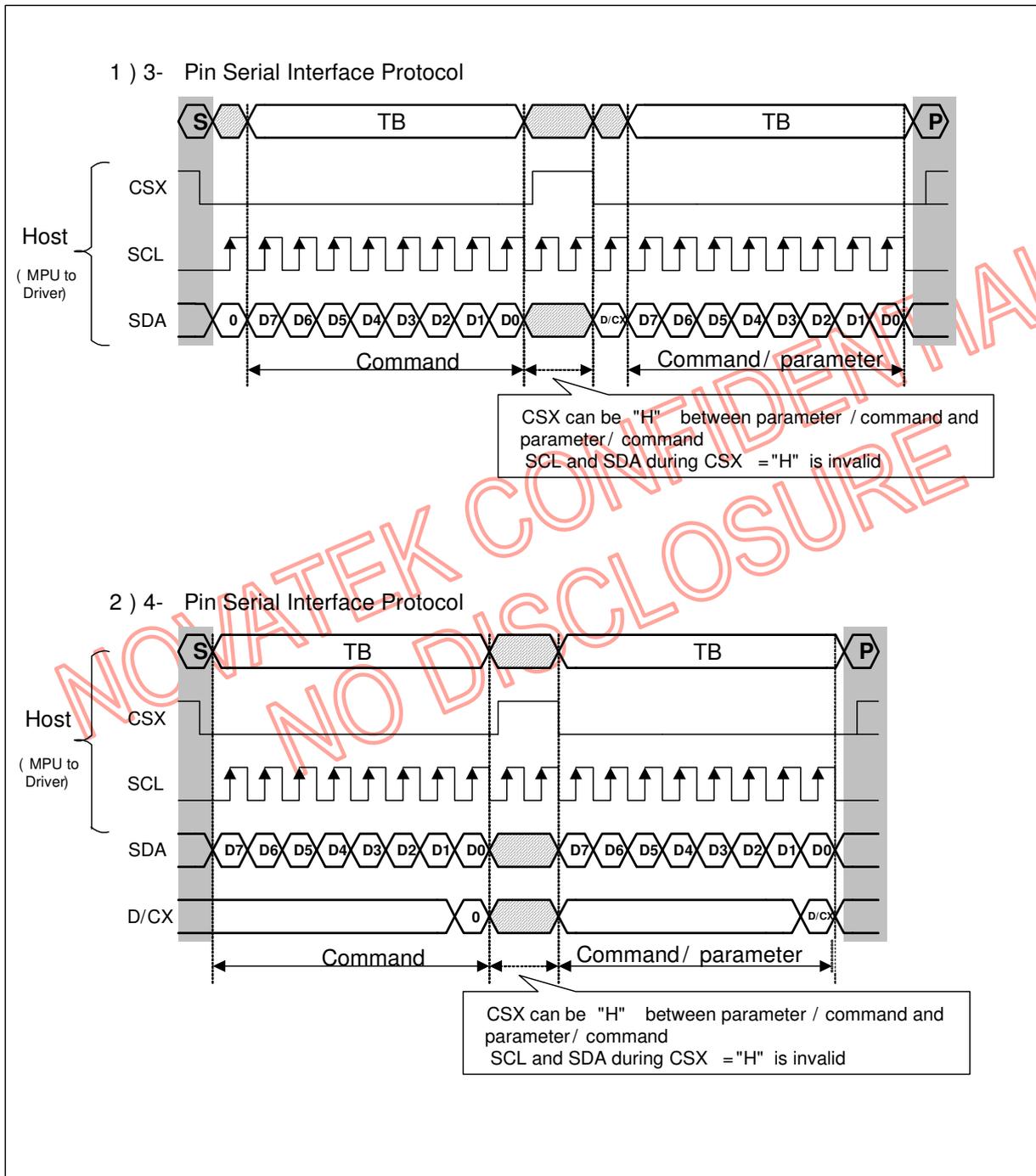


Fig. 5.2.2 Serial bus protocol, write to register with control bit in transmission

5.2.2.2 READ MODE

The read mode of the interface means that the micro controller reads register value from the NT35410. To do so the micro controller first has to send a command (Read ID or Read Register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go high before a new command is send (see **Fig. 5.2.3** and **Fig. 5.2.4**). The NT35410 samples the SDI (input data) at the rising edges, but shifts SDO (output data) at the falling SCL edges. Thus the micro controller is supported to read data at the rising SCL edges. After the read status command has been sent, the SDO line must be set to tri-state no later than at the falling SCL edge of the last bit (see **Fig. 5.2.3** and **Fig. 5.2.4**). Note: SPI can't read LV2 register.

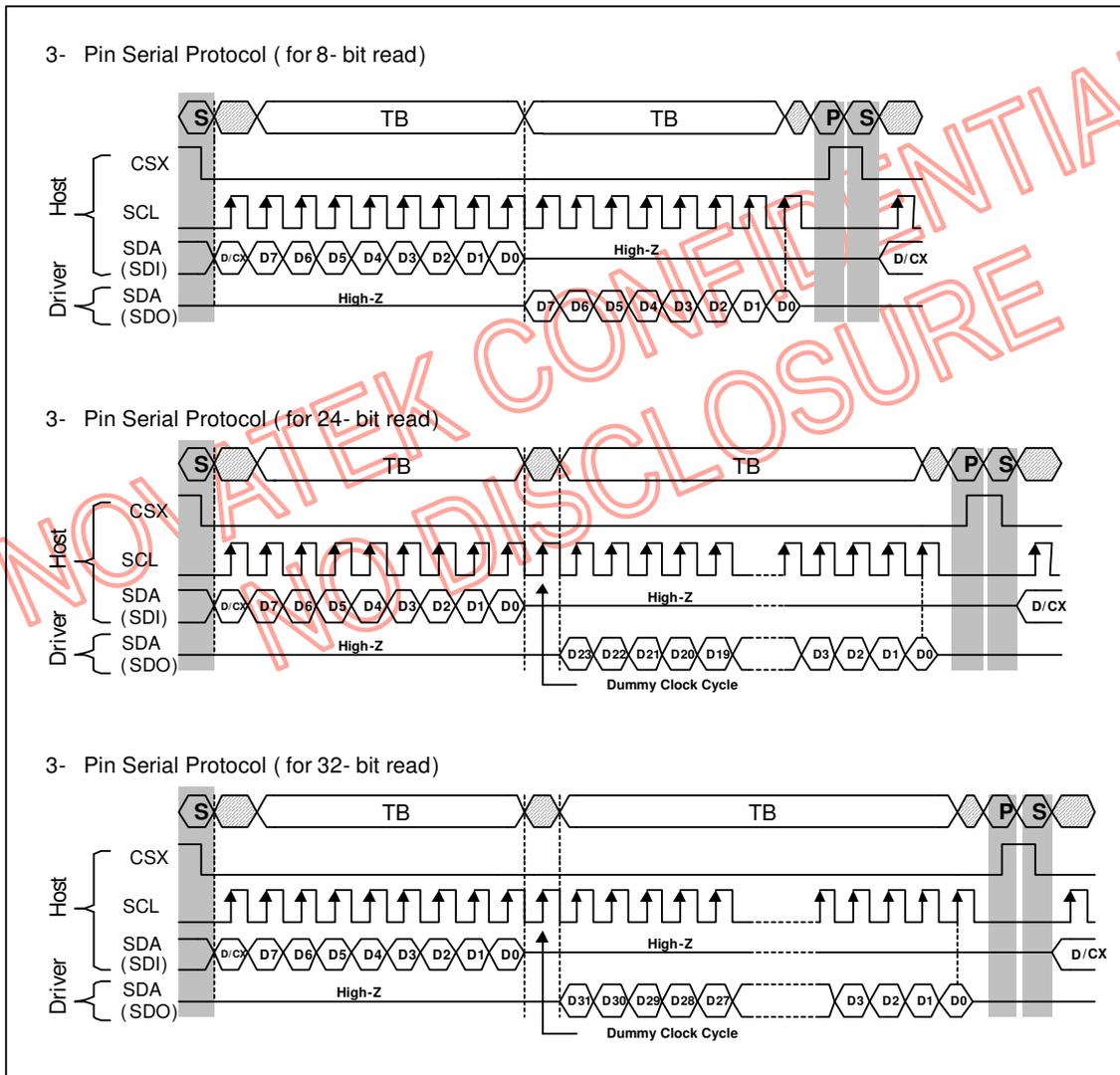


Fig. 5.2.3 Serial bus protocol, read mode (3-Pin serial interface case)

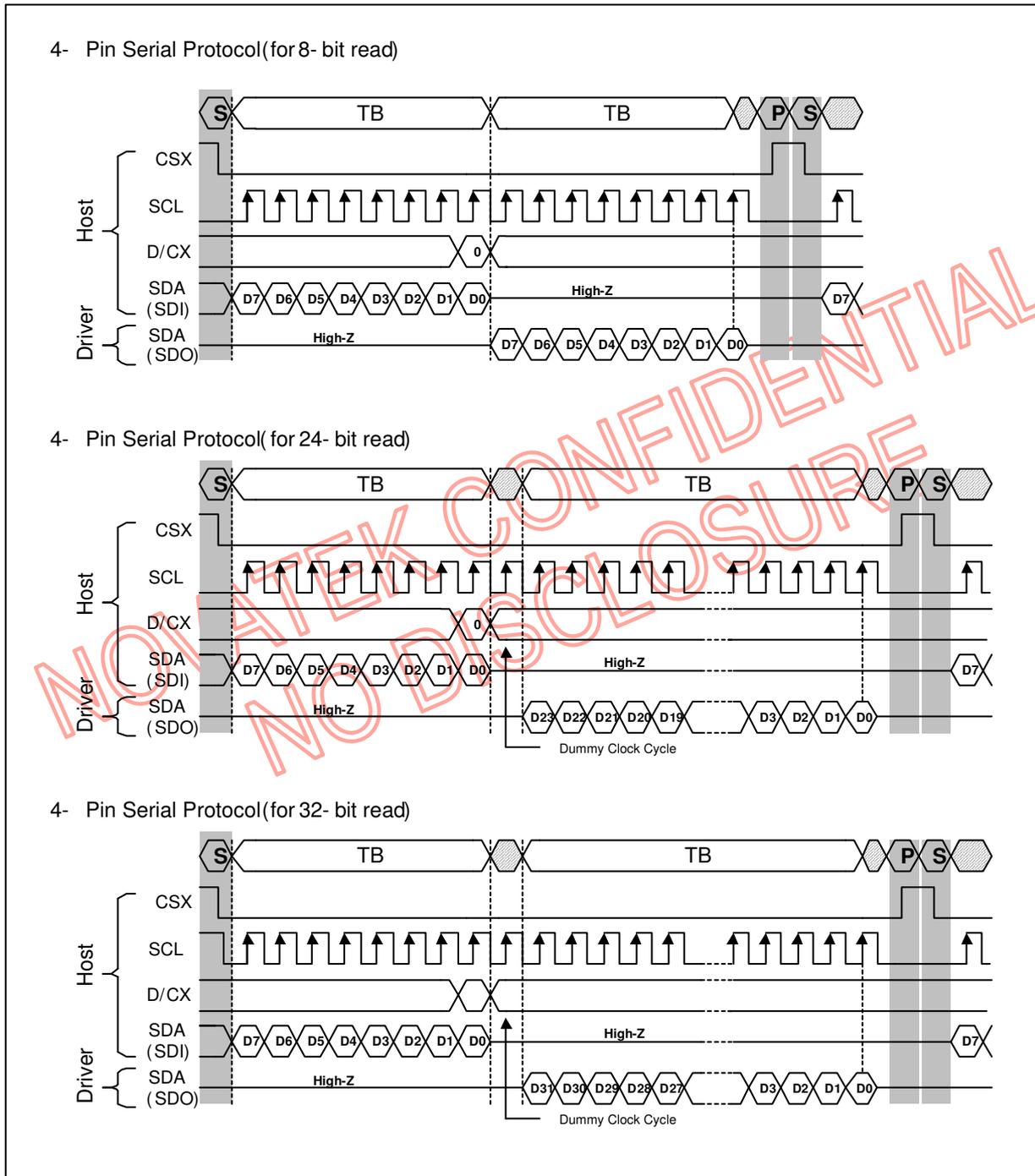


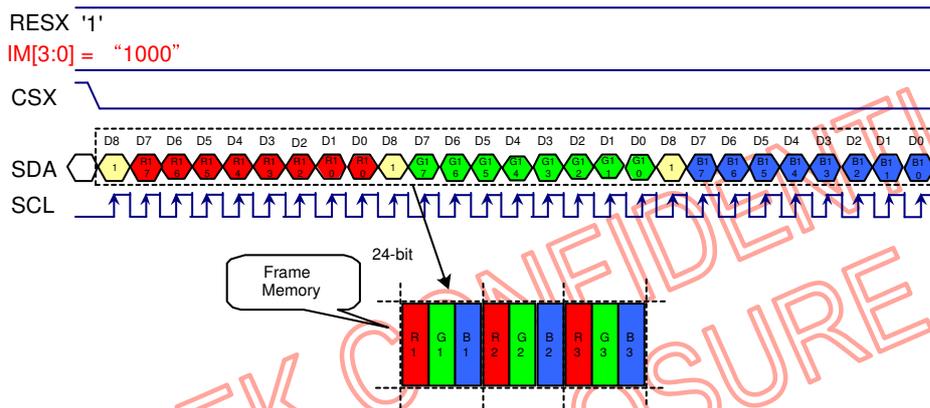
Fig. 5.2.4 Serial bus protocol, read mode (4-Pin serial interface case)

5.2.3 Display Data Format

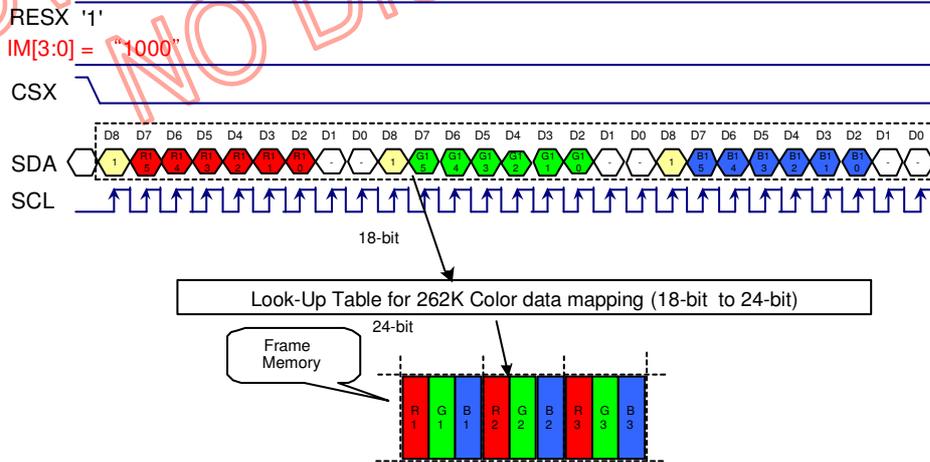
5.2.3.1 3-PINS SERIAL INTERFACE FOR DATA RAM WRITE

Different display data formats are available for three colors depth supported by the LCM listed below.

- 16M colors, RGB is 8-8-8-bit input

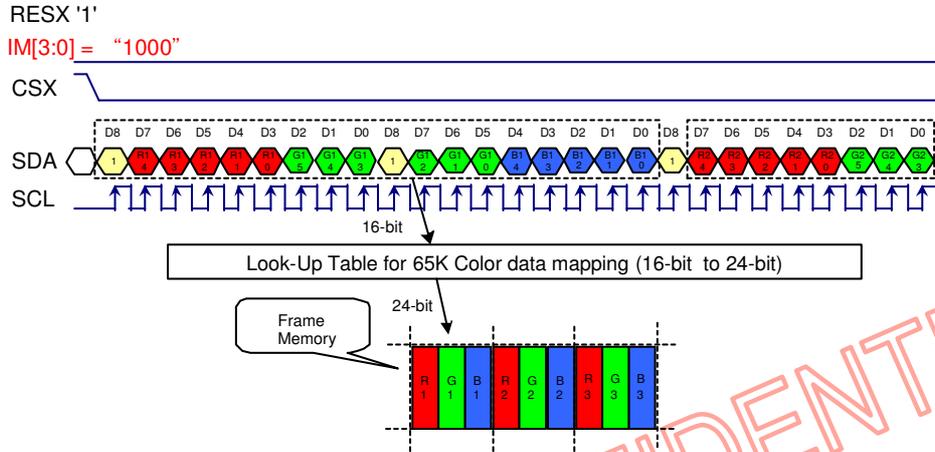


- 262K colors, RGB is 6-6-6-bit input



<https://Datasheetspdf.com/>

- 65K colors, RGB is 5-6-5-bit input

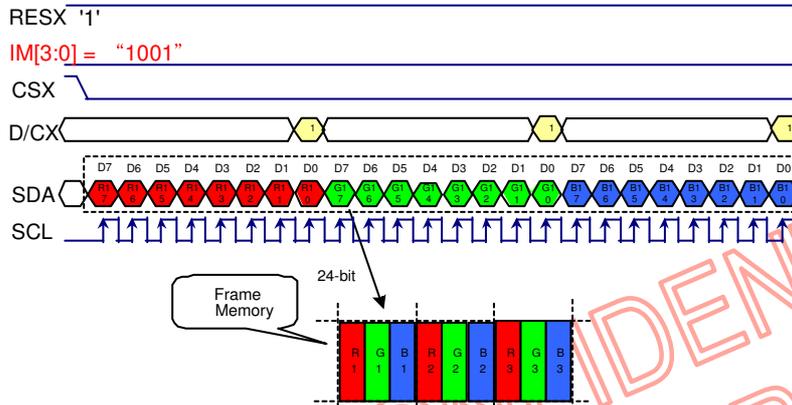


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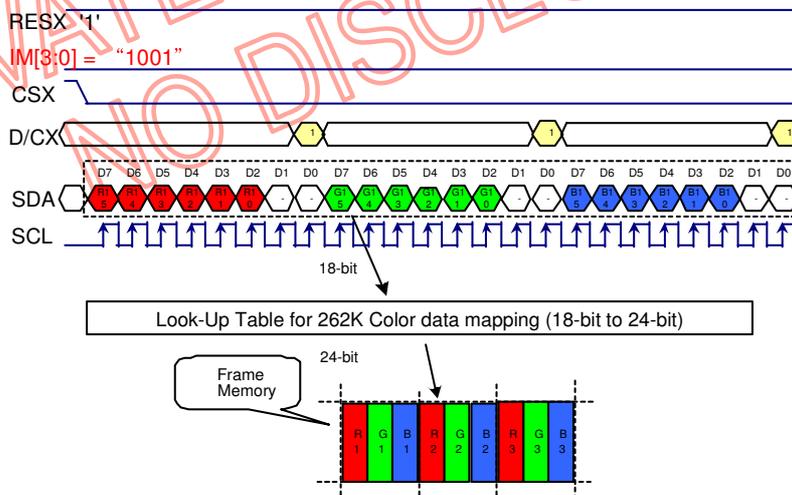
5.2.3.2 4-PINS SERIAL INTERFACE FOR DATA RAM WRITE

Different display data formats are available for three colors depth supported by the LCM listed below.

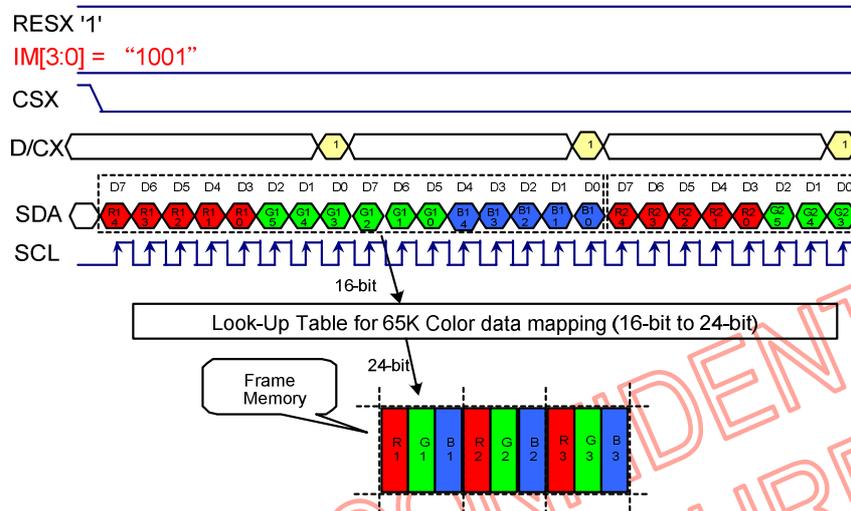
- 16M colors, RGB is 8-8-8-bit input



- 262K colors, RGB is 6-6-6-bit input



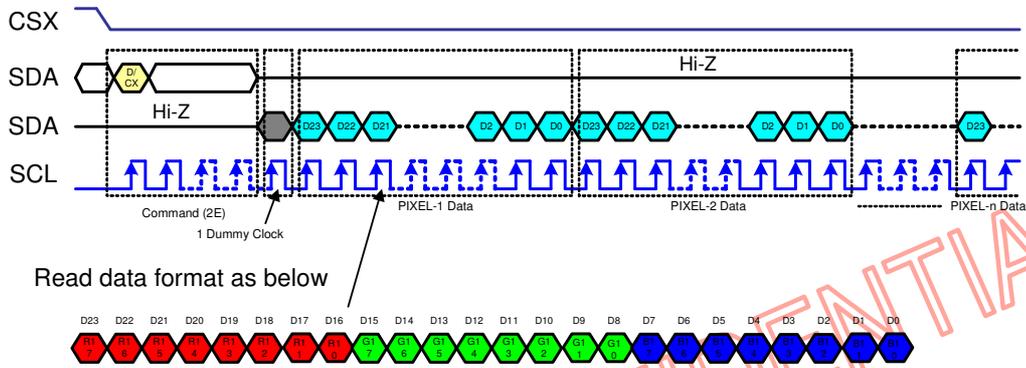
- 65K colors, RGB is 5-6-5-bit input



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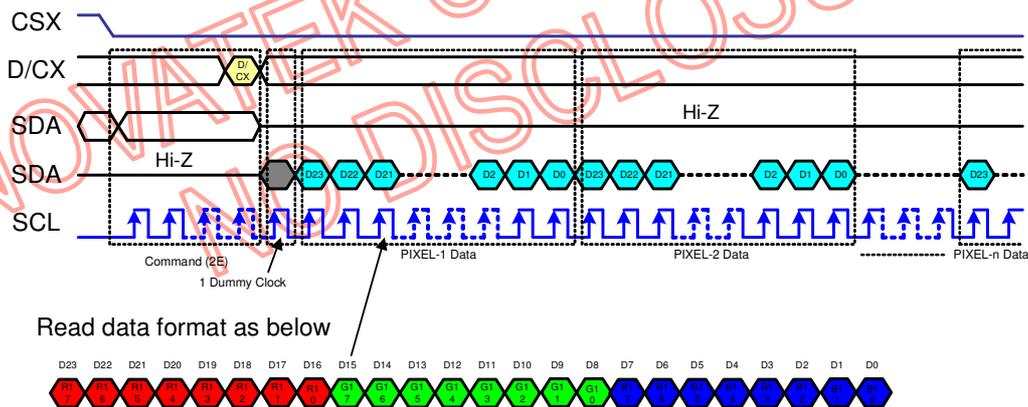
5.2.3.3 3-PINS SERIAL INTERFACE FOR DATA RAM READ

- Read data for RGB is 8-8-8-bit output



5.2.3.4 4-PINS SERIAL INTERFACE FOR DATA RAM READ

- Read data for RGB is 8-8-8-bit output



5.3 MIPI INTERFACE

5.3.1 Interface Type Selection

The selection of a given interfaces are done by setting IM3, IM2, IM1 and IM0 pins as show in **Table 5.3.1**

Table 5.3.1 Interface Type Selection

IM3	IM2	IM1	IM0	Interface	Read back selection
0	0	0	0	8080 MCU 8-bit Parallel	RDX strobe (8-bit read data and 8-bit read parameter)
0	0	0	1	8080 MCU 9-bit Parallel	RDX strobe (9-bit read data and 8-bit read parameter)
0	0	1	0	8080 MCU 16-bit Parallel	RDX strobe (16-bit read data and 8-bit read parameter)
0	0	1	1	8080 MCU 18-bit Parallel	RDX strobe (18-bit read data and 8-bit read parameter)
0	1	0	0	8080 MCU 24-bit Parallel	RDX strobe (24-bit read data and 8-bit read parameter)
1	1	0	0	SPI 3-pins serial	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
1	1	0	1	SPI 4-pins serial	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
1	0	0	1	RGB mode 1/2	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
1	1	1	0	MIPI	Follow MIPI Read Back Sequence
1	1	1	1	MDDI	Follow MDDI Read Back Sequence

Table 5.3.2 Pin Connection according to the Interface Type

IM3	IM2	IM1	IM0	Interface	RDX	WRX	DCX	Read back selection
0	0	0	0	8080 MCU 8-bit Parallel	RDX	WRX	DCX	D[23:8]: Unused, D7-D0: 8-bit Data
0	0	0	1	8080 MCU 9-bit Parallel	RDX	WRX	DCX	D[23:9]: Unused, D8-D0: 9-bit Data
0	0	1	0	8080 MCU 16-bit Parallel	RDX	WRX	DCX	D[23:16]: Unused, D15-D0: 16-bit Data
0	0	1	1	8080 MCU 18-bit Parallel	RDX	WRX	DCX	D[23:18]: Unused, D17-D0: 18-bit Data
0	1	0	0	8080 MCU 24-bit Parallel	RDX	WRX	DCX	D[23:0] : 24-bit Data
1	1	0	0	SPI 3-pins serial	Note 1	SCL	Note 1	D[23:0]: Unused, SDI, SDO, WRX pad: SCL
1	1	0	1	SPI 4-pins serial	Note 1	SCL	Note1	D[23:0]: Unused, SDI, SDO, WRX pad: SCL
1	0	0	1	RGB mode 1/2	Note 1	SCL	Note1	- SDI, SDO, DCX pad: SCL RGB mode 1/2 is selected by command via SPI.
1	1	1	0	MIPI	Note 1	Note 1	Note 1	D[23:0]: Unused, CLK_P/CLK_N, D0_P, D0_N
1	1	1	1	MDDI	Note 1	Note 1	Note 1	D[23:0]: Unused, CLK_P/CLK_N, D0_P/D0_N

Note1: Unused pins connected to VDDI.

5.3.2 MIPI

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

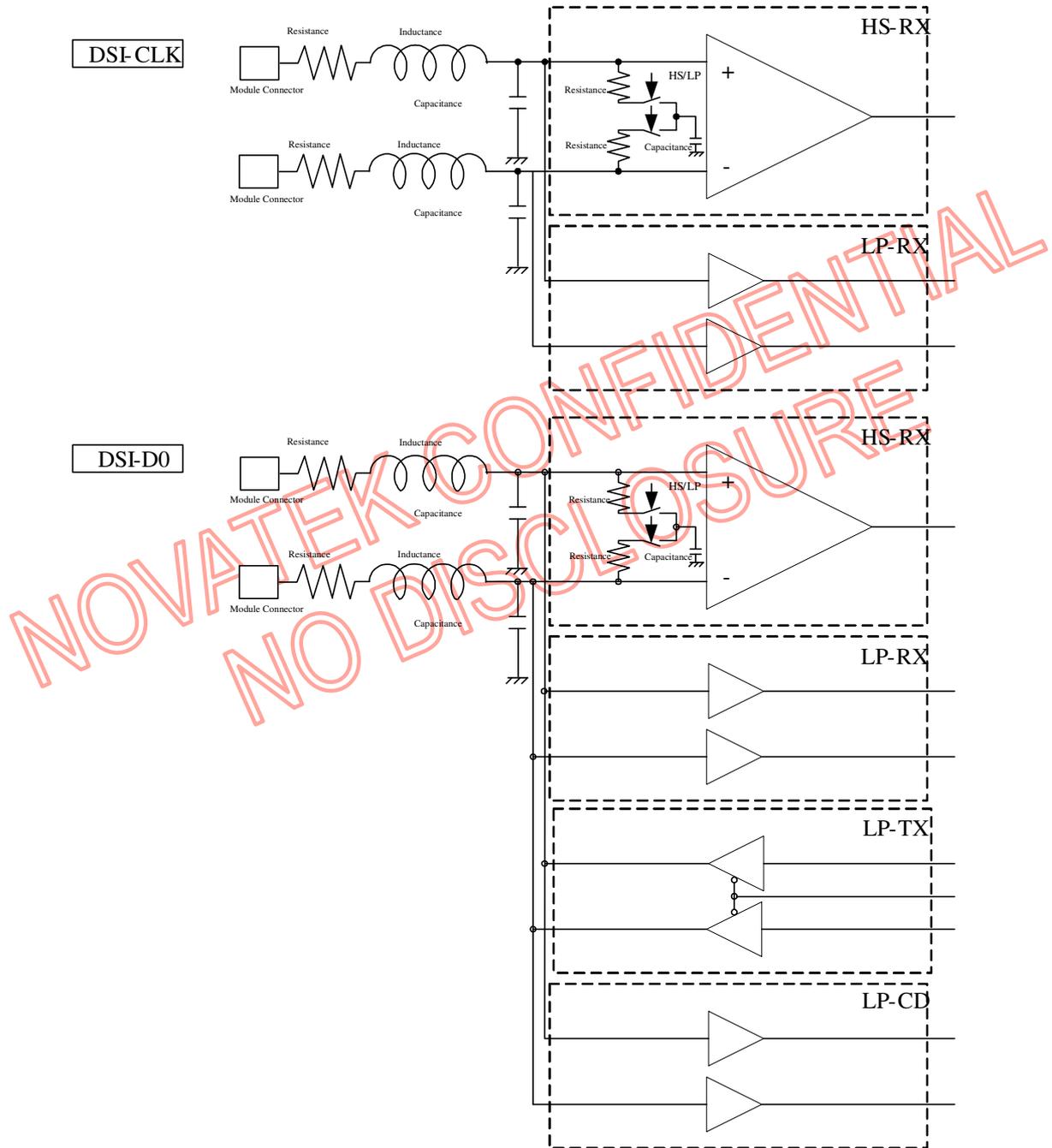
Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video Mode display modules also include a simplified form of Command Mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. Some Video Mode architectures may include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

Configuration:

	MCU (Master)	Display Module (Slave)
Clock Lane	Unidirectional Lane <ul style="list-style-type: none"> ■ Clock Only ■ Escape Mode(ULPS Only) 	Unidirectional Lane <ul style="list-style-type: none"> ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane 0	Bi-directional Lane <ul style="list-style-type: none"> ■ Forward High-Speed ■ Bi-directional Escape Mode ■ Bi-directional LPDT 	Bi-directional Lane <ul style="list-style-type: none"> ■ Forward High-Speed ■ Bi-directional Escape Mode ■ Bi-directional LPDT

5.3.3 Display Module Pin Configuration for DSI


5.3.4 Display Serial Interface (DSI)

5.3.4.1 GENERAL DESCRIPTION

Communication sequences between the MCU and the display module are described on chapter “5.3.2.3.3 Communication Sequences”.

The communication can be separated 2 different levels between the MCU and the display module:

- Low level communication what is done on the interface level
- High level communication what is done on the packet level

5.3.4.2 Interface Level Communication

5.3.4.2.1 General

The display module uses data and clock lane differential pairs for DSI (DSI-1M). Both differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode. There are used different modes and protocol in each mode when there is wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State Code	Line DC Voltage Levels		High Speed(HS)	Low-Power(LP)	
	D0+ -line	D0- -line	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

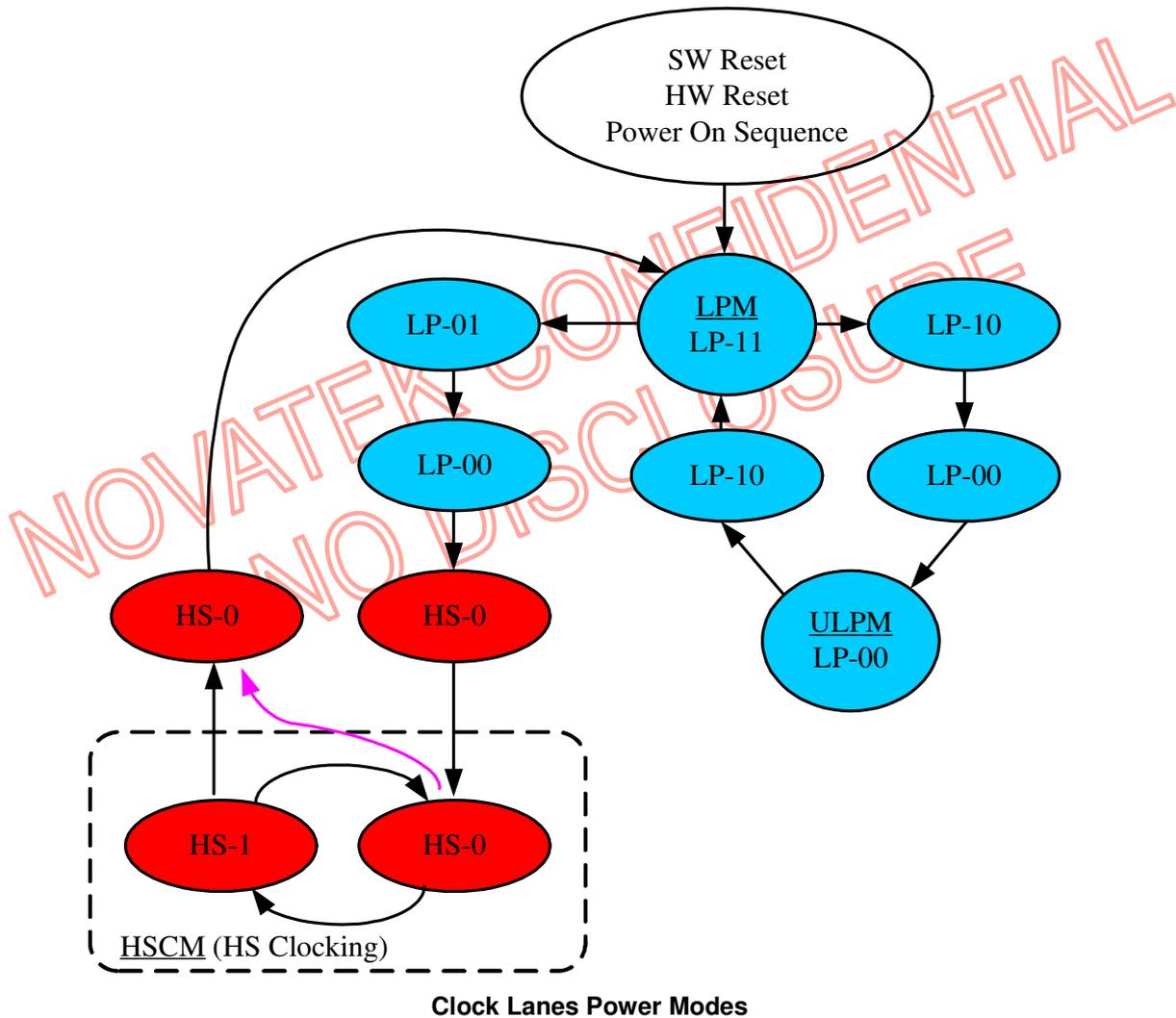
NOTES:

1. Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.
2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

5.3.4.2.2 DSI-CLK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM). Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPM). Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM). These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

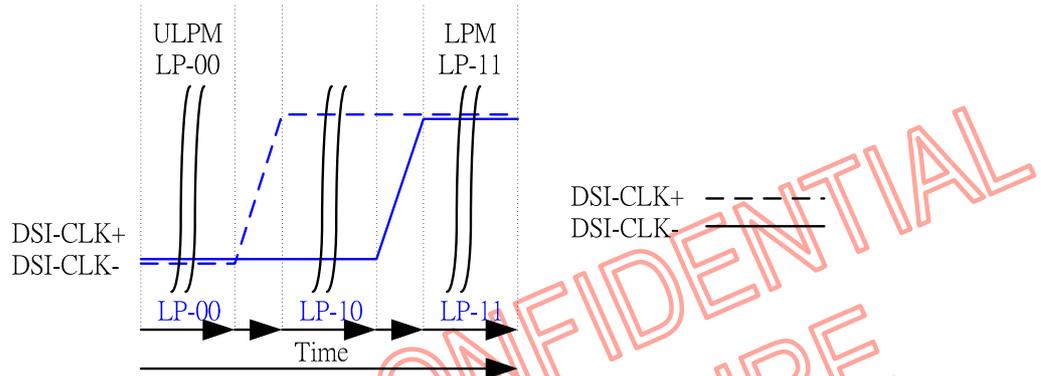
The principle flow chart of the different clock lanes power modes is illustrated below.



5.3.4.2.2.1 LOW POWER MODE (LPM)

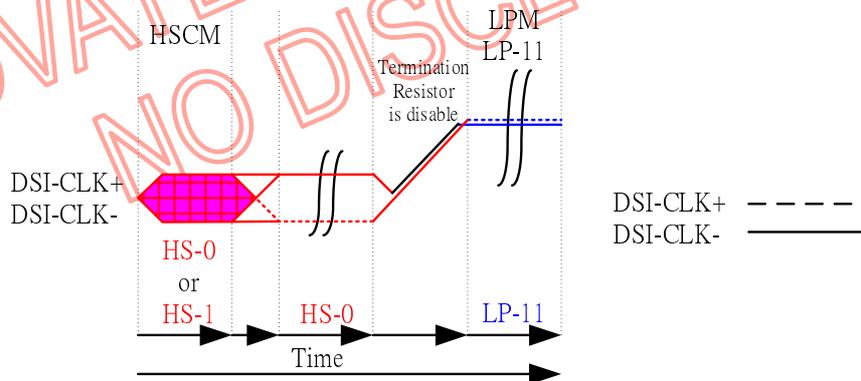
DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

- 1) After SW Reset, HW Reset or Power On Sequence =>LP-11
- 2) After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.



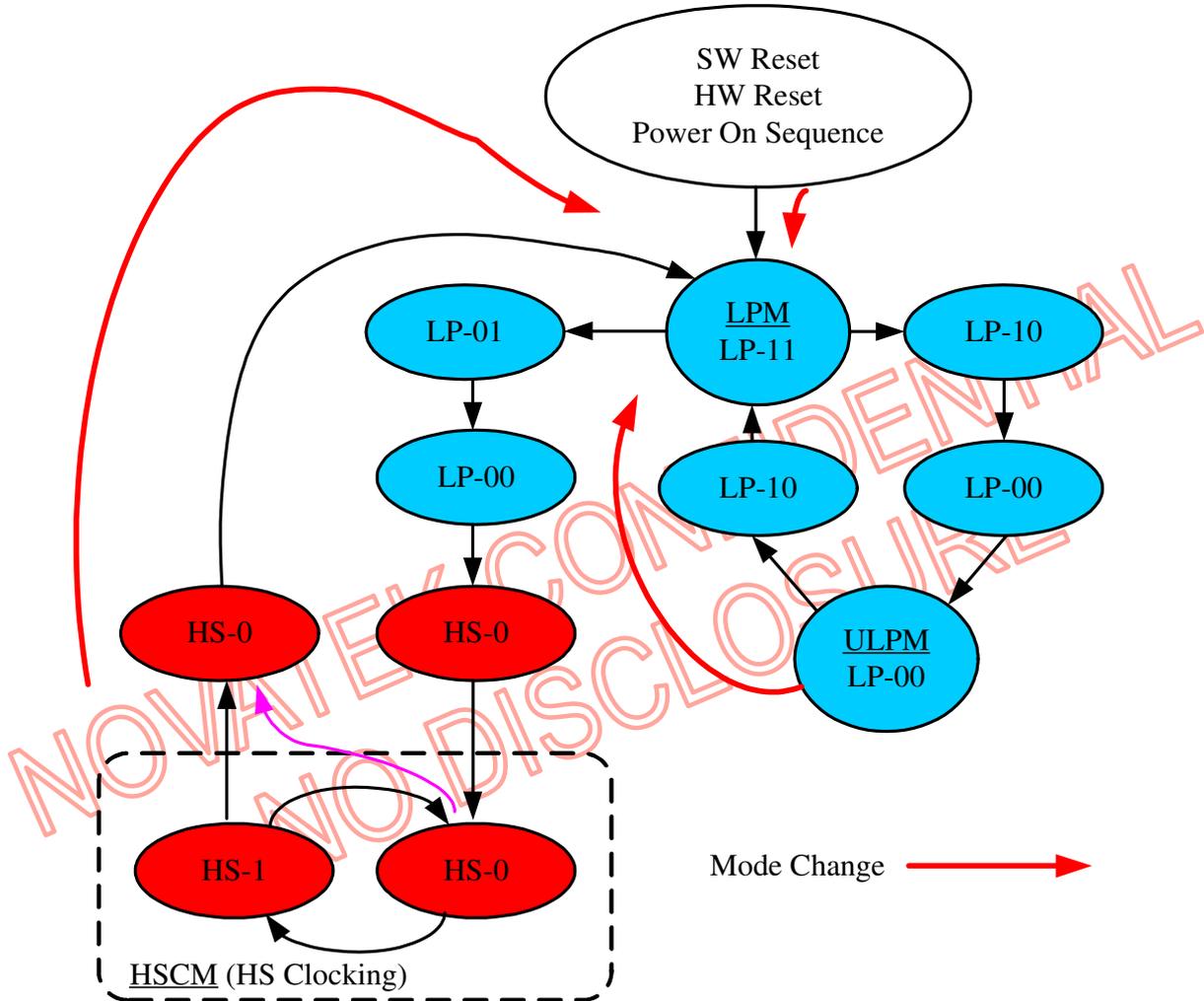
From ULPM to LPM

- 3) After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence is illustrated below.



From High Speed Clock Mode (HSCM) to LPM

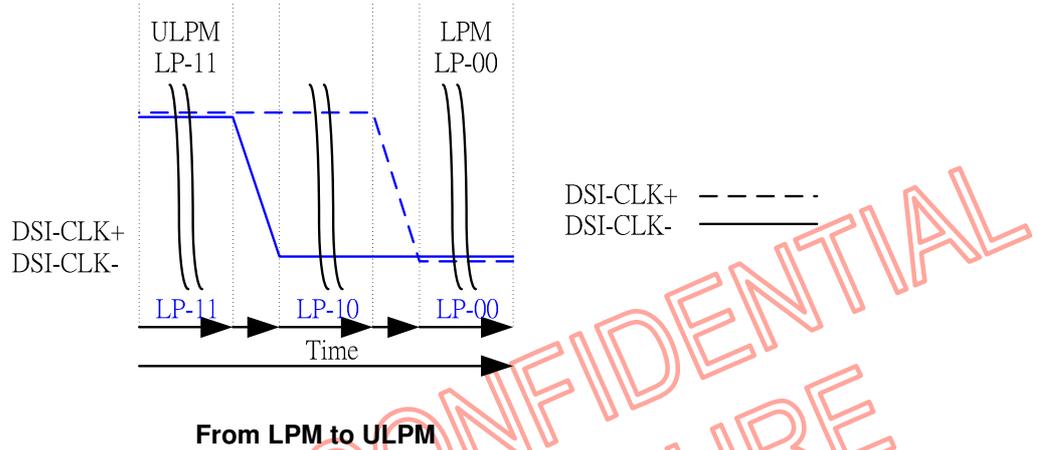
All three mode changes are illustrated a flow chart below.



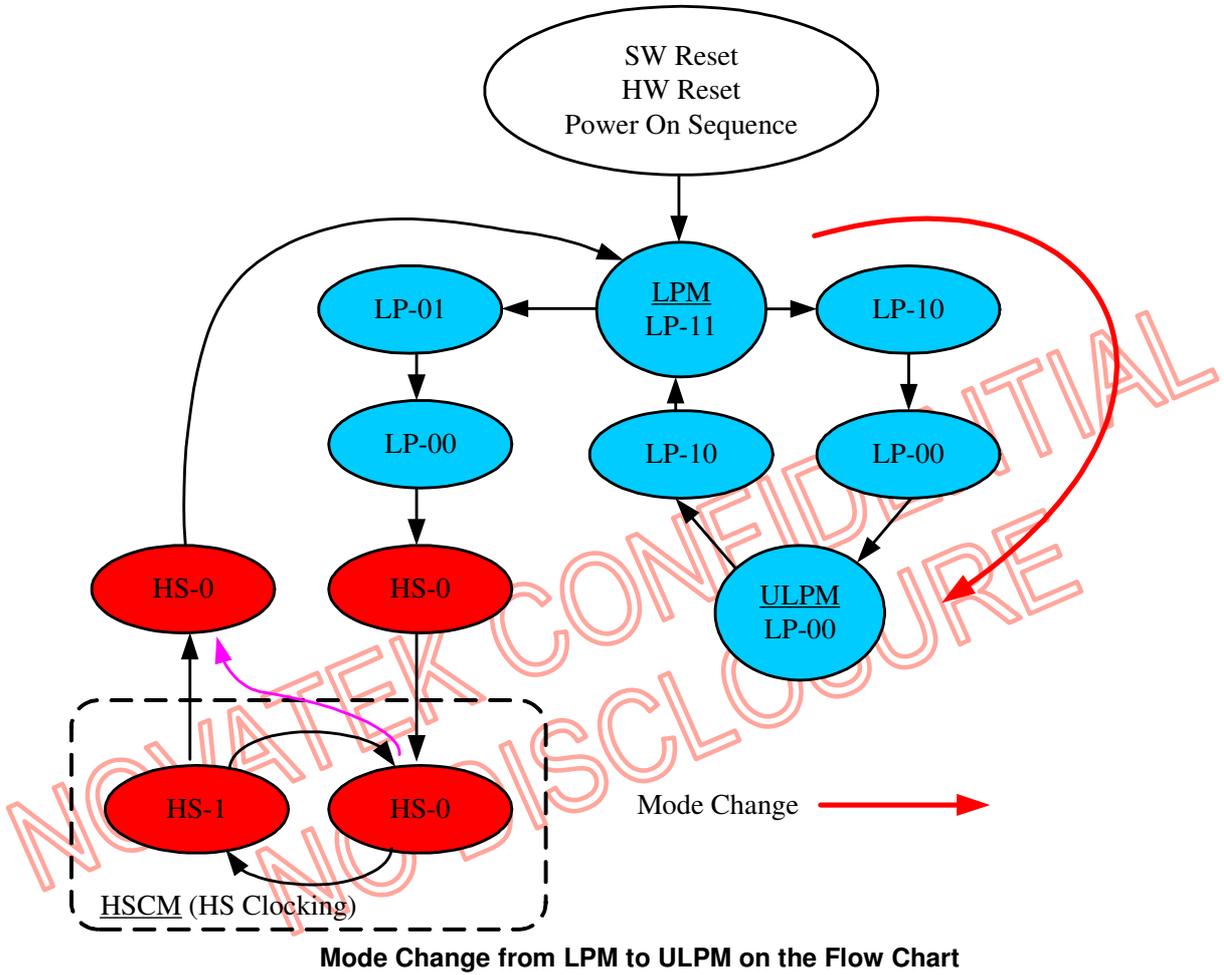
All Three Mode Change to LPM on the Flow Chart

5.3.4.2.2.2 ULTRA LOW POWER MODE (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State Code. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-10 =>LP-00 (ULPM). This sequence is illustrated below.

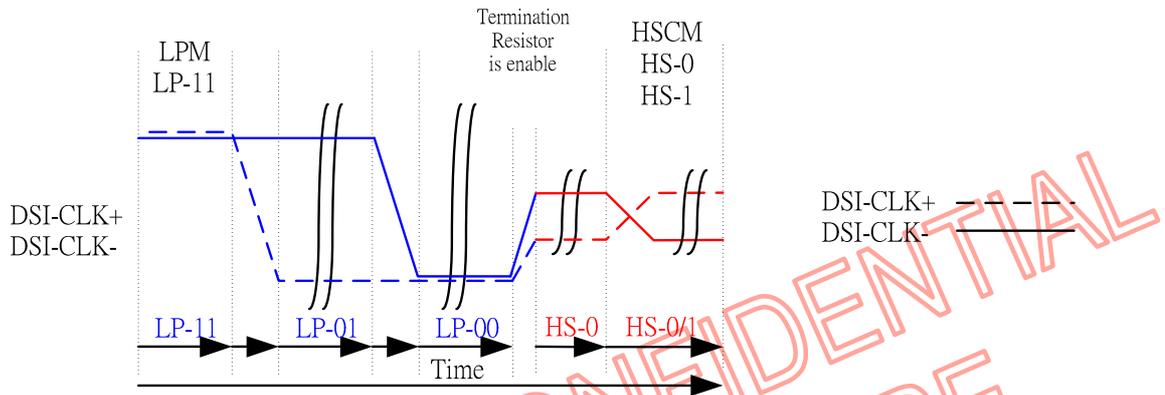


The mode change is also illustrated below.



5.3.4.2.2.3 HIGH SPEED CLOCK MODE (HSCM)

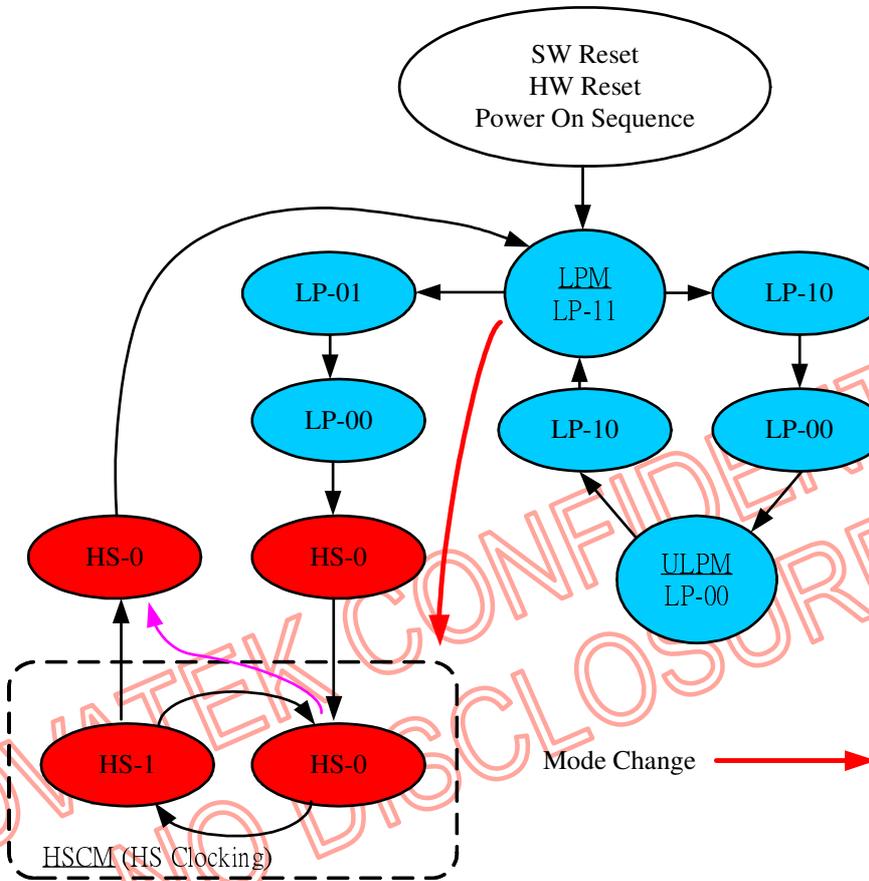
DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.



From LPM to HSCM

The mode change is also illustrated below.

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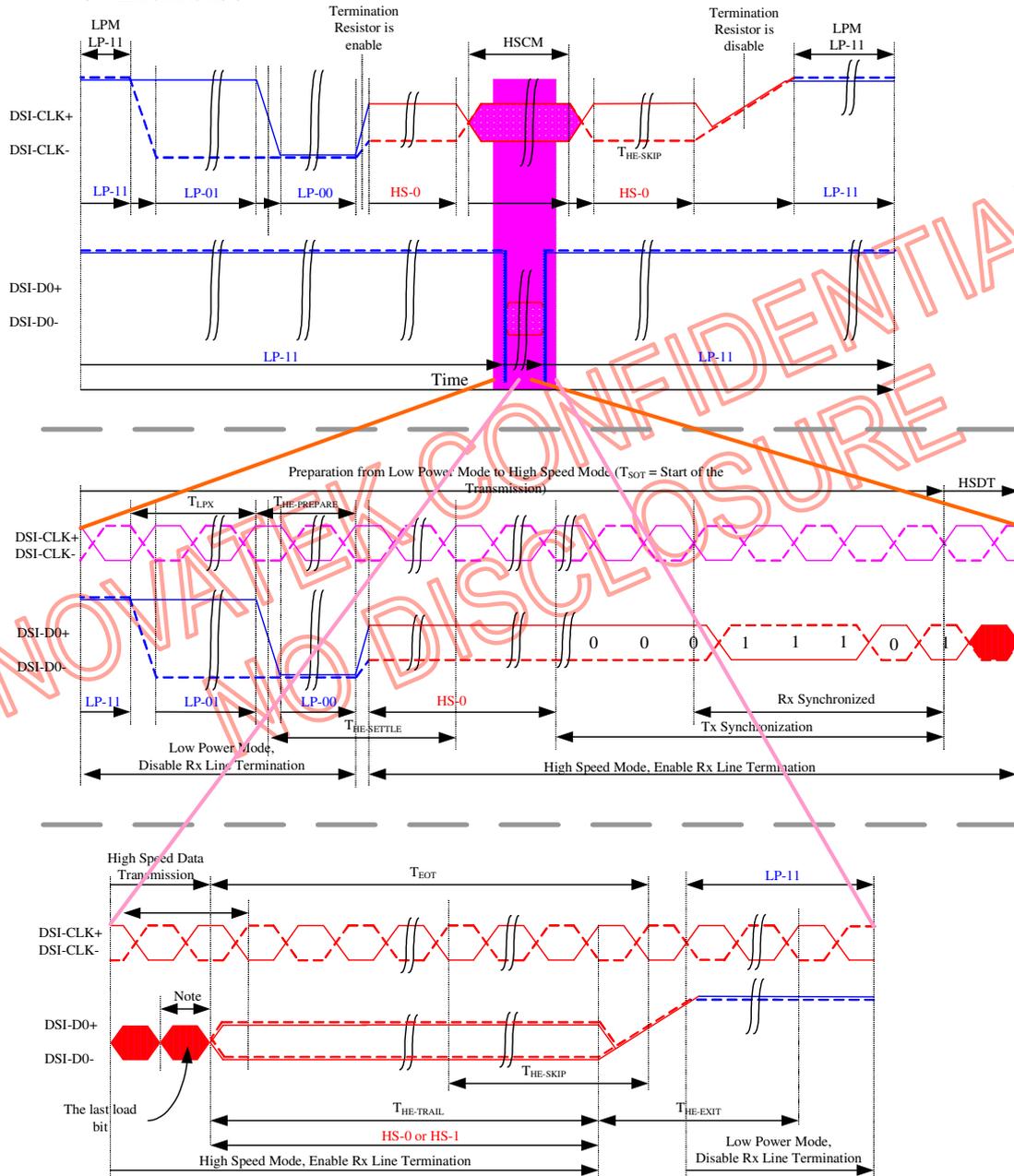
Mode Change from LPM to HSCM on the Flow Chart

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-D0+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped.

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The burst of the high speed clock consists of :

- Even number of transitions
- Start state is HS-0
- End state is HS-0



Note :
 If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
 If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

DSI-CLK+, DSI-D0+ -----
 DSI-CLK-, DSI-D0- _____

High Speed Clock Burst

5.3.4.2.3 DSI-Data Lanes

5.3.4.2.3.1 General

DSI-D0+/- Data Lanes can be driven in different modes which are:

- Escape Mode
- High-Speed Data Transmission
- Bus Turnaround Request

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11→LP-10→LP-00→LP-01→LP-00	LP-00→LP-10→LP-11(Mark-1)
High-Speed Data Transmission	LP-11→LP-01→LP-00→HS-0	(HS-0 or HS-1)→LP-11
Bus Turnaround Request	LP-11→LP-10→LP-00→LP-10→LP-00	High-Z

Notes:

1. DSI-D0+/- data lanes are used.
2. More information on section "Bus Turnaround (BTA)"

5.3.4.2.3.2 Escape Modes

Data lanes (DSI-D0+/-) can be used in different Escape Modes when data lanes are in Low Power (LP) mode.

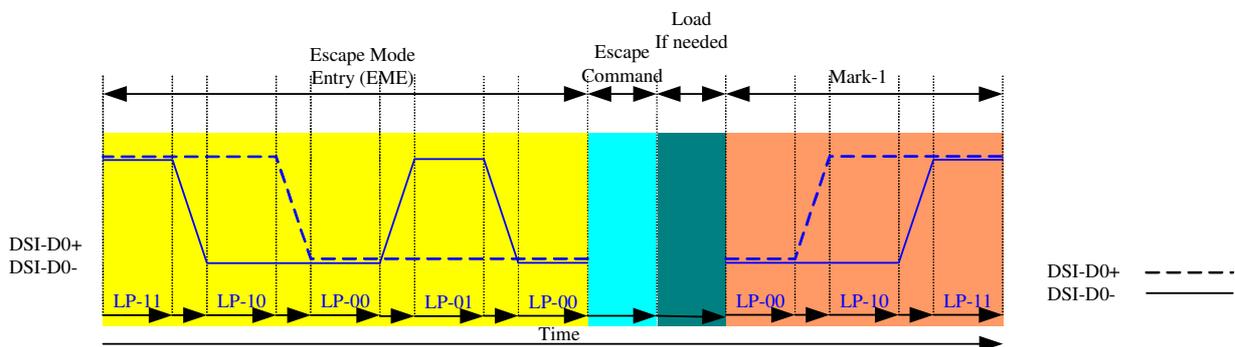
These Escape Modes are used to:

- Send "Low-Power Data Transmission" (LPDT) e.g. from the MCU to the display module
- Drive data lanes to "Ultra-Low Power State" (ULPS)
- Indicate "Remote Application Reset" (RAR), which is reset the display module
- Indicate "Tearing Effect" (TEE), which is used for a TE line event from the display module to the MCU
- Indicate "Acknowledge" (ACK), which is used for a non-error event from the display module to the MCU

The basic sequence of the Escape Mode is as follow

- Start: LP-11
- Escape Mode Entry (EME): LP-11→LP-10→LP-00→LP-01→LP-00
- Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00→LP-10→LP-11
- End: LP-11

This basic construction is illustrated below:



General Escape Mode Sequence

The number of the different Escape Commands (EC) is eight. These eight different escape commands (EC) can be divided 2 different groups: Mode or Trigger. The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode. The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

Escape commands are defined on the next table.

This basic construction is illustrated below:

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit → Last Bit Transmitted)
Low-Power Data Transmission	Mode	1110 0001 _{bin}
Ultra-Low Power Mode	Mode	0001 1110 _{bin}
Underfined-1, Note	Mode	1001 1111 _{bin}
Underfined-2, Note	Mode	1101 1110 _{bin}
Remote Application Reset	Trigger	0110 0010 _{bin}
Tearing Effect	Trigger	0101 1101 _{bin}
Acknowledge	Trigger	0010 0001 _{bin}
Unknow-5, Note	Trigger	1010 0000 _{bin}

Note: This Escape command support has not been implemented on the display module.

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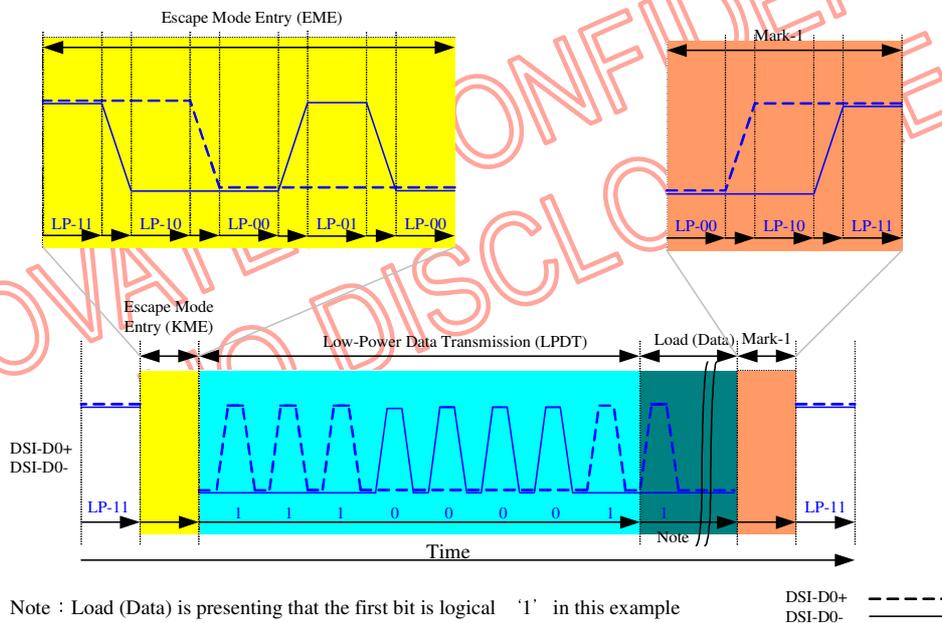
Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

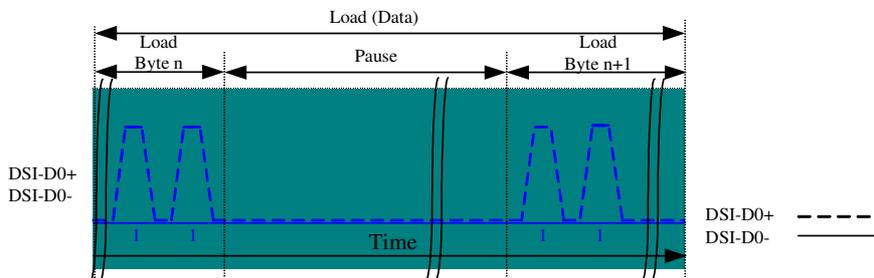
The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11→LP-10→LP-00→LP-01→LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Load (Data):
 - One or more bytes (8 bit)
 - Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
- Mark-1: LP-00→LP-10→LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Low-Power Data Transmission (LPDT)



Pause (Example)

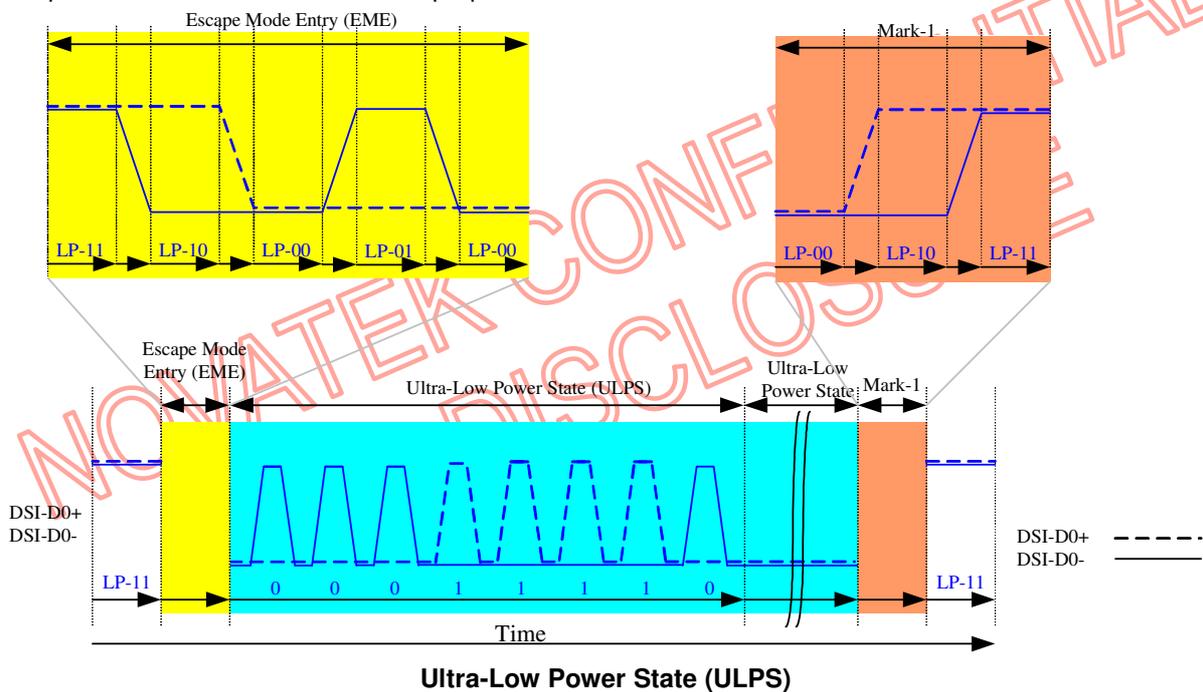
Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11→LP-10→LP-00→LP-01→LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00→LP-10→LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



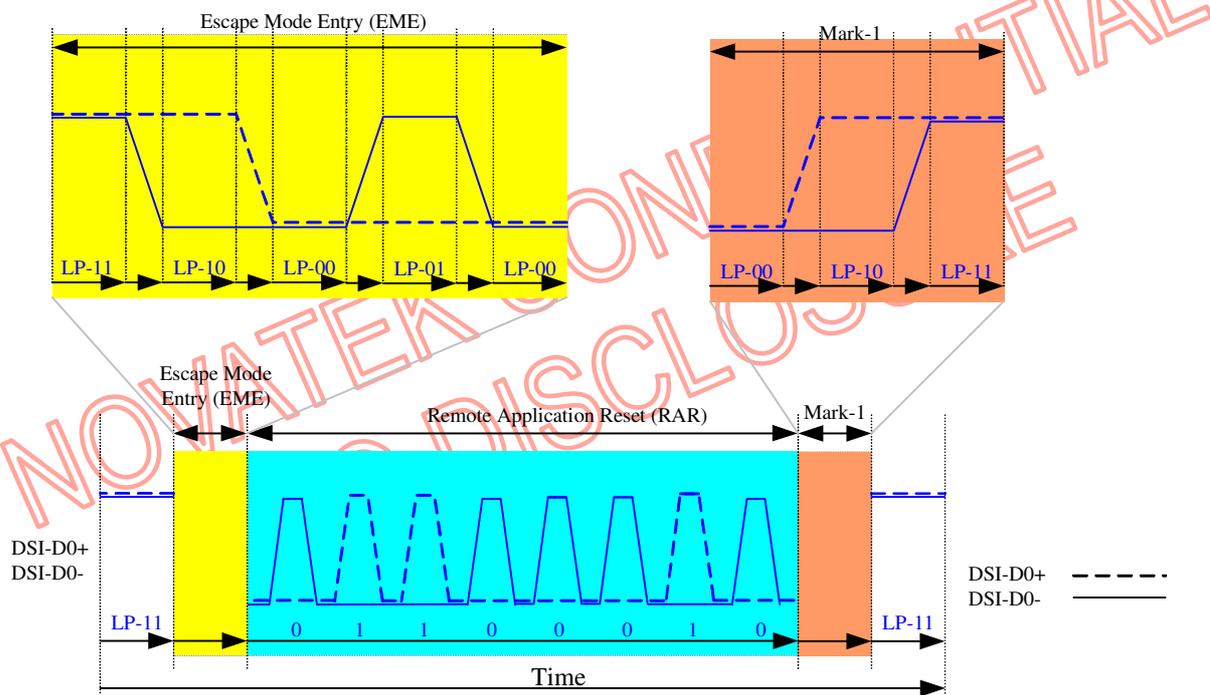
Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11→LP-10→LP-00→LP-01→LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00→LP-10→LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Remote Application Reset (RAR)

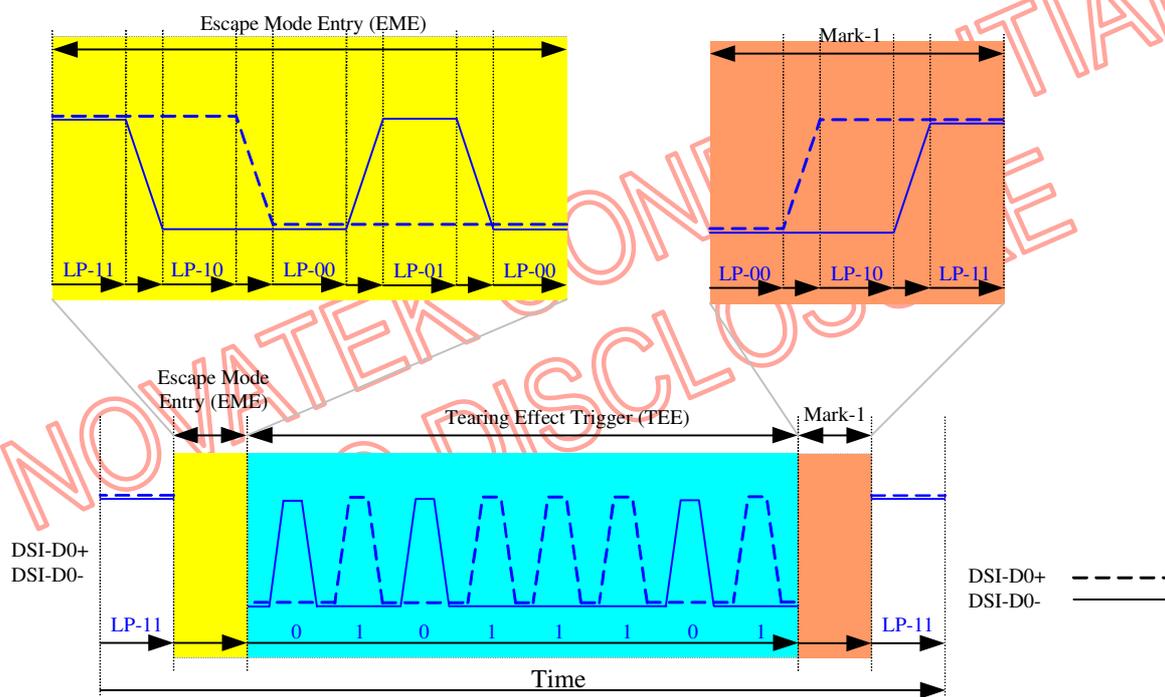
Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11→LP-10→LP-00→LP-01→LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00→LP-10→LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Tearing Effect (TEE)

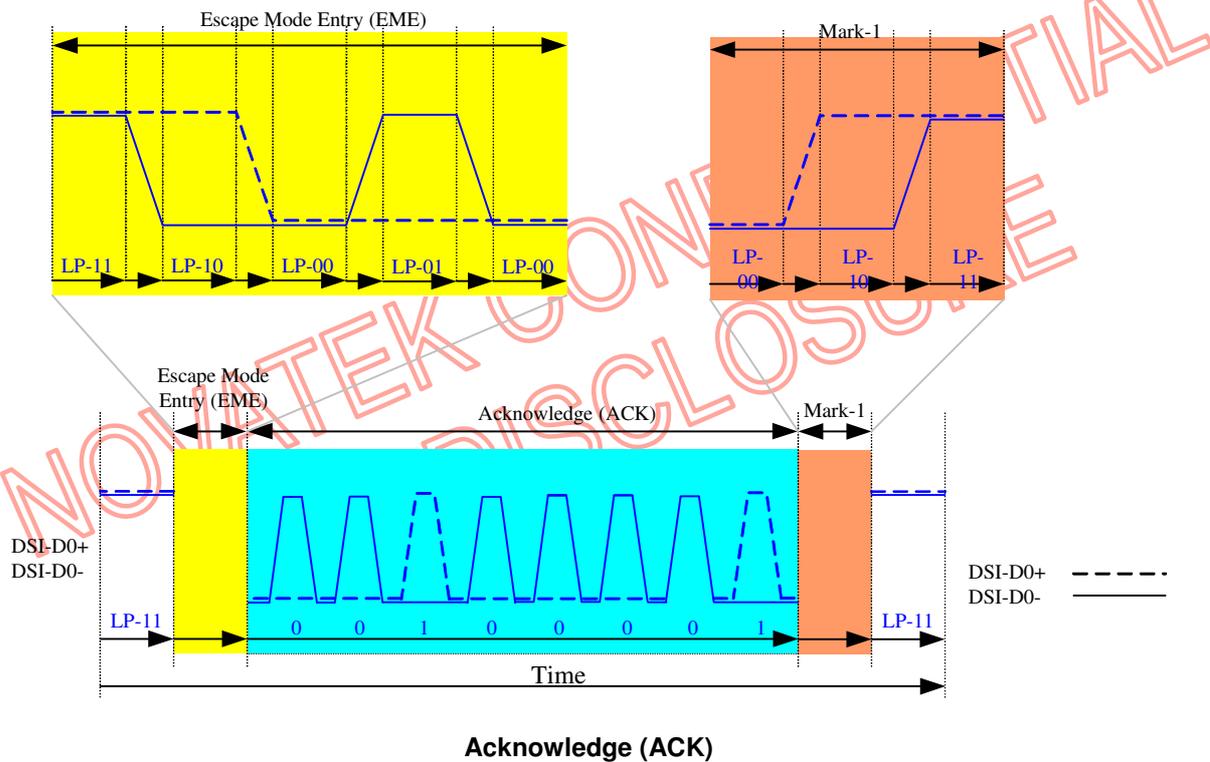
Acknowledge (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11→LP-10→LP-00→LP-01→LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00→LP-10→LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



5.3.4.2.3.3 HIGH SPEED DATA TRANSMISSION (HSDT)

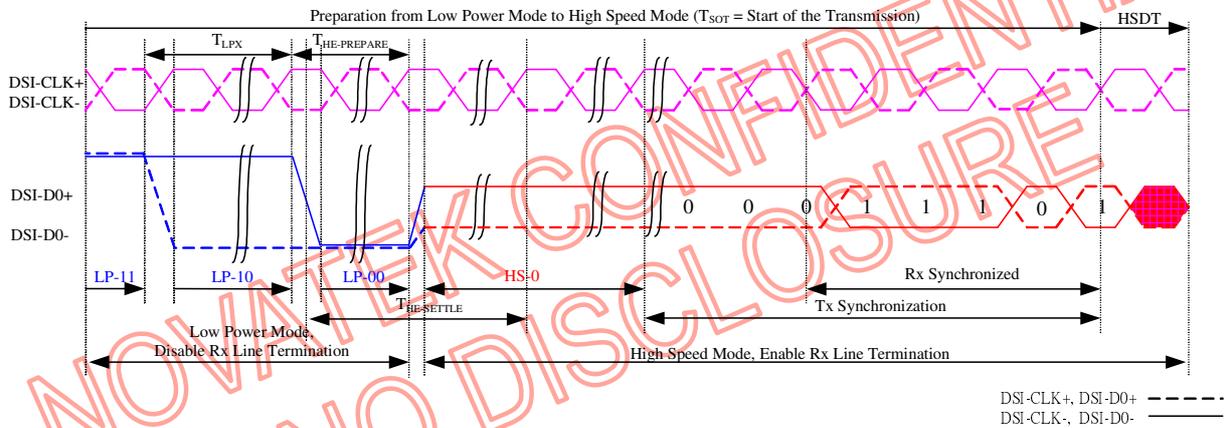
Entering High-Speed Data Transmission (T_{SOT} of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter "5.3.4.2.2.3 High-Speed Clock Mode (HSCM)".

Data lanes of the display module are entering (T_{SOT}) in the High-Speed Data Transmission (HSDT) as follows

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 → HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below



Entering High-Speed Data Transmission (T_{SOT} of HSDT)

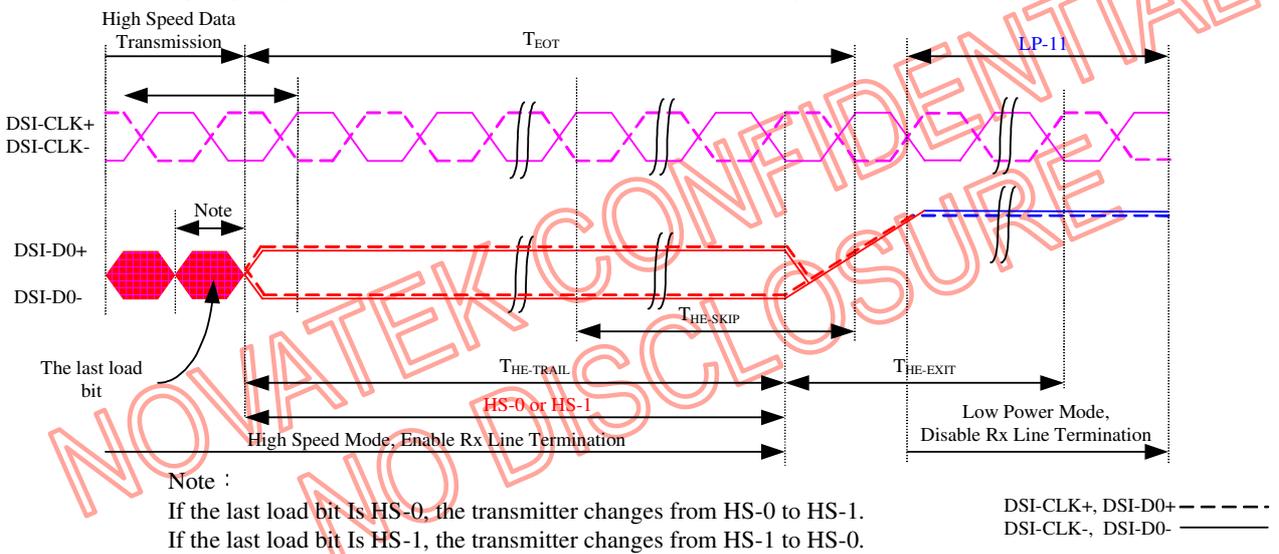
Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DSI-CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes are in LP-11 mode. See more information on chapter "5.3.4.2.2.3 High-Speed Clock Mode (HSCM)".

Data lanes of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
 - MCU changes to HS-1, if the last load bit is HS-0
 - MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below

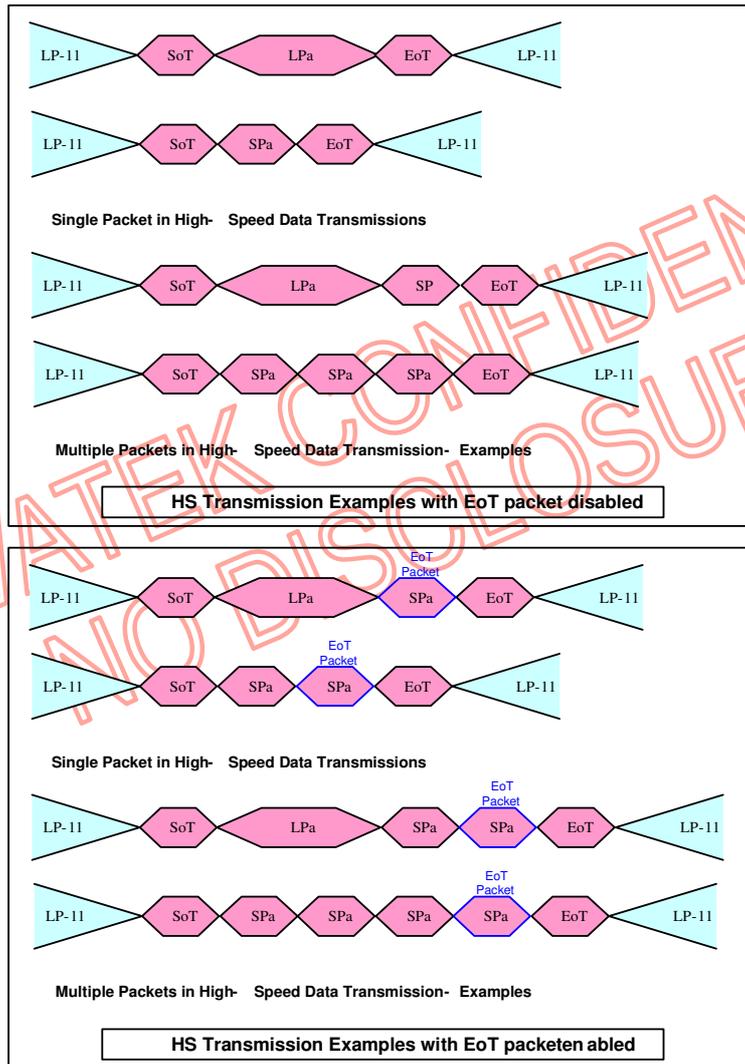


Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter “5.3.4.3.1 Short Packet (SPa) and Long Packet (LPa) Structures”.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.



Abbreviation	Explanation
EoT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Data lanes are '1's (Stop Mode)
SPa	Short Packet
SoT	Start of the Transmission

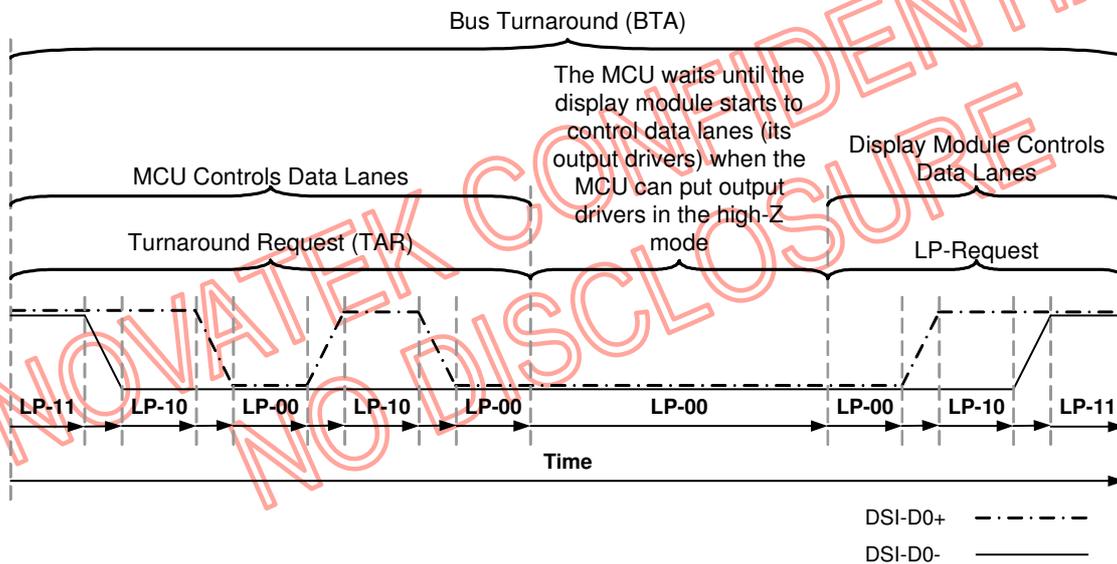
Bus Turnaround (BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU or display module are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follow.

- Start (MCU):LP-11
- Turnaround Request (MCU): LP-11 → LP-10 → LP-00 → LP-10 → LP-00
- The MCU wait until the display module is starting to control DSI-D0+/- data lanes and the MCU stop to control DSI-D0+/- data lanes (=High-Z)
- The display module changes to the stop mode: LP-00 → LP-10 → LP-11

The same bus turnaround .procedure (From the MCU to the display module) is illustrated below.



Bus Turnaround Procedure

MCU and the display module terms are switched on above figure, if the Bus Turnaround (BTA) is from the display module to the MCU..

5.3.4.3 Packet Level Communication**5.3.4.3.1 Short Packet (SPa) and Long Packet (LPa) Structure**

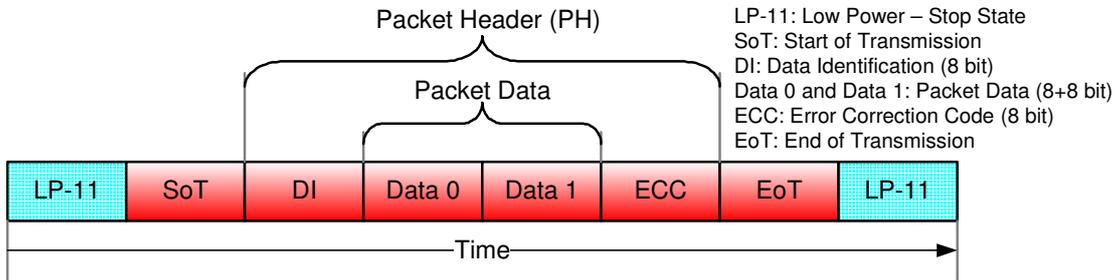
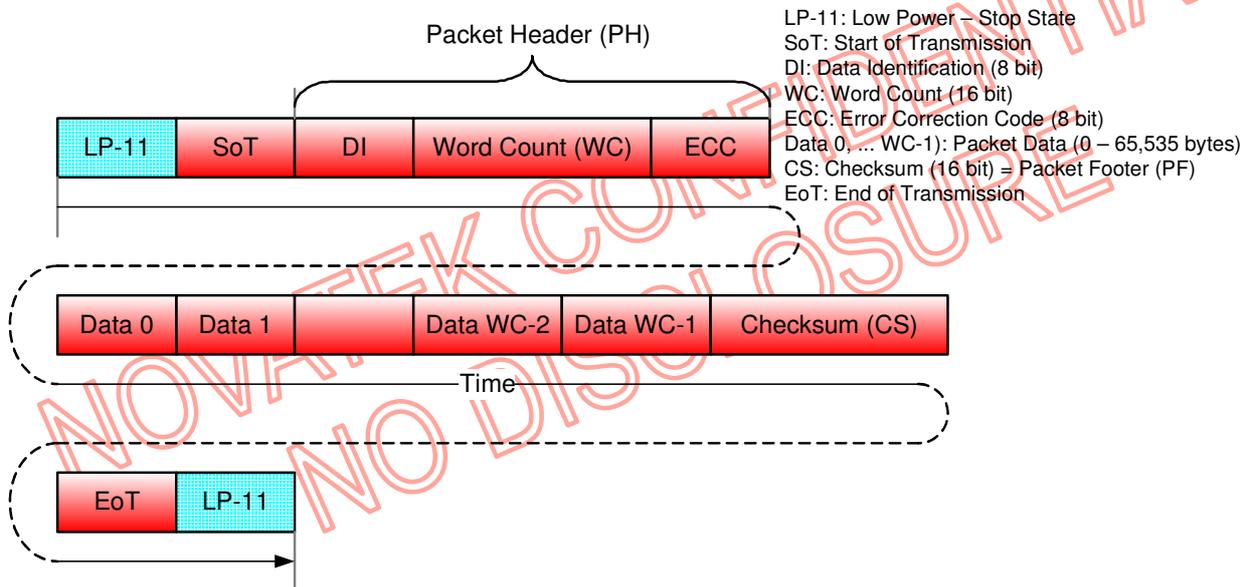
Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

The lengths of the packets are

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

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Short Packet (SPa) Structure

Long Packet (LPa) Structure
Note:

Short Packet (SPa) Structure and Long Packet (LPa) Structure are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sendings).

The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format e.g.

* LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11

* LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11

* LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11

5.3.4.3.1.1 Bit Order of the Byte on Packets

The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last.

This same order is illustrated for reference purposes below.



Bit Order of the Byte on Packets

5.3.4.3.1.2 Bit Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.



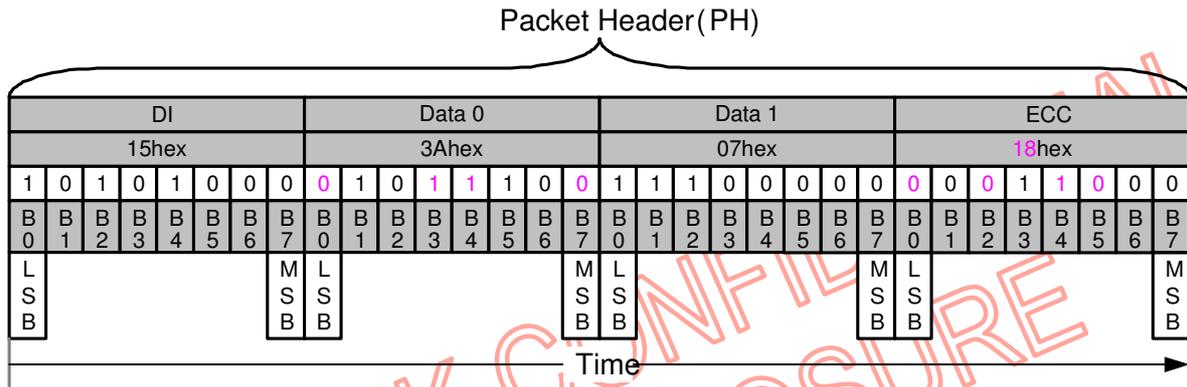
Byte Order of the Multiple Byte on Packets

5.3.4.3.1.3 Packet Header (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

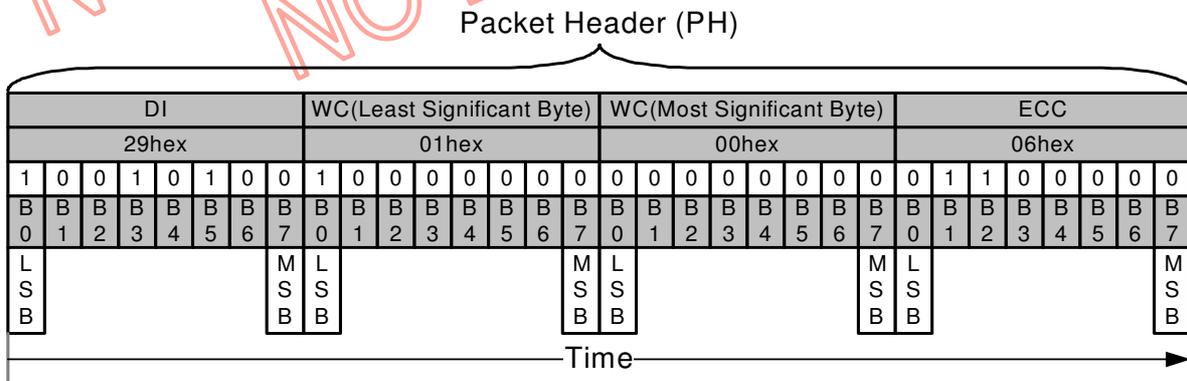
- 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)



Packet Header (PH) on Short Packet (SPa)

Long Packet (LPa):

- 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)
- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)



Packet Header (PH) on Long Packet (LPa)

Data Identification (DI)

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

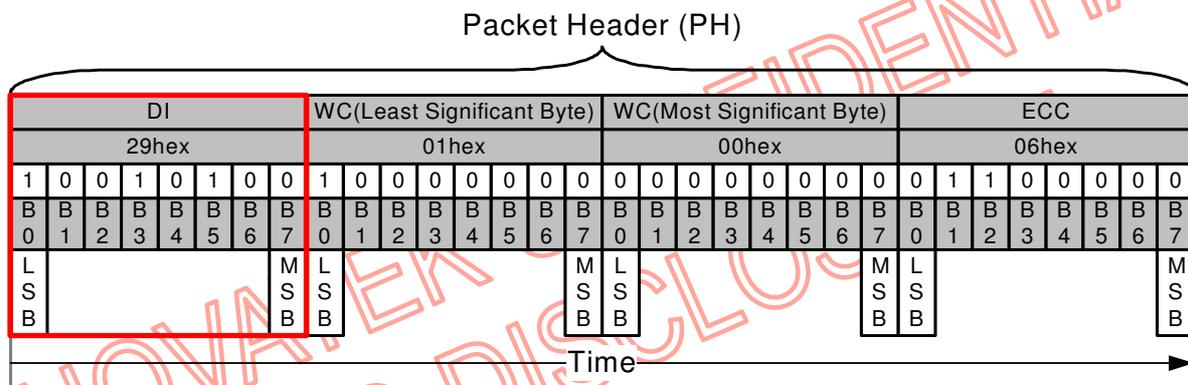
- Virtual Channel (VC), 2 bits, DI[7...6]
- Data Type (DT), 6 bits, DI[5...0]

The Data Identification (DI) structure is illustrated on a table below.

Data Identification (DI) Structure

Data Identification (DI)							
Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

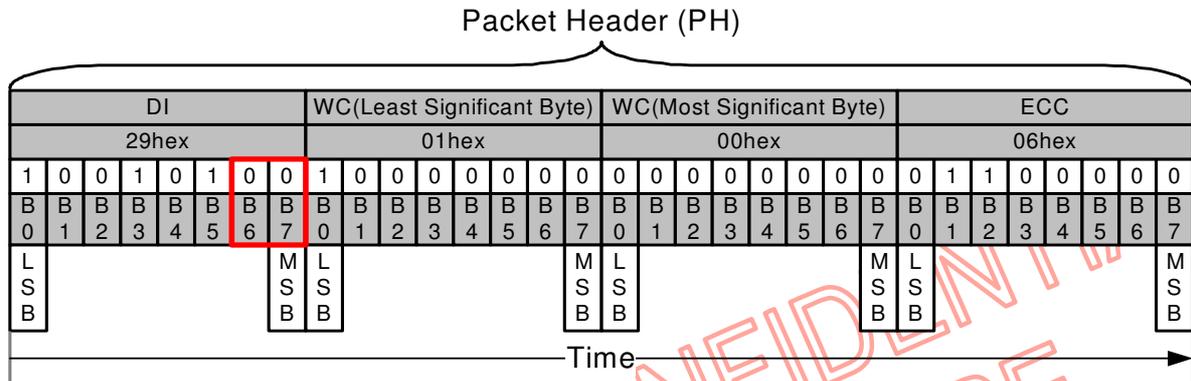
Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.


Data Identification (DI) on the Packet Header (PH)

Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI[7...6]) structure and it is used to address where a packet is wanted to send from the MCU.

Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

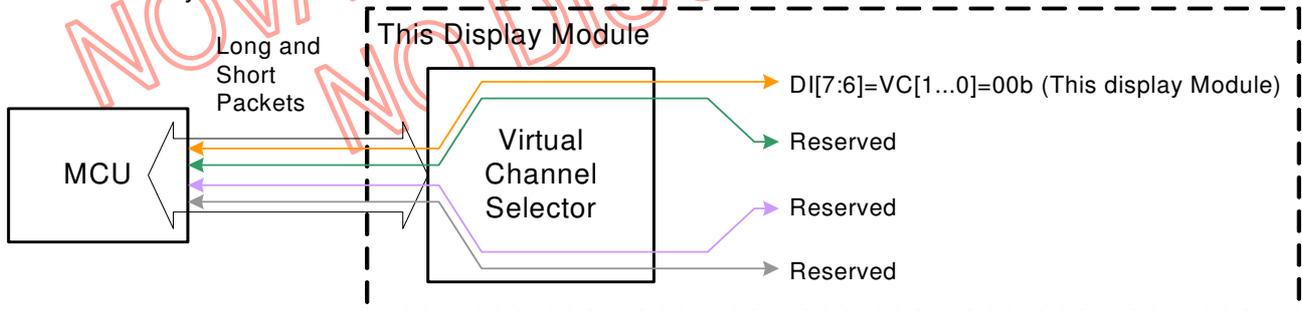


Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules. Devices are using the same virtual channel what the MCU is using to send packets to them e.g.

- The MCU is using the virtual channel 0 when it sends packets to this display module
- This display module is also using the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.



Virtual Channel (VC) Configuration

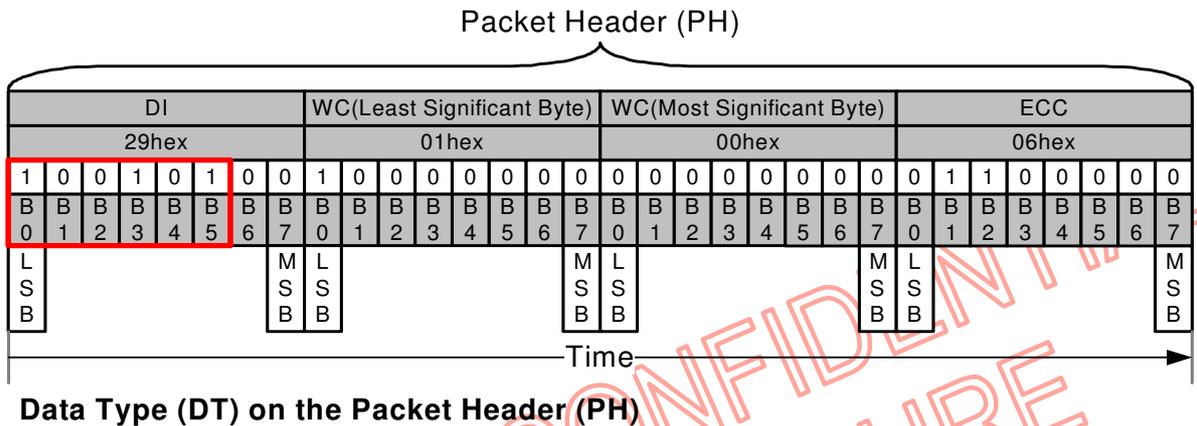
Virtual Channel (VC) always 0 (D[7...6]=VC[1...0]000b) when the MCU is sending "End of Transmission Packet" to the display module. See section "End of Transmission Packet (EoTP)

This display module is not supporting the virtual channel selector for other device (1 to 3) when only possible virtual channel (VC[1...0]) is 00b for this display module.

Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5...0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.



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This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa.

These Data Type (DT) are defined on tables below.

Data Type (DT) from MCU to the Display Module (or Other Devices)

Data Type Hex	Data Type Binary	Description	Packet Size	Note
08h	00 1000	End of Transmission packet	Short	1
05h	00 0101	DCS WRITE, no parameters	Short	
15h	01 0101	DCS WRITE, 1 parameter	Short	
06h	00 0110	DCS READ, no parameters	Short	
37h	11 0111	Set Maximum Return Packet Size	Short	
09h	00 1001	Null Packet, no data	Long	2
39h	11 1001	DCS Long Write/Write_LUT Command Packet	Long	
01h	00 0001	Sync Event, V Sync Start	Short	7
11h	01 0001	Sync Event, V Sync End	Short	7
21h	10 0001	Sync Event, H Sync Start	Short	7
31h	11 0001	Sync Event, H Sync End	Short	7
02h	00 0010	Color mode (CM) Off Command	Short	7
12h	01 0010	Color mode (CM) On Command	Short	7
22h	10 0010	Shut Down Peripheral Command	Short	7
32h	11 0010	Turn On Peripheral Command	Short	7
13h	01 0011	Generic Short Write, 1 parameter	Short	3,4,8
23h	10 0011	Generic Short Write, 2 parameter	Short	3,5,8
29h	10 1001	Generic Long Write	Long	3,8
14h	01 0100	Generic Read, 1 parameter	Short	3,4,8
24h	10 0100	Generic Read, 2 parameter	Short	3,5,8
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long	7
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long	7
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long	7
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long	7

Notes:

1. This can be used when the MCU wants to secure that there is the end of transmission in High Speed Data Transmission (HSDT) mode.
2. This can be used when the data lanes are wanted to keep in High Speed Data Transmission (HSDT) mode.
3. The receiver process packets with data type (Generic Write/Read) the same way as data type (DCS Write / Read).
4. Generic Write/Read with 1 parameter: Payload Bytes = Command + 00h.
5. Generic Write/Read with 2 parameter: Payload Bytes = Command + Parameter.
6. The receiver will ignore packets with data type that neither listed in table above nor in MIPI DSI spec.
7. The data type for Video Mode Communication: 01h, 11h, 21h, 31h, 02h, 12h, 22h, 32h, 0Eh, 1Eh, 2Eh, 3Eh will be disable (ignored packet) if bit DSIM of command B0h is set to "0".
8. The data type for Generic write/read: 13h, 23h, 29h, 14h, 24h will be disable (ignored packet) if bit DSIG of command B0h is set to "0".

Data Type (DT) from the Display Module (or Other Devices) to the MCU

From the Display Module (or Other Devices) to the MCU										
Hex	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description	Short/Lng Packet	Abbreviation	Note
02h	0	0	0	0	1	0	Acknowledge with Error Report	Short	AwER	
1Ch	0	1	1	1	0	0	DCS Read Long Response	Long	DCSRR-L	
21h	1	0	0	0	0	1	DCS Read Short Response, 1 byte returned	Short	DCSRR1-S	
22h	1	0	0	0	1	0	DCS Read Short Response, 2 byte returned	Short	DCSRR2-S	
1Ah	0	1	1	0	1	0	Generic Read Long Response	Long	GENRR-L	Note
11h	0	1	0	0	0	1	Generic Read Short Response, 1 byte returned	Short	GENRR1-S	Note
12h	0	1	0	0	1	0	Generic Read Short Response, 2 byte returned	Short	GENRR2-S	Note

The receiver will ignore other Data Type (DT) if they are not defined on tables: “Data Type (DT) from the MCU to the Display Module (or Other Devices)” or “Data Type (DT) from the Display Module (or Other Devices) to the MCU”.

Note: The data type for Generic write/read: 1Ah, 11h, 12 will be disable (ignored packet) if bit DSIG of command B0h is set to “0”.

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Packet Data (PD) on the Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

The Word Count (WC) indicates the number of Bytes of Packet of Packet Data (PD) send after the Packet Header.

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

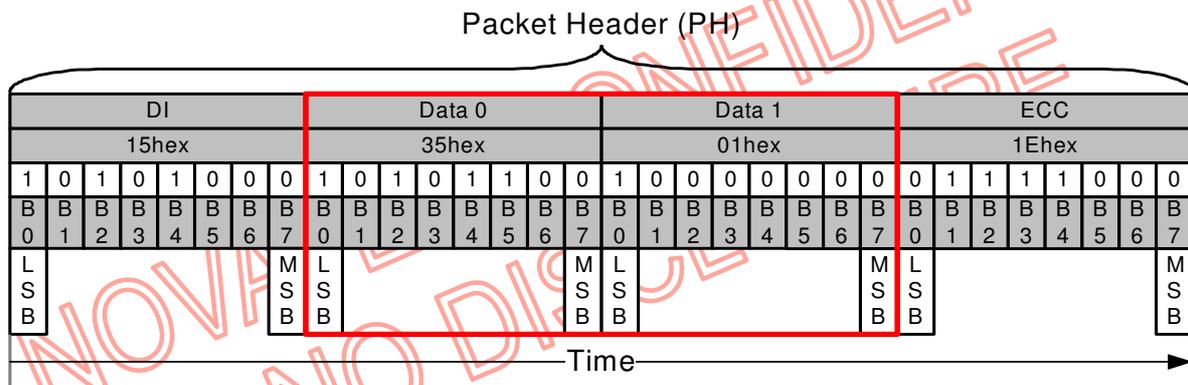
Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

Bits of Data 1 are set to '0' if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

Packet Data (PD) information:

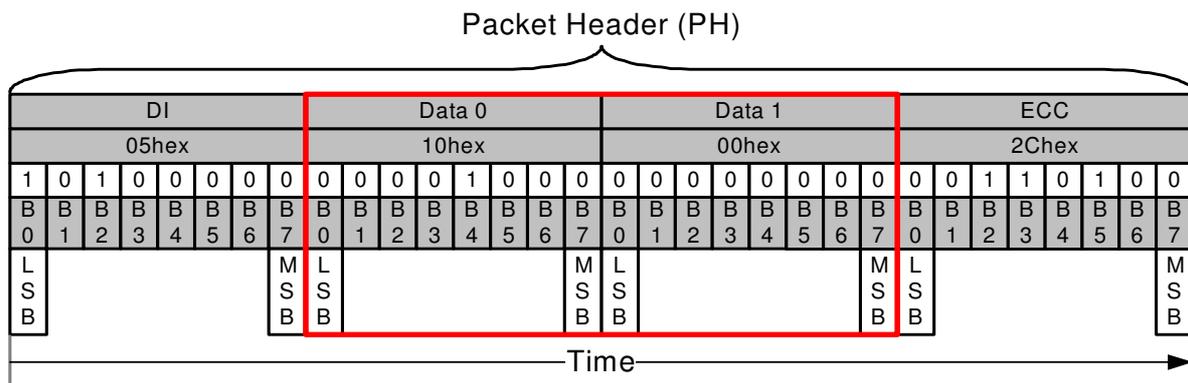
- Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI(Data Type (DT)) = 15hex)
- Data 1: 01hex (DCS's parameter)



Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

- Data 0: 10hex (DCS without parameter => DI(Data Type (DT)) = 05hex)
- Data 1: 00hex (Null)



Packet Data (PD) for Short Packet (SPa), 1 Bytes Information

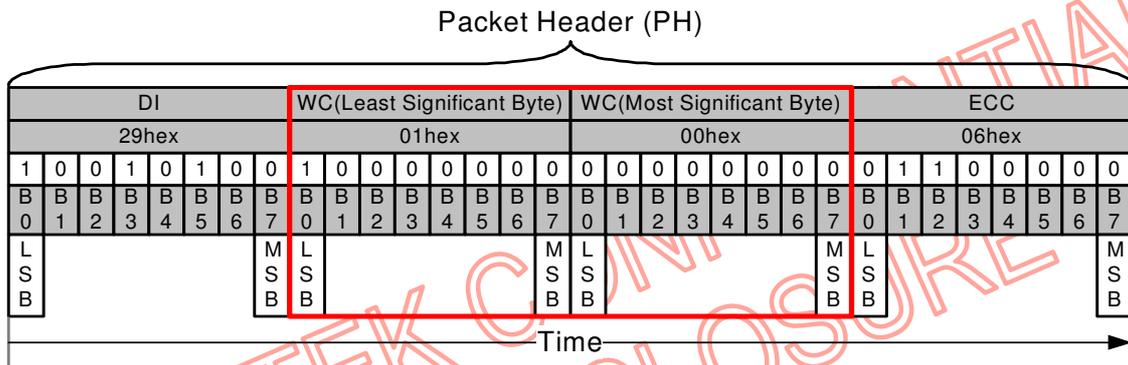
Word Count (WC) on the Long Packet (LPa)

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

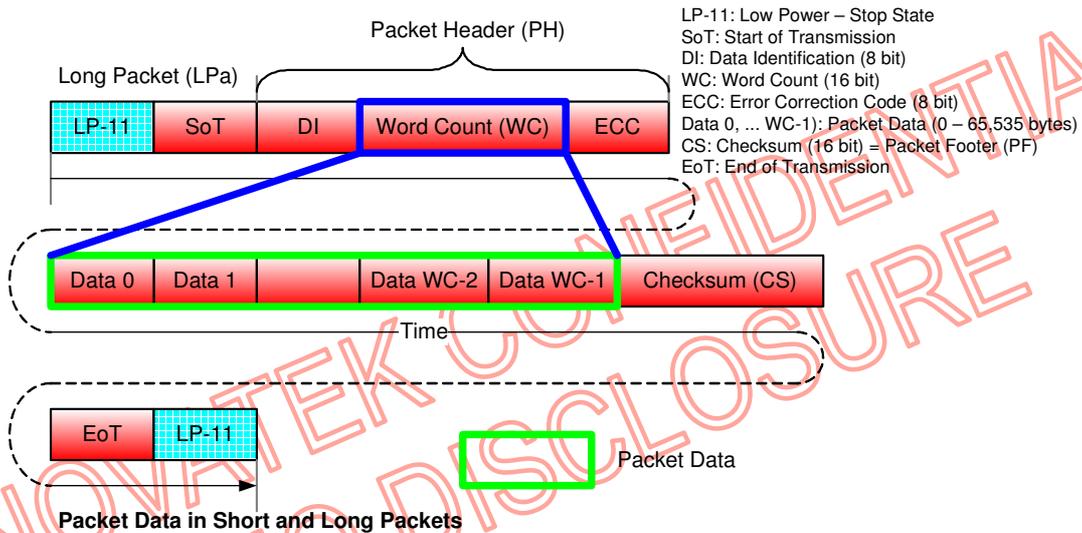
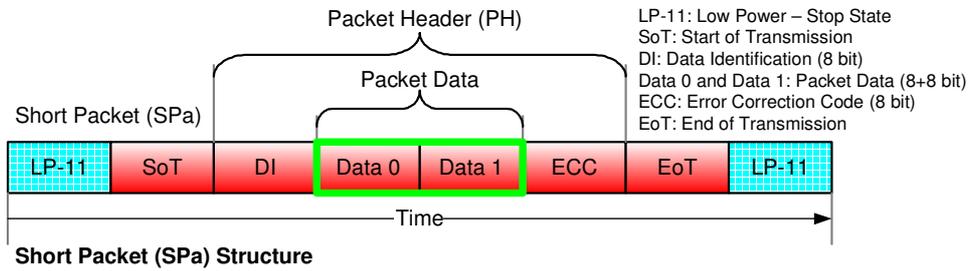
Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH).

Word Count (WC) of the Long Packet (LPa) consists of 2 bytes. The word count value should be greater than 1. These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.



Word Count (WC) on the Long Packet (LPa)



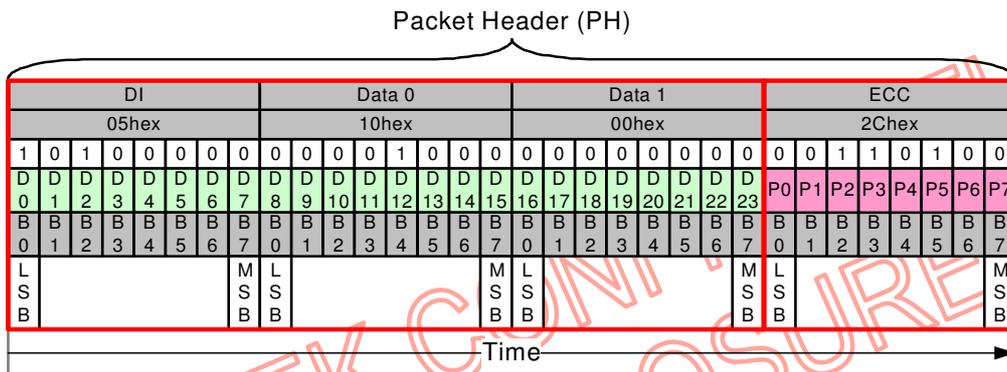
Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors:

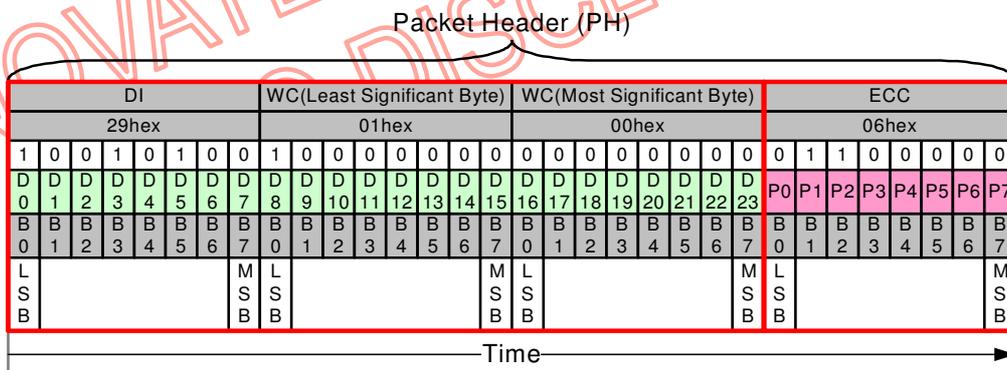
The ECC protects the following field”

- Short Packet (SPa): Data Identification (DI) byte (8 bits: D[0...7]), Packet Data (PD) bytes (16 bits :D[8...23]) and ECC (8 bits: P[0...7])
- Long Packet (LPa): Data Identification (DI) byte (8 bits: D[0...7]), Word Count (WC) bytes (16 bits : D[8...23]) and ECC (8 bits: P[0...7])

D[23...0] is illustrated for reference purposes below.



D[23...0] and P[7...0] on the Short Packet (SPa)



D[23...0] and P[7...0] on the Long Packet (LPa)

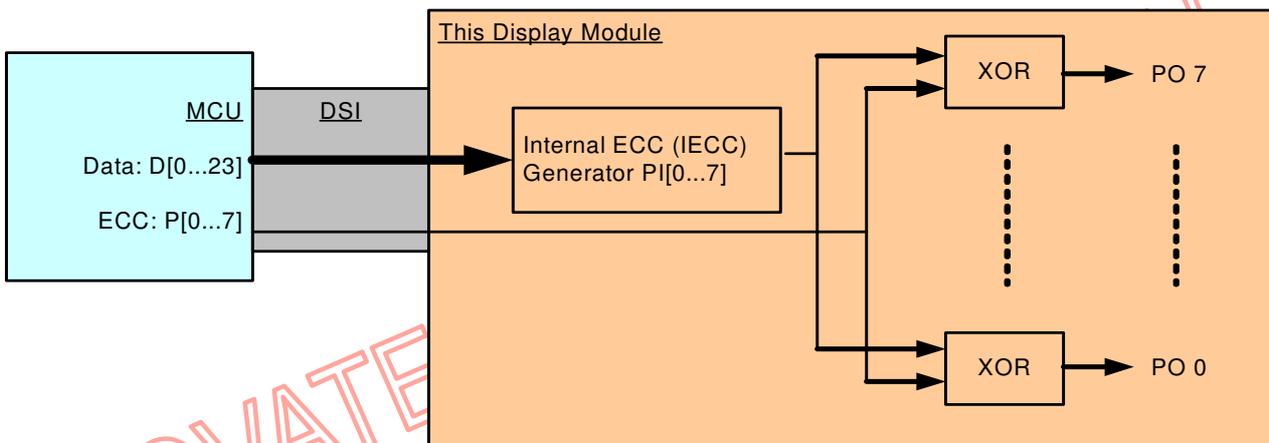
Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7...0]) of the Error Correction Code (ECC) are defined, where the symbol ‘^’ is presenting XOR function (Pn is ‘1’ if there is odd number of ‘1’s and Pn is ‘0’ if there is even number of ‘1’s), as follows.

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

The transmitter (The MCU or the Display Module) is sending data bits D[23...0] and Error Correction Code (ECC) P[7...0]. The receiver (The Display module or the MCU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7...0].

This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for reference purposes below.



Internal Error Correction Code (IECC) on the Display Module (The Receiver)

The sent data bits (D[23...0]) and ECC (P[7...0]) are received correctly, if a value of the PO[7...0] is 00h. The sent data bits (D[23...0]) and ECC (P[7...0]) are not received correctly, if a value of the PO[7...0] is not 00h.

ECC P[7...0]	1 1 0 0 0 0 0 0	03h
IECC PI[7...0]	1 1 0 0 0 0 0 0	03h
XOR(ECC,IECC) =>PO[7...0]	0 0 0 0 0 0 0 0	=00h => No Error
	L M S S B B	

Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7...0]	1 1 0 0 0 0 0 0	03h
IECC PI[7...0]	1 1 1 1 0 0 0 0	0Fh
XOR(ECC,IECC) =>PO[7...0]	0 0 1 1 0 0 0 0	=0Ch => Error
	L M S S B B	

Internal XOR Calculation between ECC and IECC Values - Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23...0] on the transmitter side.

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The number of the errors (one or more) can be defined when the value of the PO[7...0] is compared to values on the following table.

One Bit Error Value of the Error Correction Code (ECC)

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

One error is detected if the value of the PO[7...0] is on : One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

- PO[7...0] = 0Eh
- The bit of the data (D[23...0]), what is not correct, is D[3]

More than one error is detected if the value of the PO[7...0] is not on: One Bit Error Value of the Error Correction Code (ECC) e.g. PO[7...0] = 0Ch.

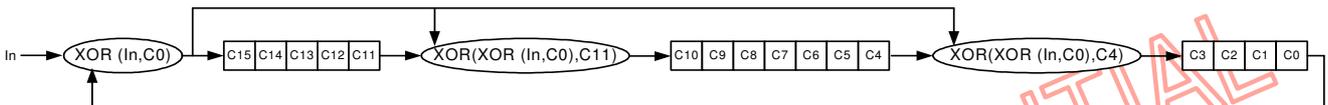
5.3.4.3.1.4 PACKET DATA (PD) ON THE LONG PACKET (LPA)

Packet Data (PD) of the Long Packet (LPA) is defined after Packet Header (PH) of the Long Packet (LPA). The number of the data bytes is defined on chapter “Word Count (WC) on the Long Packet (LPA)”.

5.3.4.3.1.5 PACKET FOOTER (PF) ON THE LONG PACKET (LPA)

Packet Footer (PF) of the Long Packet (LPA) is defined after the Packet Data (PD) of the Long Packet (LPA). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPA).

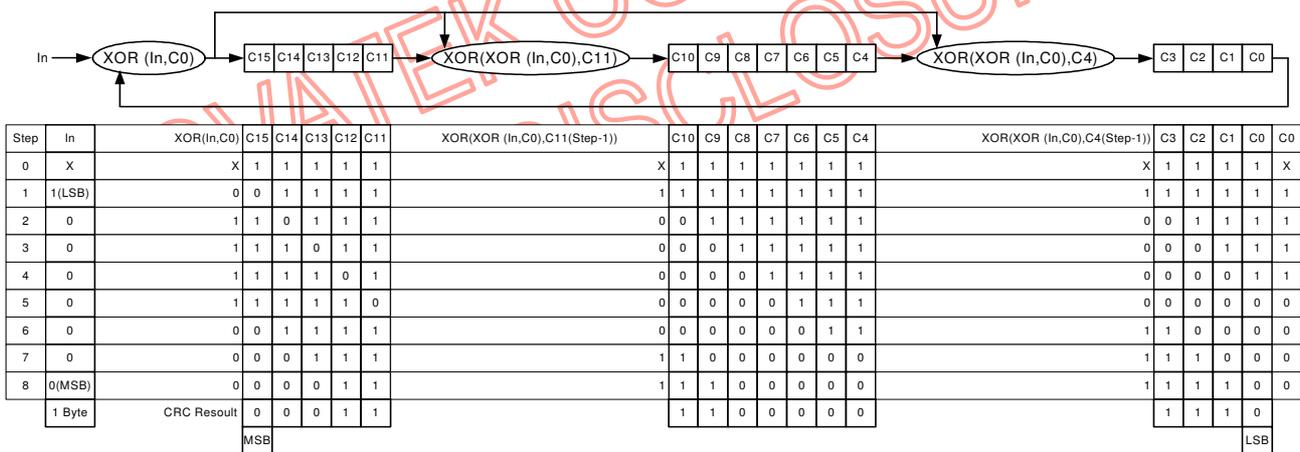
The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial $X^{16}+X^{12}+X^5+X^0$ as it is illustrated below.



16-bit Cyclic Redundancy Check (CRC) Calculation

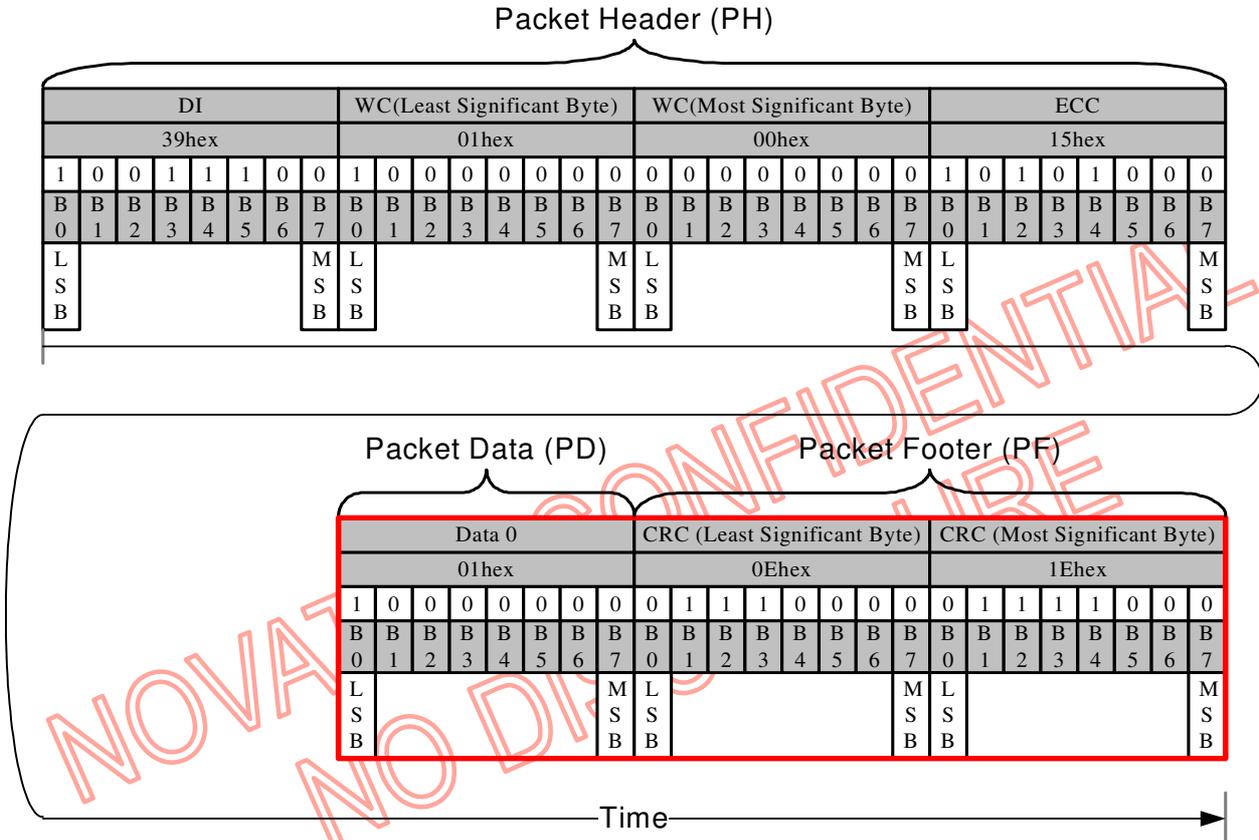
The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Least Significant Bit (LSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPA) is 01h, is illustrated (step-by-step) below.



CRC Calculation – Packet Data (PD) is 01h

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.



Packet Footer (PF) Example

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

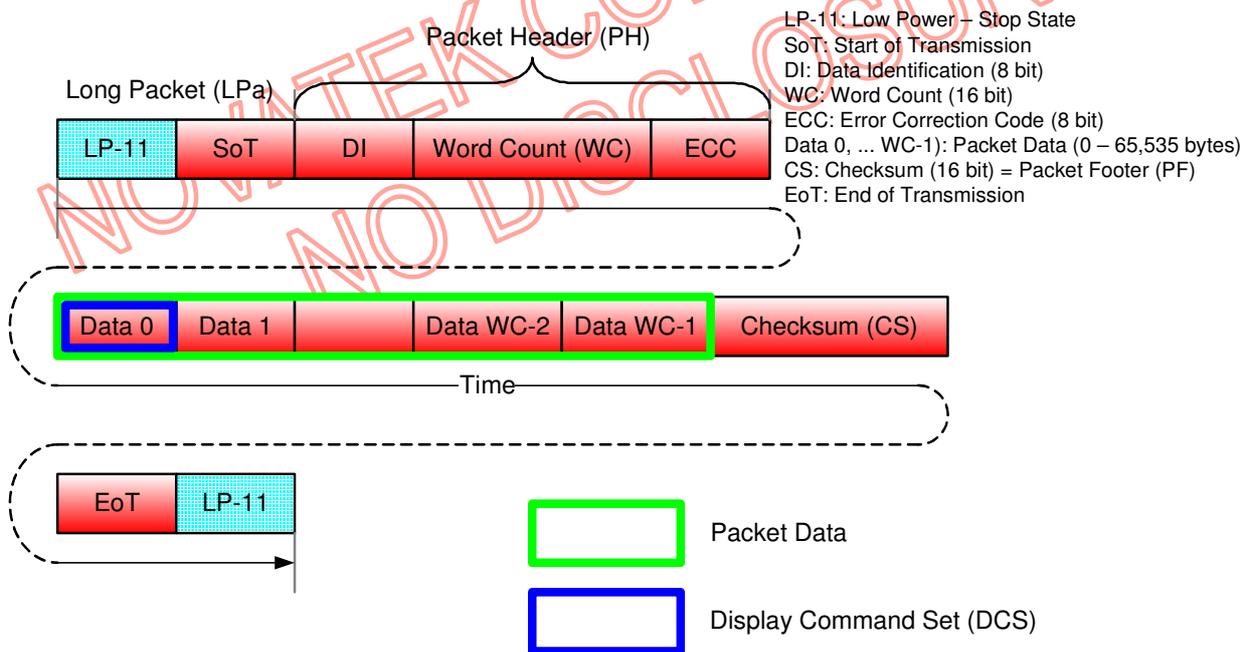
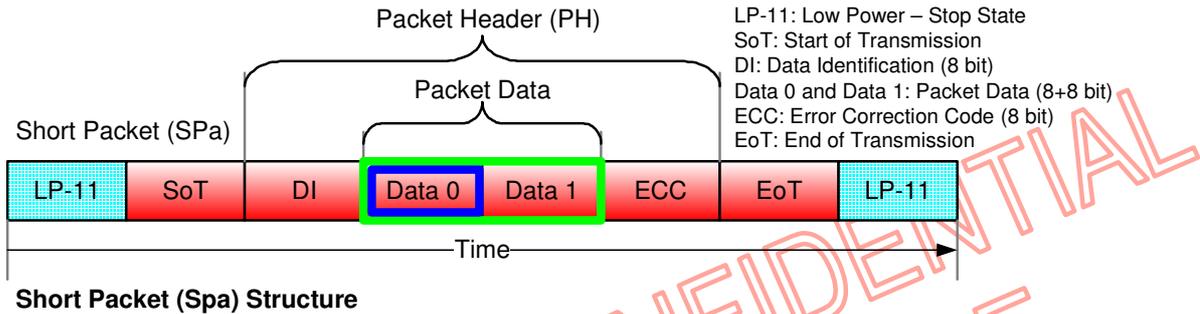
The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

5.3.4.3.2 PACKET TRANSMISSIONS

5.3.4.3.2.1 PACKET FROM THE MCU TO THE DISPLAY MODULE

Display Command Set (DCS)

Display Command Set (DCS), which is defined on chapter “6 Instruction Description”, is used from the MCU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.



Display Command Set (DCS) on Short Packet (SPa) and Long Packet (LPa)

Generic Write, 2 Parameter (GENW2-S), Data Type = 10 0011 (23h)

“Generic Write, 2 Parameter” (GENW2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0011b), from the MCU to the display module. The content of 2 payload bytes is “command” and “parameter”. These commands are defined on a table (See chapter “6 Instruction Description”) below.

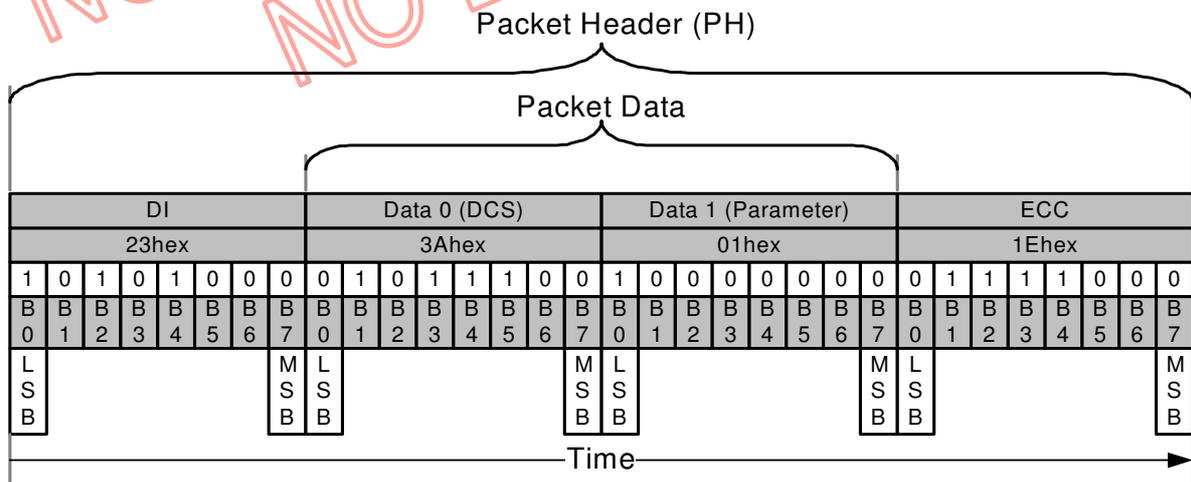
Command
GAMSET (26h)
RAMWR (2Ch), Note
TEON (35h)
MADCTL (36h)
COLMOD (3Ah)
RAMWRC (3Ch), Note
WRDISBV (51h)
WRCTRLD (53h)
WRCABC (55h)
WRCABCMB (5Eh)

Note : One Subpixel has been written.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 0011b
- Packet Data (PD)
 - Data 0: “PMCSSET (3Ah)”, Display Command Set (DCS)
 - Data 1: 01hex, Parameter of the DCS
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Generic Write, 2 Parameter (GENW2-S) – Example

Generic Write Long (GENW-L) , Data Type = 10 1001 (29h)

“Generic Write Long” (GENW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 10 1001b), from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined on a table (See chapter “6 Instruction Description”) below.

Command
NOP (00h) , Note1
SWRESET (01h) , Note1
SLPIN (10h) , Note1
SLPOUT (11h) , Note1
PTLON (12h) , Note1
NORON (13h) , Note1
INVOFF (20h) , Note1
INVON (21h) , Note1
ALLPOFF (22h)
ALLPON (23h)
GAMSET (26h) , Note2
DISPOFF (28h) , Note1
DISPON (29h) , Note1
CASET (2Ah)
RASET (2Bh)
RAMWR (2Ch) , Note2
PARLINES (30h)
TEOFF (34h) , Note1
TEON (35h) , Note2
MADCTL (36h) , Note2
IDMOFF (38h) , Note1
IDMON (39h) , Note1
COLMOD (3Ah) , Note2
RAMWRC (3Ch) , Note2
TEARLINE (44h)
WRDISBV (51h) , Note2
WRCTRLD (53h)
WRCABC (55h) , Note2
WRCABCMB (5Eh)

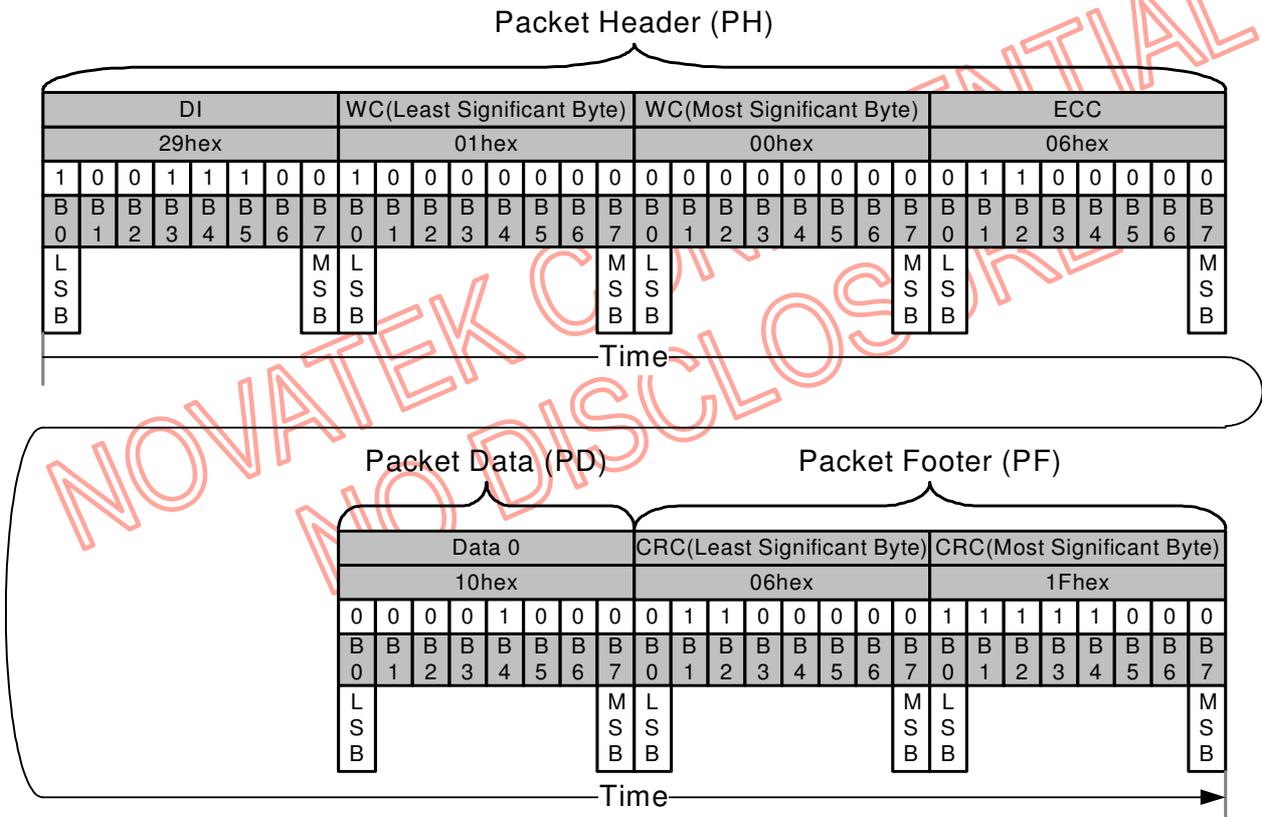
Notes :

1. Also Short Packet (Spa) can be used; See Generic Write, 1 Parameter.
2. Also Short Packet (Spa) can be used; See Generic Write, 2 Parameter.

Long Packet (Lpa), when a command (No Parameter) was sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 1001b
- Word Count (WC)
 - Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: "Sleep In (10h)", Display Command Set (DCS)
- Packet Footer (PF)

This is defined on the Long Packet (Lpa) as follows.

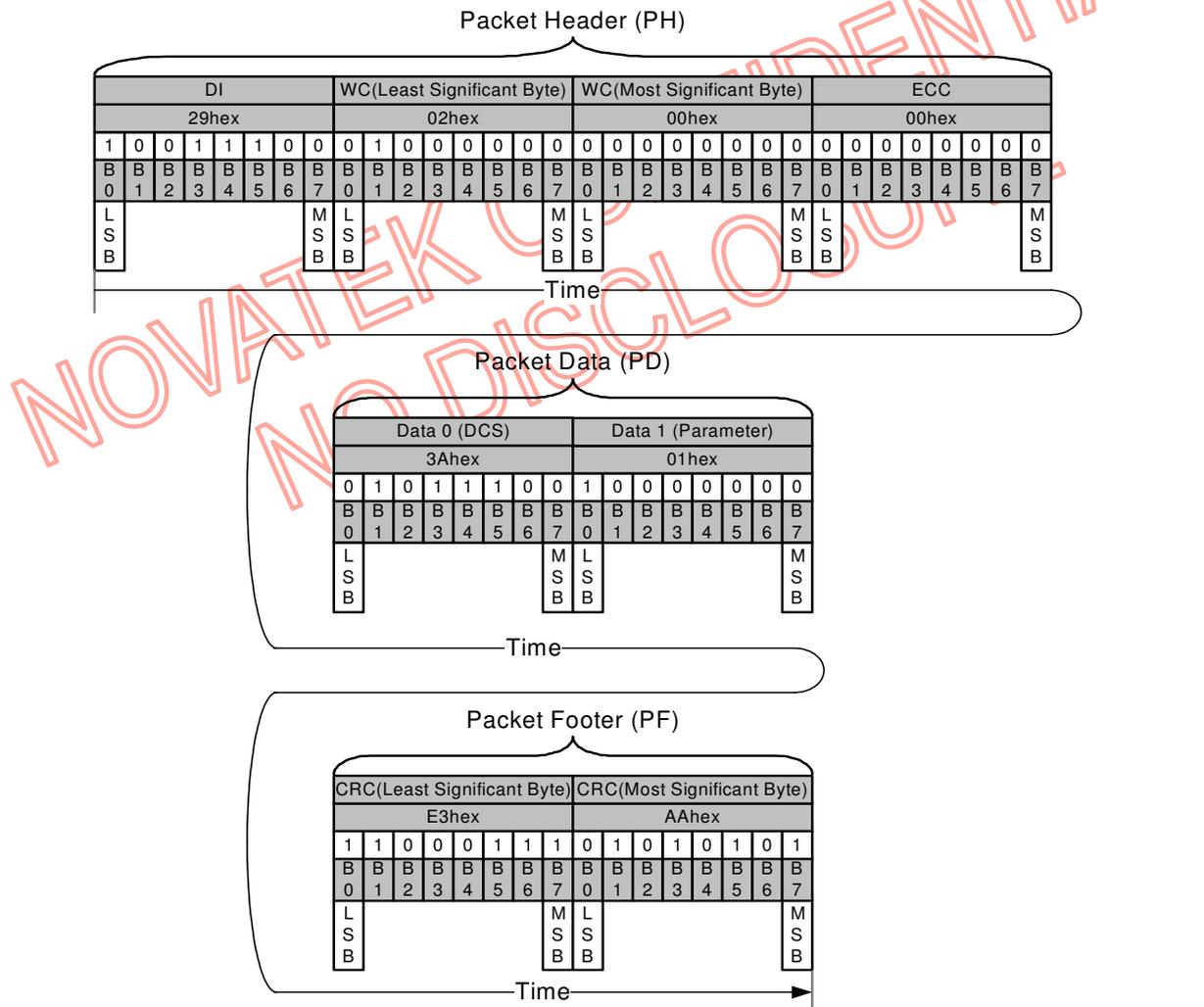


Generic Write Long (GENW-L) with DCS Only - Example

Long Packet (Lpa), when a Write (1 parameter) was sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 1001b
- Word Count (WC)
 - Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: "Gamma Set (3Ah)", Display Command Set (DCS)
 - Data 1: 01hex, Parameter of the DCS
- Packet Footer (PF)

This is defined on the Long Packet (Lpa) as follows.



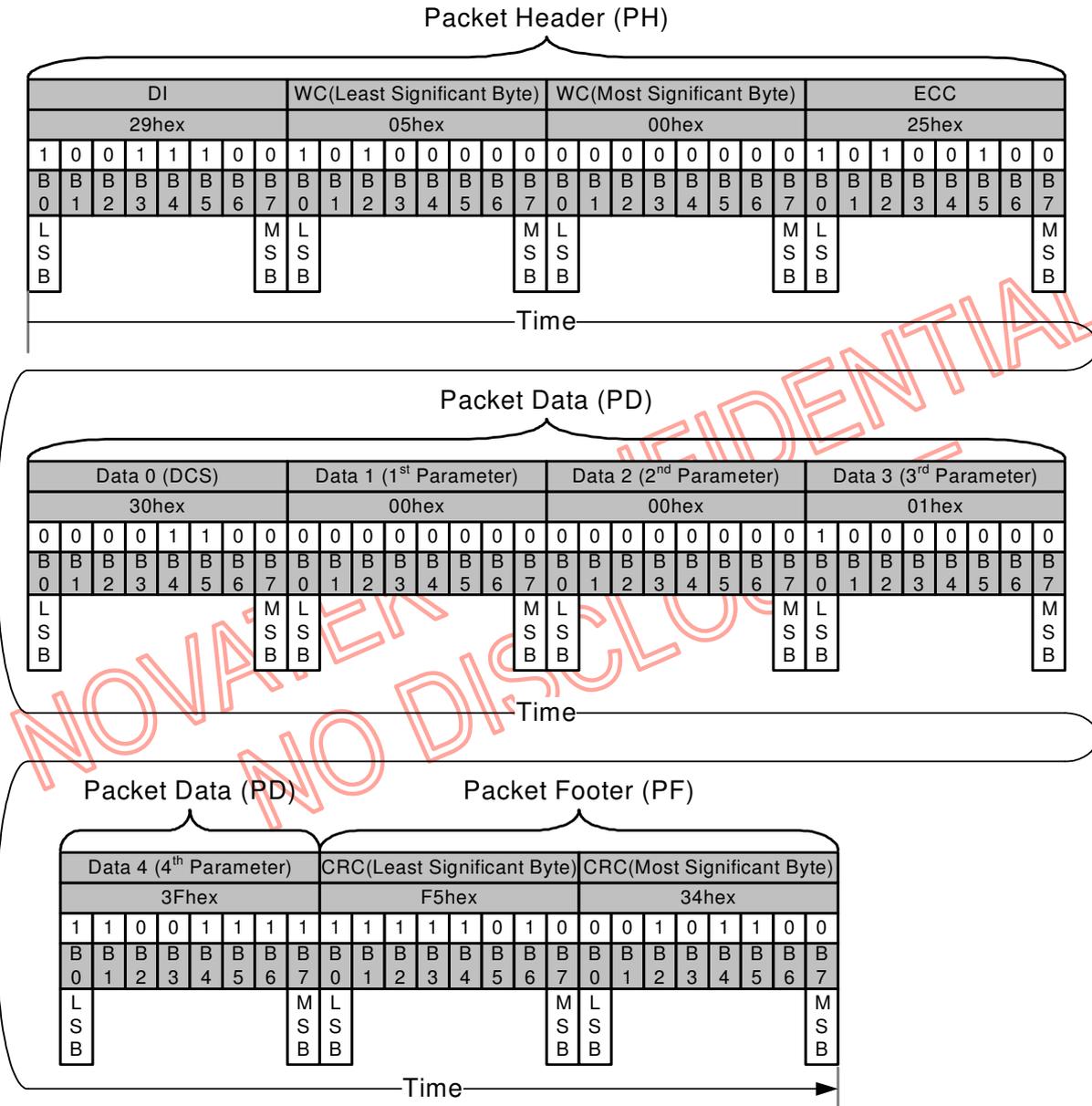
Generic Long Write with DCS and 1 Parameter - Example

Long Packet (Lpa), when a Write (4 parameters) was sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 1001b
- Word Count (WC)
 - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: "PARLINES (30h)", Display Command Set (DCS)
 - Data 1: 00hex, 1st Parameter of the DCS, Start Column SC[15...8]
 - Data 2: 00hex, 2nd Parameter of the DCS, Start Column SC[7...0]
 - Data 3: 01hex, 3rd Parameter of the DCS, End Column EC[15...8]
 - Data 4: 3Fhex, 4th Parameter of the DCS, End Column EC[7...0]
- Packet Footer (PF)

This is defined on the Long Packet (Lpa) as follows.

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Generic Write Long with DCS and 4 Parameters - Example

Generic Read, 1 Parameter (GENR1-S) , Data Type = 01 0100 (14h); Generic Read, 2 Parameter (GENR2-S) , Data Type = 10 0100 (24h)

“Generic Read, 1 Parameter / Generic Read, 2 Parameter” (GENR1-S / GENR2-S) is always using a Short Packet (Spa), what is defined on Data Type (DT, 01 0100b) and Data Type (DT, 10 0100b), from the MCU to the display module. These commands are defined on a table (See chapter “6 Instruction Description”) below.

The 1st parameter (Dummy Data) is not returned as it is done in MeSSI-8/16 cases. The first returned parameter is the 2nd parameter in DSI case.

Command
RNUMED (05h)
RDDPM (0Ah)
RDDMADCTL (0Bh)
RDDCOLMOD (0Ch)
RDDIM (0Dh)
RDDSM (0Eh)
RDDSDR (0Fh)
RAMRD (2Eh), Note
RAMRDC (3Eh), Note
RDDISBV (52h)
RDCTRLD (54h)
RDCABC (56h)
RDCABCMB (5Fh)
RDBWLB (70h)
RDBkx (71h)
RDBky (72h)
RDWx (73h)
RDWy (74h)
RDRGLB (75h)
RDRx (76h)
RDRy (77h)
RDGx (78h)
RDGy (79h)
RDBALB (7Ah)
RDBx (7Bh)
RDBy (7Ch)
RDAx (7Dh)
RDAy (7Eh)
RDDDBST (A1h)
RDDDBC (A8h)
RDFCS (AAh)
RDCCS (AFh)
RDID1 (DAh)
RDID2 (DBh)
RDID3 (DCh)

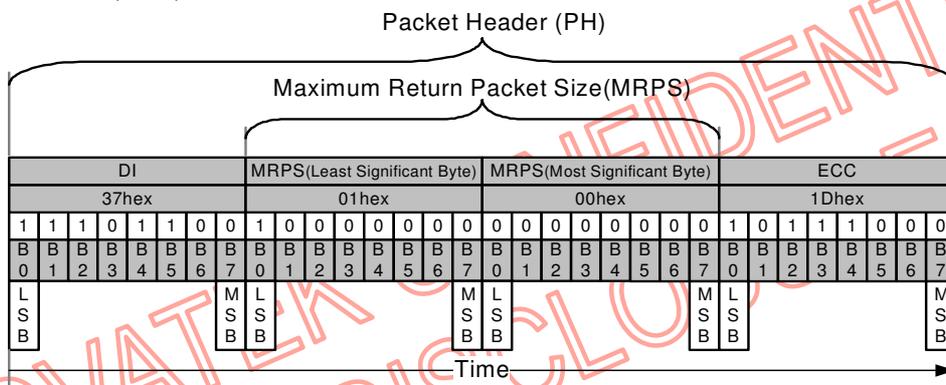
Note : One Subpixel has been read

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is “Set Maximum Return Packet Size” (SMRPS-S), which Data Type (DT) is 11 0111b

and which is using Short Packet (SPa) before the MCU can send “Display Command Set (DCS) Read, No Parameter” to the display module. This same sequence is illustrated for reference purposes below.

Step 1:

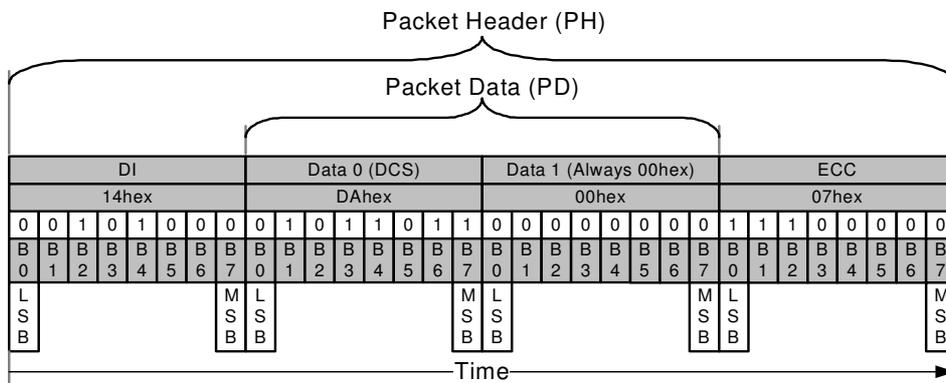
- The MCU sends “Set Maximum Return Packet Size” (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module
- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 11 0111b
- Maximum Return Packet Size (MRPS)
 - Data 0: 01hex
 - Data 1: 00hex
- Error Correction Code (ECC)



Set Maximum Return Packet Size (SMRPS-S) - Example

Step 2:

- The MCU wants to receive a value of the “Read ID1 (DAh)” from the display module when the MCU sends “Generic Read, 1 Parameter” to the display module
- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 0100b
- Packet Data (PD)
 - Data 0: “Read ID1 (DAh)”, Display Command Set (DCS)
 - Data 1: Always 00hex
- Error Correction Code (ECC)



Generic Read, 1 Parameter (GENR1-S) - Example

Step 3: The display module can send 2 different information to the MCU after Bus Turnaround (BTA)

1. An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command. See section "Acknowledge with Error Report (AwER)".
2. Information of the received command. Short Packet (SPa) or Long Packet (LPa)

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Display Command Set (DCS) Write, No Parameter (DCSWN-S) , Data Type = 00 0101 (05h)

“Display Command Set (DCS) Write, No Parameter” is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0101b), from the MCU to the display module. These commands are defined on a table (See chapter “6 Instruction Description”) below.

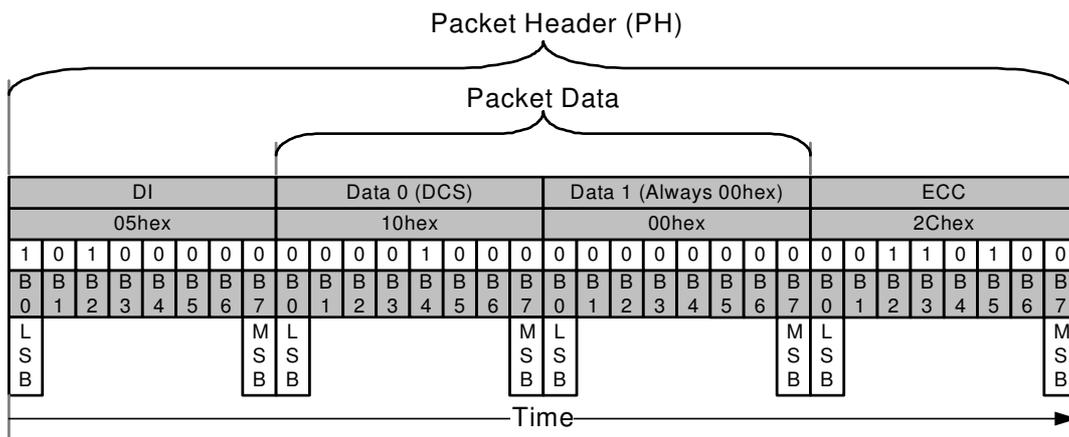
Command
NOP (00h)
SWRESET (01h)
SLPIN (10h)
SLPOUT (11h)
PTLON (12h)
NORON (13h)
INVOFF (20h)
INVON (21h)
ALLPOFF (22h)
ALLPON (23h)
DISPOFF (28h)
DISPON (29h)
Memory Write(2Ch), Note
TEOFF (34h)
IDMOFF (38h)
IDMON (39h)

Note: Subpixel has not been written

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 0101b
- Packet Data (PD)
 - Data 0: “Sleep In (10h)”, Display Command Set (DCS)
 - Data 1: Always 00hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Display Command Set (DCS) Write, No Parameter (DCSWN-S) - Example

Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) , Data Type = 01 0101 (15h)

“Display Command Set (DCS) Write, 1 Parameter” (DCSW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0101b), from the MCU to the display module. These commands are defined on a table (See chapter “6 Instruction Description”) below.

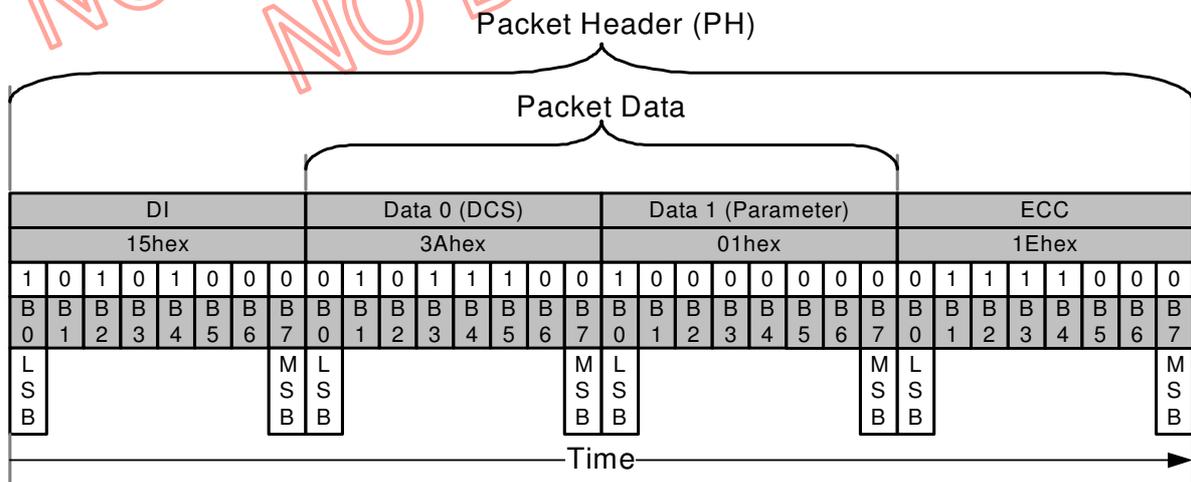
Command
GAMSET (26h)
Memory Write (2Ch), Note
TEON (35h)
MADCTL (36h)
COLMOD (3Ah)
RAMWRC (3Ch), Note
WRDISBV (51h)
WRCTRLD (53h)
WRCABC (55h)
WRCABCMB (5Eh)

Note : One Subpixel has been written.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 0101b
- Packet Data (PD)
 - Data 0: “PMCSSET (3Ah)”, Display Command Set (DCS)
 - Data 1: 01hex, Parameter of the DCS
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) – Example

Display Command Set (DCS) Write Long (DCSW-L) , Data Type = 11 1001 (39h)

“Display Command Set (DCS) Write Long” (DCSW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 11 1001b), from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined on a table (See chapter “6 Instruction Description”) below

Command
NOP (00h) , Note1
SWRESET (01h) , Note1
SLPIN (10h) , Note1
SLPOUT (11h) , Note1
PTLON (12h) , Note1
NORON (13h) , Note1
INVOFF (20h) , Note1
INVON (21h) , Note1
GAMSET (26h) , Note2
DISPOFF (28h) , Note1
DISPON (29h) , Note1
CASET (2Ah)
RASET (2Bh)
RAMWR (2Ch) , Note2
PARLINES (30h)
SCRLAR (33h)
TEOFF (34h) , Note1
TEON (35h) , Note2
MADCTL (36h) , Note2
IDMOFF (38h) , Note1
IDMON (39h) , Note1
COLMOD (3Ah) , Note2
RAMWRC (3Ch) , Note2
TEARLINE (44h)
WRDISBV (51h) , Note2
WRCTRLD (53h)
WRCABC (55h) , Note2
WRCABCMB (5Eh)

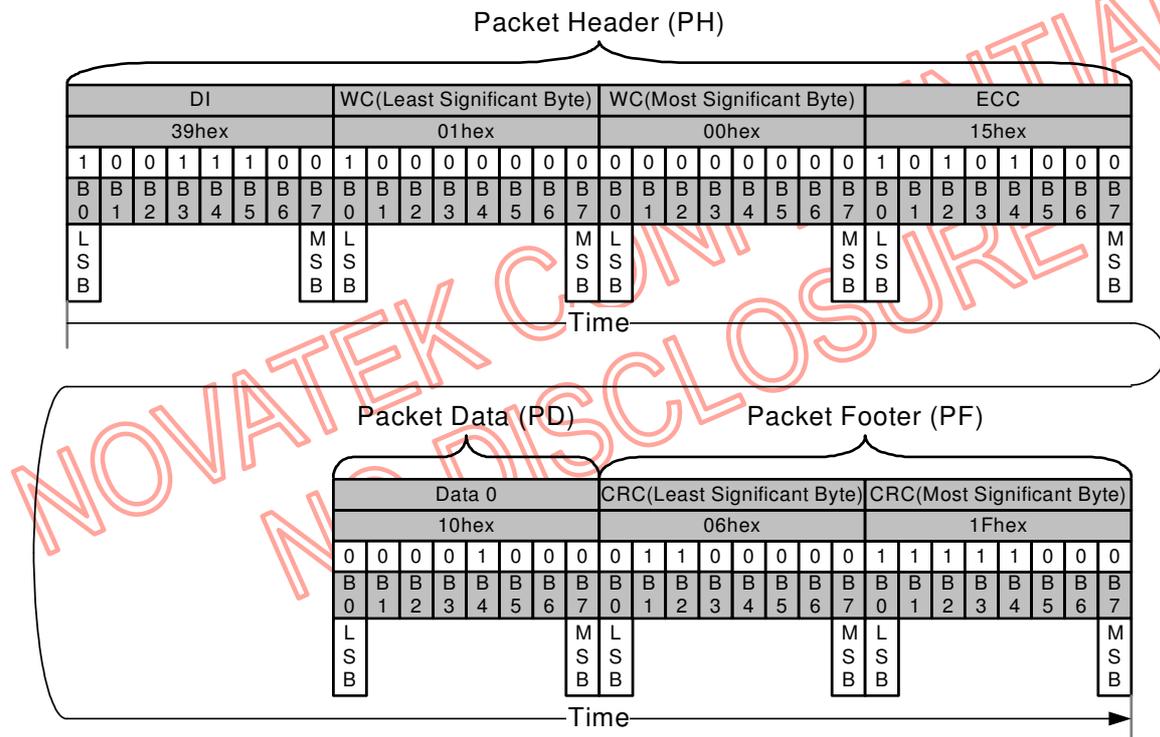
Notes :

1. Also Short Packet (SPa) can be used; See *Display Command Set (DCS) Write, No Parameter.*
2. Also Short Packet (SPa) can be used; See *Display Command Set (DCS) Write, 1 Parameter.*

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 11 1001b
- Word Count (WC)
 - Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: "Sleep In (10h)", Display Command Set (DCS)
- Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows.



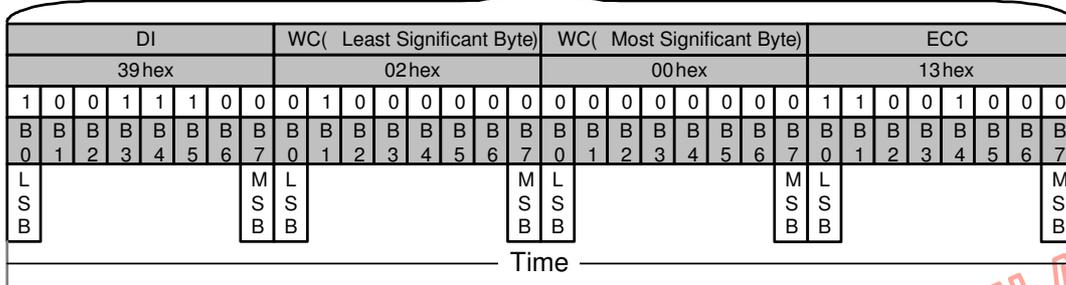
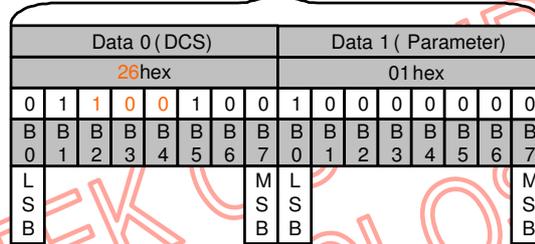
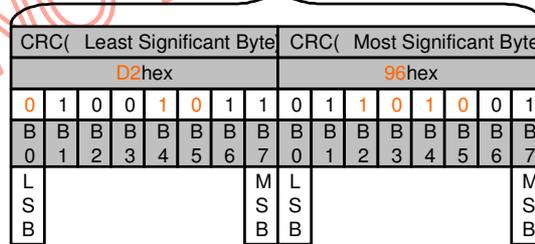
Display Command Set (DCS) Write Long (DCSW-L) with DCS Only - Example

Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 11 1001b
- Word Count (WC)
 - Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: "Gamma Set (26h)", Display Command Set (DCS)
 - Data 1: 01hex, Parameter of the DCS
- Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows.

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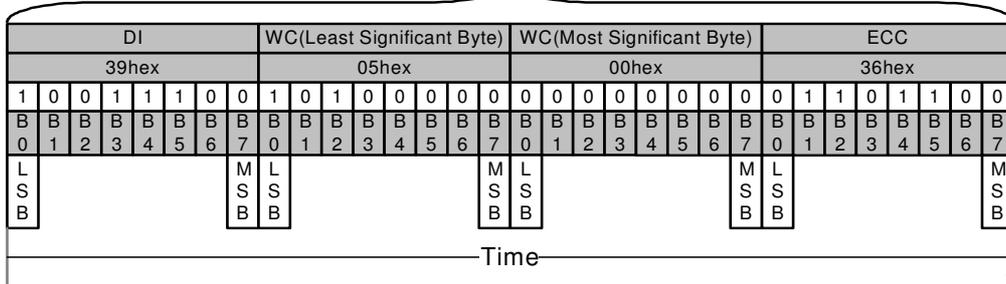
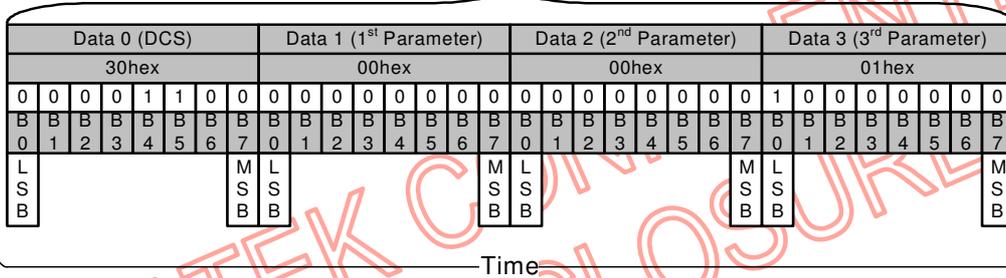
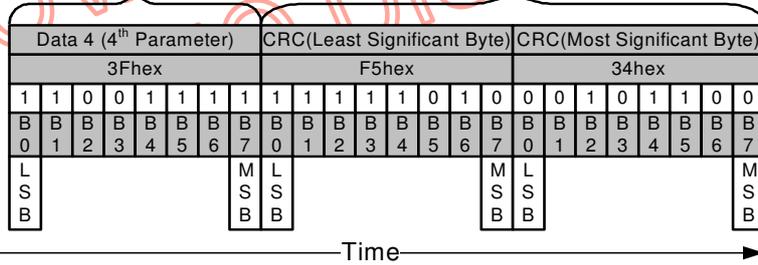
Packet Header (PH)

Packet Data (PD)

Packet Footer (PF)

Display Command Set (DCS) Write Long with DCS and 1 Parameter - Example

Long Packet (LPa), when a Write (4 parameters) was sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 11 1001b
- Word Count (WC)
 - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: "PARLINES (30h)", Display Command Set (DCS)
 - Data 1: 00hex, 1st Parameter of the DCS, Start Column SC[15...8]
 - Data 2: 00hex, 2nd Parameter of the DCS, Start Column SC[7...0]
 - Data 3: 01hex, 3rd Parameter of the DCS, End Column EC[15...8]
 - Data 4: 3Fhex, 4th Parameter of the DCS, End Column EC[7...0]
- Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows.

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NO DISCLOSURE

Packet Header (PH)

Packet Data (PD)

Packet Data (PD)
Packet Footer (PF)

Display Command Set (DCS) Write Long with DCS and 4 Parameters - Example

Display Command Set (DCS) Read, No Parameter (DCSRN-S) , Data Type = 00 0110 (06h)

“Display Command Set (DCS) Read, No Parameter” (DCSRN-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0110b), from the MCU to the display module. These commands are defined on a table (See chapter “6 Instruction Description”) below.

The 1st parameter (Dummy Data) is not returned as it is done in MeSSI-8/16 cases. The first returned parameter is the 2nd parameter in DSI case.

Command
RDNUMED (05h)
RDDPM (0Ah)
RDDMADCTL (0Bh)
RDDCOLMOD (0Ch)
RDDIM (0Dh)
RDDSM (0Eh)
RDDSDR (0Fh)
RAMRD (2Eh), Note
RAMRDC (3Eh), Note
RDDISBV (52h)
RDCTRLD (54h)
RDCABC (56h)
RDCABCMB (5Fh)
RDBWLB (70h)
RDBkx (71h)
RDBky (72h)
RDWx (73h)
RDWy (74h)
RDRGLB (75h)
RDRx (76h)
RDRy (77h)
RDGx (78h)
RDGy (79h)
RDBALB (7Ah)
RDBx (7Bh)
RDBy (7Ch)
RDAx (7Dh)
RDAy (7Eh)
RDDDBST (A1h)
RDDDBC (A8h)
RDFCS (AAh)
RDCCS (AFh)
RDID1 (DAh)
RDID2 (DBh)
RDID3 (DCh)

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is “Set Maximum Return Packet Size” (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send “Display Command Set (DCS) Read, No Parameter” to the display module. This same sequence is illustrated for reference purposes below.

-
1. An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command. See section “Acknowledge with Error Report (AwER)”.
 2. Information of the received command. Short Packet (SPa) or Long Packet (LPa)

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Null Packet, No Data (NP-L) , Data Type = 00 1001 (09h)

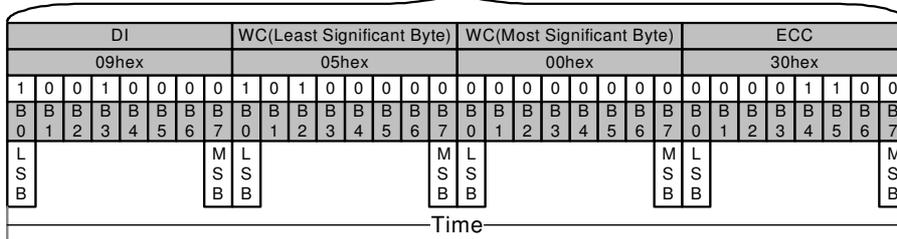
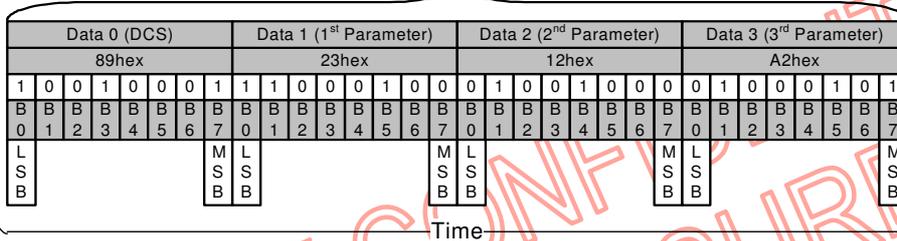
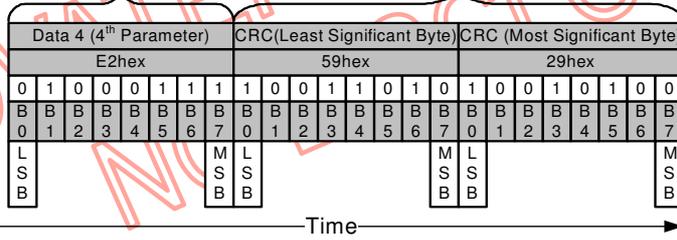
“Null Packet, No Data” (NP-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 001001b), from the MCU to the display module. The purpose of this command is keeping data lanes in the high speed mode (HSDT), if it is needed. The display module is ignored Packet Data (PD) what the MCU is sending.

Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) were sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7..6]): 00b
 - Data Type (DT, DI[5..0]): 00 1001b
- Word Count (WC)
 - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: 89h (Random data)
 - Data 1: 23h (Random data)
 - Data 2: 12h (Random data)
 - Data 3: A2h (Random data)
 - Data 4: E2h (Random data)
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

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Packet Header (PH)

Packet Data (PD)

Packet Data (PD)
Packet Footer (PF)

Null Packet, No Data (NP-L) - Example

End of Transmission Packet (EoTP)

“End of Transmission Packet” (EoTP) is always using a Short Packet (SPa), what is defined on Data Type (DT, 001000b), from the MCU to the display module. The purpose of this command is terminated the high speed mode (HPDT) properly when there is added this extra packet after the last payload packet before “End of Transmission” (EoT), which is an interface level functionality.

The display module ***is or isn't receiving*** “End of Transmission Packet” (EoTP) from the MCU during the Low Power Data Transmission (LPDT) mode before “Mark-1” (= Leaving Escape mode) what ends the Low Power Data Transmission (LPDT) mode.

The display module ***is not allowed*** to send “End of Transmission Packet” (EoTP) to the MCU during the Low Power Data Transmission (LPDT) mode

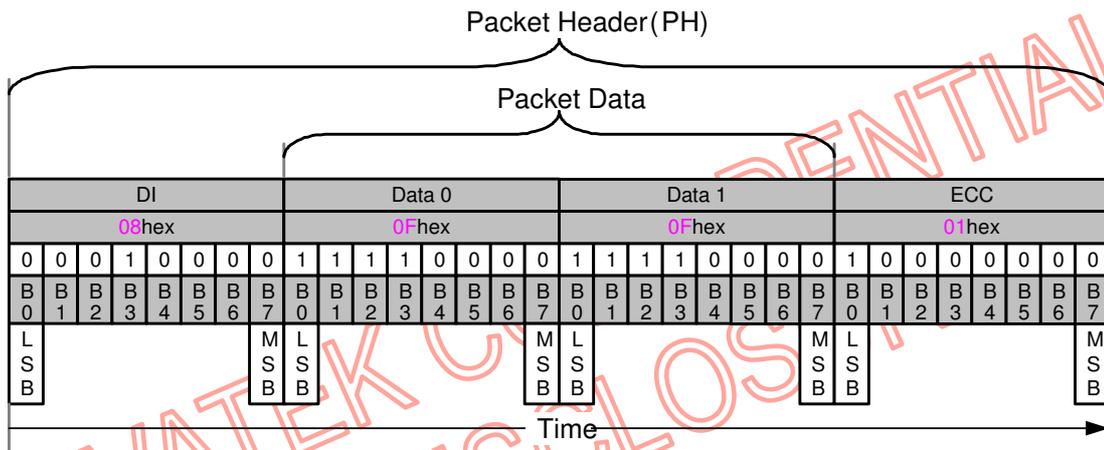
The summary of the receiving and transmitting EoTP is listed below.

Receiving and Transmitting EoTP during LPDT

Direction	Display Module (DM) in High Speed Data Transmission (HSDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MCU → Display Module	With or Without EoTP is Supported	With or Without EoTP is Supported
Display Module → MCU	HS Mode is not available (EoTP is not available)	EoTP cannot be sent by the Display Module (DM)

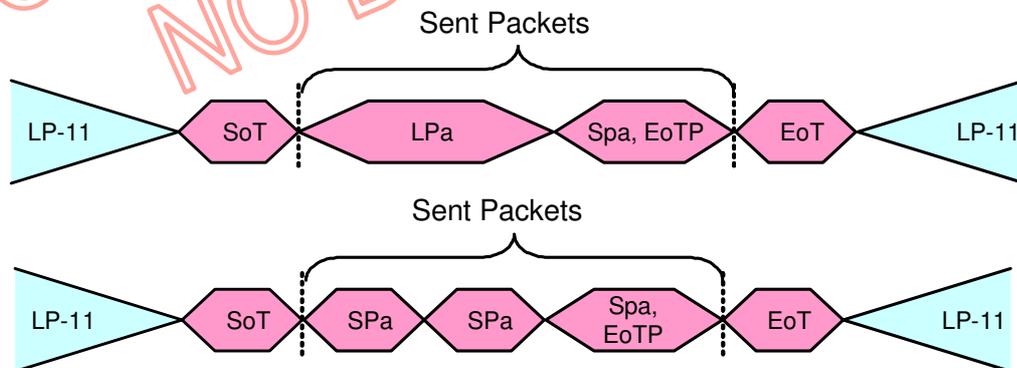
Short Packet (SPa) is using a fixed format as follow

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 1000b
- Packet Data (PD):
 - Data 0: 0Fh
 - Data 1: 0Fh
- Error Correction Code (ECC)
 - ECC: 01h



End of Transmission Packet (EoTP)

Some use case of the "End of Transmission Packet" (EoTP) are illustrated only for reference purpose below.



End of Transmission Packet (EoTP) - Examples

Sync Event (H Start, H End, V Start, V End), Data Type = xx 0001 (x1h)

Sync Events are Short packets and, therefore, can time-accurately represent events like the start and end of sync pulses. As “start” and “end” are separate and distinct events, the length of sync pulses, as well as position relative to active pixel data, e.g. front and back porch display timing, may be accurately conveyed to the peripheral. The Sync Events are defined as follows:

- Data Type = 00 0001 (01h) V Sync Start
- Data Type = 01 0001 (11h) V Sync End
- Data Type = 10 0001 (21h) H Sync Start
- Data Type = 11 0001 (31h) H Sync End

In order to represent timing information as accurately as possible a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Similarly, a V Sync End event implies an H Sync Start event for the last line of the VSA..

Sync events should occur in pairs, Sync Start and Sync End, if accurate 1054 pulse-length information needs to be conveyed. Alternatively, if only a single point (event) in time is required, a single sync event (normally, Sync Start) may be transmitted to the peripheral. Sync events may be concatenated with blanking packets to convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty for keeping the data line in HS mode, however. Display modules that do not need traditional sync/blanking/pixel timing should transmit pixel data in a high-speed burst then put the bus in Low Power Mode, for reduced power consumption. The recommended burst size is a scan line of pixels, which may be temporarily stored in a line buffer on the display module.

Color Mode On Command, and, Data Type = 01 0010 (12h)

Color Mode On is a Short packet command that switches a Video Mode display module to 8-colors mode for power saving.

Color Mode Off Command, Data Type = 00 0010 (02h)

Color Mode Off is a Short packet command that returns a Video Mode display module from 8-colors mode to normal display operation.

Shutdown Peripheral Command, Data Type = 10 0010 (22h)

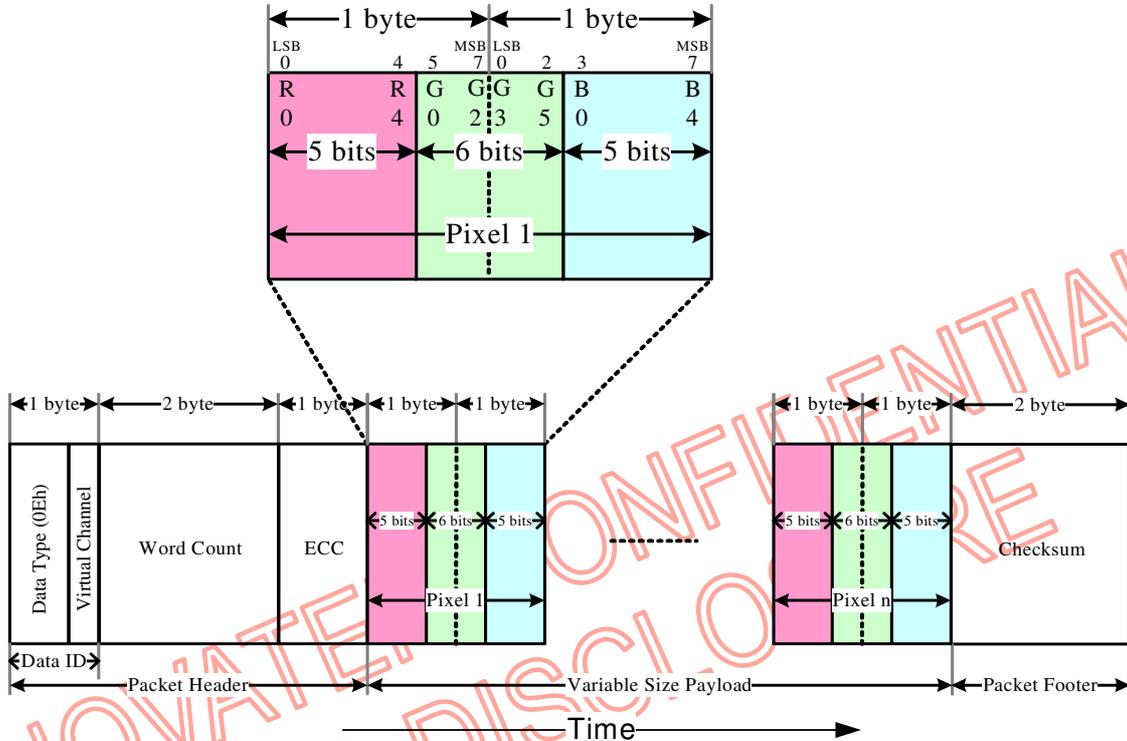
Shutdown Peripheral command is a Short packet command that turns off the display in a Video Mode display module for power saving. Note the interface shall remain powered in order to receive the turn-on, or wake-up, command.

Turn On Peripheral Command, Data Type = 11 0010 (32h)

Turn On Peripheral command is Short packet command that turns on the display in a Video Mode display module for normal display operation.

Blanking Packet (Long), Data Type = 01 1001 (19h)

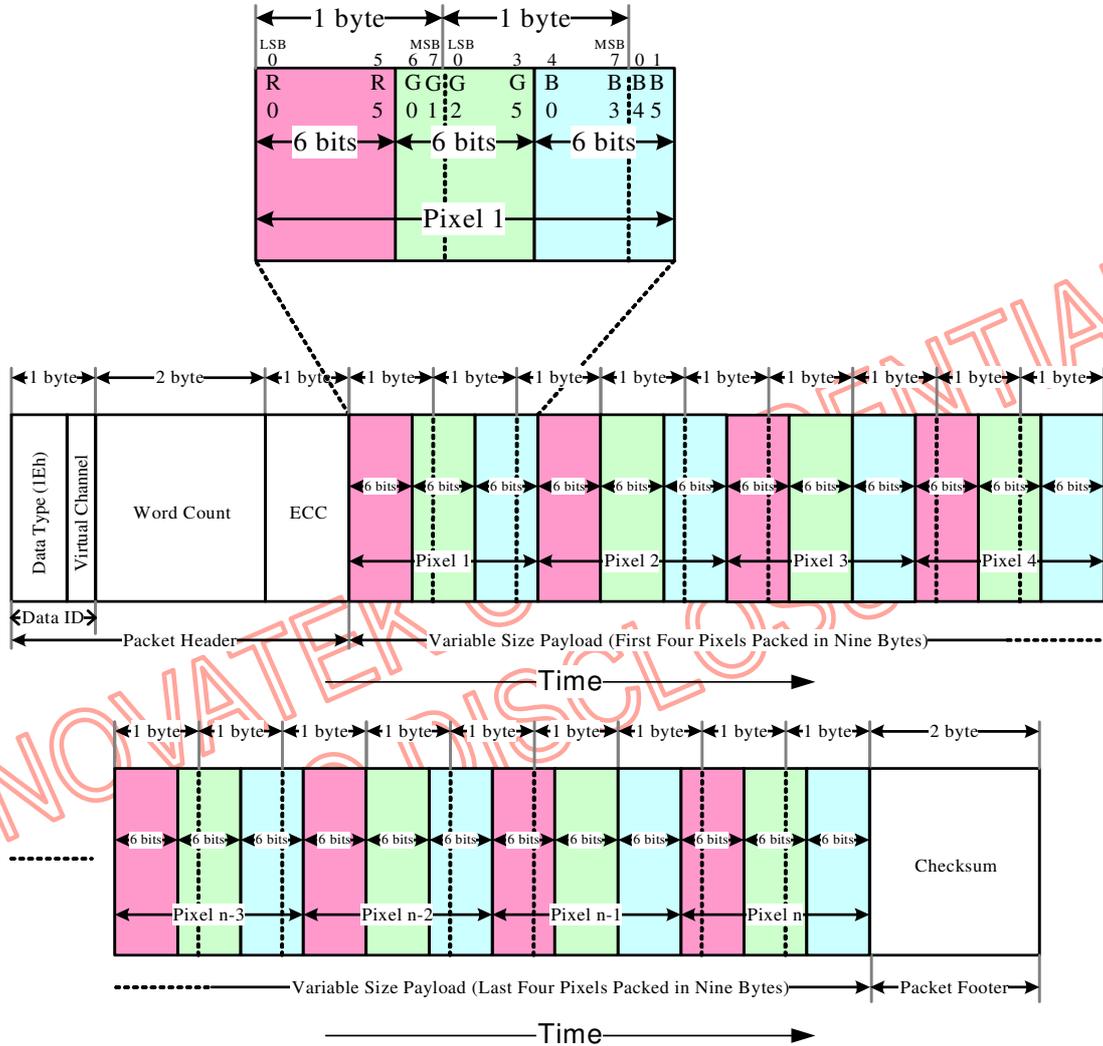
A Blanking packet is used to convey blanking timing information in a Long packet. Normally, the packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have *Sync Event* packets interspersed between blanking segments. Like all packets, the Blanking packet contents shall be an integer number of bytes. Blanking packets may contain arbitrary data as payload. The Blanking packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes, and a two-byte checksum.

Packed Pixel Stream, 16-bit Format, Long packet, Data Type = 00 1110 (0Eh)

16-bit per Pixel – RGB Color Format, Long packet

Packed Pixel Stream 16-Bit Format is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is five bits red, six bits green, five bits blue, in that order. Note that the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, the display module has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifacts.

Packed Pixel Stream, 18-bit Format, Long packet, Data type = 01 1110 (1Eh)

18-bit per Pixel (Packed)– RGB Color Format, Long packet

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device. For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the

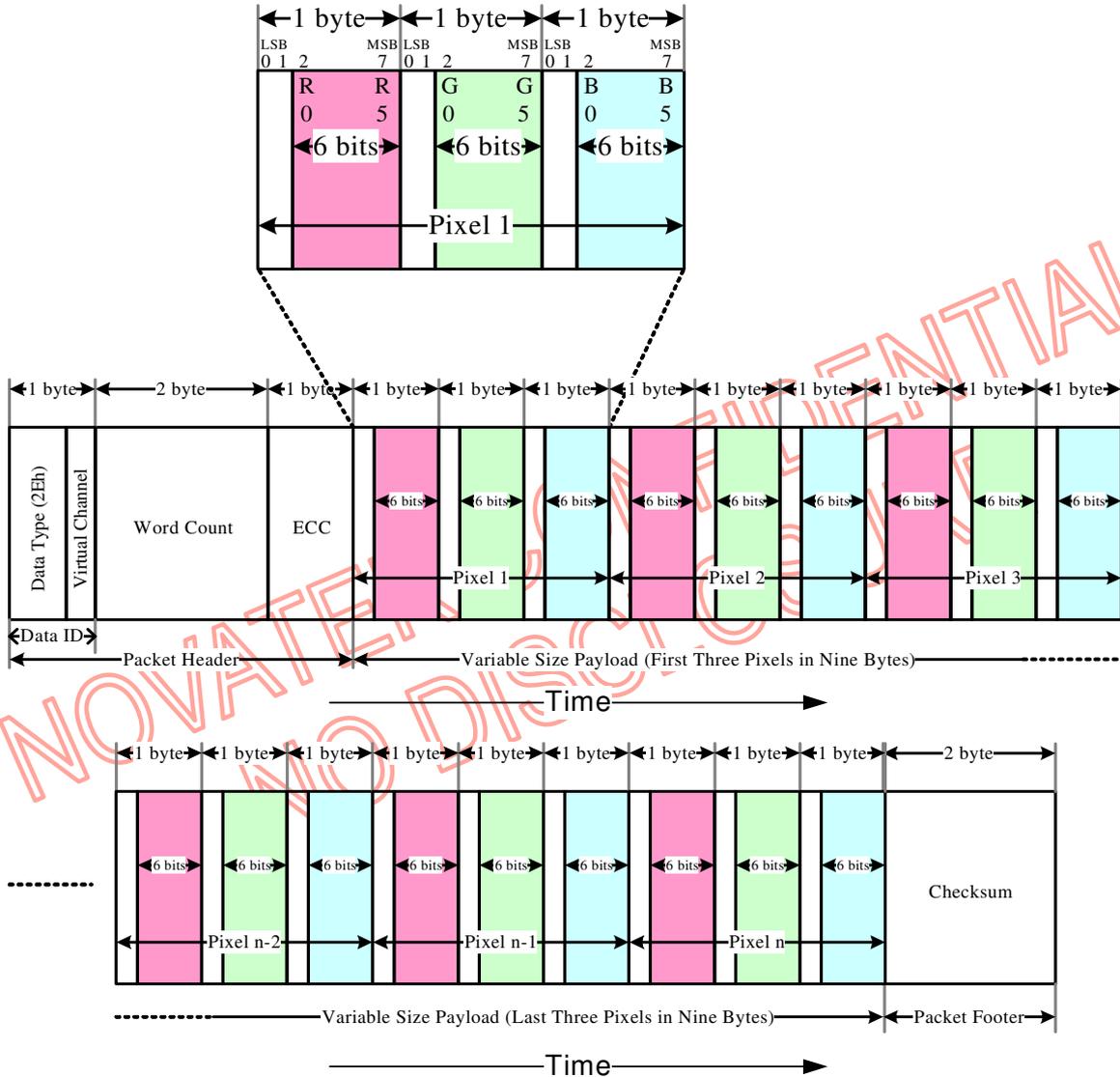


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transmission.

With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four pixels (nine bytes).

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Pixel Stream, 18-bit Format in Three Bytes, Long packet, Data Type = 101110 (2Eh)

18-bit per Pixel (Loosely Packed)– RGB Color Format, Long packet

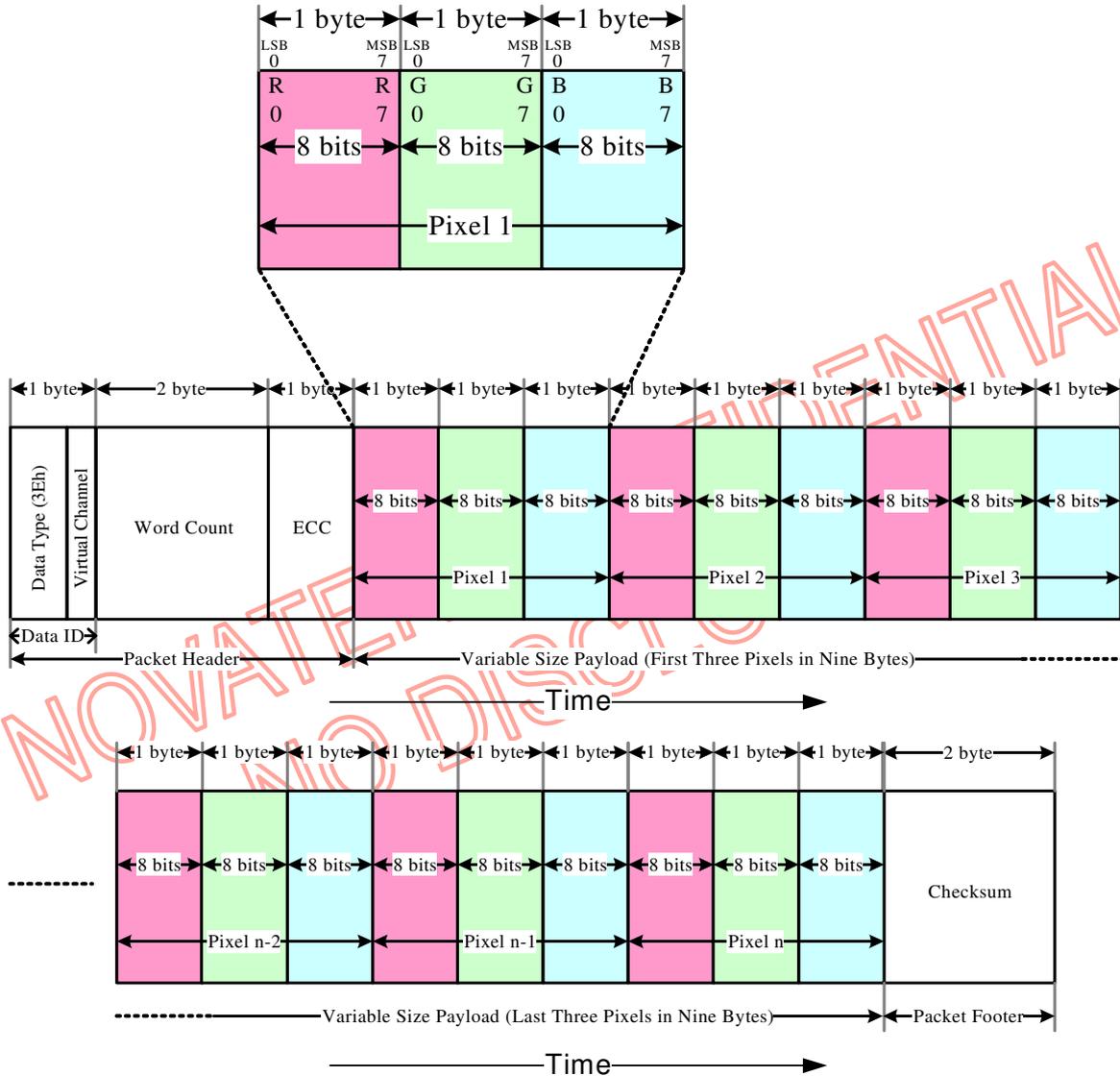
In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color

component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

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Packed Pixel Stream, 24-bit Format, Long packet, Data Type = 11 1110 (3Eh)

24-bit per Pixel – RGB Color Format, Long packet

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

5.3.4.3.2.2 PACKET FROM THE DISPLAY MODULE TO THE MCU

Used Packet Types

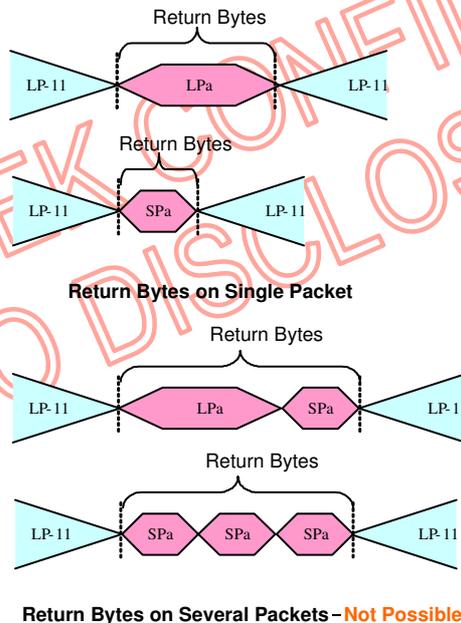
The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) (See chapter “5.3.4.3.2.1 Display Command Set (DCS) Read, No Parameter” (DCSRN-S)) or an Acknowledge with Error Report (See chapter: “5.3.4.3.2.2 Acknowledge with Error Report (AwER)” (AwER)).

The used packet type is defined on Data Type (DT). See chapter “5.3.4.3.1.3 Data Type (DT)”.

A number of the return bytes are more than the maximum size of the Packet Data (PD) on Long Packet (LPa) or Short Packet (SPa) when the display module is sending return bytes in several packets until all return bytes have been sent from the display module to the MCU.

It is also possible that the display module is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent on a packet.

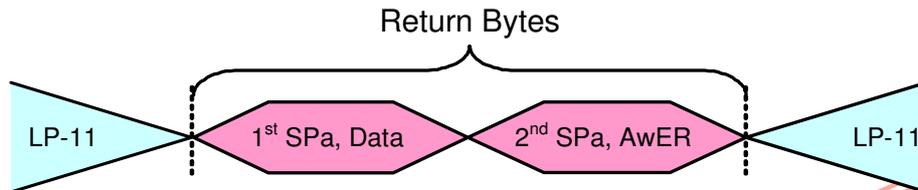
Both cases are illustrated for reference purposes below.



Data Types for Display Module-sourced Packets

Data Type Hex	Data Type Binary	Symbol	Description	Packet Size
02h	00 0010	AwER	Acknowledge & Error Report	Short
1Ch	01 1100	DCSRR-L	DCS Long Read Response	Long
21h	10 0001	DCSRR1-S	DCS Short Read Response, 1 Byte returned	Short
22h	10 0010	DCSRR2-S	DCS Short Read Response, 2 Byte returned	Short
1Ah	01 1010	GENRR-L	Generic Long Read Response	Long
11h	01 0001	GENRR1-S	Generic Short Read Response, 1 Byte returned	Short
12h	01 0010	GENRR2-S	Generic Short Read Response, 2 Byte returned	Short

The display module is return 2 packets (1st packet: Data, 2nd packet Acknowledge with Error Report) to the MCU when the display module has received a read command. See section “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” where has been detected and corrected a single bit error by the EEC (See bit 8 on Table” Acknowledge with Error Report (AwER) for Short Packet (SPa) Response”). This return packets are illustrated for reference purpose below.



AwER = Acknowledge with Error Report

Exception when Return Bytes on Several Packet

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Acknowledge with Error Report (AwER), Data Type = 00 0010(02h)

“Acknowledge with Error Report” (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0010b), from the display module to the MCU.

The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to ‘1’, as they are defined on the following table.

Acknowledge with Error Report (AwER) for Long Packet (LPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to ‘0’ internally
15	DSI Protocol Violation

Acknowledge with Error Report (AwER) for Short Packet (SPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Set to “0” internally (Only for Long Packet (LP))
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to ‘0’ internally
15	DSI Protocol Violation

<https://Datasheetspdf.com/>

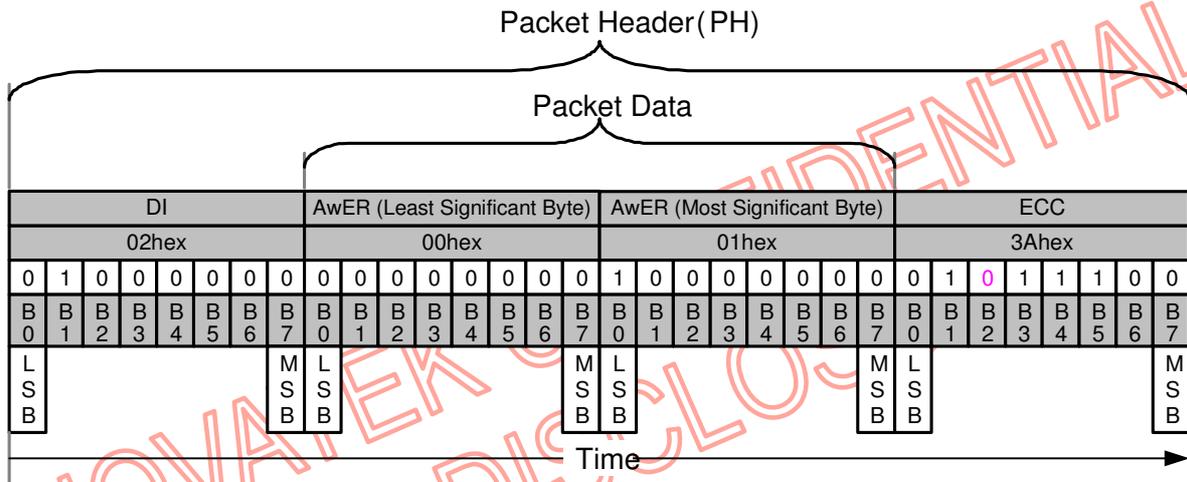
These errors are only included on the last packet, which has been received from the MCU to the display module before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

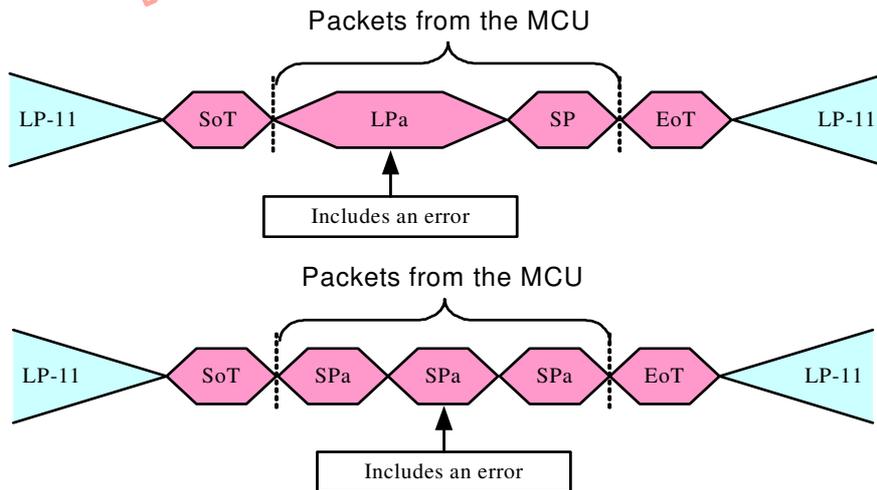
- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 0010b
- Packet Data (PD):
 - Bit 8: ECC Error, single-bit (detected and corrected)
 - AwER: 0100h
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Acknowledge with Error Report (AwER) - Example

It is possible that the display module has received several packets, which have included errors, from the MCU before the MCU is doing Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.



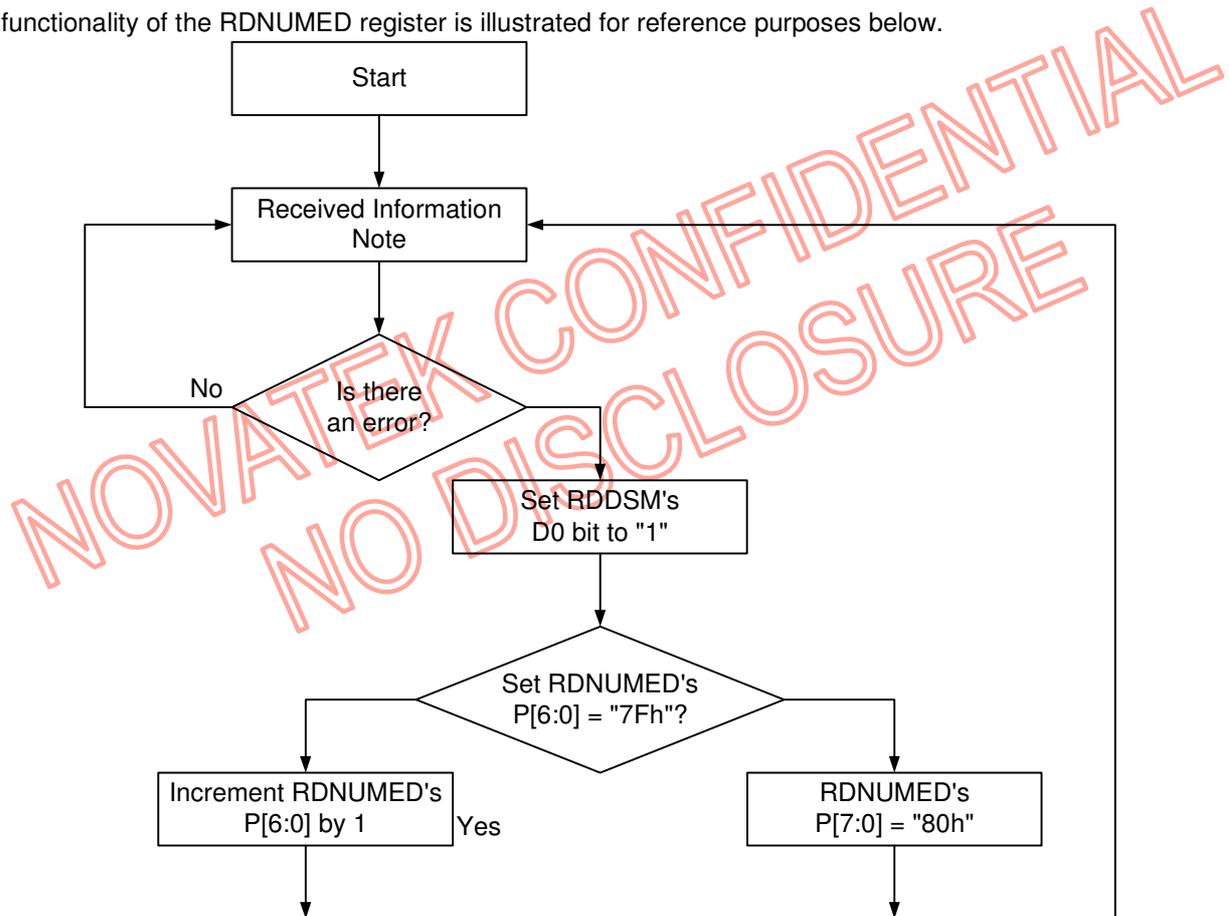
Errors Packets

Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)” commands.

The bit D0 of the “Read Display Signal Mode (0Eh)” command has been set to ‘1’ if a received packet includes an error.

The number of the packets, which are including an ECC or CRC, are calculated on the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h as well as set the bit D0 of the “Read Display Signal Mode (0Eh)” command to ‘0’ after the MCU has read the RDNUMED register from the display module.

The functionality of the RDNUMED register is illustrated for reference purposes below.



Note:

1. This information can Interface or Packet Level Communication but it is always from the MCU to the display module in this case.
2. CRC or ECC error

DCS Read Long Response (DCSRR-L), Data Type = 01 1100(1Ch)

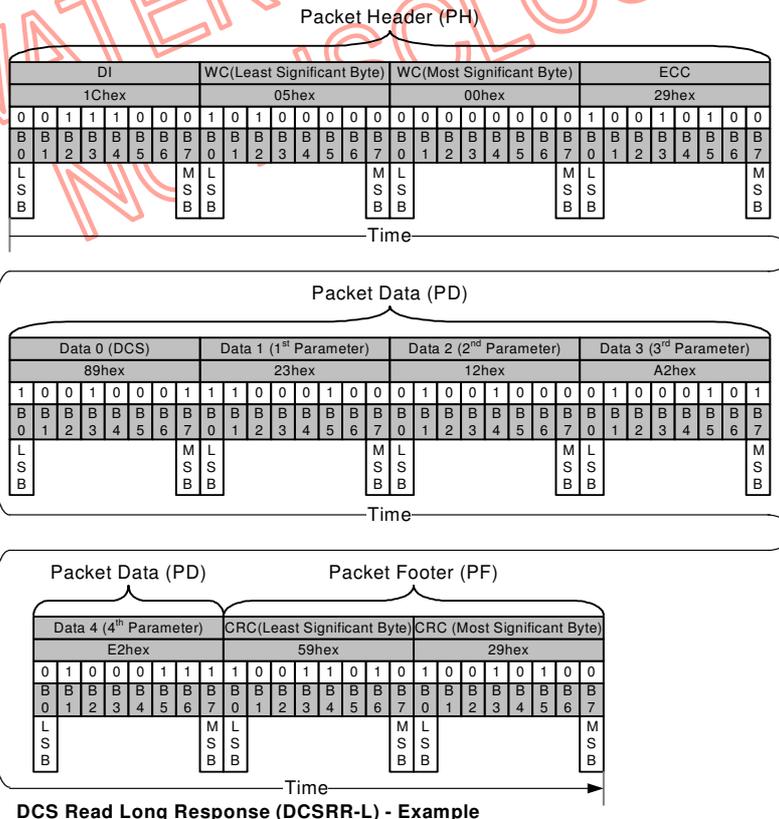
“DCS Read Long Response” (DCSRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 01 1100b), from the display module to the MCU. “DCS Read Long Response” (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

“DCS Read Long Response” (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 1100b
- Word Count (WC)
 - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: 89h
 - Data 1: 23h
 - Data 2: 12h
 - Data 3: A2h
 - Data 4: E2h
- Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.



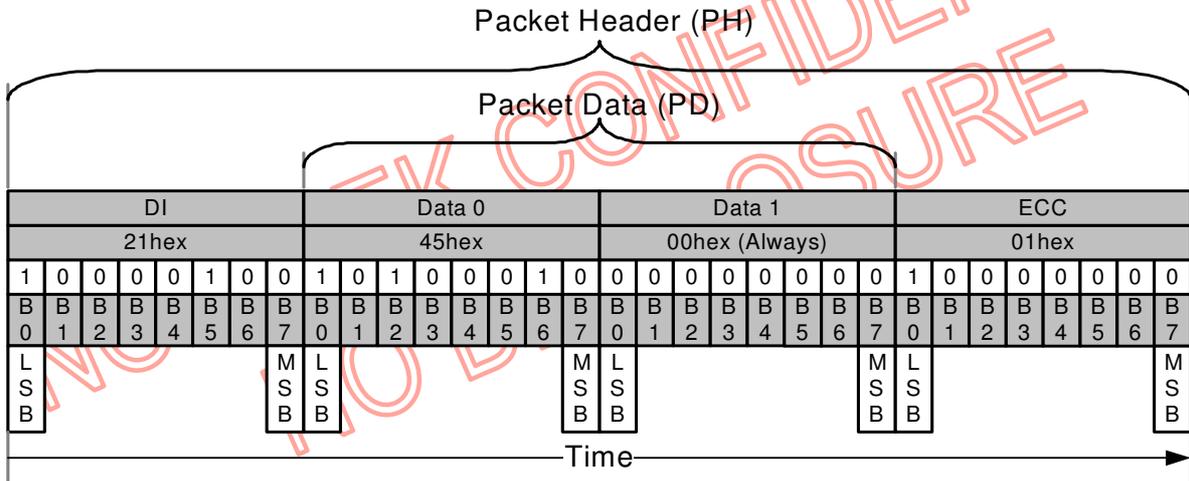
DCS Read Short Response, 1 Byte Returned (DCSRR1-S), Data Type = 10 0001(21h)

“DCS Read Short Response, 1 Byte Returned” (DCSRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0001b), from the display module to the MCU. “DCS Read Short Response, 1 Byte Returned” (DCSRR1-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 0001b
- Packet Data (PD):
 - Data 0: 45h
 - Data 1: 00h (Always)
- Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.



DCS Read Short Response, 1 Byte Returned (DCSRR1-S) - Example

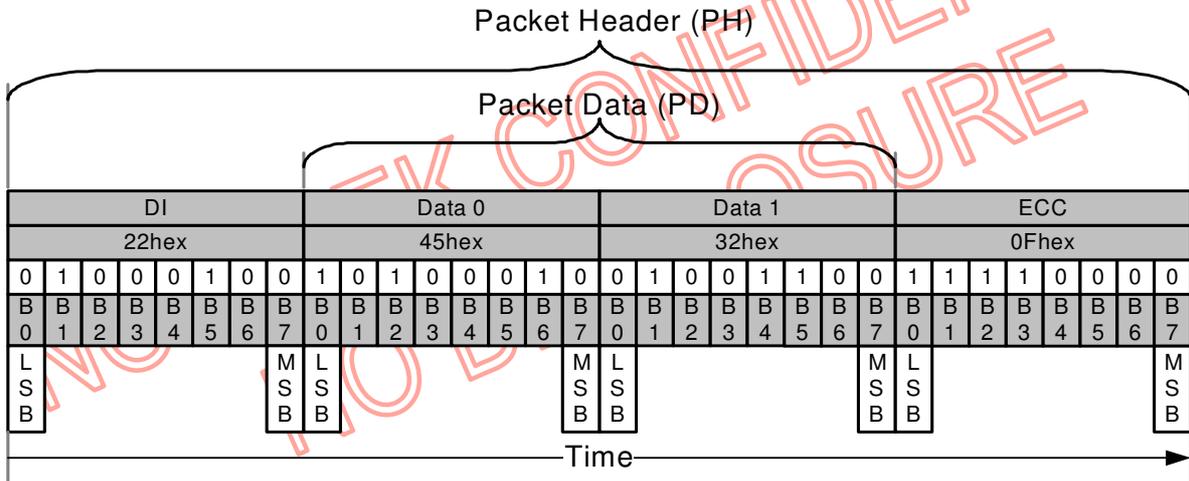
DCS Read Short Response, 2 Bytes Returned (DCSRR2-S), Data Type = 10 0010(22h)

“DCS Read Short Response, 2 Bytes Returned” (DCSRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0010b), from the display module to the MCU. “DCS Read Short Response, 2 Bytes Returned” (DCSRR2-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 0010b
- Packet Data (PD):
 - Data 0: 45h
 - Data 1: 32h
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



DCS Read Short Response, 2 Bytes Returned (DCSRR2-S) - Example

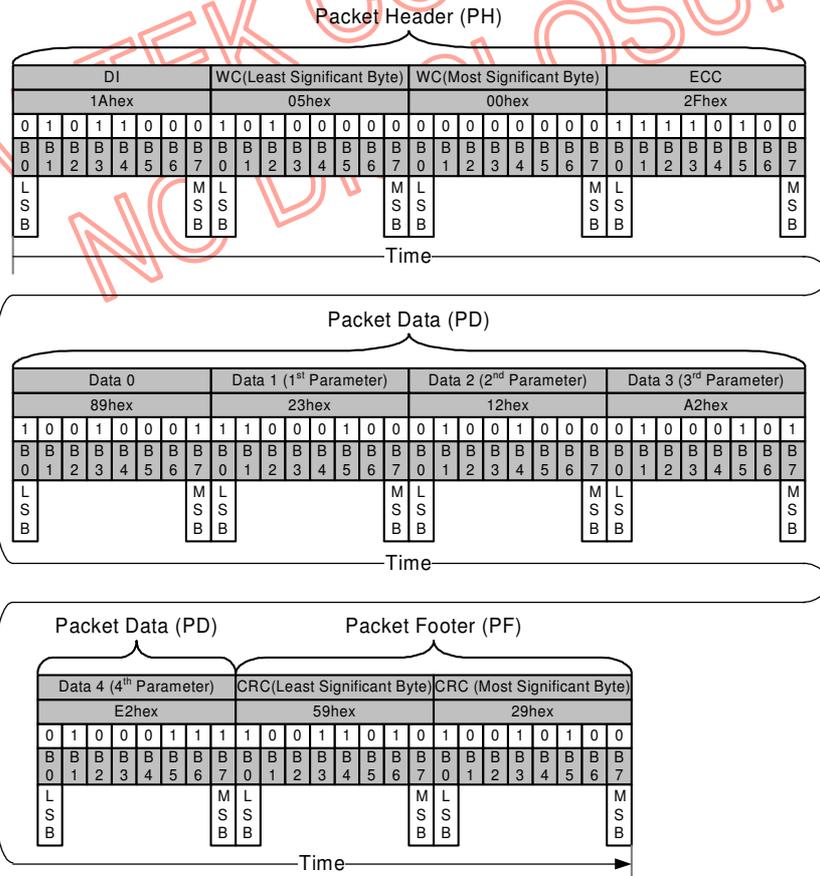
Generic Read Long Response (GENRR-L), Data Type = 01 1010(1Ah)

“Generic Read Long Response” (GENRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 01 1010b), from the display module to the MCU. “Generic Read Long Response” (GENRR-L) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module.

Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 1010b
- Word Count (WC)
 - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: 89h
 - Data 1: 23h
 - Data 2: 12h
 - Data 3: A2h
 - Data 4: E2h
- Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.



Generic Read Long Response (GENRR-L) - Example

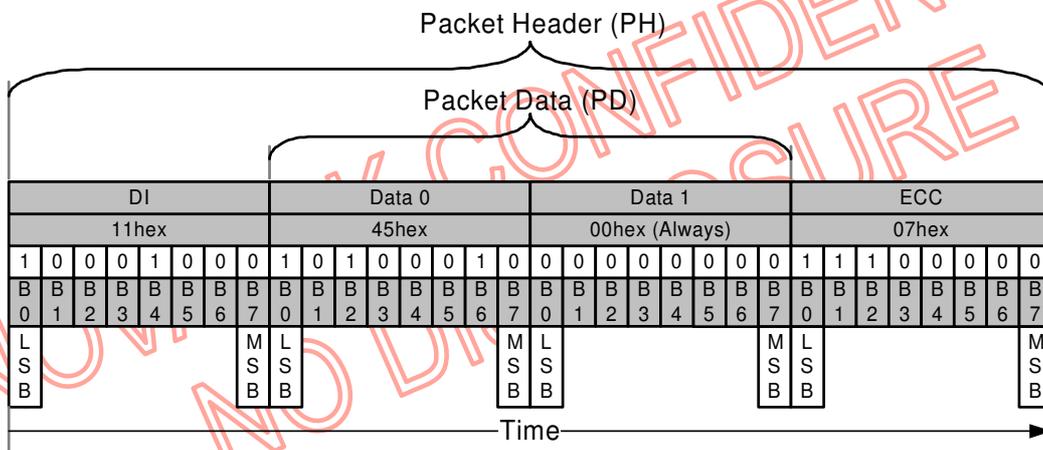
Generic Read Short Response, 1 Byte Returned (GENRR1-S), Data Type = 01 0001(11h)

“Generic Read Short Response, 1 Byte Returned” (GENRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0001b), from the display module to the MCU. “Generic Read Short Response, 1 Byte Returned” (GENRR1-S) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 0001b
- Packet Data (PD):
 - Data 0: 45h
 - Data 1: 00h (Always)
- Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.



Generic Read Short Response, 1 Byte Returned (GENRR1-S) - Example

5.3.4.3.3 COMMUNICATION SEQUENCES

5.3.4.3.3.1 GENERAL

The communication sequences can be done on interface or packet levels between the MCU and the display module. See chapters “Interface Level Communication” and “Packet Level Communication”.

This communication sequence description is for DSI data lanes and it has been assumed that the needed low level communication is done on DSI clock lanes (DSI-CLK+/-) automatically.

Functions of the interface level communication is described on the following table.

Interface Level Communication

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop state
	LPDT	Low power data transmission
	ULPS	Ultra-Low power state
	RAR	Remote application reset
	TEE	Tearing effect event
	ACK	Acknowledge (No error)
	BTA	Bus turnaround
High Speed	HSDT	High speed data transmission

Functions of the packet level communication are described on the following table.

Packet Level Communication

Packet Sender	Abbreviation	Packet Size	Packet Description
MCU	DCSW1-S	SPa	DCS Write, 1 Parameter
	DCSWN-S	SPa	DCS Write, No Parameter
	DCSW-L	LPa	DCS Write, Long
	DCSRN-S	SPa	DCS Read, No Parameter
	SMRPS-S	SPa	Set maximum return packet size
	NP-L	LPa	Null packet, No data
Display Module	AwER	SPa	Acknowledge with error report
	DCSRR-L	LPa	DCS Read, Long Response
	DCSRR1-S	SPa	DCS Read, Short Response
	DCSRR2-S	SPa	DCS Read, Short Response

5.3.4.3.3.2 SEQUENCES
DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is defined on chapter “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” and example sequences, how this packet is used, is described on following tables.

DCS Write, 1 Parameter Sequence - Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, 1 Parameter Sequence - Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

DCS Write, 1 Parameter Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=>	LP-11	-	If no error => goto line 8 If error => goto line 13
7						
8	-	-	<=>	ACK	-	No error
9	-	-	<=>	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12						
13	-	-	<=>	LPDT	AwER	Error report
14	-	-	<=>	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” is defined on chapter “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” and example sequences, how this packet is used, is described on following tables.

DCS Write, No Parameter Sequence - Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence - Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error => goto line 13
7						
8	-	-	<=	ACK	-	No error
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12						
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End

DCS Write Long Sequence

A Long Packet (LPa) of “Display Command Set (DCS) Write Long (DCSW-L)” is defined on chapter “Display Command Set (DCS) Write Long (DCSW-L)” and example sequences, how this packet is used, is described on following tables.

DCS Write, Long Sequence - Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, Long Sequence - Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

DCS Write, Long Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error => goto line 13
7						
8	-	-	<=	ACK	-	No error
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12						
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End

DCS Write, Long Sequence - Example 4

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	Memory Write (2Ch)
3	DCSW-L	HSDT	=>	-	-	Memory Write Continue(3Ch)
4	DCSW-L	HSDT	=>	-	-	Memory Write Continue(3Ch)
5	DCSW1-S	HSDT	=>	-	-	Memory Write Continue(3Ch) with 1 parameter
6	EoTP	HSDT	=>	-	-	End of Transmission Packet
7	-	LP-11	=>	-	-	End

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DCS Read, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” is defined on chapter “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” and example sequences, how this packet is used, is described on following tables.

DCS Read, No Parameter Sequence - Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	SMRPS-S	HSDT	=>	-	-	Define how many data byte is wanted to read: 1 byte
3	DCSRN-S	HSDT	=>	-	-	wanted to get a response ID1 (DAh)
4	EoTP	HSDT	=>	-	-	End of Transmission Packet
5	-	LP-11	=>	-	-	
6	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
7	-	-	<=	LP-11	-	If no error => goto line 9 If error => goto line 14 If error is corrected by ECC => go to line 19
8						
9	-	-	<=	LPDT	DCSRR1-S	Response 1 byte return
10	-	-	<=	LP-11	-	
11	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
12	-	LP-11	=>	-	-	End
13						
14	-	-	<=	LPDT	AwER	Error report
15	-	-	<=	LP-11	-	
16	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
17	-	LP-11	=>	-	-	End
18						
19	-	-	<=	LPDT	DCSRR1-S	Responded 1 byte return
20	-	-	<=	LPDT	AwER	Error Report (Error is Corrected by ECC)
21	-	-	<=	LP-11	-	
22	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
23	-	LP-11	=>	-	-	End

DCS Read, No Parameter Sequence - Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	SMRPS-S	HSDT	=>	-	-	Define how many data byte is wanted to read : 200 byte
3	DCSRN-S	HSDT	=>	-	-	wanted to get a response "Memory Read" (2Eh)
4	EoTP	HSDT	=>	-	-	End of Transmission Packet
5	-	LP-11	=>	-	-	
6	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
7	-	-	<=	LP-11	-	If no error => goto line 9 If error => goto line 14 If error is corrected by ECC => go to line 19
8						
9	-	-	<=	LPDT	DCSRR-L	Responded 200 bytes return
10	-	-	<=	LP-11	-	
11	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
12	-	LP-11	=>	-	-	End
13						
14	-	-	<=	LPDT	AwER	Error report
15	-	-	<=	LP-11	-	
16	-	BTA	<=>	BTA	-	Interface control change from the display module t to he MCU
17	-	LP-11	=>	-	-	End
18						
19	-	-	<=	LPDT	DCSRR-L	Responded 200 bytes return
20	-	-	<=	LPDT	AwER	Error Report (Error is Corrected by ECC)
21	-	-	<=	LP-11	-	
22	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
23	-	LP-11	=>	-	-	End

Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined on chapter “Null Packet, No Data (NP-L)” and example sequences, how this packet is used, is described on following tables.

Null Packet, No Parameter Sequence - Example

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only high speed data transmission is used.
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

End of Transmission Packet

A Short Packet (SPa) of “End of Transmission (EoT)” is defined on chapter “End of Transmission Packet (EoT)” and an example sequences, how this packet is used, is described on following tables.

End of Transmission Packet - Example

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only high speed data transmission is used.
2	EoTP	HSDT	=>	-	-	End of Transmission Packet
3	-	LP-11	=>	-	-	End

5.3.4.4 VIDEO MODE COMMUNICATION

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

5.3.4.4.1 TRANSMISSION PACKET SEQUENCES

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. In the following sections, *Burst Mode* refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

- Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
- Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
- Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. It is recommended to return to LP state once per scan-line during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero, and burst mode will be indistinguishable from non-burst mode.

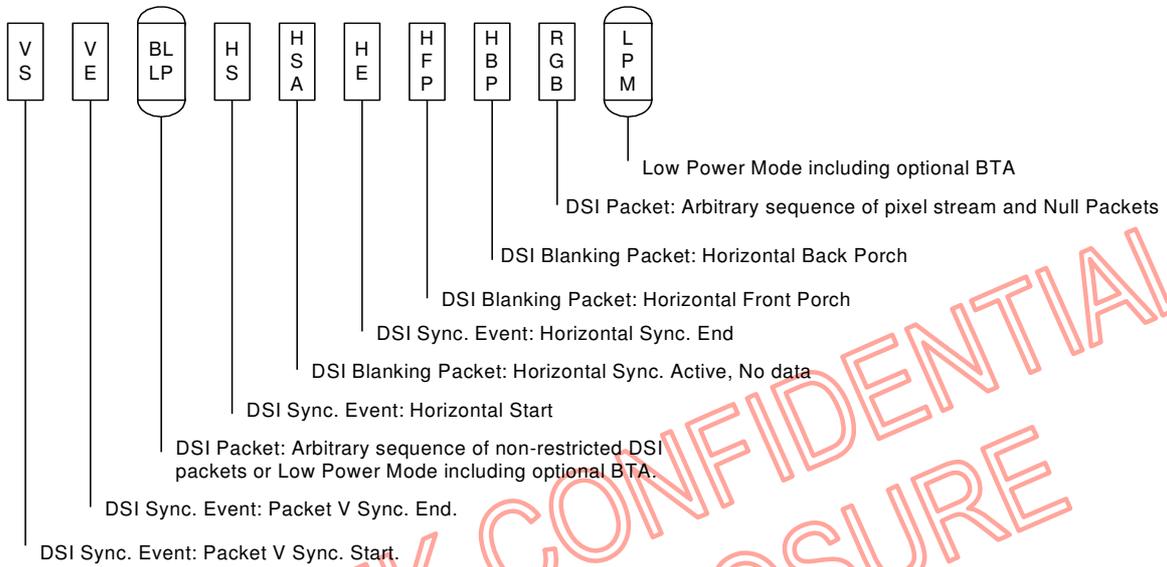
During the BLLP the DSI Link may do any of the following:

- Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX
- Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode
- Transmit one or more non-video packets from the host processor to the peripheral using HS Mode
- If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode
- Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VS; all other lines shall start with HS. This is also true in the special case when $VSA+VBP=0$. Note that the position of synchronization packets, such as VS and HS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. If necessary, a horizontal scan-line of active pixels may be divided into two or more packets. However, individual pixels shall not be split across packets.

Transmission packet components used in the figures in this section are defined in Figure below unless otherwise specified.

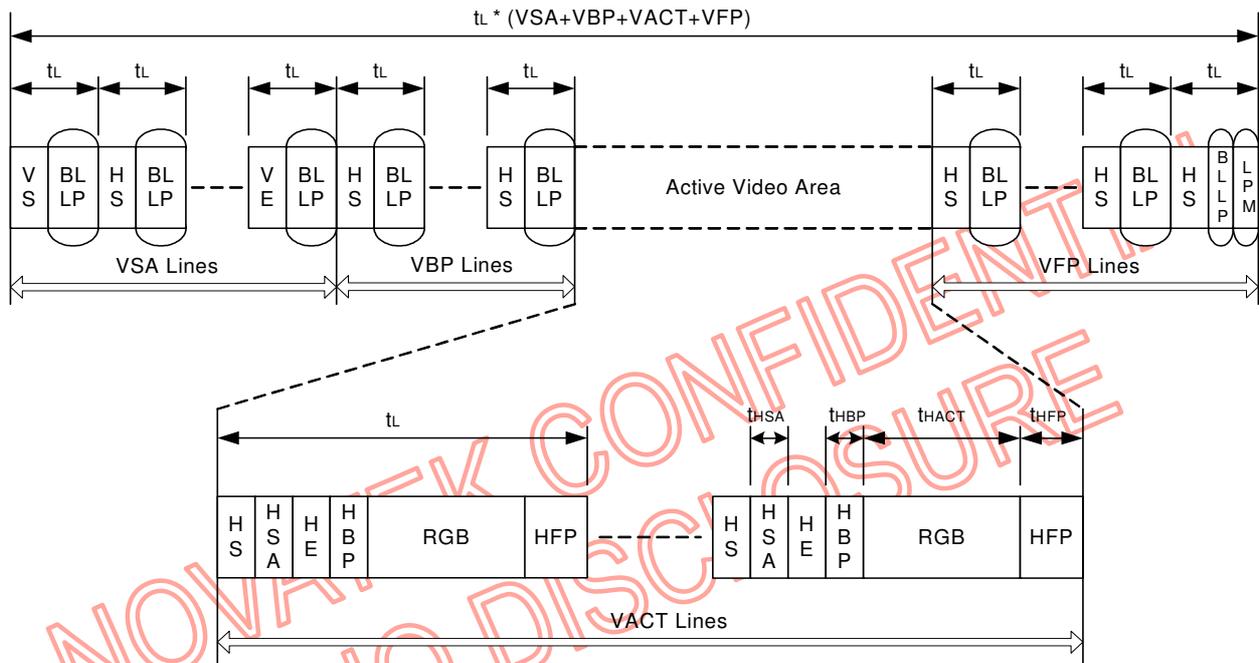


DSI Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

5.3.4.4.2 NON-BURST MODE WITH SYNC PULSES

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure below.

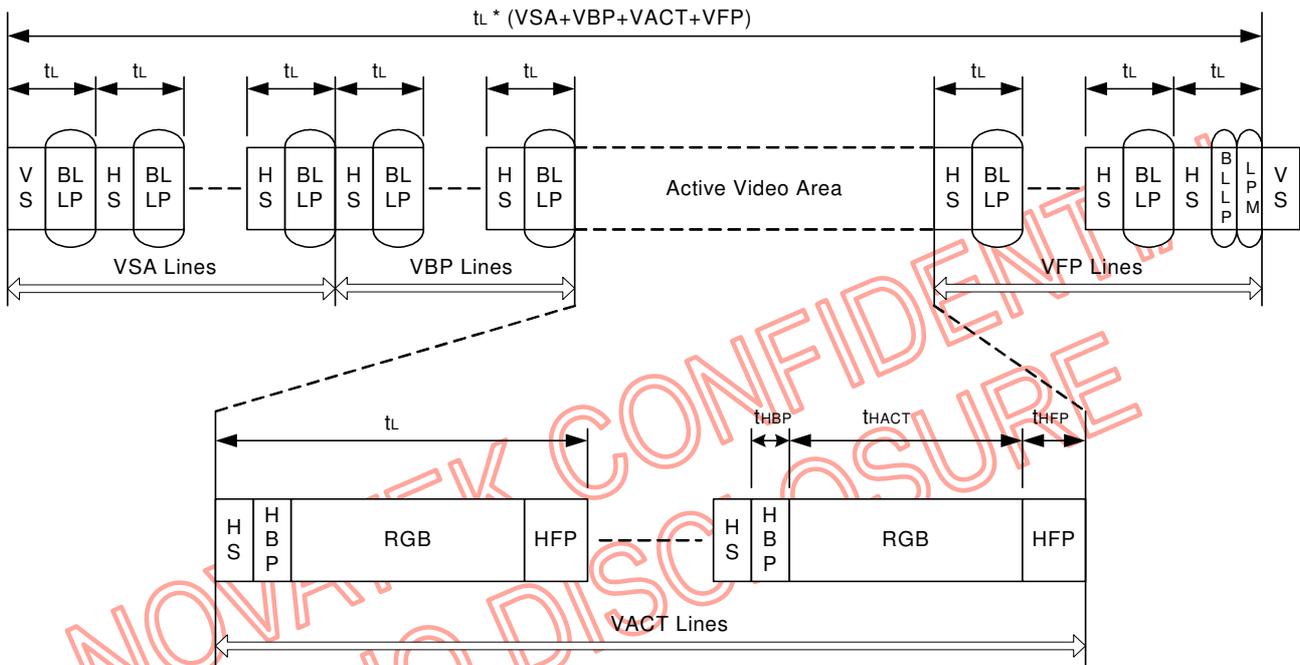


DSI Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End

Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

5.3.4.4.3 NON-BURST MODE

This mode is a simplification of the format described in section 5.3.4.4.2 “Non-Burst Mode with Sync Pulse”. Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel display interface such as DPI-2. An example of this mode is shown in Figure below.

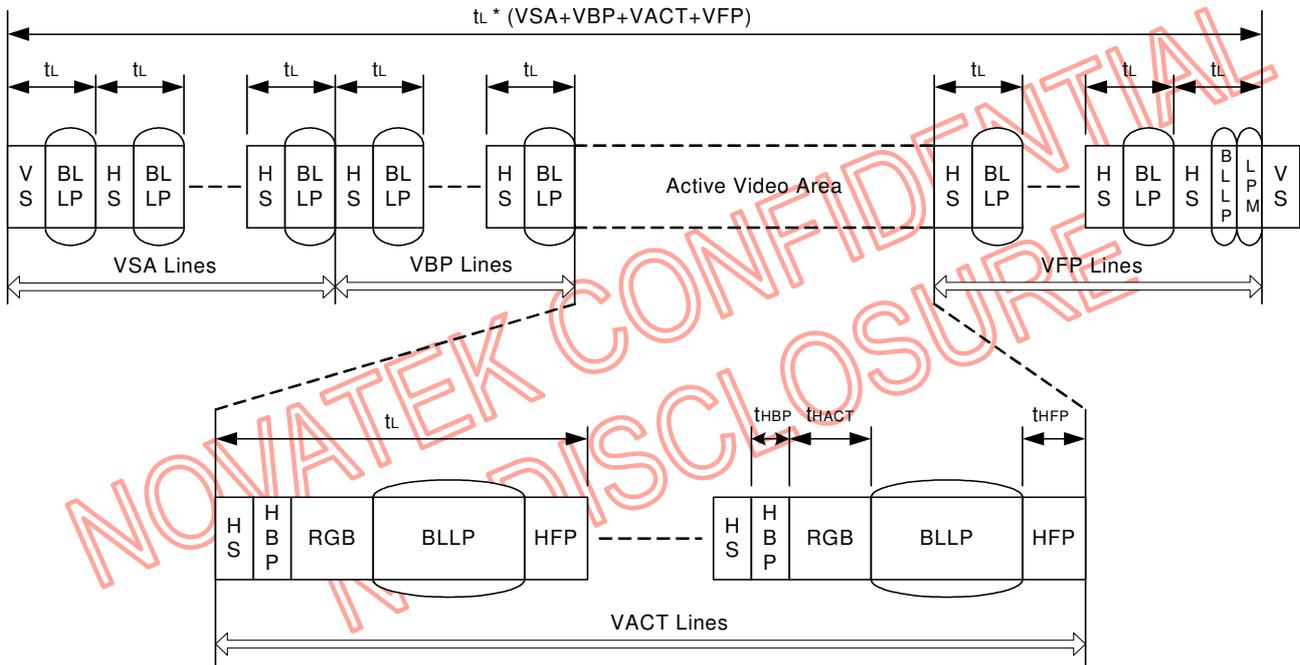


DSI Video Mode Interface Timing: Non-burst Transmission

As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

5.3.4.4.4 BURST MODE

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. Following HS pixel data transmission, the bus goes to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in Figure below.



DSI Video Mode Interface Timing: Burst Transmission

Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

5.3.4.4.5 Parameters

Below table documents the parameters used in the preceding figures. Peripheral supplier companies are responsible for specifying suitable values for all blank fields in the table. The host processor shall meet these requirements to ensure interoperability.

Required Peripheral Timing Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
BRPHY	Bit rate total on all Lanes	nHD	80	-	500	Mbps
tL	Line time	nHD	-	24.44	-	us
tHBP	Horizontal back porch	nHD	1	-	-	us
tHACT	Time for image data	1 data lane	15	-	Note3	us
HACT	Active pixels per line	nHD	-	360	-	pixels
tHFP	Horizontal front porch	-	1	-	-	us
VSA	Vertical sync active	-	1	-	-	H
VBP	Vertical back porch	-	40, Note2	-	-	H
VACT	Active lines per frame	nHD	-	640	-	H
VFP	Vertical front porch	-	2	-	-	H

Note1: Frame rate (Typ)=60Hz

Note2: VBP (min) value can change by command set.

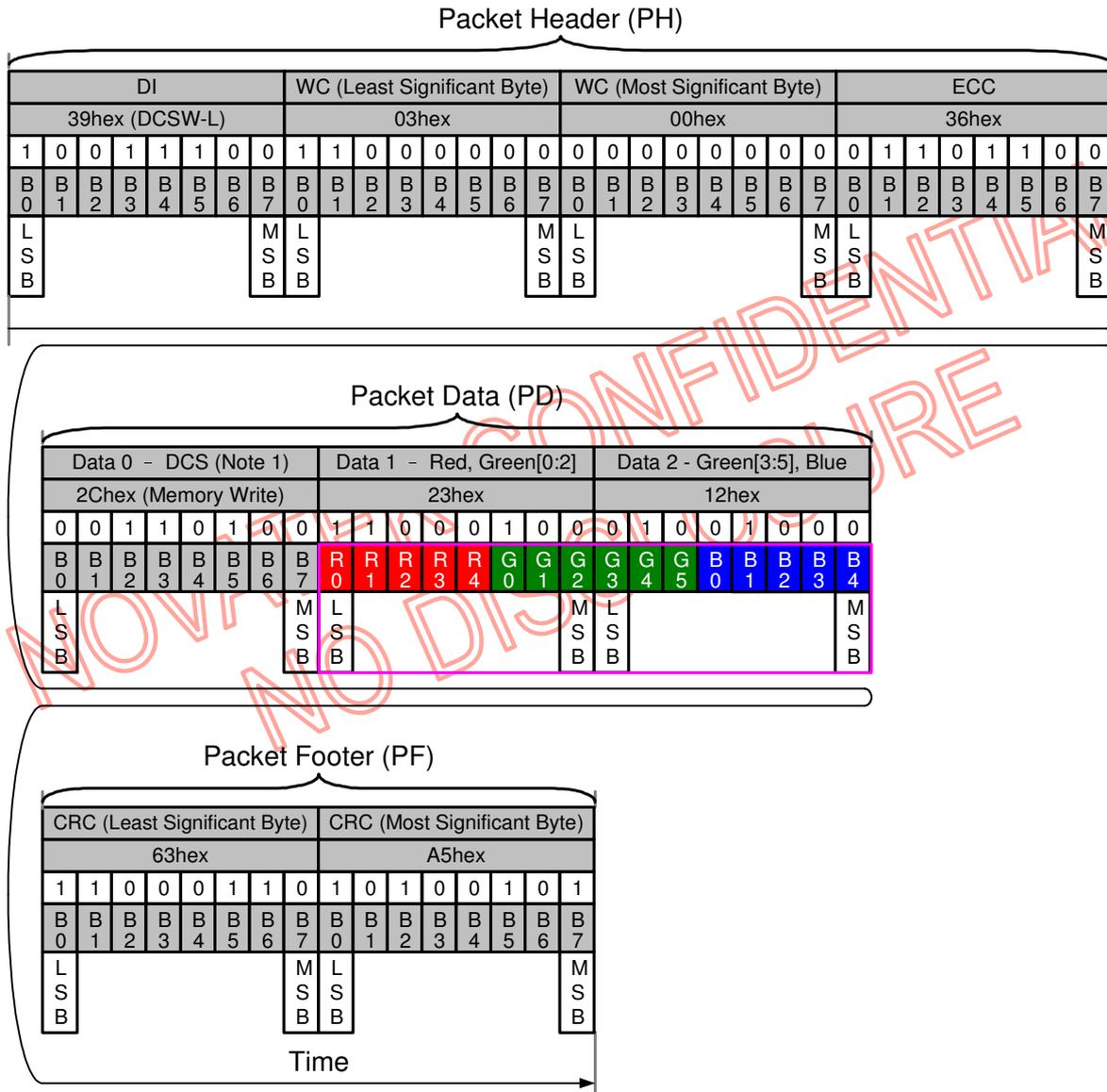
Note3: tHACT+tHFP+tHBP ≥ tL

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5.3.5 Memory Write/Read Format

- 16 bit/pixel Writing

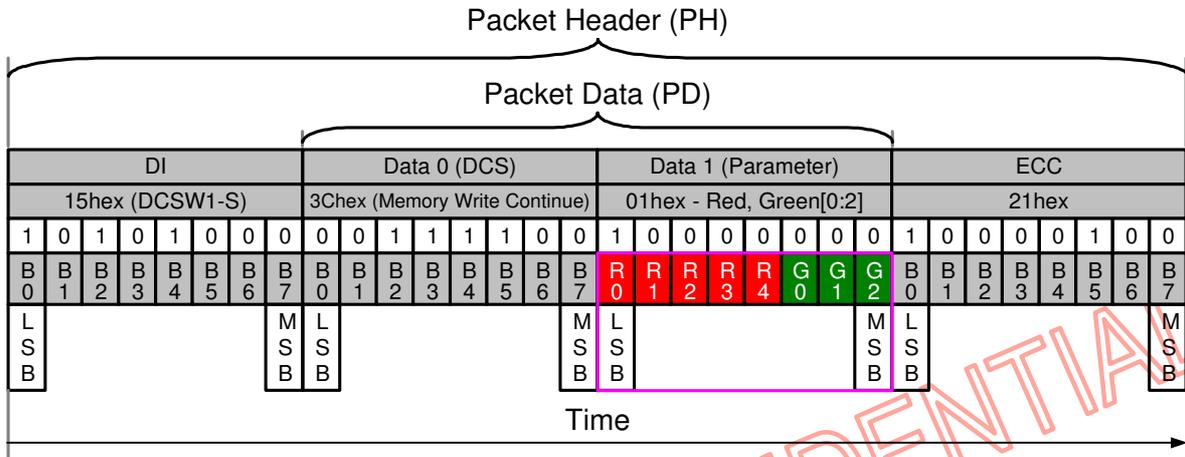
The MCU can send to the display module a following packet.



Notes:

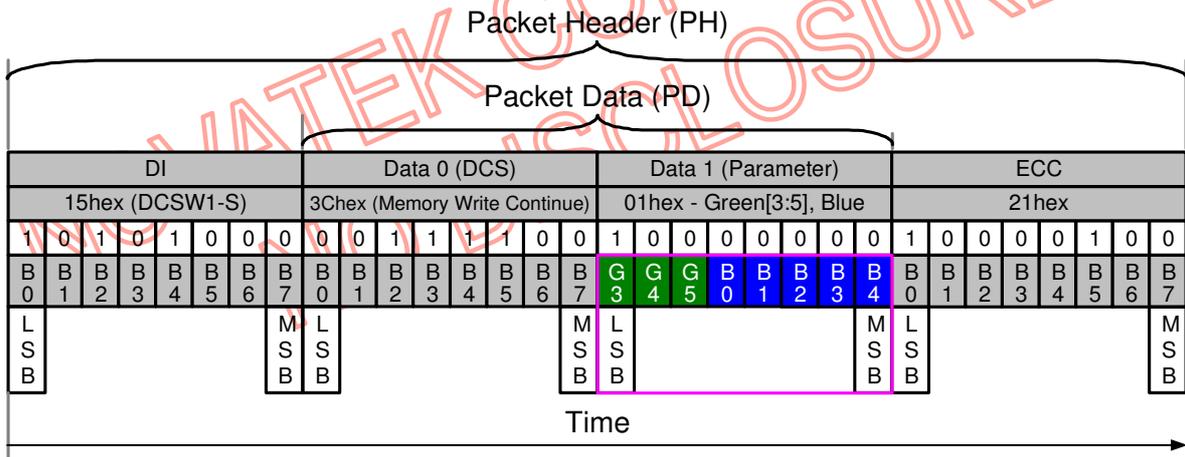
1. Memory Write (2Ch) or Memory Write Continue (3Ch)
2. It is possible that one pixel information is split in one different packets which are ending and starting as follows: RG – GB (2 packets)
3. Packet can include several pixel (Not only one pixel as in this example)

One Pixel Write (DCSW-L) – Example 1



Note: DCS (Data 0) can also be "Memory Write (2Ch)" command

Red/Green[0:2] Subpixel Write (DCSW1-S) – Example 2



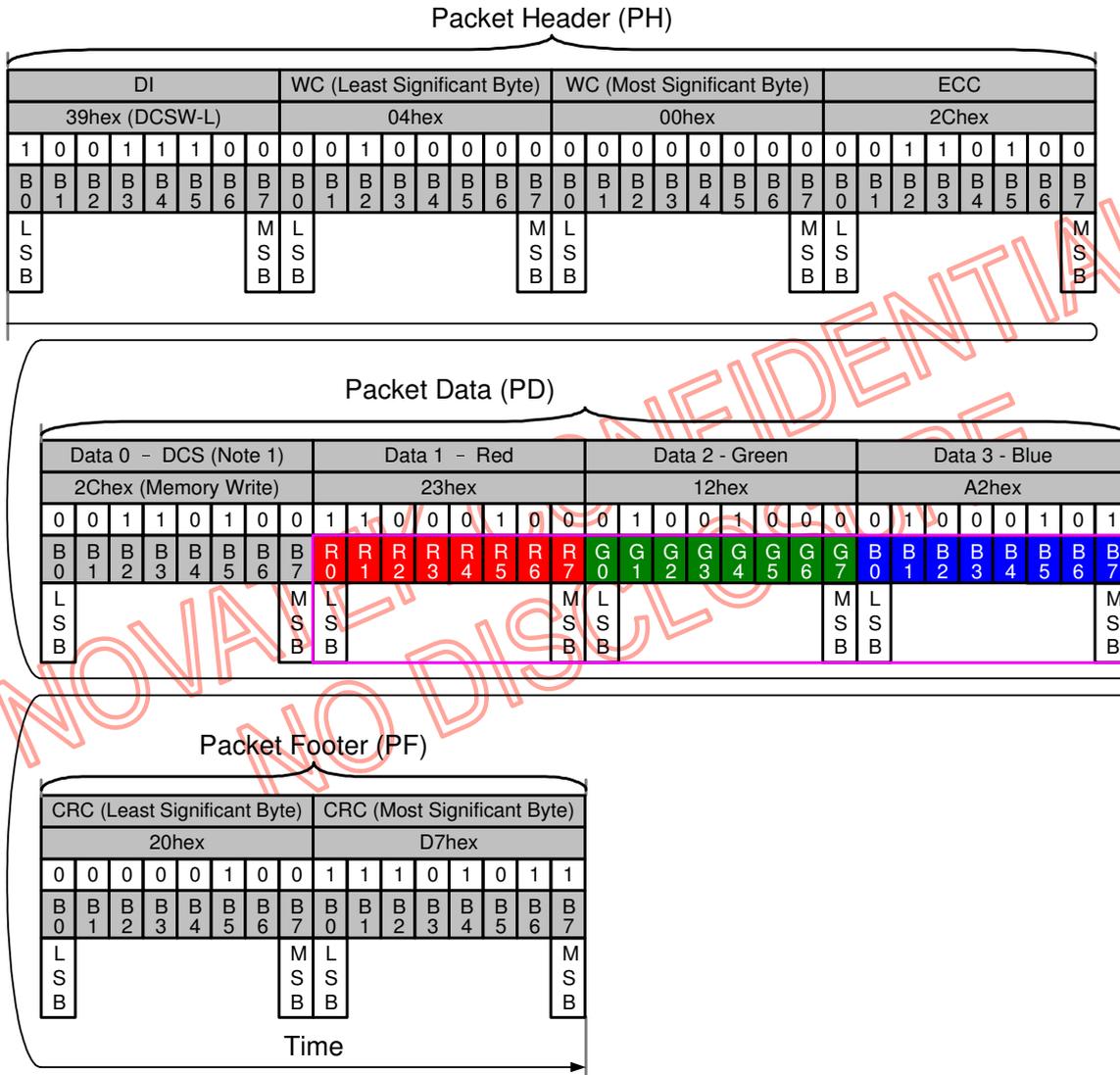
Notes:

1. DCS (Data 0) can not be "Memory Write (2Ch)" command. It must always be "Memory Write Continue (3Ch)".
2. Previous data byte was R[0:4]G[0:2]

Green[3:5]/Blue Subpixel Write (DCSW1-S) – Example 3

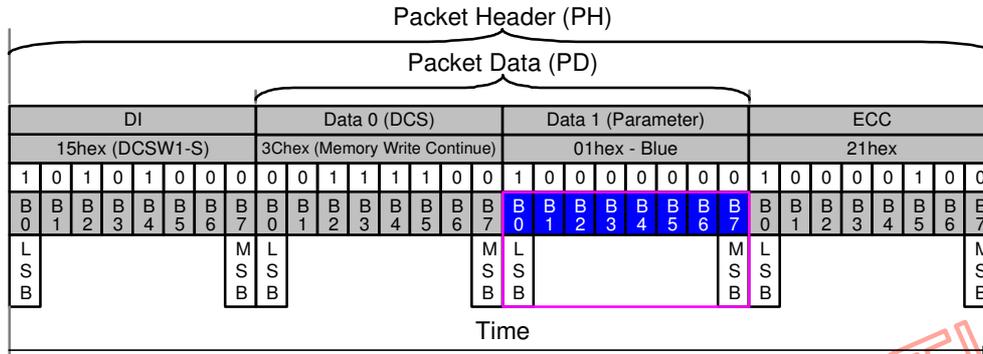
- 24 bit/pixel Writing

The MCU can send to the display module a following packet.


Notes:

1. Memory Write (2Ch) or Memory Write Continue (3Ch)
2. It is possible that one pixel information is split in one different packets which are ending and starting as follows:
 - R - GB (2 packets)
 - RG - B (2 packets)
 - R - G - B (3 packets)
3. Packet can include several pixel (Not only one pixel as in this example)

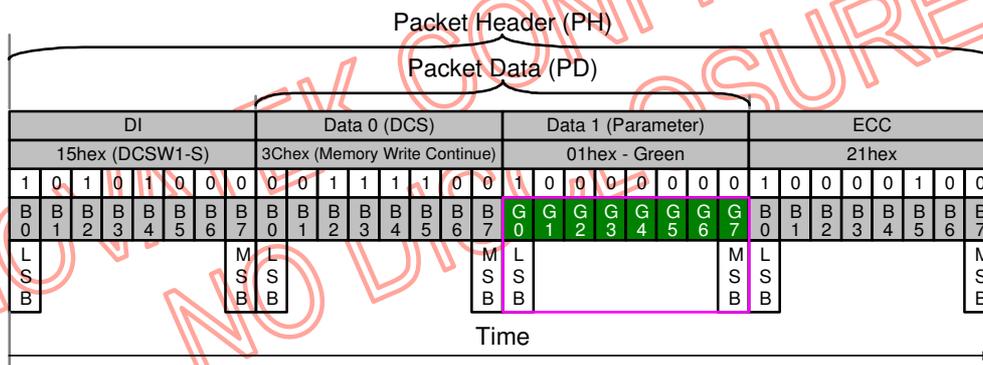
One Pixel Write (DCSW-L) - Example 1



Notes:

1. DCS (Data 0) can not be "Memory Write (2Ch)" command. It must be always be "Memory Write Continue(3Ch)" .
2. Previous data byte was G[0:7]

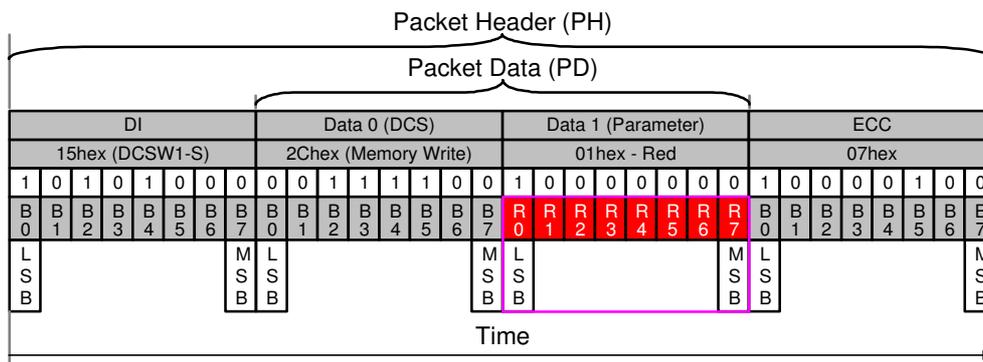
Blue Subpixel Write (DCSW1-S) - Example 2



Notes:

1. DCS (Data 0) can not be "Memory Write (2Ch)" command. It must always be "Memory Write Continue (3Ch)".
2. Previous data byte was R[0:7]

Green Subpixel Write (DCSW1-S) - Example 3

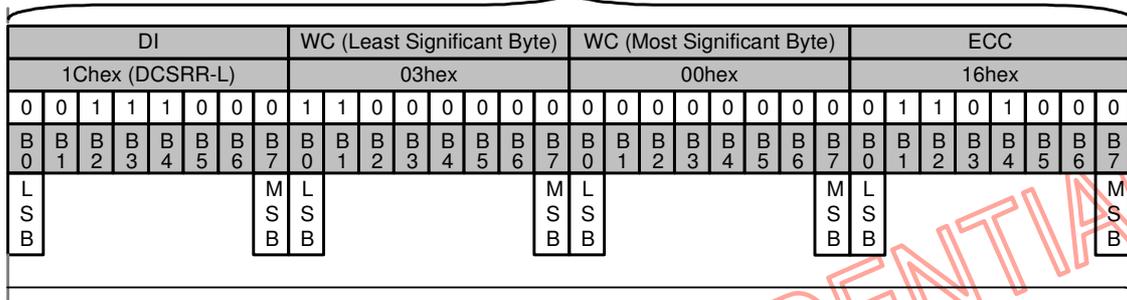
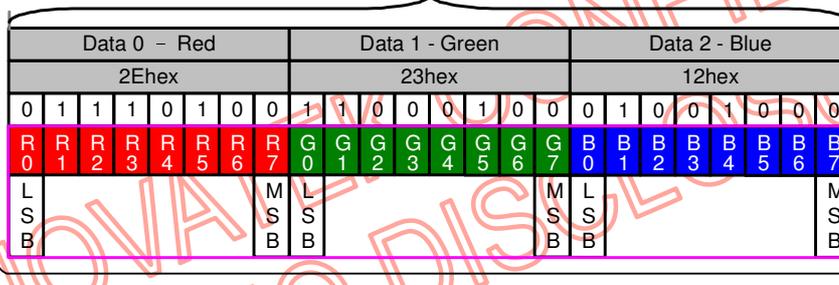
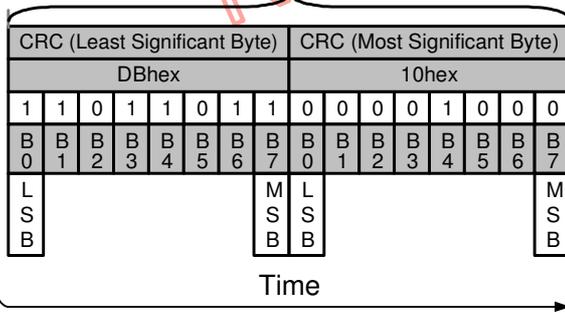


Note: DCS (Data 0) can also be "Memory Write Continue (3Ch)" command.

Red subpixel Write (DCSW1-S) - Example 4

- 24 bit/pixel Reading

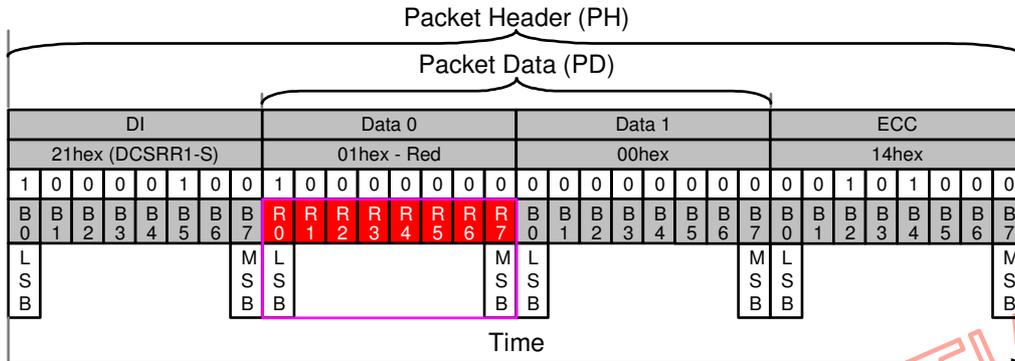
The display module can send to the MCU following packets after the MCU has a read command “Memory Read (2Eh” or “memory Read Continue (3Ch)”.

Packet Header (PH)

Packet Data (PD)

Packet Footer (PF)


Note: It is possible that one pixel information is split in two or three different packets:

- R - GB (2 packets)
- RG - B (2 packets)
- R - G - B (3 packets)

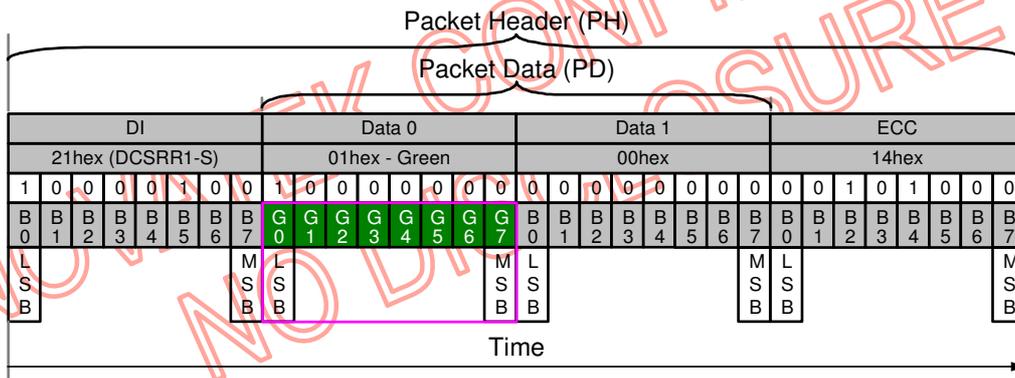
One Pixel Read Response (DCSRR-L) - Example 1



Notes:

1. Data 1 is always "00h".
2. Previous data byte was B[0:7]

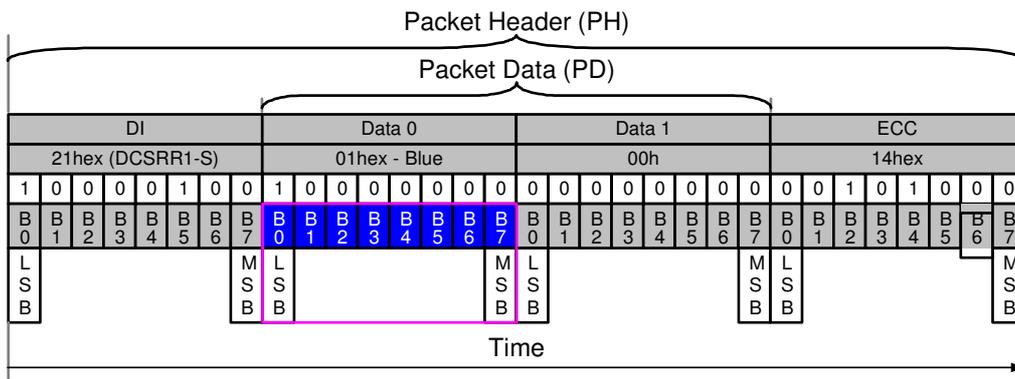
Red Subpixel Response (DCSRR1-S) - Example 2



Notes:

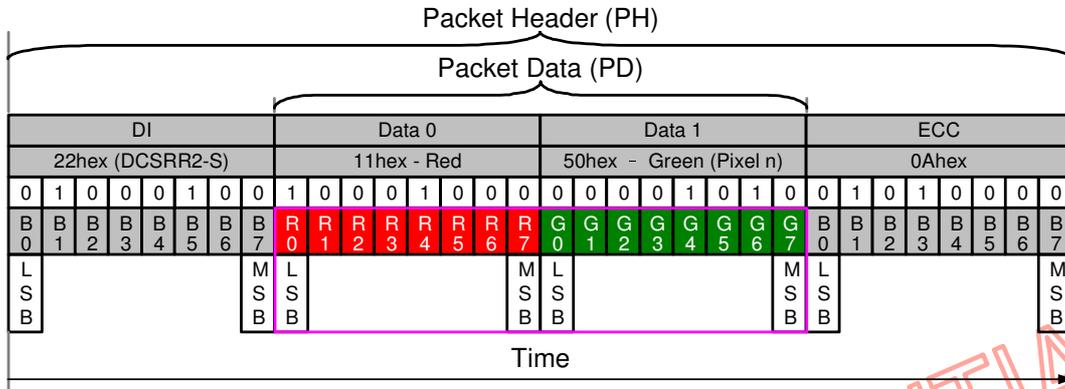
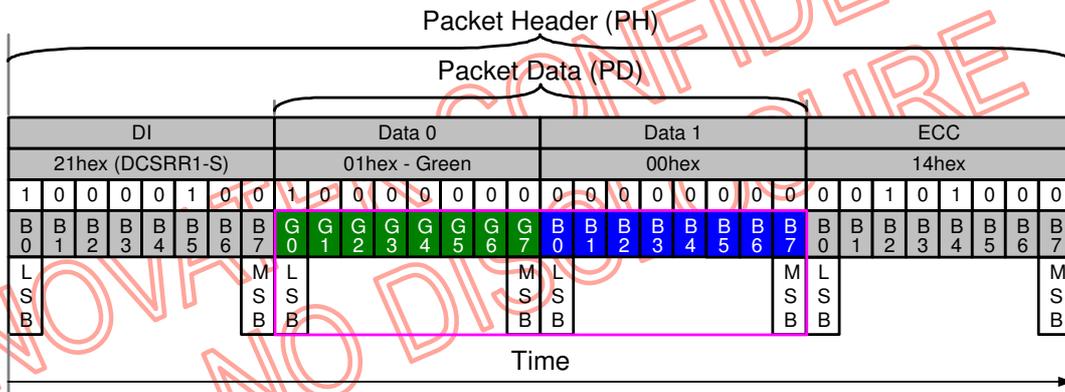
1. Data 1 is always "00h".
2. Previous data byte was R[0:7]

Green Subpixel Response (DCSRR1-S) - Example 3

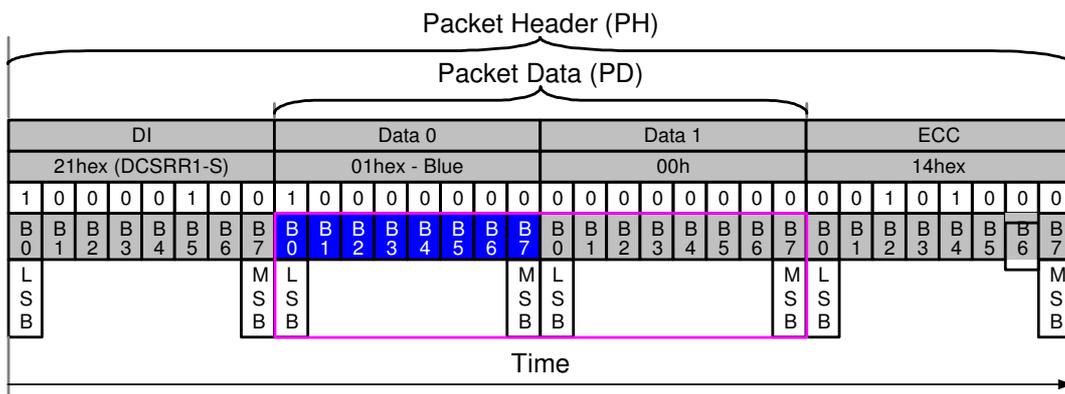


Note: Data 1 is always "00h".

Blue subpixel Response (DCSRR1-S) - Example 4


Red and Green Subpixels Response (DCSRR2-S) - Example 5


Note: Previous data byte was R[0:7]

Green and Blue Subpixels Response (DCSRR2-S) - Example 6


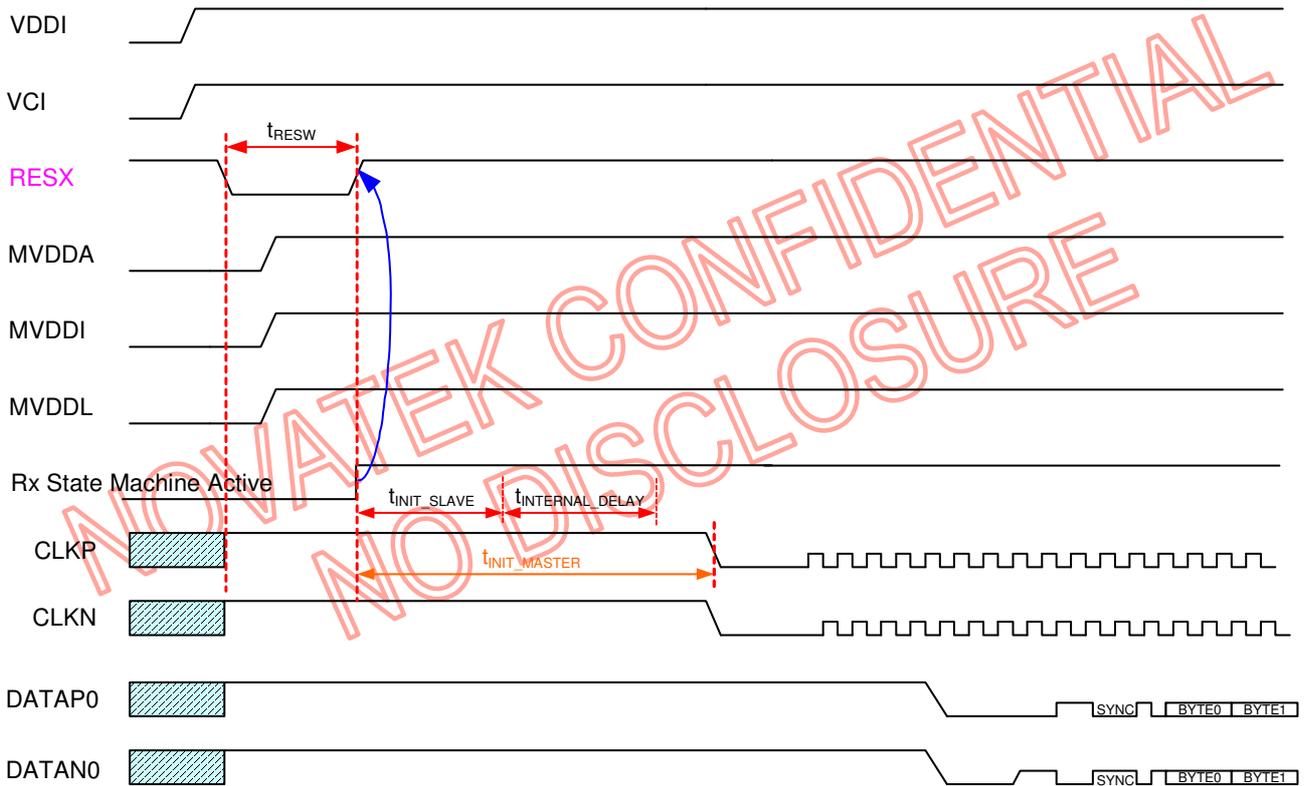
Note: Previous data byte G[0:7]

Blue and Red Subpixels Response (DCSRR2-S) - Example 7

5.3.6 System Power-Up and Initialization

After power-on, the host processor shall observe an initialization period, t_{INIT} , during which it shall drive a sustained Tx-Stop state (LP-11) on all Lanes of the Link.

Figure below illustrates an example power-up sequence for a DSI display module. In the figure, a hardware reset (RESX) mechanism is assumed for initialization. Internally within the display module, de-assertion of RESX could happen after both IO and core voltages were ramped up. In this example, the host's t_{INIT_MASTER} parameter is programmed for driving LP-11 for a period longer than the sum of t_{RESW} , t_{INIT_SLAVE} and $t_{INTERNAL_DELAY}$. The display module may ignore all Lane activities during this time.



$$(t_{INIT_MASTER}) \geq (t_{RESW} + t_{INIT_SLAVE} + t_{INTERNAL_DELAY})$$

Symbol	Parameter	Min	Typ	Max	Units
t_{INIT_MASTER}	MIPI Tx initialize time	5	-	-	mS
t_{RESW}	Reset "L" pulse width	Note	-	-	μ S
t_{INIT_SLAVE}	MIPI Rx initialize time	4	-	-	mS
$t_{INTERNAL_DELAY}$	Internal delay time.	500	-	-	μ S

Note: See section "7.7.6 Reset Input Timing"

5.4 MDDI INTERFACE

The NT35410 supports the Mobile Display Digital Interface (MDDI) is a differential small amplitude serial interface for high-speed data transfer through the following four lines: D0_P/D0_N and CLK_P/CLK_N.

The specifications of MDDI supported by the NT35410 meet the MDDI specifications Version 1.2 as published by the Video Electronics Standards Association (VESA).

The NT35410 offers the Bi-direction Link to use for the register and display data read / write.

For power saving, the NT35410 offers both Hibernation mode (Send shutdown packet), and enter deep standby mode to reduce power consumption.

The NT35410 supports the MDDI Type-I of the MDDI specifications Version 1.2 and the application diagram is illustrated as Fig. 5.4.1.

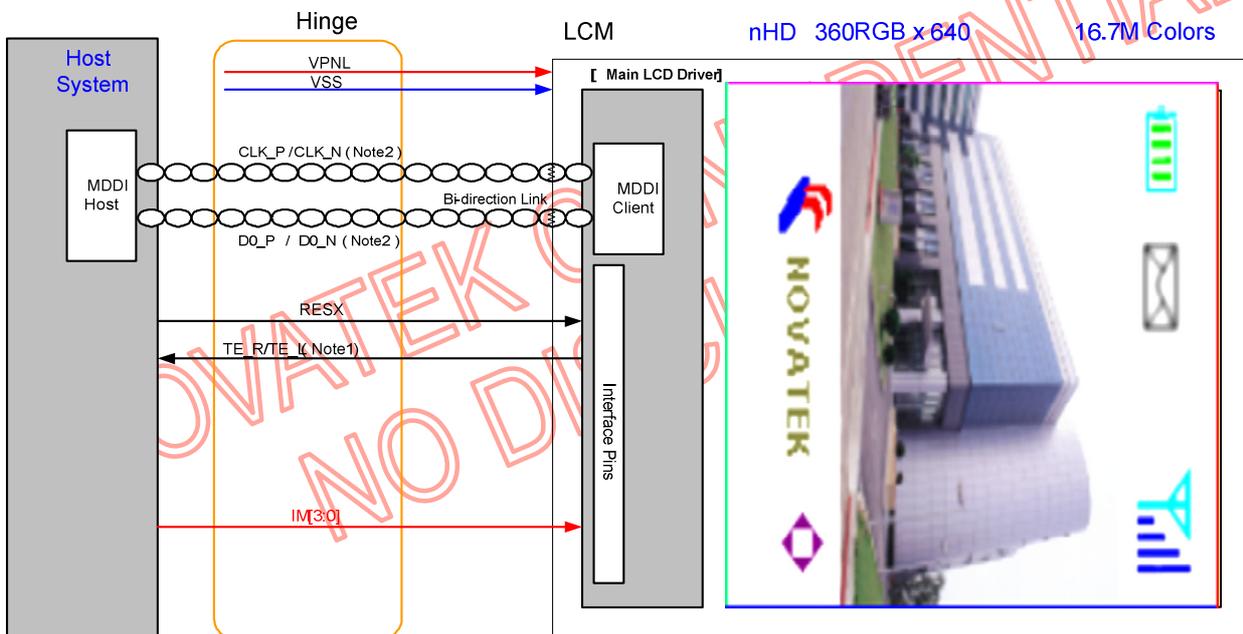


Fig. 5.4.1 MDDI application diagram

Notes:

1. Based on the system configuration, use TE signal as the reference signal for moving picture display to avoid the tearing effect.
2. In MDDI mode, an internal terminal resistor of 100 ohm are embedded between D0_P/D0_N and CLK_P/CLK_N.
3. When enter to the MDDI interface from other interface, the Host needs to wait 100ms and can start to send any packet. For example wake up packet.
4. After shutting down the MDDI interface the Host needs to wait 500ns and can start to send wake up packet to wake up the MDDI link.

5.4.1 MDDI Link Protocol by The NT35410

The NT35410's MDDI Link Protocol is in accordance with the MDDI specifications as published by VESA; refer to these specifications for more information on the MDDI Link Protocol.

DO NOT send any packets that are not supported by the NT35410 into a system containing the NT35410. Supported MDDI packets are as follows:

Table 5.4.1 Summary of MDDI packets supported by NT35410

NT35410 MDDI packets	Packet Name	Packet Type	Direction
<i>Link Control Packet</i>	<i>Sub-frame header packet</i>	<i>15359 (0x3BFF)</i>	<i>Forward</i>
	<i>Filler packet</i>	<i>0</i>	<i>Forward/Reverse</i>
	<i>Link Shutdown packet</i>	<i>69 (0x45)</i>	<i>Forward</i>
	<i>Reverse link encapsulation packet</i>	<i>65 (0x41)</i>	<i>Forward</i>
	<i>Round-trip delay measurement packet</i>	<i>82 (0x52)</i>	<i>Forward</i>
	<i>Client capability packet</i>	<i>66 (0x42)</i>	<i>Reverse</i>
	<i>Client request and status packet</i>	<i>70 (0x46)</i>	<i>Reverse</i>
	<i>Forward Link Skew Calibration Packet</i>	<i>83(0x53)</i>	<i>Forward</i>
<i>Register Access Packet</i>	<i>Register access packet</i>	<i>146 (0x92)</i>	<i>Forward/Reverse</i>
<i>Basic Media Stream Packet</i>	<i>Video stream packet</i>	<i>16 (0x10)</i>	<i>Forward</i>
	<i>Flexible video stream packet</i>	<i>20 (0x14)</i>	<i>Forward</i>
	<i>Windowless video stream packet</i>	<i>22 (0x16)</i>	<i>Forward</i>

5.4.2 MDDI Link Packet Descriptions by the NT35410

Sub-frame Header Packet

The Sub-Frame Header Packet is the first packet of every sub-frame.

Sub-frame Header Packet								
Packet Length	Packet Type =0x3bff	Unique word = 0x005a	Reversed 1	Sub-frame Length	Protocol Version	Sub-frame Count	Media-frame Count	CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	2 bytes	4 bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 0x3bff

Unique Word: unique word is 0x005a

Reserved 1: not used (set to zero)

Sub-frame Length: specify the number of bytes per sub-frame

Protocol version:

Bits [15:2] – Reserved for future expansion. These should be set to all zero.

Bits[1:0] – Sub-frame operational mode

- “00” – Sub-frame lengths strictly followed.
- “01” – Sub-frame lengths are flexible. Sub-frame packets should be sent at the first opportunity after the sub-frame length has been transmitted.
- “10” – Sub-frame lengths are unlimited. No more sub-frame packets are required to be transmitted after the first Sub-Frame packet at startup.

Sub-frame Count: specify the number of sub-frame header packet

Media-frame Count: specify the number of media-frames

CRC: error check

Filler Packet

The Filler Packet is sent when no other information is available to be sent on the forward or reverse link.

Filler Packet			
Packet Length	Packet Type=0	Filler Bytes (all zero recommended)	CRC
2 bytes	2 bytes	(Packet_Length - 4) bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

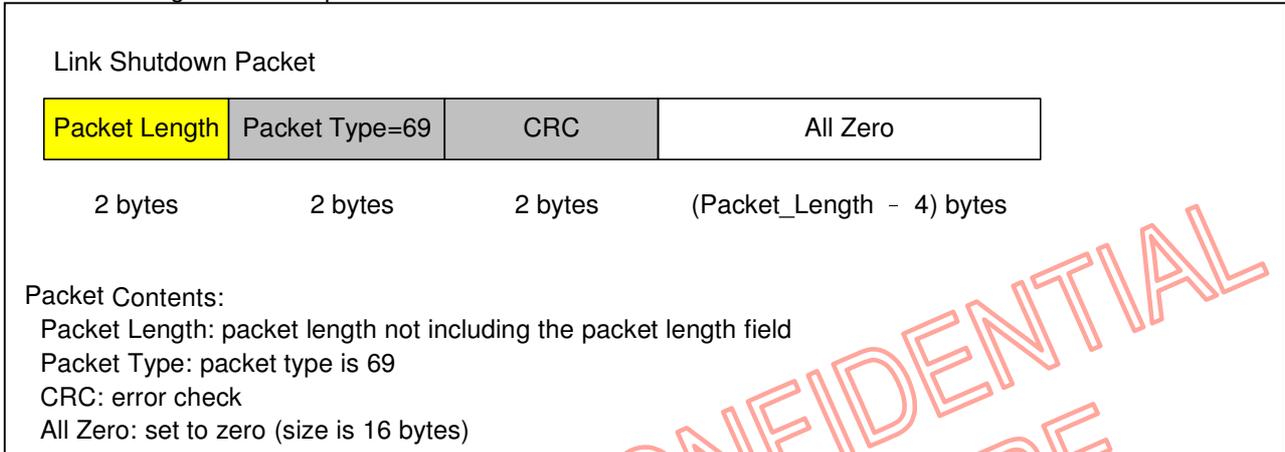
Packet Type: packet type is 0

Filler Bytes: set to zero

CRC: error check

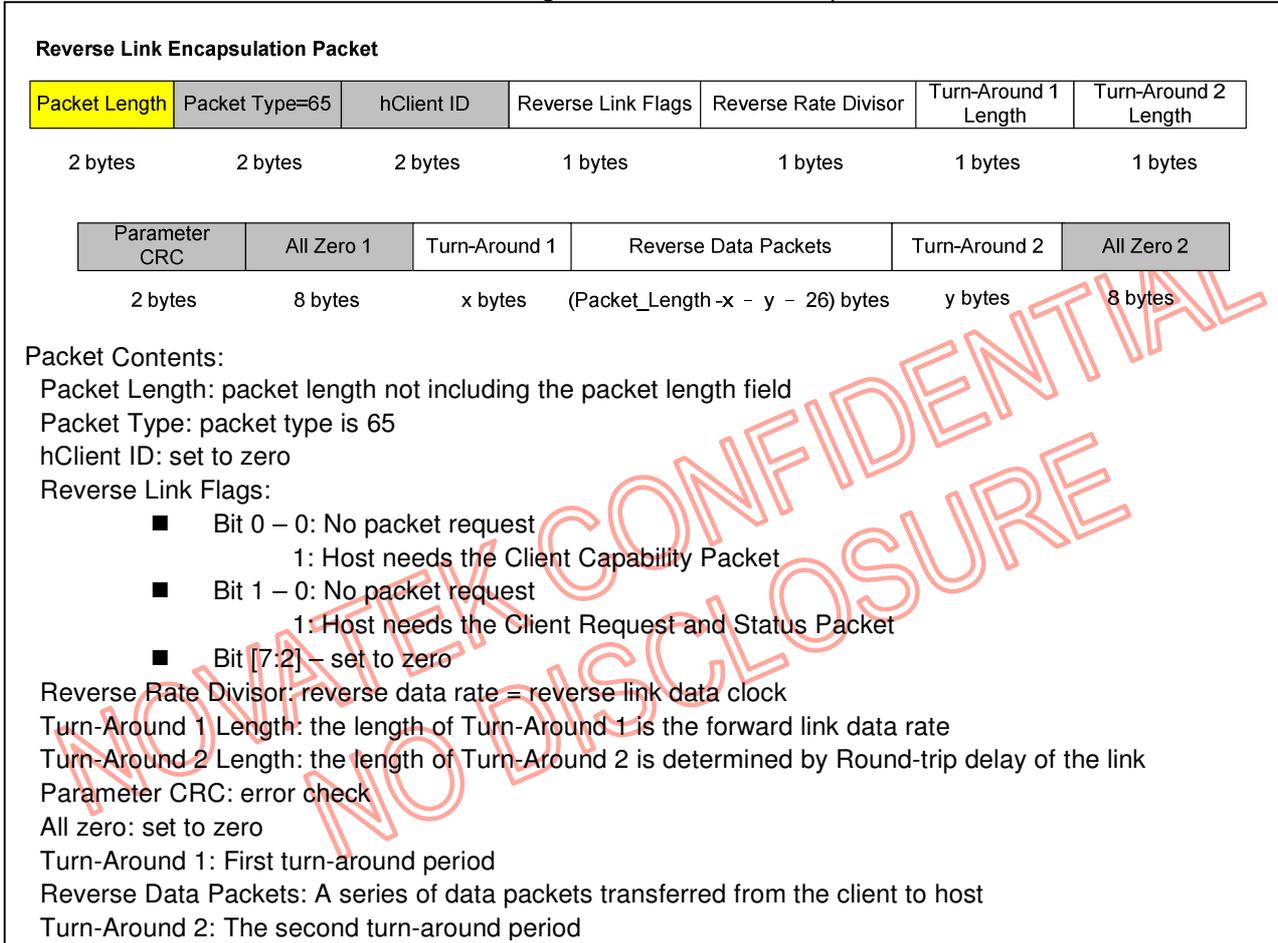
Link Shutdown Packet

The Link Shutdown Packet is sent from the host to the client to indicate that the MDDI data and strobe will be shut down and go into a low-power hibernation state.


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Reverse Link Encapsulation Packet

Data is transferred in the reverse direction using the Reverse Link Encapsulation Packet.



Round-Trip Delay Measurement Packet

The Round-Trip Delay Measurement Packet is used to measure the propagation delay from the host to the client plus the delay from the client back to the host. This packet is most useful when the MDDI link is running at the maximum speed intended for a particular application. The packet may be sent in Type I mode and at a lower data rate to increase the range of the Round-Trip delay measurement.

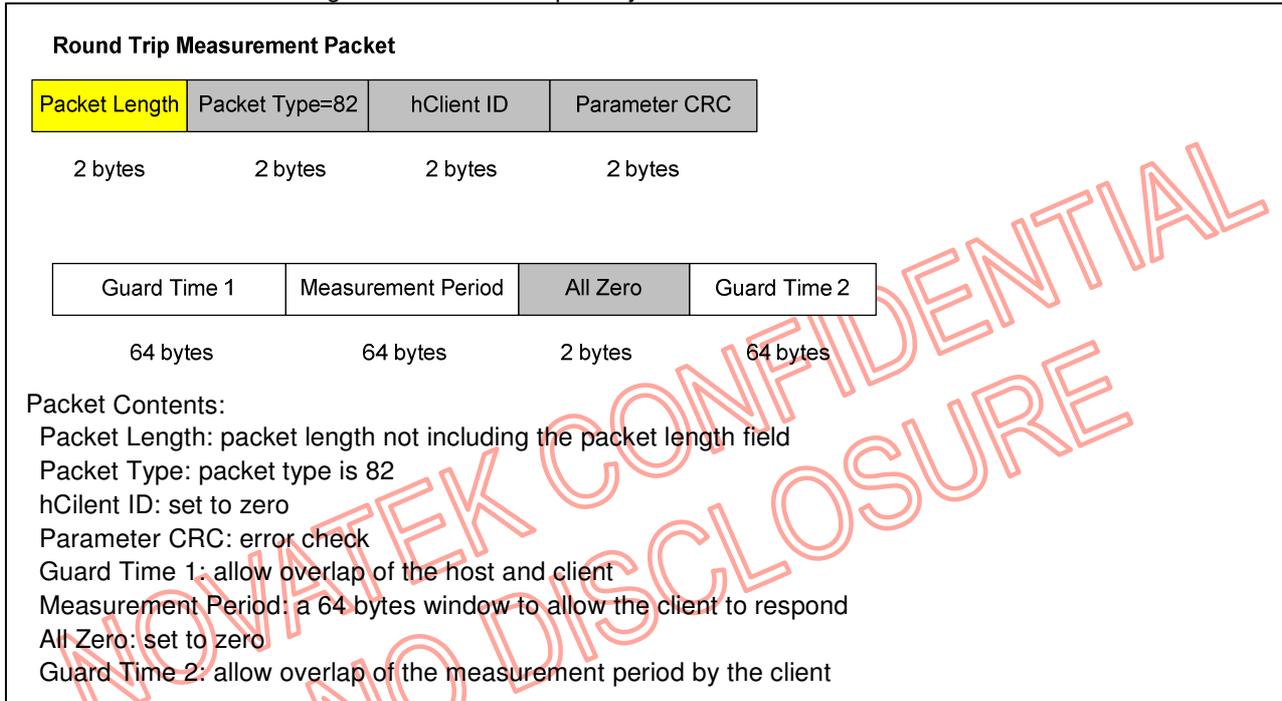


Fig. 5.4.2 illustrates the timing of events during the Round-Trip Delay Measurement Packet.

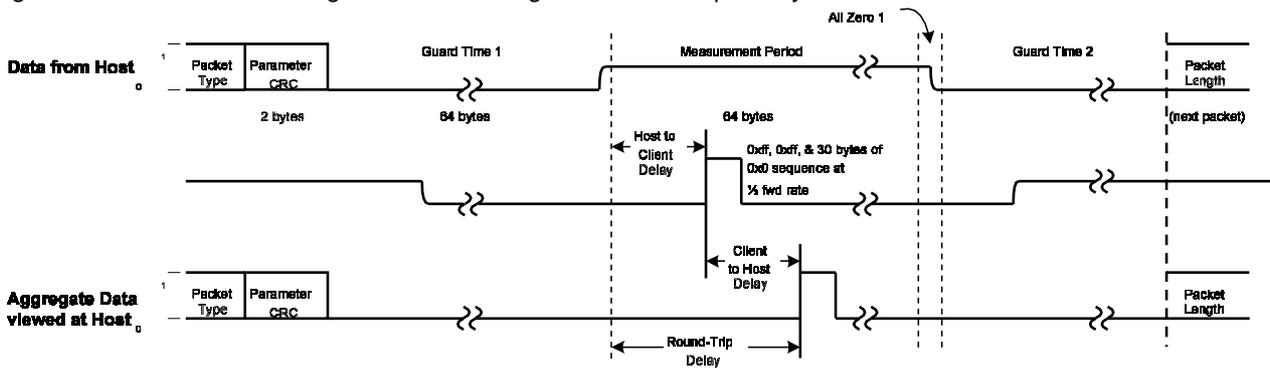


Fig. 5.4.2 Round-Trip Delay Measurement Timing

Client Capability Packet

It is recommended that the client send a Client Capability Packet to the host after forward link synchronization is acquired, and it is required when requested by the host via the Reverse Link Flags in the Reverse Link Encapsulation Packet.

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Client Capability Packet

Packet Length	Packet Type=66	cClient ID	Protocol Version	Min Protocol Version	Pre-calibration Data Rate Capability	Interface Type Capability
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	1 bytes
Number of Alt Displays	Post-calibration Data Rate Capability	Bitmap Width	Bitmap Height	Display Window Width	Display Window Height	Color Map Size
1 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	4 bytes
Color Map RGB Width	RGB Capability	Monochrome Capability	Reserved 1	Y Cb Cr Capability	Bayer Capability	Reserved 2
2 bytes	2 bytes	1 bytes	1 bytes	2 bytes	2 bytes	2 bytes
Client Feature Capability	Max Video Frame Rate	Min Video Frame Rate	Min Sub-frame rate	Audio Buffer Depth	Audio Channel Capability	Audio Sample Rate Capability
4 bytes	1 bytes	1 bytes	2 bytes	2 bytes	2 bytes	2 bytes
Audio Sample Resolution	Mic Sample Resolution	Mic Sample Rate Capability	Keyboard Data Format	Pointing Device Data Format	Content Protection Type	Mfr Name
1 bytes	1 bytes	2 bytes	1 bytes	1 bytes	2 bytes	2 bytes
Product Code	Reserved 3	Serial Number	Week of Mfr	Year of Mfr	CRC	
2 bytes	2 bytes	4 bytes	1 bytes	1 bytes	2 bytes	

Packet Contents:

Packet Length: packet length not including the packet length field
 Packet Type: packet type is 0042h
 cClient ID: set to zero
 Protocol Version: set to 0002h
 Min Protocol Version: specify the minimum protocol version (0001h)
 Pre-Calibration Data Rate Capability: specify the maximum data rate the client can receive (190h)
 Interface Type Capability: set to zero
 Number of Alt Displays: set to zero
 Post-Calibration Data Rate Capability: specify the maximum data rate the client can receive (190h)
 Bitmap Width: specify the width of the bitmap
 Bitmap Height: specify the height of the bitmap
 Display Window Width: specify the width of the display window
 Display Window Height: specify the height of the display window
 Color Map Size: set to zero
 Color Map RGB Width: set to zero
 RGB Capability: specify the resolution of RGB format (8888h)
 Monochrome Capability: set to zero
 Reserved 1: set to zero
 Y Cb Cr Capability: set to zero
 Bayer Capability: set to zero
 Reserved 2: set to zero
 Client Feature Capability Indicators: 00CC8000h
 Maximum Video Frame Rate Capability: specify the maximum video frame (3Ch)
 Minimum Video Frame Rate Capability: specify the minimum video frame (00h)
 Minimum Sub-frame Rate: specify the minimum sub-frame rate (01h)
 Audio Buffer Depth: set to zero
 Audio Channel Capability: set to zero
 Audio Sample Rate Capability: Set to zero
 Audio Sample Resolution: set to zero
 Mic Audio Sample Resolution: set to zero
 Mic Sample Rate Capability: set to zero
 Keyboard Data Format: set to zero
 Pointing Device Data Format: set to zero
 Content Protection Type: set to zero
 Mfr Name: set to B9F6h
 Product Code: set to 5410h
 Reserved 3: set to zero
 Serial Number: set to zero
 Week of Manufacture: set to zero
 Year of Manufacture: 0Ah
 CRC: error check

Client Request and Status Packet

The host needs a small amount of information from the client so it can configure the host-to-client link in an optimum manner. The Client Request and Status Packet is required to report errors and status to the host.

Client Request and Status Packet							
Packet Length	Packet Type=70	cClient ID	Reverse Link Request	CRC Error Count	Client Status	Client Busy Flags	CRC
2 bytes	2 bytes	2 bytes	2 bytes	1 bytes	1 bytes	2 bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 70

cClient ID: set to zero

Reverse Link Request: specify the number of bytes the client needs in the reverse link in the next sub-frame to send information to the host.

CRC Error Count: count the number of CRC errors occurred

Client Status:

- Bit 0 – 1: capability has changed
0: capability has not changed
- Bit 1 – indicates the client has detected an error
- Bit [7:2] – set to zero

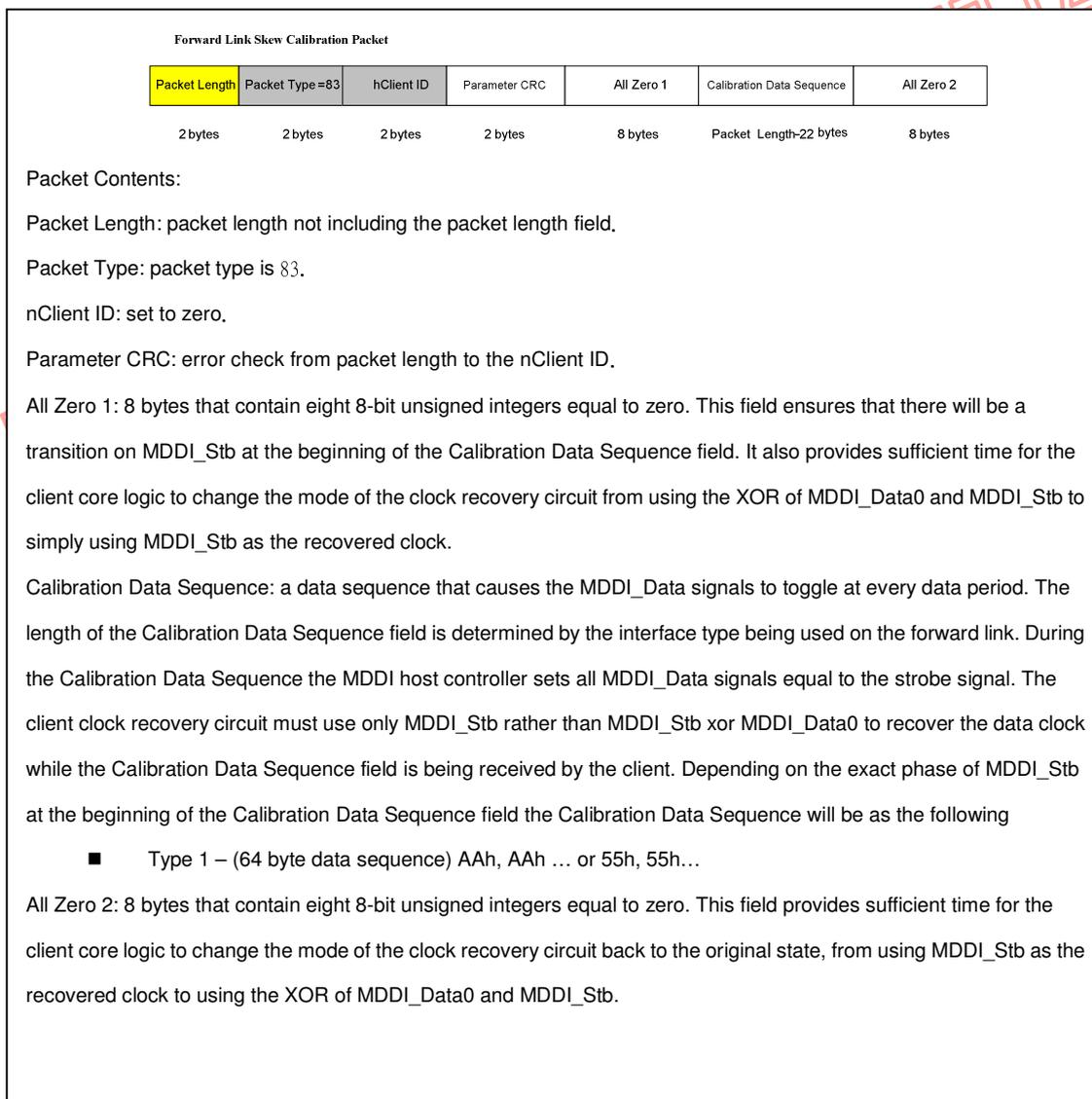
Client Busy Flags:

- Bit 0 – bitmap block transfer function is busy
- Bit 1 – bitmap area fill function is busy
- Bit 2 – bitmap pattern fill function is busy
- Bit 3 – the graphics subsystem is busy
- Bit [15:4] – set to zero

CRC: error check

Forward Link Skew Calibration Packet

This packet allows the client to calibrate itself for differences in the propagation delay of the MDDI_Data signals with respect to the MDDI_Stb signal. Without delay skew compensation the maximum data rate must be limited to account for the worst-case variation in these delays. It is recommended that this packet only be sent when the forward link data rate is configured to 50 Mbps or lower. After sending this packet to calibrate the client the data rate may be stepped up above 50 Mbps. With the data rate set too high during the skew calibration process the client might synchronize to an alias of the bit period which would cause the delay skew compensation setting to be off by more than one bit time, resulting in erroneous data clocking. The greatest possible Interface Type must be selected prior to sending the Forward Link Skew Calibration Packet so that all existing data bits are calibrated.



Register Access Packet

Register Access Packet is utilized when setting instruction to the NT35410. This packet cannot be used for RAM access.

Register Access Packet							
Packet Length	Packet Type =146	bClient ID	Read/Write Info	Register Address	Parameter CRC	Register Data List	Register Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	(Packet Length - 14) bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 146

bClient ID: set to zero

Read/Write Info:

Bits [15:14]	Read/Write Flags
00	Write
01	Reserved
10	Read
11	Response to read

Bit [13:0] – specifies the number of 32-bit register data list items to be transferred in the Register Data List Filed.

Register Address: upper bits shall set to zero

Parameter CRC: error check from packet length to the register address

Register Data List: written (or read) registers to (from) client

Register Data CRC: error check of the register data list

Video Stream Packet

The NT35410 supports the Video Stream Packet to transfer display data including RGB data to RAM.

Video Stream Packet							
Packet Length	Packet Type=16	bClient ID	Video Data Format Descriptor	Pixel Data Attributes	X Left Edge	Y Top Edge	
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	
X Right Edge	Y Bottom Edge	X Start	Y Start	Pixel Count	Parameter CRC	Pixel Data	Pixel Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	(Packet_Length - 26) bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field
 Packet Type: packet type is 16
 bClient ID: set to zero
 Video Data Format Descriptor

[15:12]	[11:8]	[7:4]	[3:0]	Transfer pixel format
0101	0x8	0x8	0x8	Packed 24 bits pixel RGB format (R:G:B=8:8:8)
0101	0x6	0x6	0x6	Packed 18 bits pixel RGB format (R:G:B=6:6:6)
0101	0x5	0x6	0x5	Packed 16 bits pixel RGB format (R:G:B=5:6:5)
Others setting disabled				

Pixel Data Attributes: The pixel data is written to RAM buffer of NT35410 (00C3h)
 X Left Edge: Specify the X coordinate of the left edge of the screen window filled by the Pixel Data field.
 Y Top Edge: Specify the Y coordinate of the top edge of the screen window filled by the Pixel Data field
 X Right Edge: Specify the X coordinate of the right edge of the window being updated.
 Y Bottom Edge: Specify the Y coordinate of the bottom edge of the window being updated.
 X Start: Specify X start address for the first pixel in the Pixel Data field below.
 Y Start: Specify Y start address for the first pixel in the Pixel Data field below.
 Pixel Count: specify the number of pixels
 Parameter CRC: error check from packet length to the pixel count
 Pixel Data: the raw video data

Table 5.4.1 Pixel Data Format

MDDI data byte	D7	D6	D5	D4	D3	D2	D1	D0	Color	
RGB 5:6:5	Byte n	G2	G1	G0	B4	B3	B2	B1	B0	65K-Color (1 pixel/ 16 bits RGB format)
	Byte n+1	R4	R3	R2	R1	R0	G5	G4	G3	
RGB 6:6:6	Byte n	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color (1 pixel/ 18 bits RGB format)
	Byte n+1	R3	R2	R1	R0	G5	G4	G3	G2	
	Byte n+2	B5	B4	B3	B2	B1	B0	R5	R4	
RGB 8:8:8	Byte n	B7	B6	B5	B4	B3	B2	B1	B0	16.7M-Color (1 pixel/ 24 bits RGB format)
	Byte n+1	G7	G6	G5	G4	G3	G2	G1	G0	
	Byte n+2	R7	R6	R5	R4	R3	R2	R1	R0	

Flexible Video Stream Packet

The NT35410 supports the Flexible Video Stream Packet to transfer display data including RGB data to RAM. This allows for a reduction in the number of fields sent in an environment where one or more fields are not changing values.

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Flexible Video Stream Packet

Packet Length	Packet Type=20	bClient ID	Field Present Flags	Video Data Format Description	Pixel Data Attributes	X Left Edge	Y Top Edge
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes

X Right Edge	Y Bottom Edge	X Start	Y Start	Pixel Count	Parameter CRC	Pixel Data	Pixel Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	Packet Length - present header bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is **20**

bClient ID: set to zero

Field Present Flags: indicates the field in the packet is present (value "1") or not present (value "0").

- Bit 0: indicates the presence of the Video Data Format Description Field.
- Bit 1: indicates the presence of the Pixel Data Attributes Field.
- Bit 2: indicates the presence of the X Left Edge Field.
- Bit 3: indicates the presence of the Y Top Edge Field.
- Bit 4: indicates the presence of the X Right Edge Field.
- Bit 5: indicates the presence of the Y Bottom Edge Field.
- Bit 6: indicates the presence of the X Start Field.
- Bit 7: indicates the presence of the Y Start Field.
- Bit 8: indicates the presence of the Pixel Count Field.
- Bits [15:9] are all "0".

Video Data Format Descriptor

[15:12]	[11:8]	[7:4]	[3:0]	Transfer pixel format
0101	0x8	0x8	0x8	Packed 24 bits pixel RGB format (R:G:B=8:8:8)
0101	0x6	0x6	0x6	Packed 18 bits pixel RGB format (R:G:B=6:6:6)
0101	0x5	0x6	0x5	Packed 16 bits pixel RGB format (R:G:B=5:6:5)
Others setting disabled				

X Left Edge: Specify the X coordinate of the left edge of the screen window filled by the Pixel Data field.

Y Top Edge: Specify the Y coordinate of the top edge of the screen window filled by the Pixel Data field

X Right Edge: Specify the X coordinate of the right edge of the window being updated.

Y Bottom Edge: Specify the Y coordinate of the bottom edge of the window being updated.

X Start: Specify X start address for the first pixel in the Pixel Data field below.

Y Start: Specify Y start address for the first pixel in the Pixel Data field below.

Pixel Data Attributes: The pixel data is written to RAM buffer of NT35410 (00C3h)

Pixel Count: specify the number of pixels

Parameter CRC: error check from packet length to the pixel count

Pixel Data: the raw video data

Pixel Data CRC: error check of the pixel data

Windowless Video Stream Packet

The NT35410 supports the Windowless Video Stream Packet to transfer display data including RGB data to RAM. This packet type assumes that full screen updates are always occurring and therefore there is no need for the window information.

Windowless Video Stream Packet										
Packet Length	Packet Type=22	bClient ID	Video Data Format Description	Pixel Data Attributes	Pixel Count	Parameter CRC				
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes				
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th style="padding: 5px;">Pixel Data</th> <th style="padding: 5px;">Pixel Data CRC</th> </tr> <tr> <td style="text-align: center; padding: 5px;">Packet Length - 14 bytes</td> <td style="text-align: center; padding: 5px;">2 bytes</td> </tr> </table>		Pixel Data	Pixel Data CRC	Packet Length - 14 bytes	2 bytes					
Pixel Data	Pixel Data CRC									
Packet Length - 14 bytes	2 bytes									

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 22

bClient ID: set to zero

Video Data Format Descriptor

[15:12]	[11:8]	[7:4]	[3:0]	Transfer pixel format
0101	0x8	0x8	0x8	Packed 24 bits pixel RGB format (R:G:B=8:8:8)
0101	0x6	0x6	0x6	Packed 18 bits pixel RGB format (R:G:B=6:6:6)
0101	0x5	0x6	0x5	Packed 16 bits pixel RGB format (R:G:B=5:6:5)
Others setting disabled				

Pixel Data Attributes: The pixel data is written to RAM buffer of NT35410(00C3h)

Pixel Count: specify the number of pixels

Parameter CRC: error check from packet length to the pixel count

Pixel Data: the raw video data

Pixel Data CRC: error check of the pixel data

5.4.3 Writing Video Data to Memory Sequence

In order to write video data to memory, the following sequence should be programmed. This packet should be followed by video stream packets.

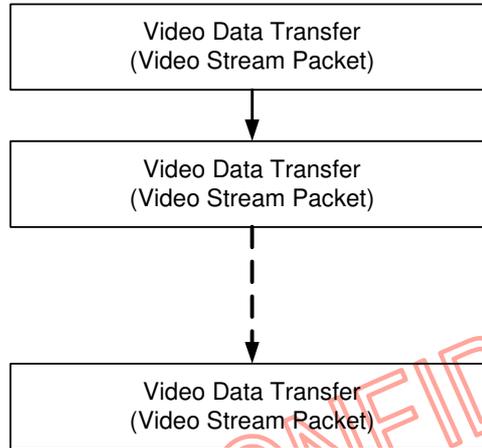


Fig. 5.4.3 Writing Video Data to Memory Sequence

5.4.4 Writing Register Sequence

In order to write registers, register access packet should be used. Register access packet is used to write data to register.

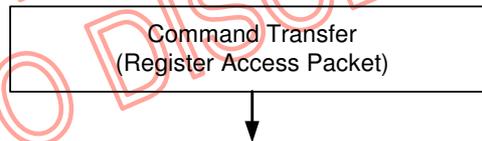


Fig. 5.4.4 Writing Register Sequence

5.4.5 Reading Video Data from Memory Sequence

In order to read a pixel data from memory (readable one pixel only), the following sequence should be programmed. Memory read command (2E00h) is followed by reverse encapsulation packet. DDI transmits video pixel data through encapsulation packet. Please refer to VESA spec for detailed description.

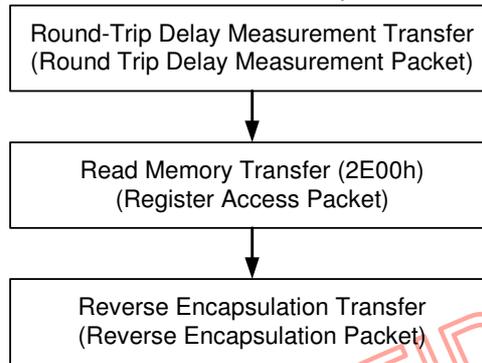


Fig. 5.4.5 Reading Video Data from Memory Sequence

Notes:

1. X addresses for memory data read is set by 2A00h and 2A01h (XS[15:0]).
The parameters of 2A00h and 2A01h are stored on relative registers while command 2A00h~2A03h are executed completely. See also section "6.1 Instruction Code" and Note 2.
2. Y addresses for memory data read is set by 2B00h and 2B01h (YS[15:0]).
The parameters of 2B00h and 2B01h are stored on relative registers while command 2B00h~2B03h are executed completely. See also section "6.1 Instruction Code" and Note 2.

5.4.6 Reading Register Sequence

In order to read registers, the following sequence should be programmed. Next, register read command is followed by reverse encapsulation packet. DDI transmits register data through encapsulation packet. Please refer to VESA spec for detailed description.

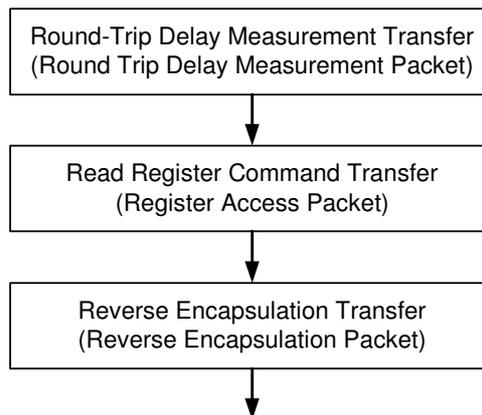


Fig. 5.4.6 Reading Register Sequence

5.4.7 Hibernation Setting

The Client MDDI of the NT35410 provides a hibernation setting. The methods for waking up the hibernation mode can be determined based on actual usage.

Wake-up	Condition
Host-Initiated Wake-up	Wake up the MDDI link by MDDI Host

Note: In the Hibernation state, the data is retained in RAM and the display operation is maintained. Hibernation setting and wake-up sequence must in accordance with VESA-MDDI specifications.

Hibernation setting sequence

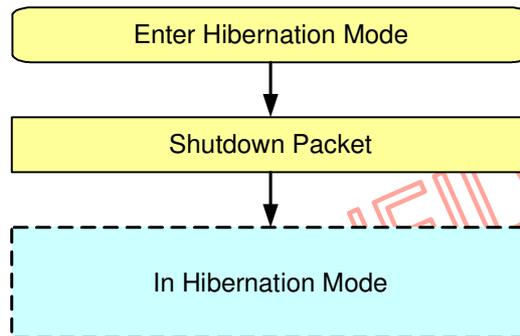


Fig. 5.4.7 Enter Hibernation Mode Sequence

Hibernation Wake-up sequence

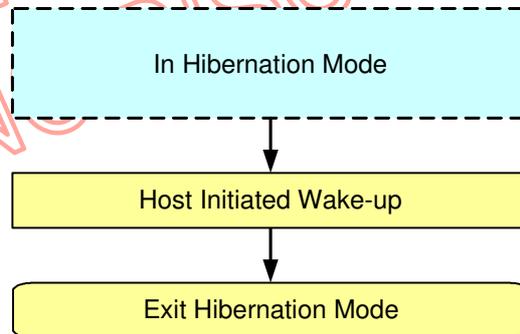


Fig. 5.4.8 Hibernation Wake-up Sequence

5.5 INTERFACE PAUSE

It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then NT35410 will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command as been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

This applies to the following 4 conditions:

- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter

Parallel Interface Pause

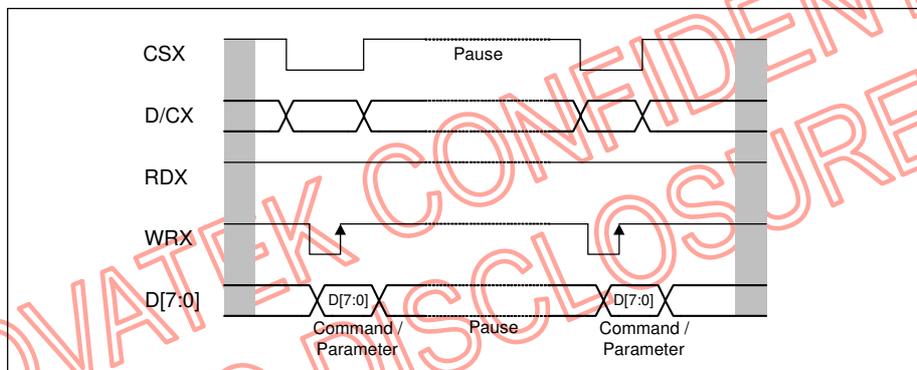


Fig. 5.4.1 Parallel bus protocol, write mode – paused by CSX

Serial Interface Pause

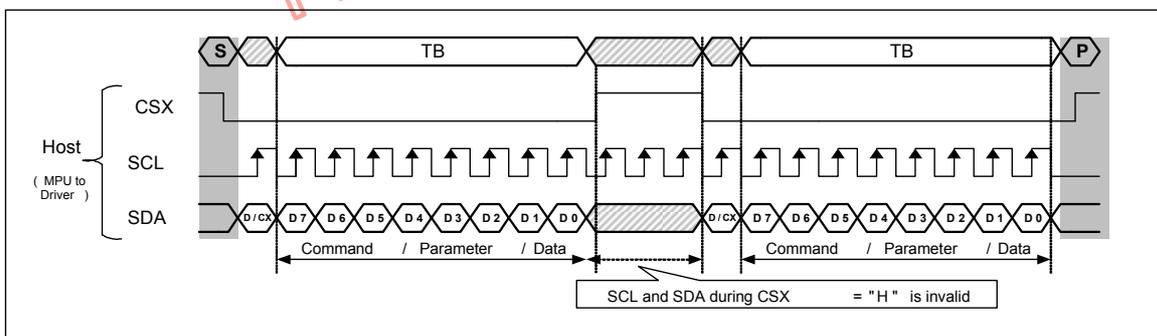


Fig. 5.4.2 Serial bus protocol, write mode – paused by CSX (3-Pin serial case)

MIPI Interface Pause

Pause can be done on DSI between Packets when they are sent to same or different receiver (Virtual Channel (VC)) e.g.

- 1) Same receiver: Packet 1 (VC=00) → Packet 2 (VC=00) → Packet 3 (VC=00) → ...
- 2) Different receiver: Packet 1 (VC=00) → Packet 2 (VC=00) → Packet 3 (VC=00) → ...

The means that "→" symbol means a pause on DSI.

5.6 DATA TRANSFER RECOVERY

If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then NT35410 will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been High state. See the following example (See **Fig. 5.6.1**)

If there is a break in data transmission by CSX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then NT35410 will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example (See **Fig. 5.6.2**)

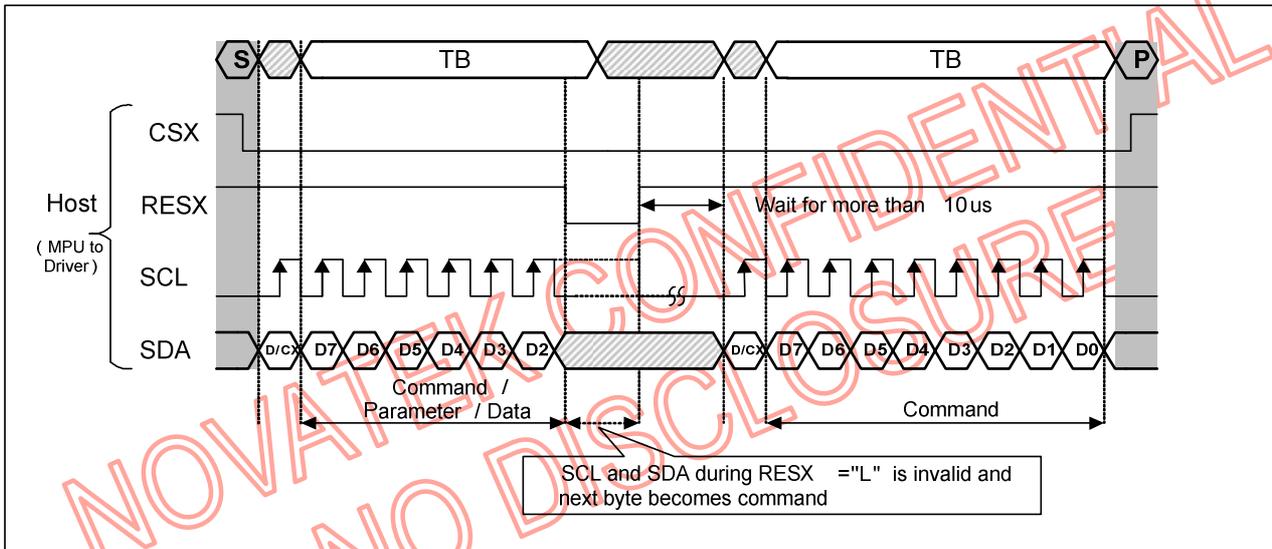


Fig. 5.6.1 Serial bus protocol, write mode – interrupted by RESX

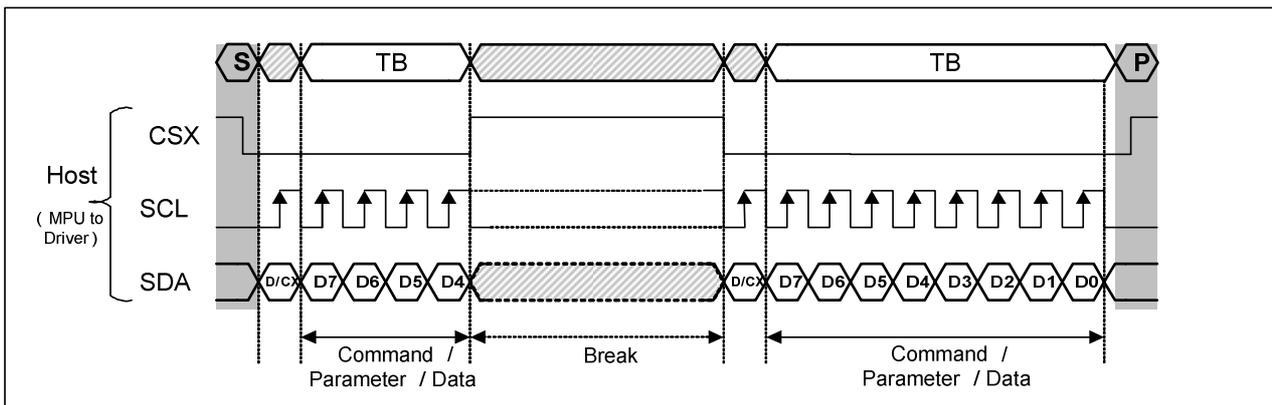


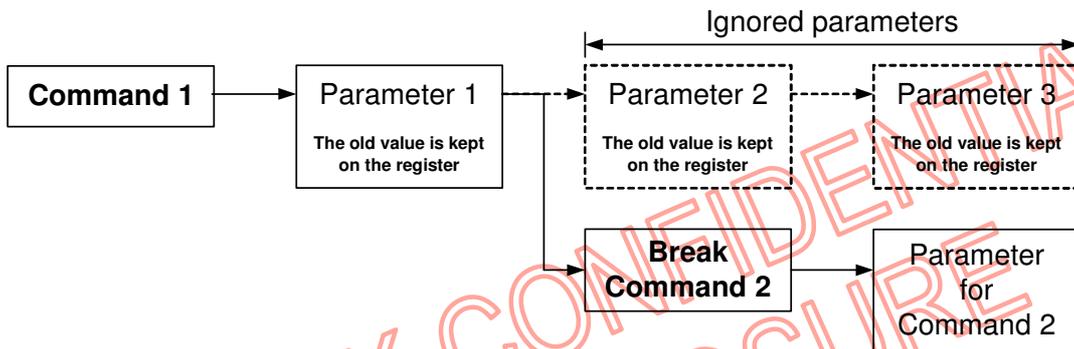
Fig. 5.6.2 Serial bus protocol, write mode – interrupted by CSX

Regarding the data transfer break mechanism, there are some different between different interface. When NT35410 work in MIPI interface, it illustrated for reference purposes below.

Without break



With break (See and check also exceptions*)



Break can be e.g. another command or noise pulse.

Fig. 5.6.3 Break during Parameter

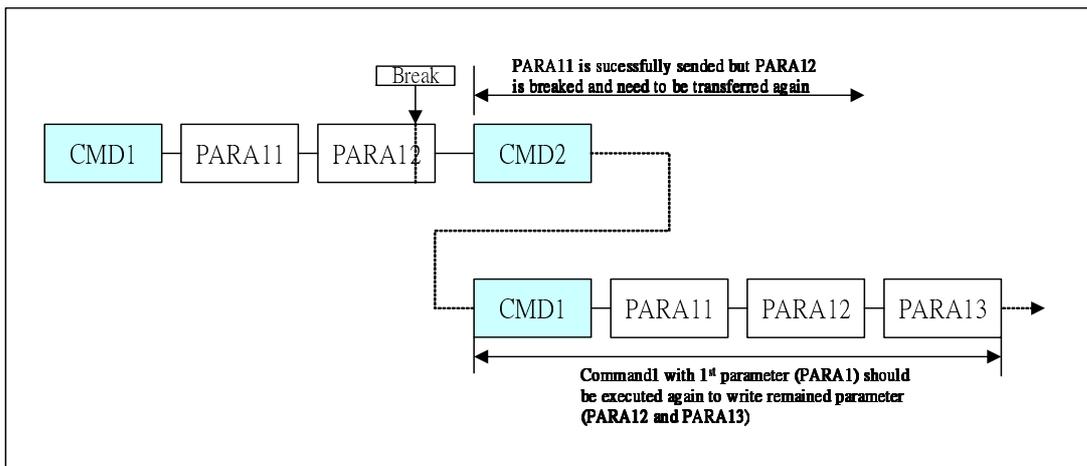
*) See also an exception on section “6.1 Instruction Code” and Note 2.

The MCU can create a break condition when it is forcing DSI data lanes in the LP-11 mode

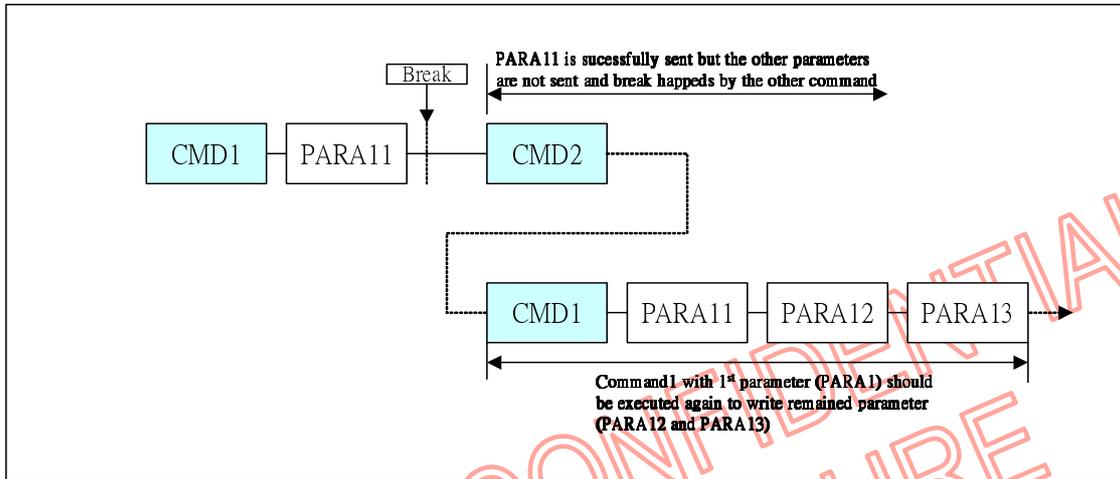
The NT35410 stops to control DSI data lanes (change from a transmitter mode to a received mode) if it was controlling DSI data lanes as a transmitter when the MCU is forcing DSI data lanes in the LP-11.

The break condition can be done any time when the MCU or the driver IC is controlling DSI data lanes e.g. the driver IC is sending data to the MCU.

Except MIPI interface, the data transfer break mechanism illustrated for reference purposes below.



If a 2 or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.



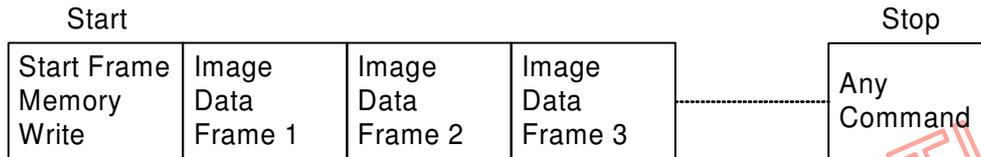
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5.7 DISPLAY MODULE DATA TRANSFER MODES

The NT35410 has one color mode for transferring data to the frame Memory and it is 24-bit color per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

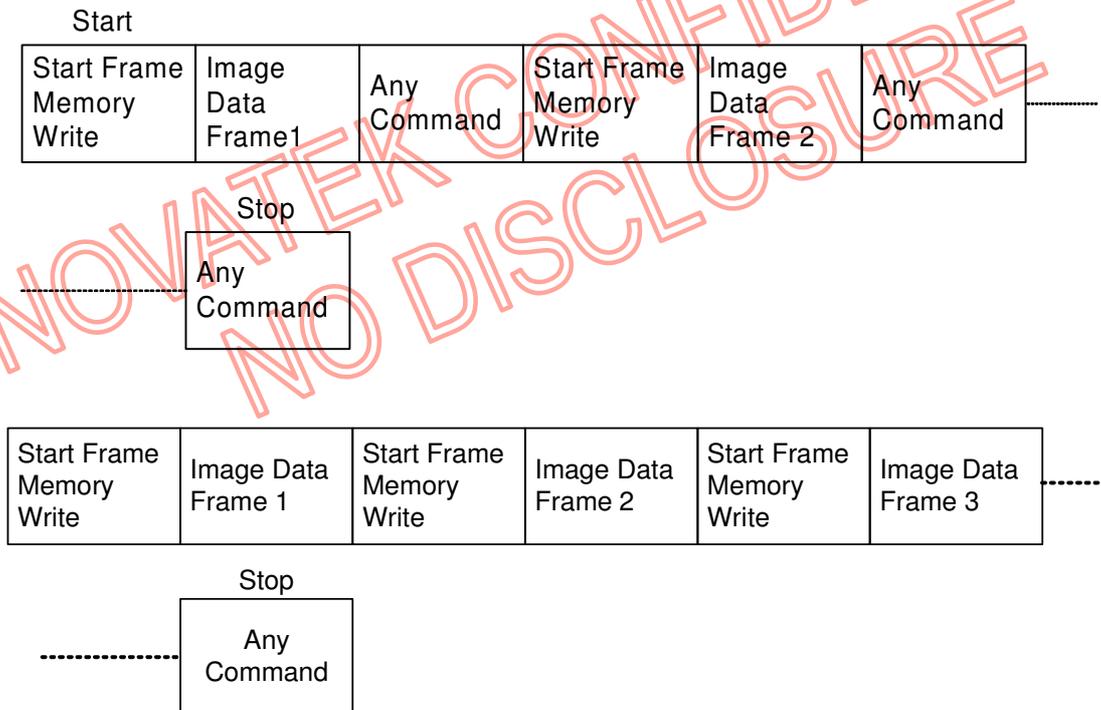
Method 1

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.



Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.



NOTES:

- 1) The Frame Memory can contain odd and even number of pixels for both Methods. Only complete pixel data will be stored in the Frame Memory.
- 2) "Memory Write Continue (2Ch)" or "Memory Read Continue (2Eh)" commands are not stopping writing or reading to/from the frame memory. These commands can be used if there is wanted to continue the writing or reading to/from the frame memory when "Any Command" has stopped the memory writing or reading.
- 3) "Any Command" can be as same as "Start Frame Memory Write".

5.8 RGB INTERFACE

5.8.1 General Description

For direct interface with both graphic controller and MPU, NT35410 offer RGB interface mode to display video signal. The parallel RGB interface includes: VS, HS, DE, PCLK, D[23:0]. The interface is activated after Power On sequence (See section Power On/Off Sequence)

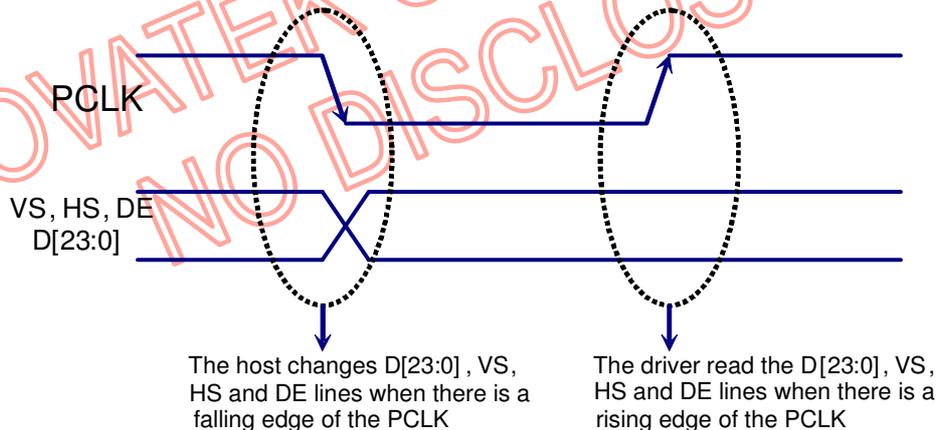
Pixel clock (PCLK) is running all the time without stopping and it is used to entering VS, HS, DE and D[23:0] states when there is a rising edge of the PCLK. The PCLK cannot be used as continues internal clock for other functions of the display module e.g. Sleep In –mode etc.

Vertical synchronization (VS) is used to tell when there is received a new frame of the display. This is negative ("0", low) active and its state is read to the display module by a rising edge of the PCLK signal.

Horizontal synchronization (HS) is used to tell when there is received a new line of the frame. This is negative ("0", low) active and its state is read to the display module by a rising edge of the PCLK signal.

Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a positive ("1", high) active and its state is read to the display module by a rising edge of the PCLK signal. D[23:0] (24-bit: R7-R0, G7-G0 and B7-B0; 18-bit: R5-R0, G5-G0 and B5-B0; 16-bit: R4-R0, G5-G0 and B4-B0) are used to tell what is the information of the image that is transferred on the display (When DE= "1" and there is a rising edge of PCLK). D[23:0] can be "0" (low) or "1" (high). These lines are read by a rising edge of the PCLK signal.

The PCLK cycle is described in the follow figure.



Note: PCLK is an unsynchronized signal (It can be stopped)

5.8.2 RGB Interface Timing Chart

The image information must be correct on the display, when the timings are in range on the interface. However, the image information can be incorrect on the display, when timings are not out of range on the interface (Out of the range timings cannot on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.) when there is returned from out of the range to in range interface timing.

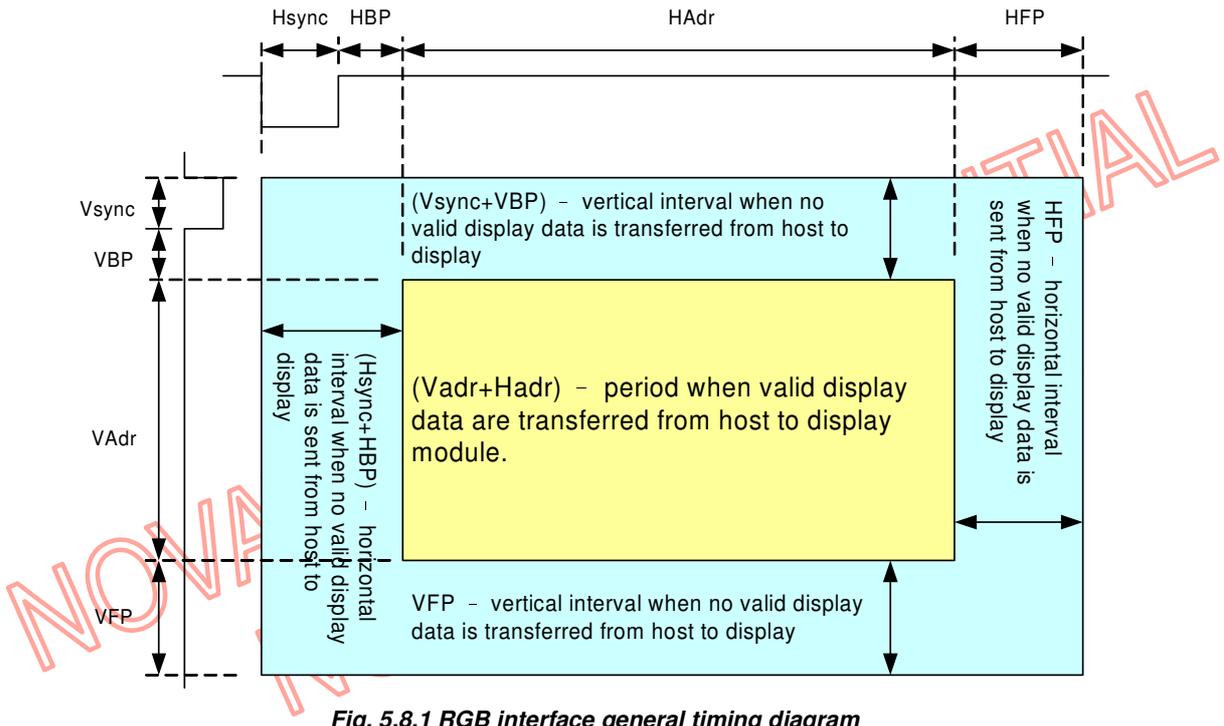


Fig. 5.8.1 RGB interface general timing diagram

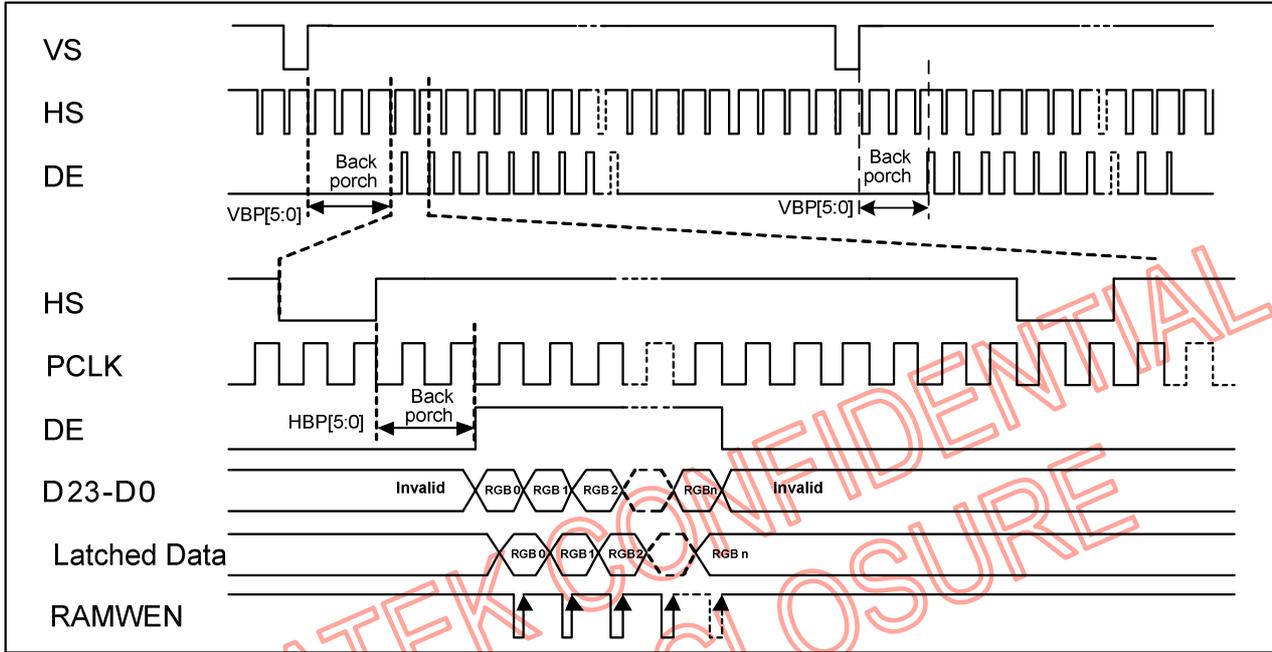


Fig. 5.8.2 Video signal data writing method in RGB Mode 1 Interface

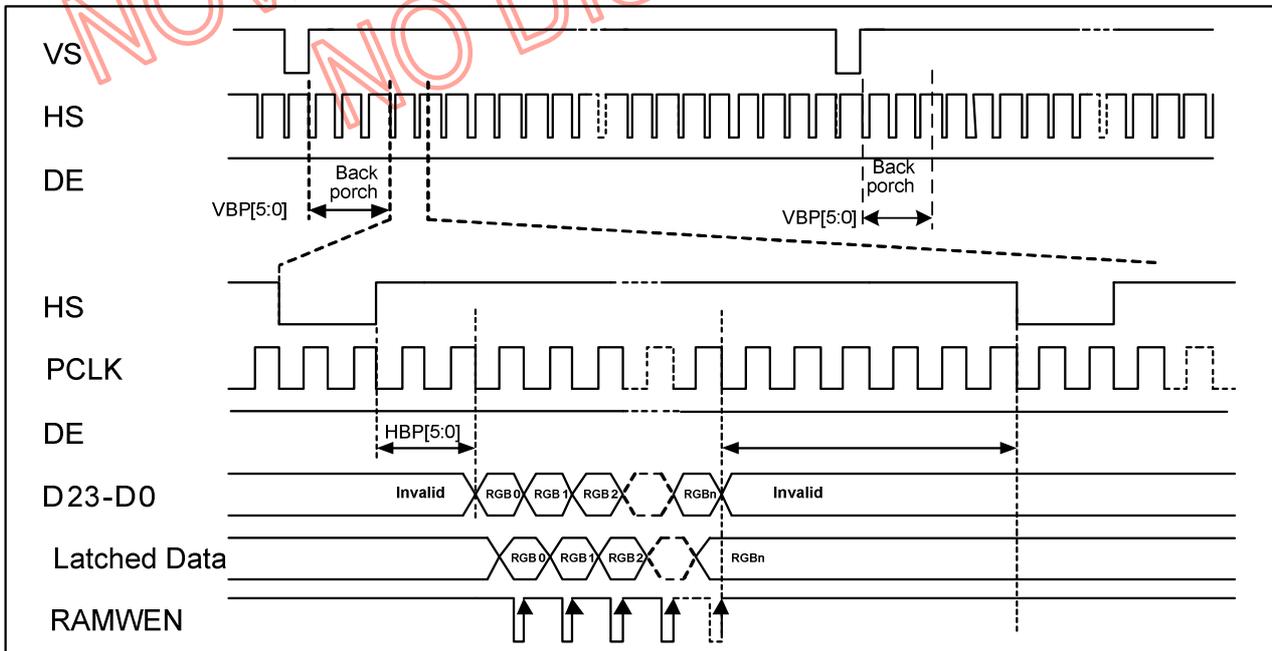


Fig. 5.8.3 Video signal data writing method in RGB Mode 2 Interface

5.8.3 RGB Interface Mode Set

RGB I/F Mode	PCLK	DE	D23-D0	VS	HS	Register VBP[5:0], HBP[5:0]
RGB Mode 1 (SYNC + DE)	Used	Used	Used	Used	Used	Not used
RGB Mode 2 (SYNC only)	Used	Not used	Used	Used	Used	Used

In RGB Mode 1, writing data to line buffer is done by PCLK and Video Data Bus (D23 to D0), when DE is high state. The external clocks (PCLK, VS and HS) are used for internal displaying clock. So, controller must always transfer PCLK, VS and HS signal to NT35410.

In RGB Mode 2, back porch of Vsync VBP is defined by VBP[5:0] of RGBBPCTR command. And back porch of Hsync HBP is defined by HBP[5:0] of RGBPCTR command.

5.8.3.1 INTERFACE TYPE SELECTION

The selection of a given interfaces are done by setting IM3, IM2, IM1 and IM0 pins as show in **Table 5.8.3.1**

Table 5.8.3.1 Interface Type Selection

IM3	IM2	IM1	IM0	Interface	Read back selection
0	0	0	0	8080 MCU 8-bit Parallel	RDX strobe (8-bit read data and 8-bit read parameter)
0	0	0	1	8080 MCU 9-bit Parallel	RDX strobe (9-bit read data and 8-bit read parameter)
0	0	1	0	8080 MCU 16-bit Parallel	RDX strobe (16-bit read data and 8-bit read parameter)
0	0	1	1	8080 MCU 18-bit Parallel	RDX strobe (18-bit read data and 8-bit read parameter)
0	1	0	0	8080 MCU 24-bit Parallel	RDX strobe (24-bit read data and 8-bit read parameter)
1	1	0	0	SPI 3-pins serial	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
1	1	0	1	SPI 4-pins serial	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
1	0	0	1	RGB mode 1/2	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
1	1	1	0	MIPI	Follow MIPI Read Back Sequence
1	1	1	1	MDDI	Follow MDDI Read Back Sequence

Table 5.8.3.2 Pin Connection according to the Interface Type

IM3	IM2	IM1	IM0	Interface	RDX	WRX	DCX	Read back selection
0	0	0	0	8080 MCU 8-bit Parallel	RDX	WRX	DCX	D[23:8]: Unused, D7-D0: 8-bit Data
0	0	0	1	8080 MCU 9-bit Parallel	RDX	WRX	DCX	D[23:9]: Unused, D8-D0: 9-bit Data
0	0	1	0	8080 MCU 16-bit Parallel	RDX	WRX	DCX	D[23:16]: Unused, D15-D0: 16-bit Data
0	0	1	1	8080 MCU 18-bit Parallel	RDX	WRX	DCX	D[23:18]: Unused, D17-D0: 18-bit Data
0	1	0	0	8080 MCU 24-bit Parallel	RDX	WRX	DCX	D[23:0] : 24-bit Data
1	1	0	0	SPI 3-pins serial	Note 1	SCL	Note 1	D[23:0]: Unused, SDI, SDO, WRX pad: SCL
1	1	0	1	SPI 4-pins serial	Note 1	SCL	Note1	D[23:0]: Unused, SDI, SDO, WRX pad: SCL
1	0	0	1	RGB mode 1/2	Note 1	SCL	Note1	- SDI, SDO, DCX pad: SCL RGB mode 1/2 is selected by command via SPI.
1	1	1	0	MIPI	Note 1	Note 1	Note 1	D[23:0]: Unused, CLK_P/CLK_N, D0_P, D0_N
1	1	1	1	MDDI	Note 1	Note 1	Note 1	D[23:0]: Unused, CLK_P/CLK_N, D0_P/D0_N

Note1: Unused pins connected to VDDI.

5.8.4 RGB Interface Bus Width Set

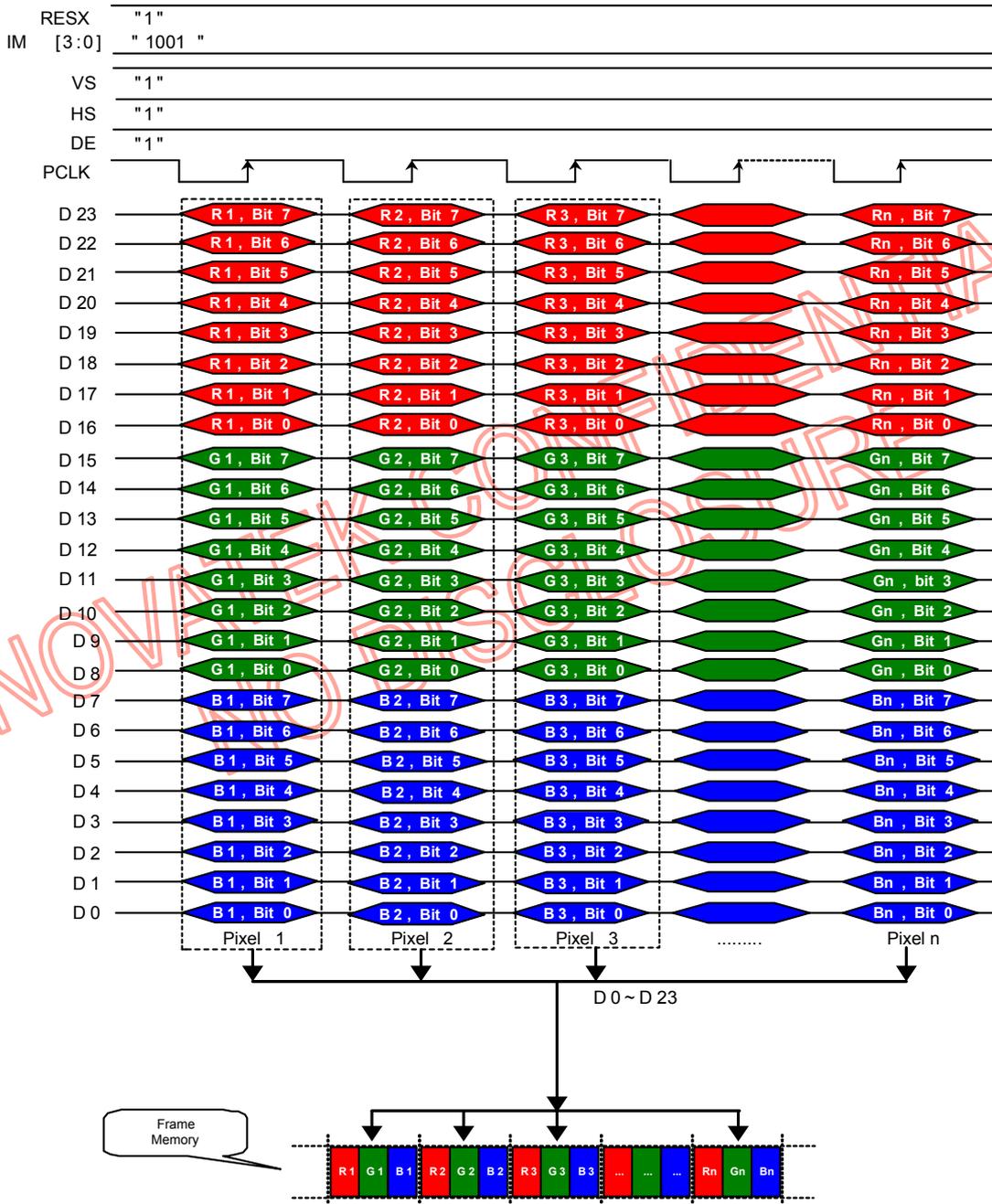
All 3-kinds of bus width can be available during RGB interface mode (selected by the COLMOD command (3Ah): VIPF[3:0]).

VIPF[3:0]	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus Width
0111	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	24-bit data
0110	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	18-bit data
0101	x	x	R4	R3	R2	R1	R0	x	x	x	G5	G4	G3	G2	G1	G0	x	x	B4	B3	B2	B1	B0	x	16-bit data
1001	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Reverse
101x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
110x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
111x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	

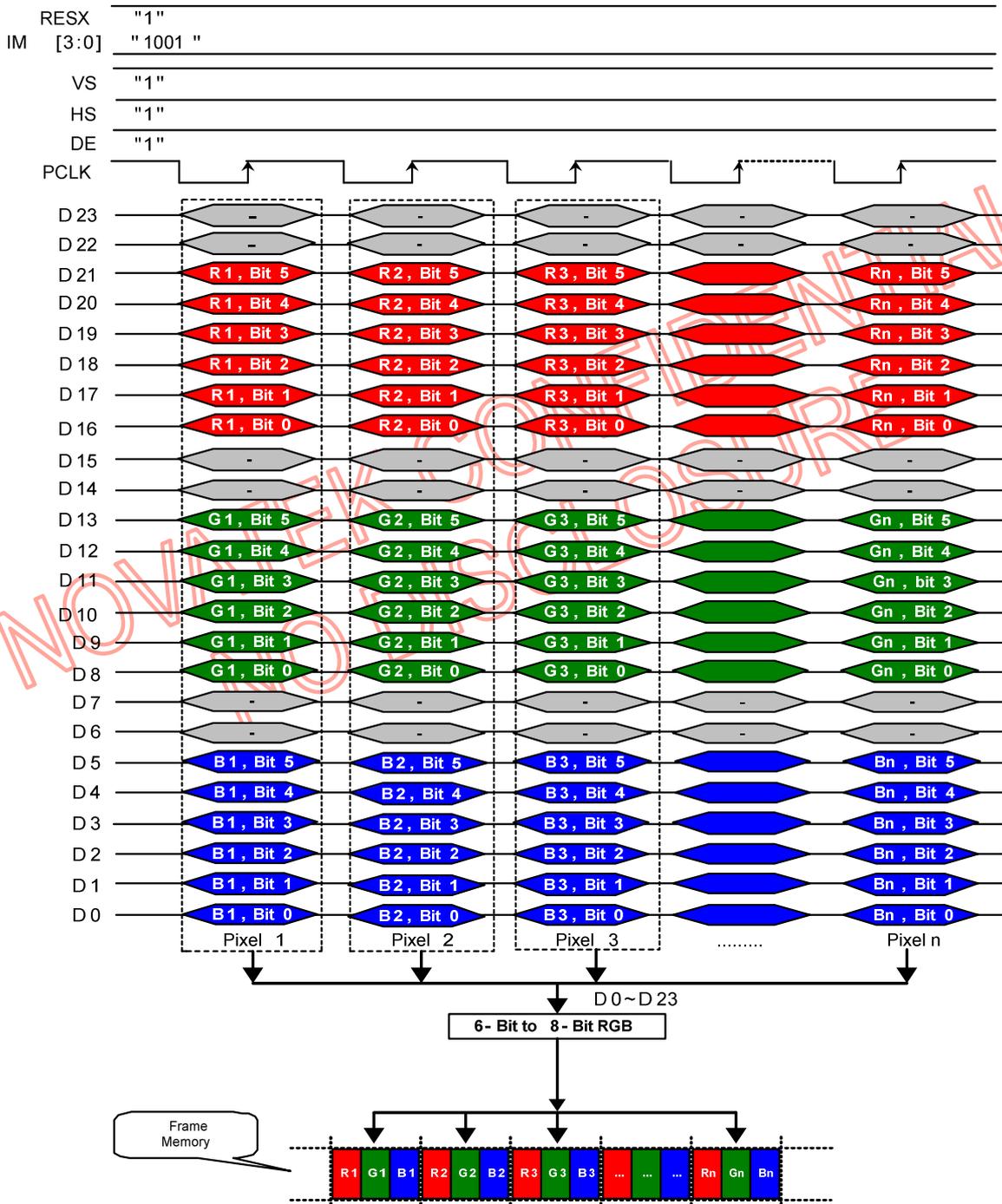
NOTE: Unused RGB data bus connected with VSS.

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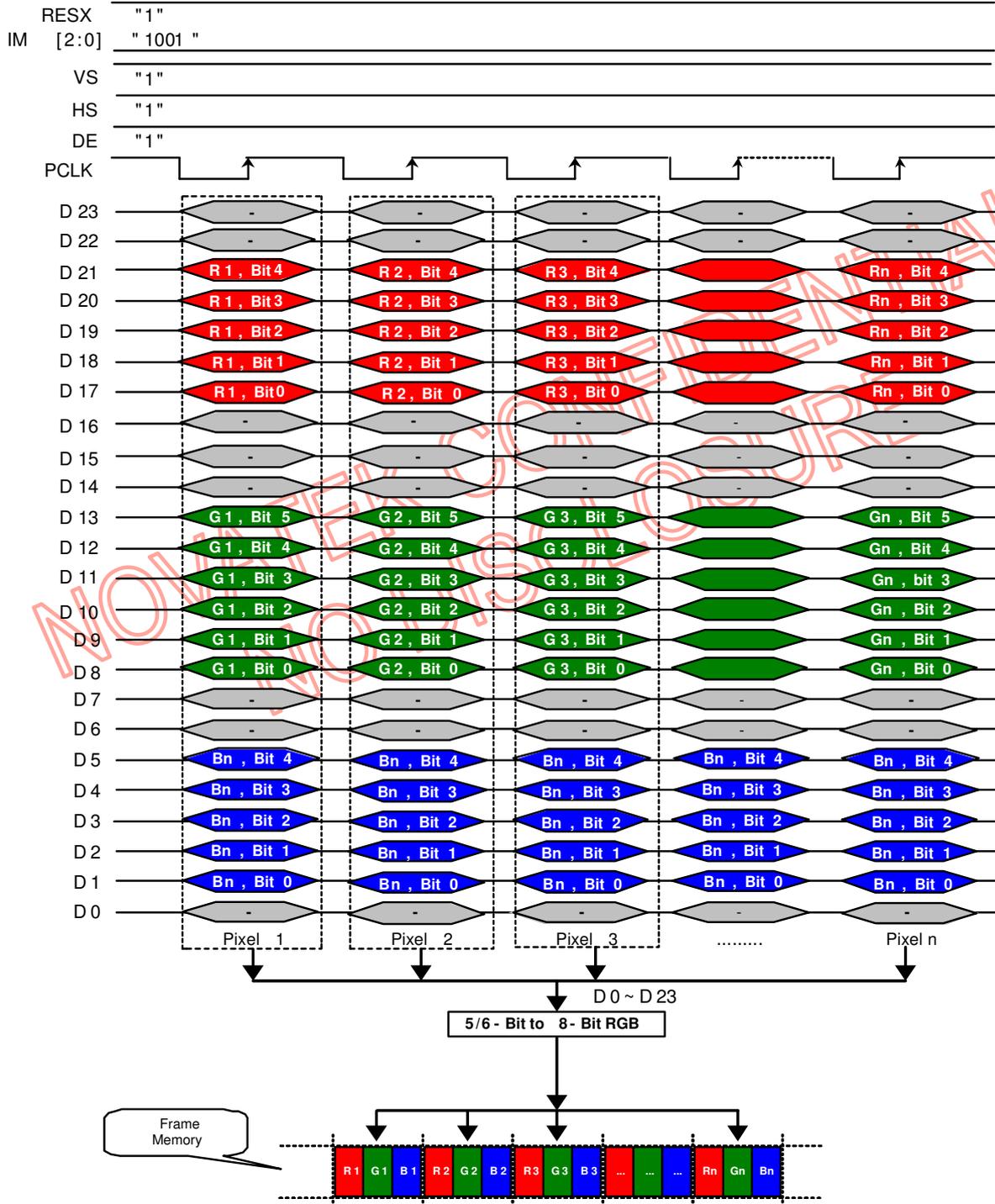
Write data for 24-bit RGB interface bus width set is shown below.



Write data for 18-bit RGB interface bus width set is shown below.



Write data for 16-bit RGB interface bus width set is shown below.



5.9 FRAME MRMORY

5.9.1 Address Counter

The address counter sets the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 8-8-8-bit), according to the data formats. As soon as this pixel-data information is complete the "Write access" is activated on the RAM. The address pointers address the locations of RAM.

When DISP[1:0]="00", the address ranges are X=0 to X=359 (167h) and Y=0 to Y=639 (27Fh).

When DISP[1:0]="01", the address ranges are X=0 to X=359 (167h) and Y=0 to Y=479 (1DFh).

When DISP[1:0]="10", the address ranges are X=0 to X=319 (13Fh) and Y=0 to Y=479 (1DFh).

Addresses outside these ranges are not allowed. Before writing to the RAM a window must be defined. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example, the whole display contents will be written when DISP[1:0]="00", if the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=539 (167h), YE=639 (27Fh).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET" and "MADCTL" (see section 6 command list), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. **Section 5.9.3** show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data must be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as below:

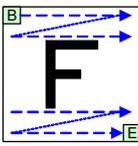
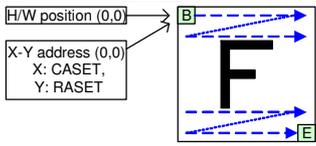
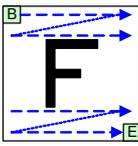
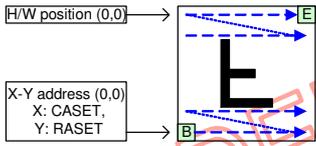
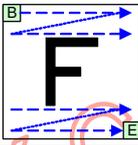
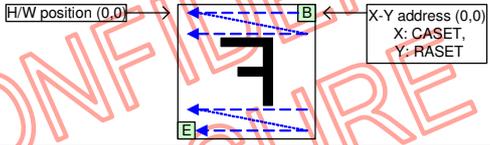
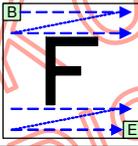
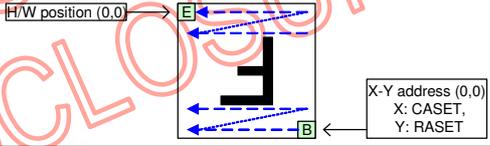
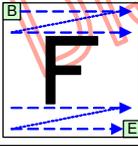
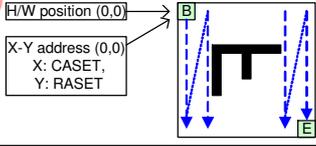
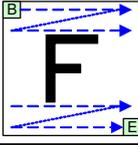
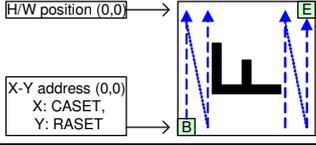
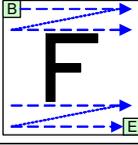
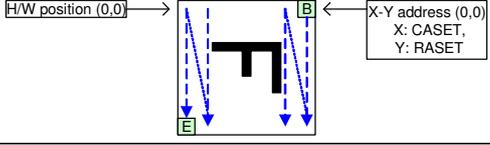
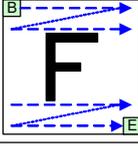
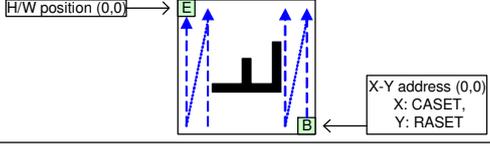
Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column (XS)"	Return to "Start Row (YS)"
Complete Pixel Pair Read / Write action	Twice Increment by 1 (First Pixel n then Pixel n+1)	No change
The Column counter value is larger than "End Column (XE)"	Return to "Start Column (XS)"	Increment by 1
The Column counter value is larger than "End Column (XE)" and the Row counter value is larger than "End Row (YE)"	Return to "Start Column (XS)"	Return to "Start Row (YS)"

NOTE:

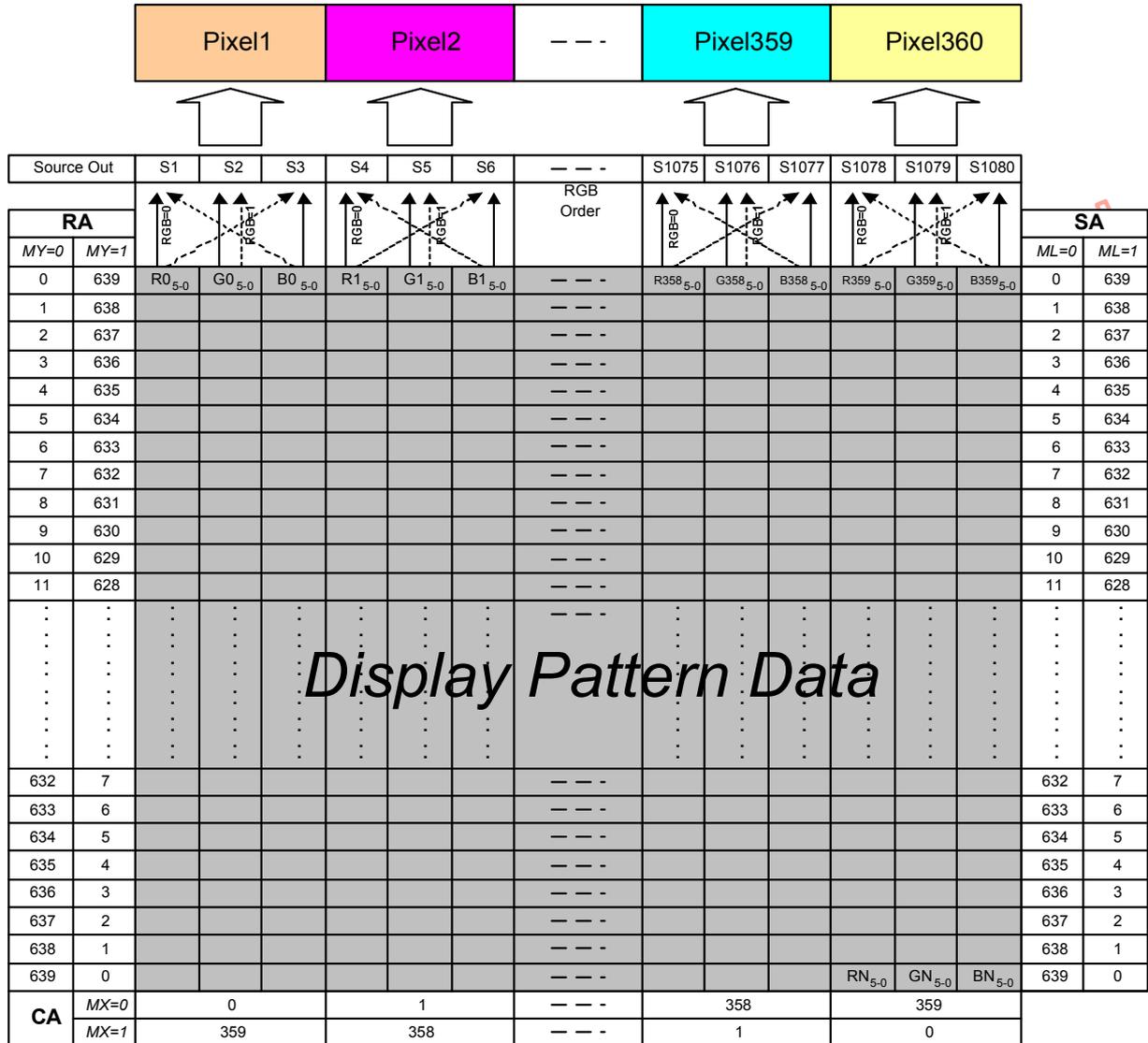
Data is always written to the Frame Memory in the order, regardless of the Memory Write Direction set by command MADCTL (36h) bit MY, MX and MV. The write order for each pixel unit is (R, G, B) transferred from (D2, D1, D0) = (R, G, B). One pixel unit represents 1 column and 1 page counter value on the Frame Memory

5.9.3 Interface to Memory Write Direction

The resultant image for each orientation setting is illustrated below.

Display Data Direction	MADCTR Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

NOTE: MV=D5 parameter of MADCTL command, MX=D6 parameter of MADCTL command, MY=D7 parameter of MADCTL command

5.9.4 Frame Memory to Display Address Mapping
5.9.4.1 USING 360RGB X 640 RESOLUTION (SMX=SMY=SRGB='0')

NOTE:

RA = Row Address,

CA = Column Address,

SA = Scan Address,

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

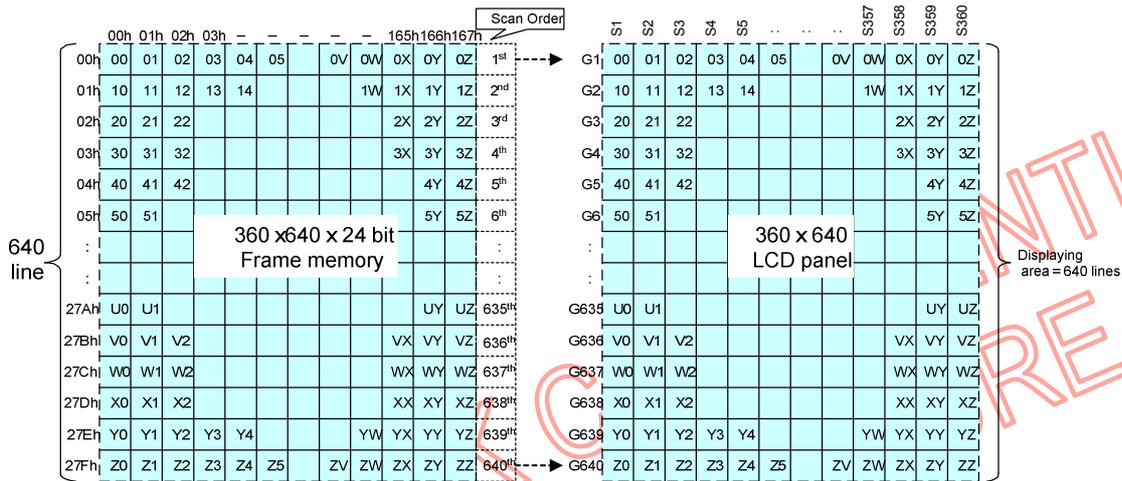
RGB= Red, Green and Blue pixel position change, D3 parameter of MADCTL command

5.9.5 Normal Display On or Partial Mode On

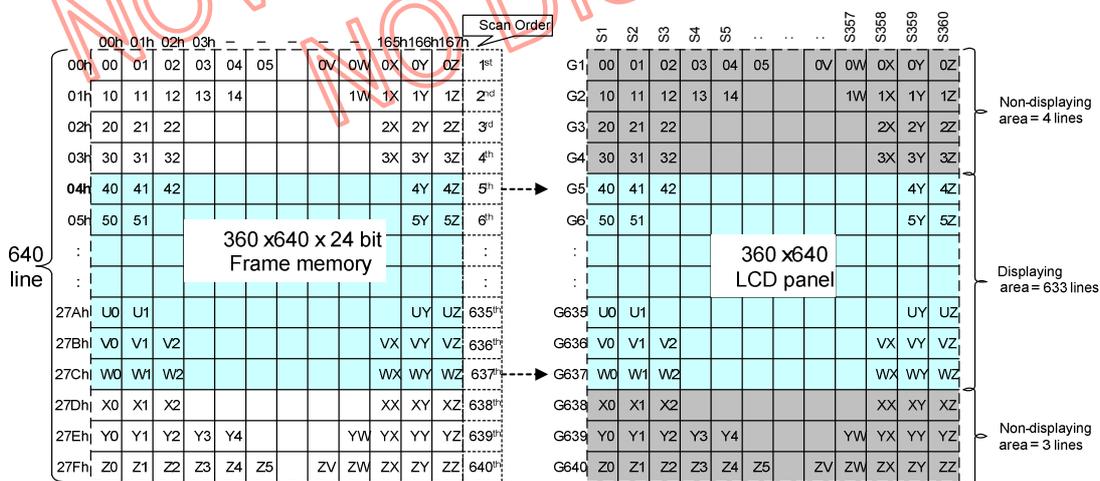
5.9.5.1 PARTIAL MODE

In this mode, the content of the frame memory within an area where column pointer is 00h to 167h and page pointer is 000h to 27Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

Example1) Normal Display On



Example2) Partial Display On (PSL [15:0] = 04h, PEL [15:0] = 279h)



5.9.6 Vertical Scrolling

5.9.6.1 SCROLLING

There is vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

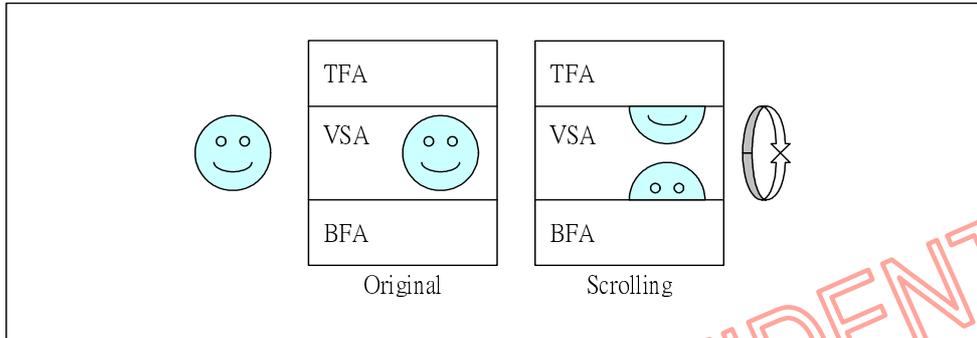
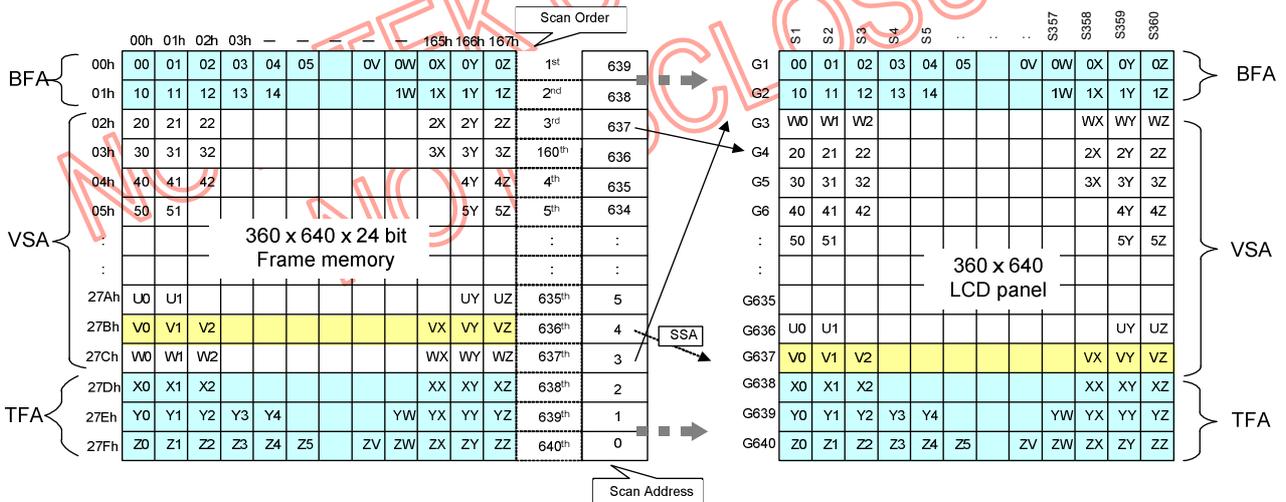
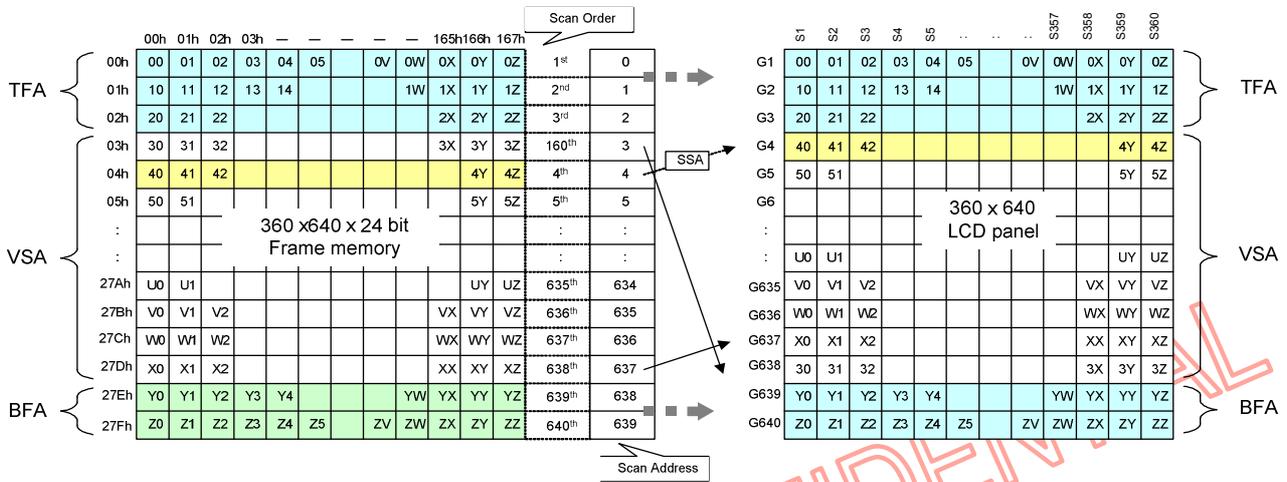


Fig. Difference between Scrolling and original

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=640. In this case, scrolling is applied as shown below.
 Example1) Panel size=360 x 640, TFA =3, VSA=635, BFA=2, SSA=4, MADCTL (ML)=0: Scrolling



Example2) Panel size=360 x 640, TFA =3, VSA=635, BFA=2, SSA=4, MADCTL (ML)=1: Scrolling (TFA and BFA are exchanged)



5.9.6.2 VERTICAL SCROLL EXAMPLE

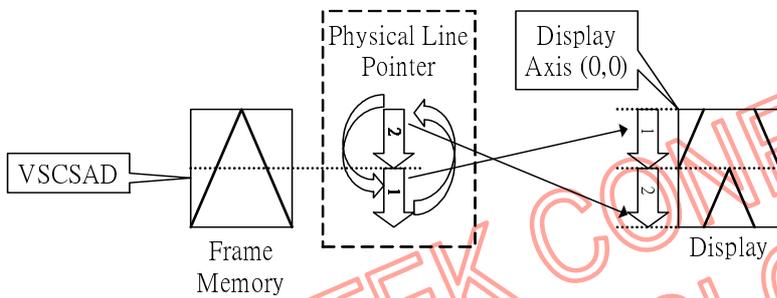
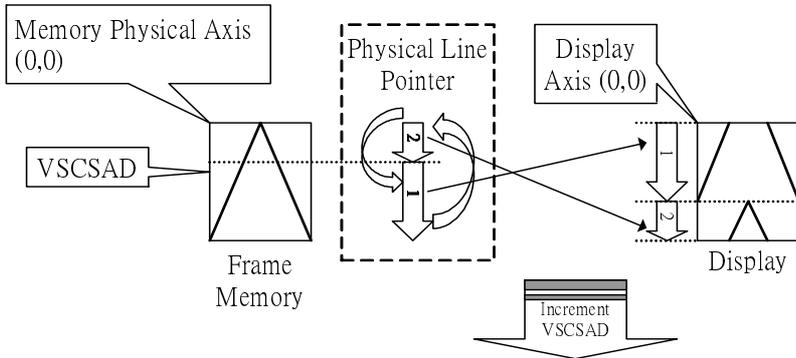
There are 2 cases of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

Case 1: $TFA + VSA + BFA \neq 640$

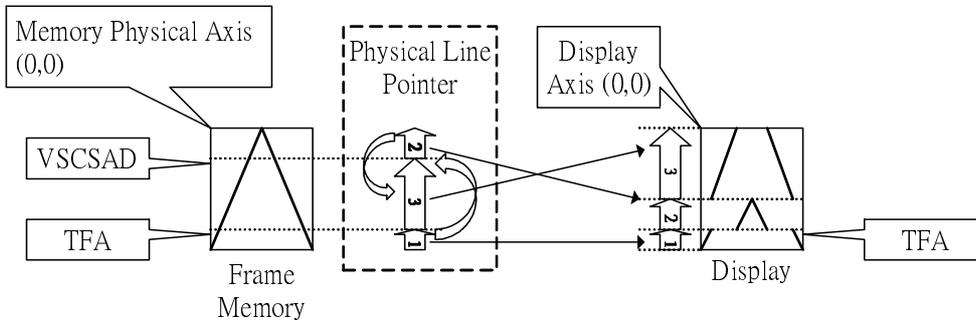
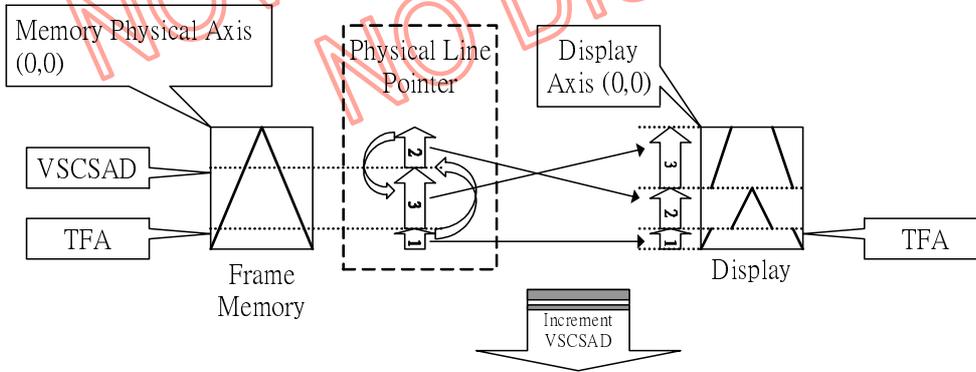
N/A. Do not set $TFA + VSA + BFA \neq 640$. In that case, unexpected picture will be shown.

Case 2: $TFA + VSA + BFA = 640$ (Scrolling)

Example1) When MADCTL parameter ML=“0”, TFA=0, VSA=640, BFA=0 and VSCSAD=40.



Example2) When MADCTL parameter ML="1", TFA=30, VSA=330, BFA=0 and VSCSAD=80.



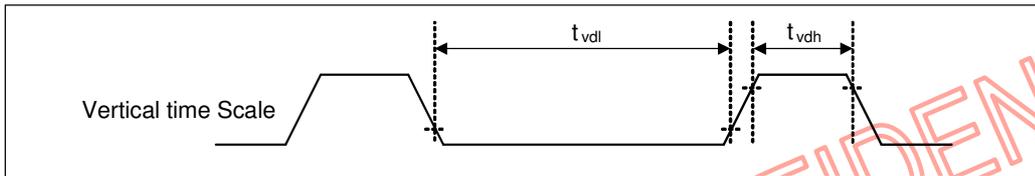
5.10 TEARING EFFECT INFORMATION

5.10.1 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

5.10.1.1 TEARING EFFECT LINE MODES

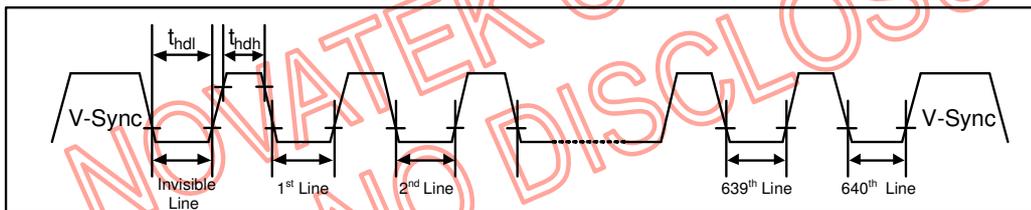
Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



t_{vdh} = The LCD display is not updated from the Frame Memory

t_{vdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

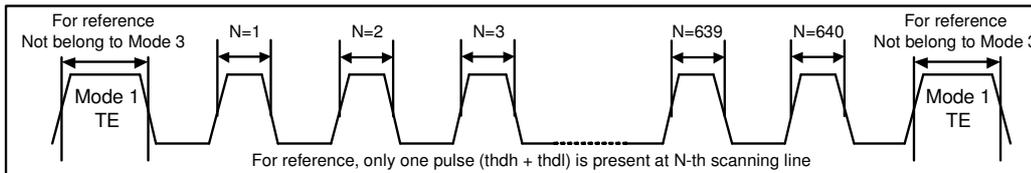
Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 480 H-sync (or 640 H-sync) pulses per field.



t_{thh} = The LCD display is not updated from the Frame Memory

t_{thd} = The LCD display is updated from the Frame Memory (except Invisible Line – see above)

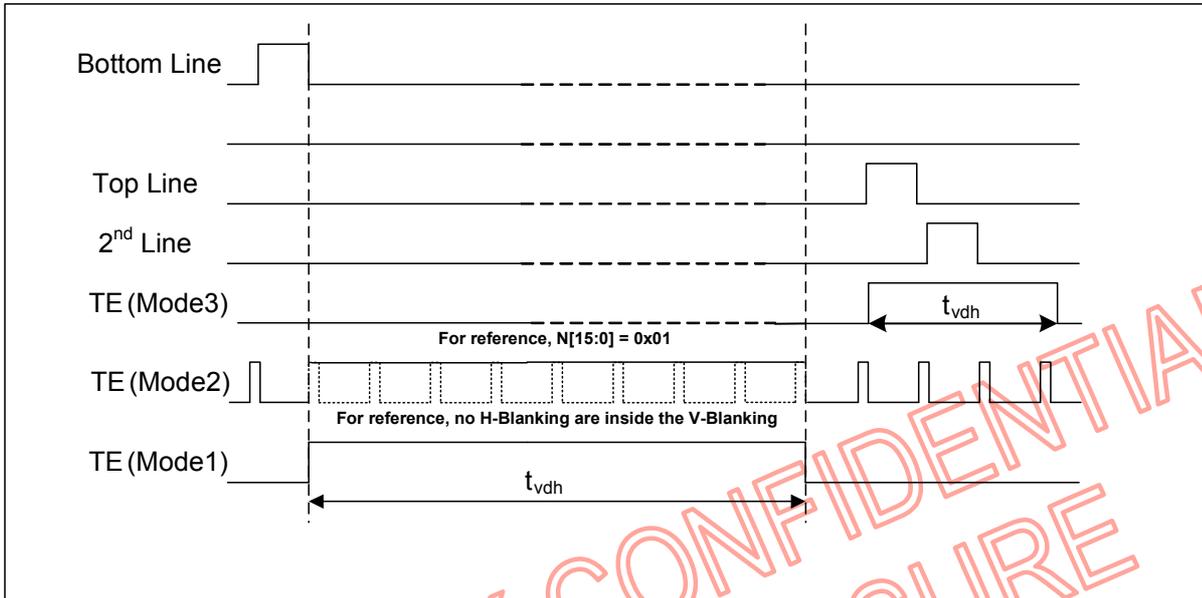
Mode 3, this mode turn on the Tearing Effect Output signal when vertical scanning reaches line N.



N = The N-th scanning line which set by register N[15:0] of command STESL (44h)

The TE mode selection is described as below table

DOPCTR (B0h)	TEOFF (34h) TEON (35h)	STESL (44h)	TE Output
DSITE	M	N[15:0]	
0	X	X	TE off (no output)
1	34h	X	TE off (no output)
1	35h with M=0	N[15:0]=0	TE high in V-porch region (Mode 1)
1	35h with M=0	N[15:0]≠0	TE high at N-th line (Mode 3)
1	35h with M=1	X	TE high in all V-porch and H-porch region (Mode 2)



NOTE: During Sleep In Mode, the Tearing Output Pin is active Low

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5.10.1.2 TEARING EFFECT LINE TIMING

The Tearing Effect signal is described below:

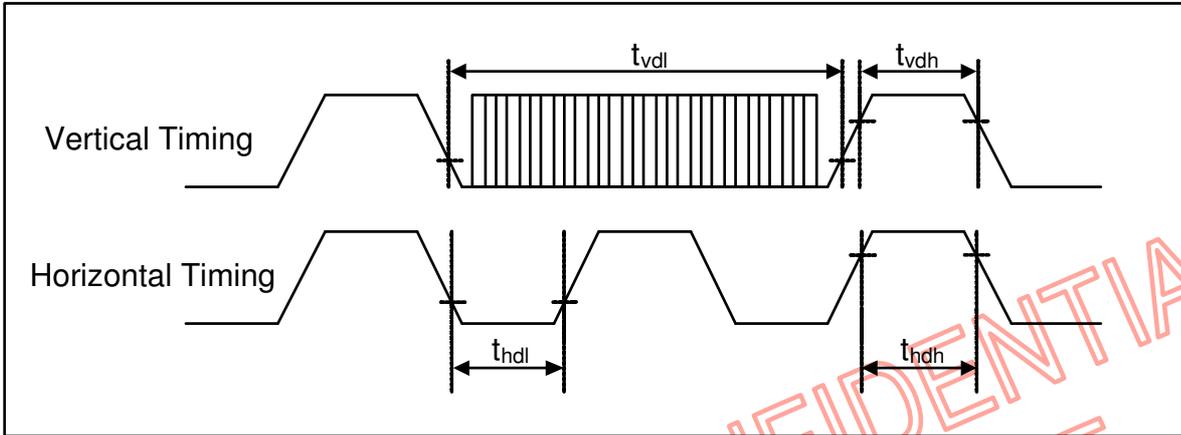


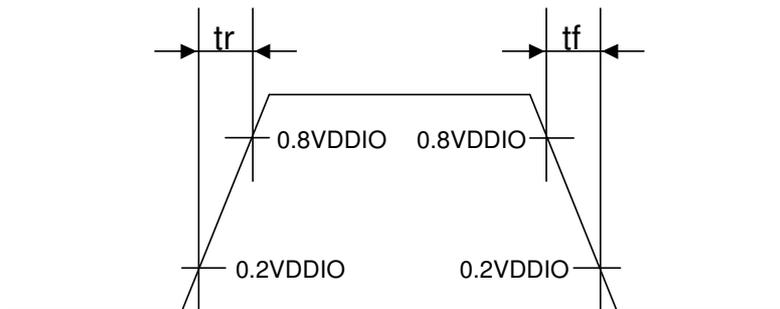
Table 5.10.1 AC characteristics of Tearing Effect Signal

Symbol	Parameter	min	max	unit	Description
tvdl	Vertical Timing Low Duration	14.26	-	ms	
tvdh	Vertical Timing High Duration	1000	-	μ s	
thdl	Horizontal Timing Low Duration	17.986	-	μ s	(360x480)
thdh	Horizontal Timing High Duration	-	13.662	μ s	(360x480)

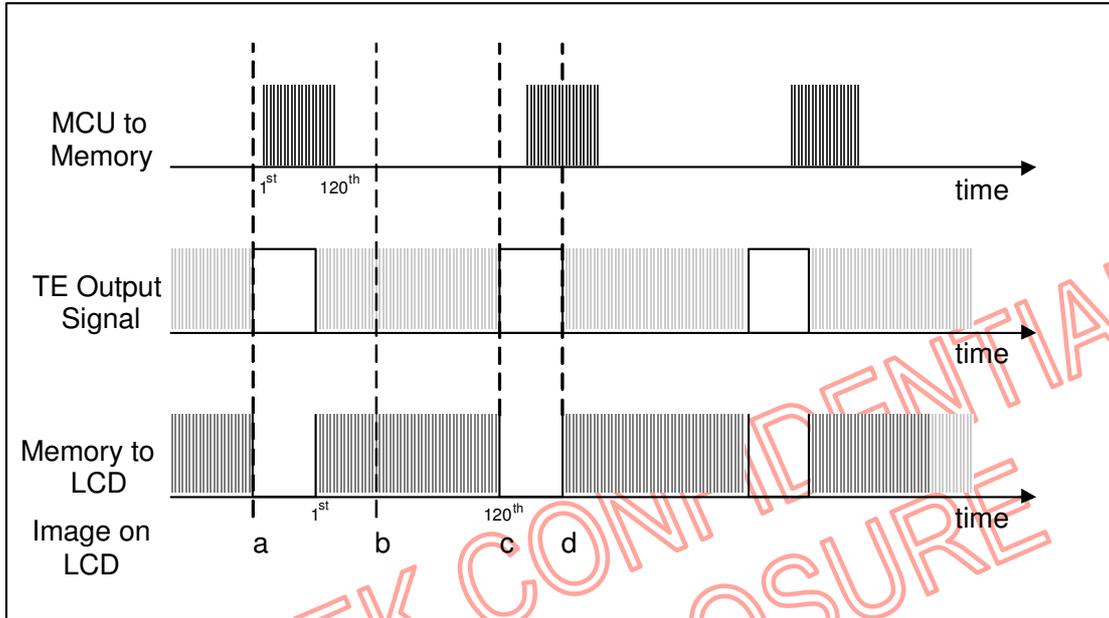
Notes:

1. The timings in above table apply when MADCTL ML=0 and ML=1.
2. The signal's rise and fall times (t_r , t_f) are stipulated to be equal to or less than 15ns when the maximum load is 50 Ω .

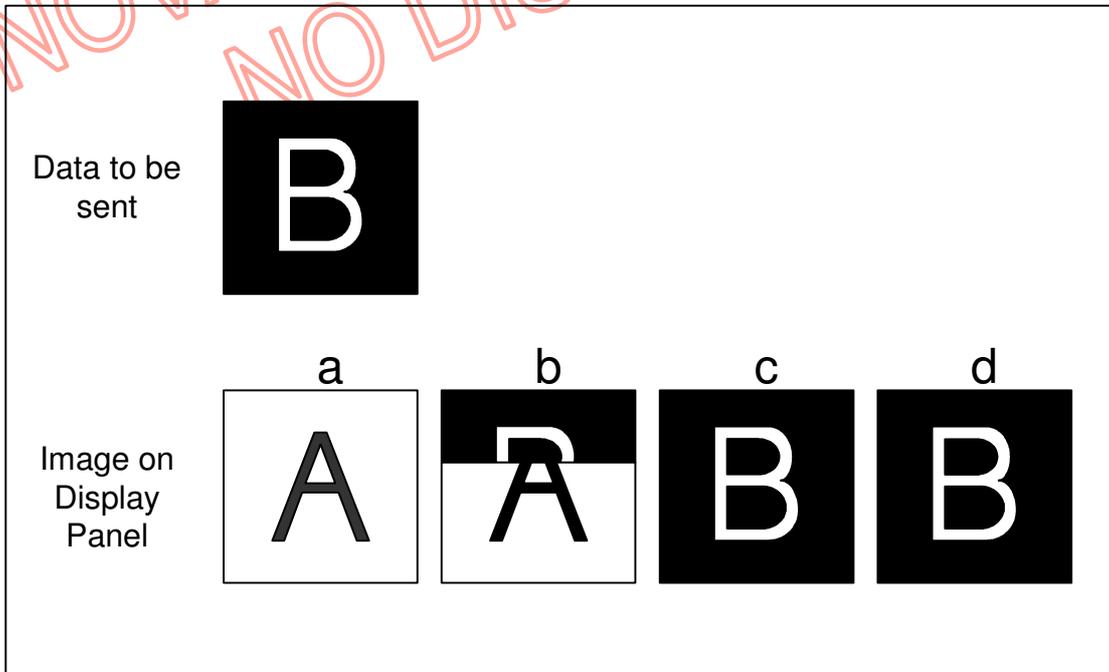
The signal's rise and fall times (t_f , t_r) are stipulated to be equal to or less than 15ns.

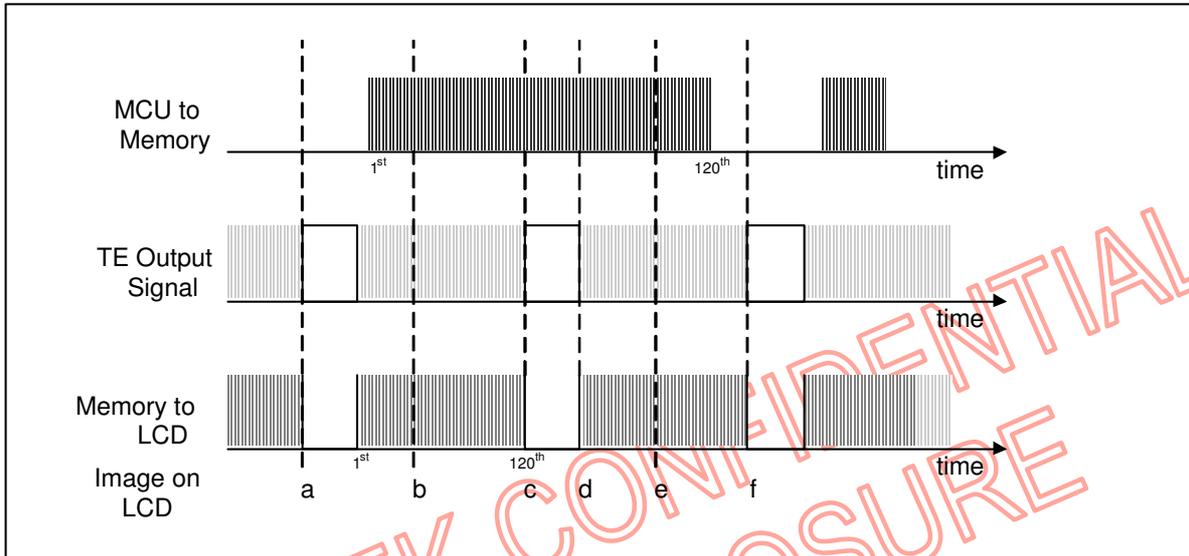


The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

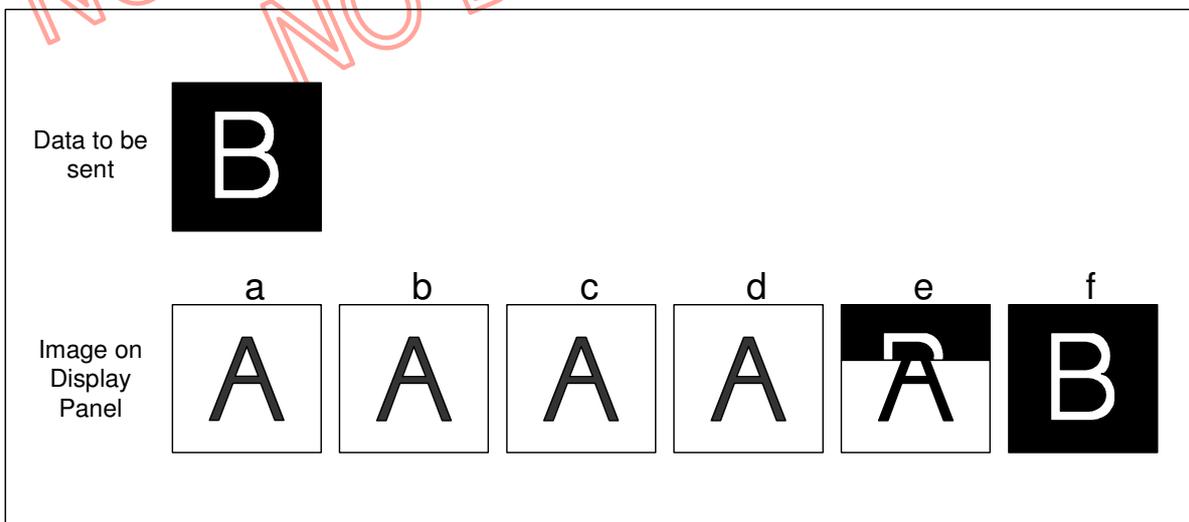
5.10.1.3 EXAMPLE 1: MPU WRITE IS FASTER THAN PANEL READ.


Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



5.10.1.4 EXAMPLE 2: MPU WRITE IS SLOWER THAN PANEL READ.


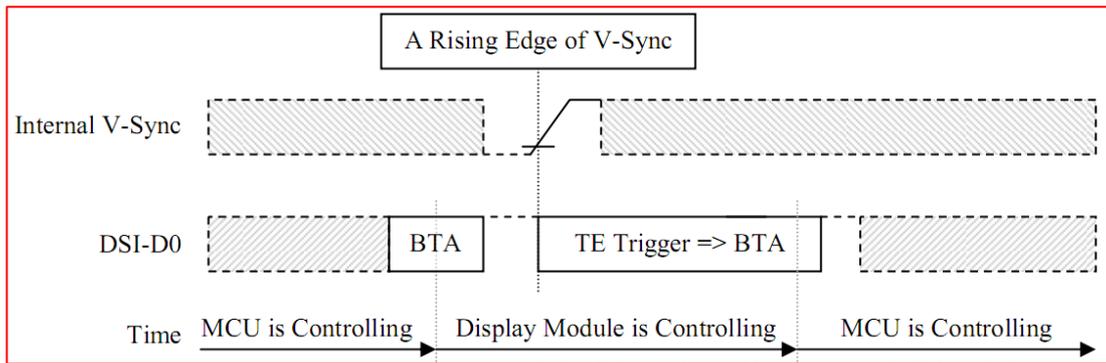
The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.



5.10.2 Tearing Effect Bus Trigger

A Tearing Effect Bus Trigger information supplies to the MCU a Panel synchronization trigger and this Tearing Effect Bus Trigger information can be enabled or disabled by “Tearing Effect Line On (35h)” and “Tearing Effect Line Off (34h)” commands when the only mode of the Tearing Effect Signal is V-Sync information.

The driver IC is sending this trigger information in Escape Mode after the Bus Turnaround (BTA). See section “Tearing Effect (TEE)”

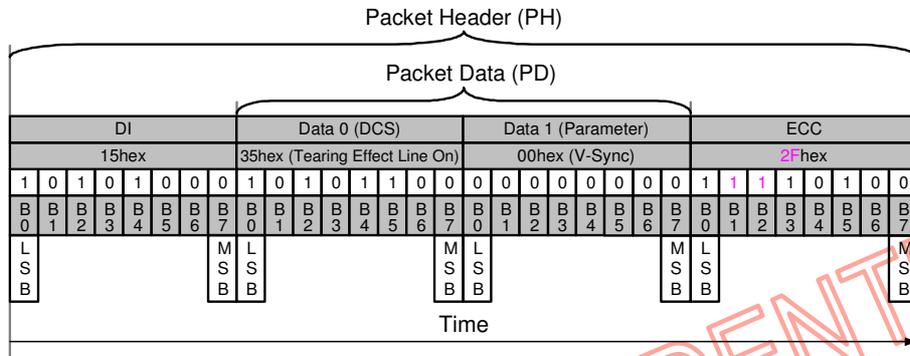


A RISING EDGE OF THE V-SYNC AND DSI-D0

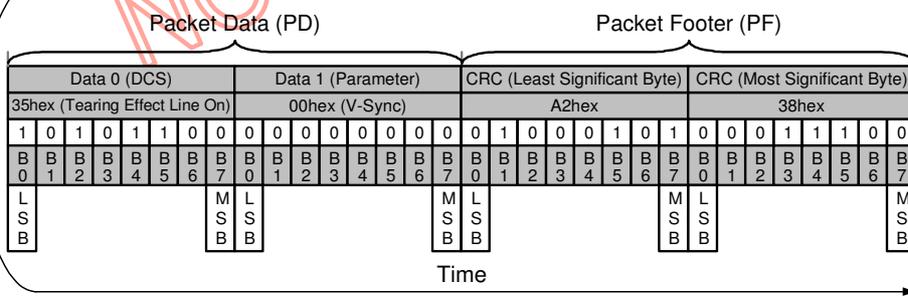
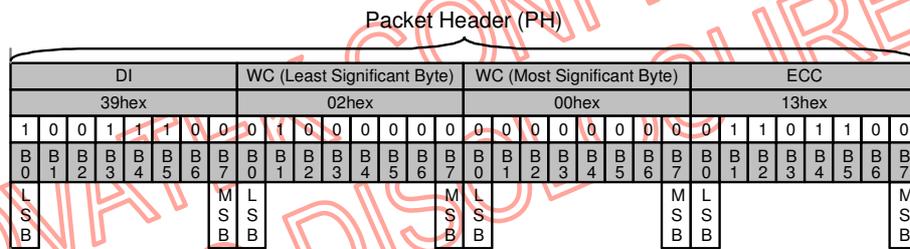
The Tearing Effect Bus Trigger can only use in DSI case without the TE line.

5.10.2.1 TEARING EFFECT BUS TRIGGER ENABLE

The MCU can enable the Tearing Effect Bus Trigger on the driver IC in 2 different ways when Short Packet (SPa) or Long Packet (LPa) is used. These cases are illustrated below.:



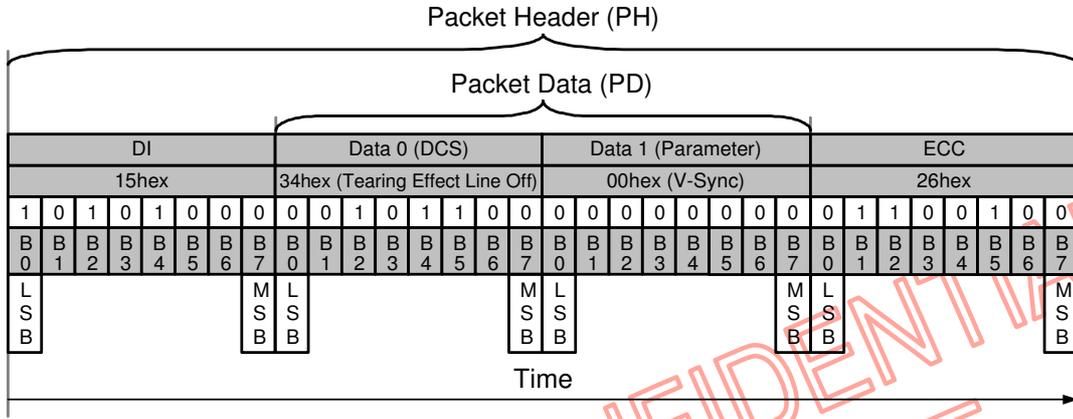
Tearing Effect Bus Trigger Enable (DCSW1-S) – Short Packet (SPa)



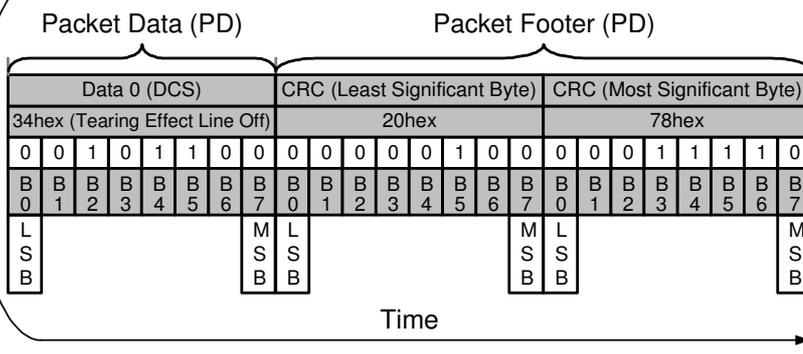
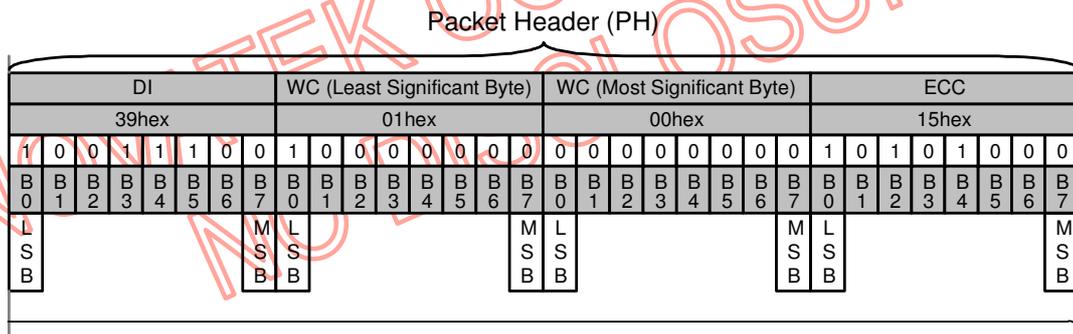
Tearing Effect Bus Trigger Enable (DCSW-L) – Long Packet (LPa)

5.10.2.2 TEARING EFFECT BUS TRIGGER DISABLE

The MCU can disable the Tearing Effect Bus Trigger on the driver IC in 2 different ways when Short Packet (SPa) or Long Packet (LPa) is used. These cases are illustrated below.:



Tearing Effect Bus Trigger Disable (DCSW1-S) - Short Packet (SPa)



Tearing Effect Bus Trigger Disable (DCSW-L) - Long Packet (LPa)

5.10.2.3 TEARING EFFECT BUS TRIGGER SEQUENCES
Tearing Effect Bus Trigger Enable Sequence – DCSW-L and HSDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	Tearing Effect Bus Trigger Enable
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error is corrected by ECC => goto line 19 If error => goto line 30
7						
8	-	-	<=	ACK	-	No Error
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	
12	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
13	-	-	<=	LP-11	-	
14	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Sync
15	-	-	<=	LP-11	-	
16	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
17	-	LP-11	=>	-	-	End
18						
19	-	-	<=	LPDT	AwER	Error Report
20	-	-	<=	LP-11	-	
21	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
22	-	LP-11	=>	-	-	
23	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
24	-	-	<=	LP-11	-	
25	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Sync
26	-	-	<=	LP-11	-	
27	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
28	-	LP-11	=>	-	-	End

29						
30	-	-	<=	LPDT	AwER	Error Report
31	-	-	<=	LP-11	-	
32	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
33	-	LP-11	=>	-	-	If the MCU is not forcing BTA => goto line 34 If the MCU is forcing BTA => goto line 35
34	-	LP-11	=>	-	-	End
35						
36	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
37	-	-	<=	LP-11	-	Dead-Lock (No TE information)
38	-	LP-11	=>	-	-	The MCU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
39	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
40	-	-	<=	LP-11	-	
41	-	-	<=	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported)
42	-	-	<=	LP-11	-	
43	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
44	-	LP-11	=>	-	-	End

Notes:

1. Lines 1 ~ 17 are needed for every frame.
2. Bit 5 and Bit 7 of the AwER are applied.

Tearing Effect Bus Trigger Enable Sequence – DCSW-L and LPDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	LPDT	=>	-	-	Tearing Effect Bus Trigger Enable
3	-	LP-11	=>	-	-	
4	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
5	-	-	<=	LP-11	-	If no error => goto line 7 If error is corrected by ECC => goto line 18 If error => goto line 29
6						
7	-	-	<=	ACK	-	No Error
8	-	-	<=	LP-11	-	
9	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
10	-	LP-11	=>	-	-	
11	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
12	-	-	<=	LP-11	-	
13	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Sync
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
16	-	LP-11	=>	-	-	End
17						
18	-	-	<=	LPDT	AwER	Error Report
19	-	-	<=	LP-11	-	
20	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
21	-	LP-11	=>	-	-	
22	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
23	-	-	<=	LP-11	-	
24	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Sync
25	-	-	<=	LP-11	-	
26	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
27	-	LP-11	=>	-	-	End

28						
29	-	-	<=	LPDT	AwER	Error Report
30	-	-	<=	LP-11	-	
31	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
32	-	LP-11	=>	-	-	If the MCU is not forcing BTA => goto line 33 If the MCU is forcing BTA => goto line 35
33	-	LP-11	=>	-	-	End
34						
35	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
36	-	-	<=	LP-11	-	Dead-Lock (No TE information)
37	-	LP-11	=>	-	-	The MCU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
38	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
39	-	-	<=	LP-11	-	
40	-	-	<=	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported)
41	-	-	<=	LP-11	-	
42	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
43	-	LP-11	=>	-	-	End

Notes:

1. Lines 1 ~ 16 are needed for every frame.
2. Bit 5 and Bit7 of the AwER are applied.

Tearing Effect Bus Trigger Enable Sequence – DCSW1-S and HSDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	Tearing Effect Bus Trigger Enable
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error is corrected by ECC => goto line 19 If error => goto line 30
7						
8	-	-	<=	ACK	-	No Error
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	
12	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
13	-	-	<=	LP-11	-	
14	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Sync
15	-	-	<=	LP-11	-	
16	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
17	-	LP-11	=>	-	-	End
18						
19	-	-	<=	LPDT	AwER	Error Report
20	-	-	<=	LP-11	-	
21	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
22	-	LP-11	=>	-	-	
23	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
24	-	-	<=	LP-11	-	
25	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Sync
26	-	-	<=	LP-11	-	
27	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
28	-	LP-11	=>	-	-	End

29						
30	-	-	<=	LPDT	AwER	Error Report
31	-	-	<=	LP-11	-	
32	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
33	-	LP-11	=>	-	-	If the MCU is not forcing BTA => goto line 34 If the MCU is forcing BTA => goto line 36
34	-	LP-11	=>	-	-	End
35						
36	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
37	-	-	<=	LP-11	-	Dead-Lock (No TE information)
38	-	LP-11	=>	-	-	The MCU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
39	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
40	-	-	<=	LP-11	-	
41	-	-	<=	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported)
42	-	-	<=	LP-11	-	
43	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
44	-	LP-11	=>	-	-	End

Notes:

1. Lines 1 ~ 17 are needed for every frame.
2. Bit 5 and Bit 7 of the AwER are applied.

Tearing Effect Bus Trigger Enable Sequence – DCSW1-S and LPDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	LPDT	=>	-	-	Tearing Effect Bus Trigger Enable
3	-	LP-11	=>	-	-	
4	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
5	-	-	<=	LP-11	-	If no error => goto line 7 If error is corrected by ECC => goto line 18 If error => goto line 29
6						
7	-	-	<=	ACK	-	No Error
8	-	-	<=	LP-11	-	
9	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
10	-	LP-11	=>	-	-	
11	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
12	-	-	<=	LP-11	-	
13	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Sync
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
16	-	LP-11	=>	-	-	End
17						
18	-	-	<=	LPDT	AwER	Error Report
19	-	-	<=	LP-11	-	
20	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
21	-	LP-11	=>	-	-	
22	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
23	-	-	<=	LP-11	-	
24	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Sync
25	-	-	<=	LP-11	-	
26	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
27	-	LP-11	=>	-	-	End

28						
29	-	-	<=	LPDT	AwER	Error Report
30	-	-	<=	LP-11	-	
31	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
32	-	LP-11	=>	-	-	If the MCU is not forcing BTA => goto line 33 If the MCU is forcing BTA => goto line 35
33	-	LP-11	=>	-	-	End
34						
35	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
36	-	-	<=	LP-11	-	Dead-Lock (No TE information)
37	-	LP-11	=>	-	-	The MCU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
38	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
39	-	-	<=	LP-11	-	
40	-	-	<=	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported)
41	-	-	<=	LP-11	-	
42	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
43	-	LP-11	=>	-	-	End

Notes:

1. Lines 1 ~ 16 are needed for every frame.
2. Bit 5 and Bit 7 of the AwER are applied.

Tearing Effect Bus Trigger Disable Sequence – DCSWN-S and LPDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	LPDT	=>	-	-	Tearing Effect Bus Trigger Disable
3	-	LP-11	=>	-	-	

Tearing Effect Bus Trigger Disable Sequence – DCSWN-S and HSDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	HSDT	=>	-	-	Tearing Effect Bus Trigger Disable
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	

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5.11 CHECKSUM

The display module consists of two 8-bit checksum registers, which are used for checksum calculations for "Instruction Code" area registers (includes the frame memory), on the display module.

One of the checksum registers is "First Checksum" (FCS) and another is "Continue Checksum" (CCS).

These register values are set to 00h as an initial value when there is started to calculate a new checksum.

The display module is starting to calculate the new checksum after there is a write access on "Instruction Code" area registers. This means that read commands are not used as a calculation starting trigger in this case.

The checksum calculation is always interrupted, when there is a new write access on Nokia area registers. The checksum calculation is also started from the beginning.

The result of the first finished checksum calculation is stored on the FCS register, which value is kept until there is the new write access on "Instruction Code" area registers and the new checksum value is calculated in the first time again.

The maximum time, when the FCS is readable, is 150ms after there is the last write access on "Instruction Code" area registers.

The checksum calculation is continuing after the finished first checksum calculation where the FCS has gotten the checksum value. These new checksum values are always stored on CCS register (Old value is replaced a new one) after the last Nokia area register has been calculated to the checksum.

The maximum time, when the CCS is readable in the first time, is 300ms after there is the last write access on "Instruction Code" area registers.

There is always updated a checksum comparison bit (See section: "Read Display Self-Diagnostic Result (0Fh)" and bit D0) when there is compared FCS and CCS checksums after a new checksum value is stored on CCS.

The maximum time, when the comparison has been done between FCS and CCS in the first time, is 300ms then the comparison has been done in every 150ms (this is maximum time).

User can read FCS, CCS and Comparison bit D0 values. See section: "Read First Checksum (AAh)", "Read Continue Checksum (AFh)" and "Read Display Self-Diagnostic Result (0Fh)".

There can be an overflow during a checksum calculation. These overflow bits are not needed to store anywhere. This means that these overflow bits can be ignored by the display module.

An example of the checksum calculation:

- Register Values: A1h, 12h, 81h, DEh, F2h
- Calculated Value: 304h (= A1h + 12h + 81h + DEh + F2h)
- Ignored Bits: 3h
- Stored Checksum: 04h

This checksum calculation function is only running in "Sleep Out" mode and it is stopped in "Sleep In" mode.

Table 5.11.1 Checksum Sequence

Step Note1	Time Note2	Action	Temporary Register	First Checksum Register (FCS)	Continue Checksum Register (CCS)	Comment
1	0	Initialization	Set to 00h	Set to 00h	Set to 00h	The last write action on "Instruction Code" area registers => FCS an CCS registers are initialized
2	0 150ms	Continue sum of "Instruction Code" area registers	Counting	-	-	The first register counting is running
3	150ms	Stores sum of registers on FCS register	Set to 00h after value is moved to FCS register	Stores sum of "Instruction Code" area registers on FCS register	-	The result of the first register counting is stored on FCS register. The result of the FCS is available to the MPU
4	150ms 300ms	Continue sum of "Instruction Code" area registers	Counting	-	-	The second register counting is running
5	300ms	1) Stores sum of registers on CCS register 2) Compares stored FCS and CCS value	Set to 00h after value is moved to CCS register	-	Stores sum of "Instruction Code" area registers on CCS register	The result of the comparison is stored on separated registers, which can read separated read commands. The result of the CCS and comparison result are available to the MPU
6	300ms 450ms	Continue sum of "Instruction Code" area registers	Counting	-	-	The third register counting is running
7	450ms	1) Stores sum of registers on CCS register 2) Compares stored FCS and CCS value	Set to 00h after value is moved to CCS register	-	Stores sum of "Instruction Code" area registers on CCS register	The result of the comparison is stored on separated registers, which can read separated read commands. The result of the CCS and comparison result are available to the MPU
8	450 600ms	Continue sum of "Instruction Code" area registers	Counting	-	-	The fourth register counting is running
9	600ms	1) Stores sum of registers on CCS register 2) Compares stored FCS and CCS value	Set to 00h after value is moved to CCS register	-	Stores sum of "Instruction Code" area registers on CCS register	The result of the comparison is stored on separated registers, which can read separated read commands. The result of the CCS and comparison result are available to the MPU
10	etc	-	-	-	-	Same sequence continue e.g. step 4 and 5

5.12 POWER ON/OFF SEQUENCE

VPNL and VDDI can be powered on / off in any order.

During power off, if LCD is in the Sleep Out mode, VPNL and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VPNL can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

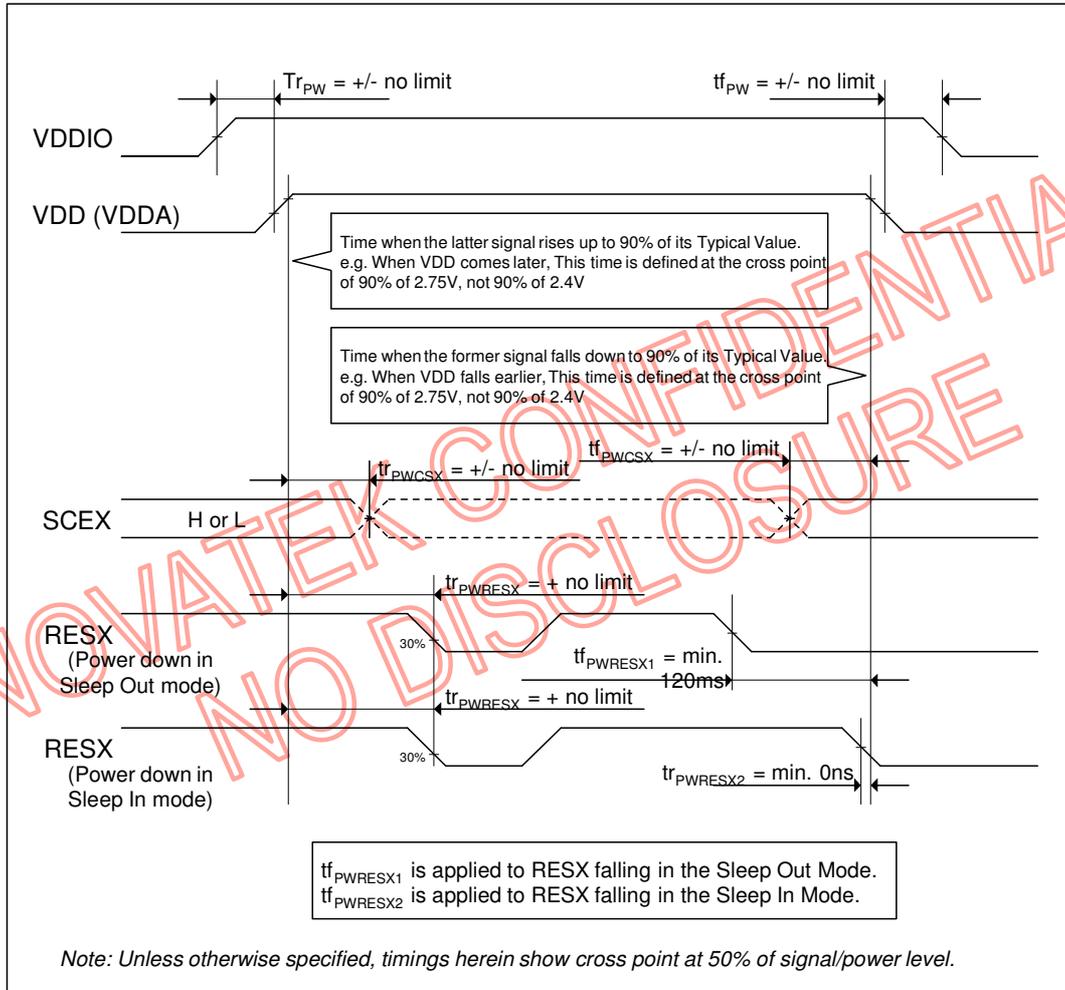
Notes:

1. *There will be no damage to the display module if the power sequences are not met.*
2. *There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.*
3. *There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.*
4. *If RESX line is not held stable by host during Power On Sequence as defined in Sections 5.12.1 and 5.12.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.*
5. *There is not a limit for Rise/Fall time on VDDI and VPNL.*
6. *The display module can also initialize and calibrate CLK_P/CLK_N and D0_P/D0_N lanes within 5ms after LP-11 (Clock and Data Channels), VDDI and VPNL are applied and H/W Reset is not active (5ms is as same as the Reset Canceling Time).*

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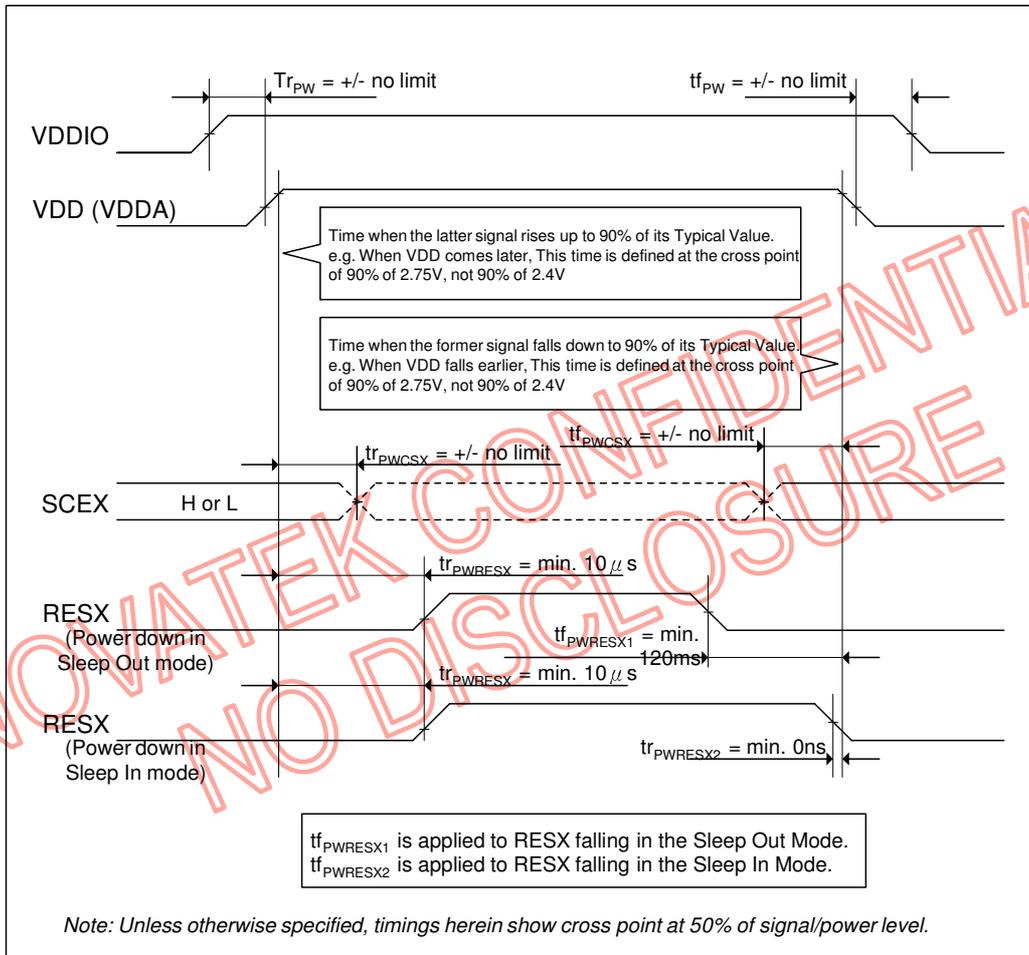
5.12.1 Case 1 – RESX line is held High or Unstable by Host at Power On

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VPINL and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



5.12.2 Case 2 – RESX line is held Low by host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VPNL and VDDI have been applied.



5.12.3 Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until "Power On Sequence" powers it up.

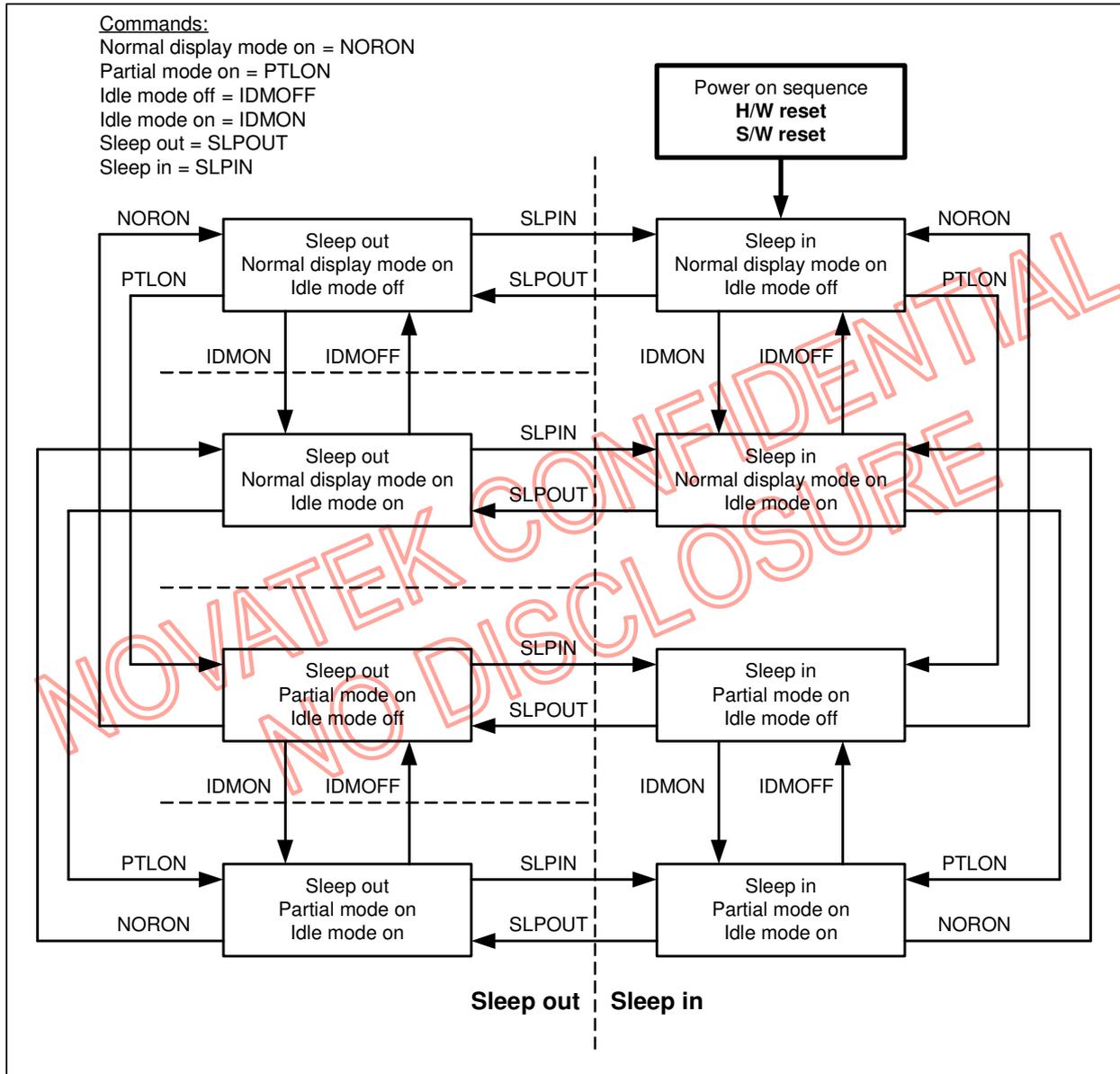
5.13 POWER LEVEL MODES

5.13.1 Definition

6 level modes are defined they are in order of maximum power consumption to minimum power consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
In this mode, the display is able to show maximum 16.7M colors.
2. Partial Mode On, Idle Mode Off, Sleep Out
In this mode, part of the display is used with maximum 16.7M colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
In this mode, the full display is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out
In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode
 - 5.1 Sleep In Mode (RAMKP=1).
In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. Only the MPU interface and registers are working. Contents of the frame memory can be safe.
 - 5.2 Sleep In Mode (RAMKP=0).
In this mode, the DC/DC converter, internal oscillator, panel driver circuit, and SRAM power are stopped. Only the MPU interface and registers are working. Contents of the frame memory can not keep.
6. Power Off Mode
In this mode, VDDI and VPNL are removed.

NOTE: Transition between mode 1~5 is controllable by MPU commands. Mode 6 is entered only when both power supplies for I/O and analog circuits are removed.

5.13.2 Power Level Mode Flow Chart

NOTES:

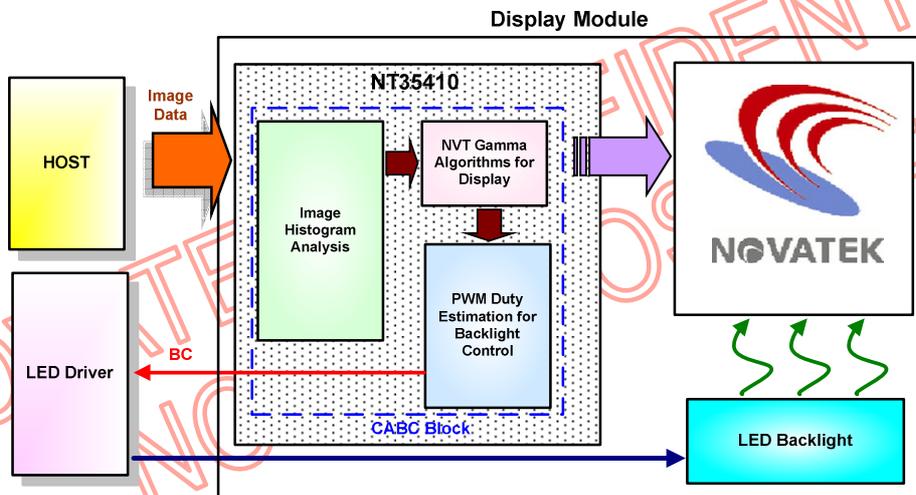
- 1) There is not any abnormal visual effect when there is changing from one power mode to another power mode.
- 2) There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode

5.14 Content Adaptive Brightness Control (CABC) function

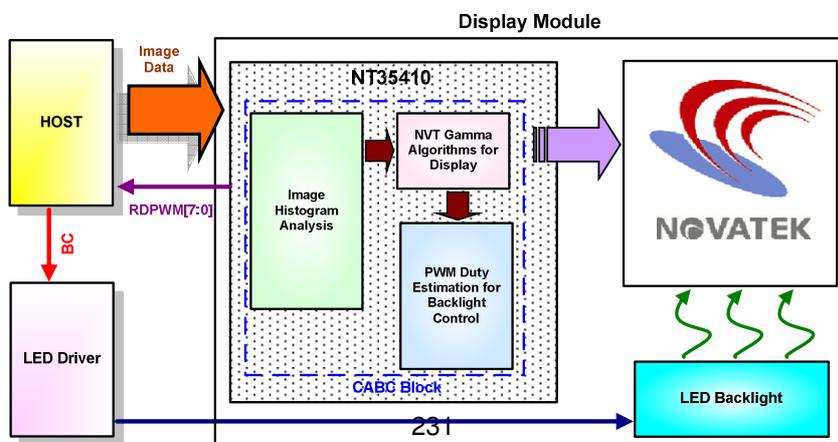
5.14.1 Dynamic Backlight Control Function

The NT35410 supports Backlight-Control function to control brightness of backlight and to process image dynamically. This function enables to reduce backlight power and minimize the effect of reduced power on the display image. The display image is dynamically controlled by CABC block. The availability of this function ranges from moving picture such as TV image to still picture such as menu. The brightness of backlight and image processing coefficient are calculated so that image data is optimized. Backlight power is reduced without changing display image. The Backlight-Control function is supported for the following two architectures:

1. When bit BL of “Write CTRL Display (53h)” command is ‘1’, the PWM signal is used to directly control the LED driver IC. The LED driver IC is controlled entirely via the NT35410.



2. When bit BL of “Write CTRL Display (53h)” command is ‘0’, the host processor reads LED brightness information internally generated by CABC processing from the NT35410. Then, the LED driver IC is controlled from the host processor. There is the time difference between brightness adjustment by PWM and displaying data processed from the NT35410.



5.14.1.1 CONTENT ADAPTIVE BRIGHTNESS CONTROL

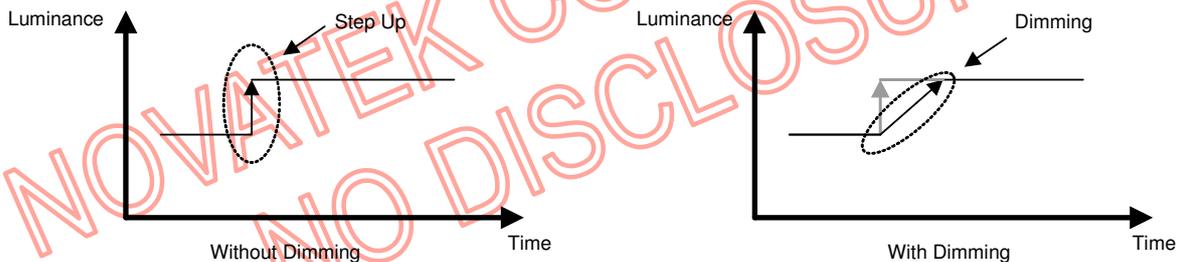
A Content Adaptive Brightness Control function can be used to reduce the power consumption of the luminance source. Content adaptation means that content grey level scale can be increased while simultaneously lowering brightness of the backlight to achieve same perceived brightness. The adjusted grey level scale and thus the power consumption reduction depend on the content of the image.

This function and its different modes can be controlled. See command “Write Content Adaptive Brightness Control (55h)” (bits: C1 and C0) for more information. Definition of Modes:

- **Off mode:** Content Adaptive Brightness Control functionality is totally off.
- **UI [User interface] image mode:** Optimized for UI image. It is kept image quality as much as possible. Target power consumption reduction ratio: 10% or less
- **Still picture mode:** Optimized for still picture. Some image quality degradation would be acceptable. Target power consumption reduction ratio: more than 30%
- **Moving image mode:** Optimized for moving image. It is focused on the biggest power reduction with image quality degradation. Target power consumption reduction ratio: more than 30%.

5.14.1.2 DISPLAY BACKLIGHT DIMMING CONTROL

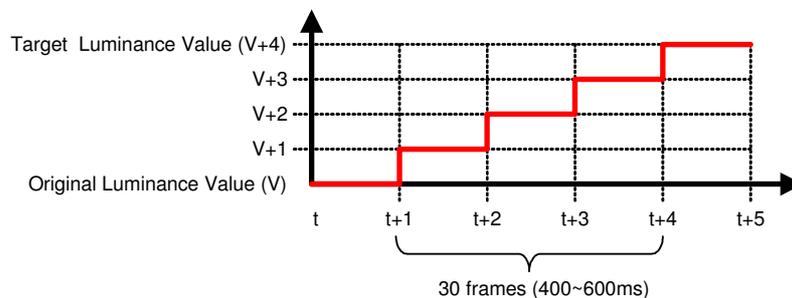
A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from one brightness level to another. This dimming function curve is the same in increment and decrement directions. The basic idea is described below.



Dimming function can be enabled and disabled. See command “Write CTRL Display (53h)” (bit DD) for more information.

From the original brightness value to the target brightness value, the transferring time steps between these two brightness values are equal making the transition linear. The dimming function is working similarly in both upward and downward directions.

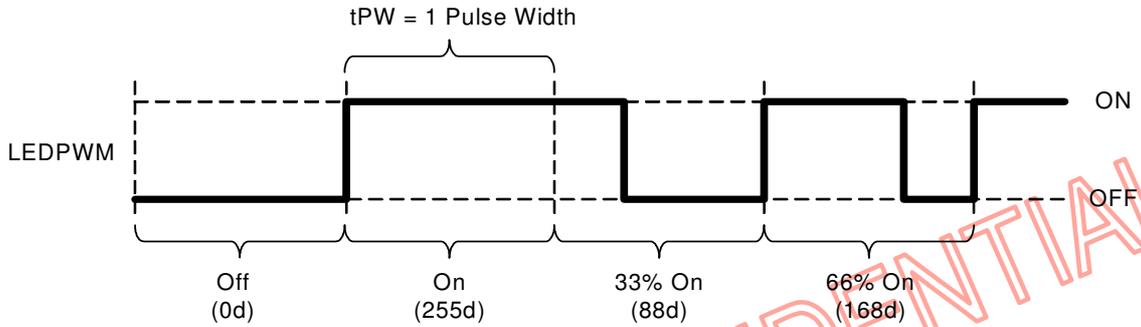
An upward example is illustrated below:



5.14.1.3 BRIGHTNESS CONTROL LINE

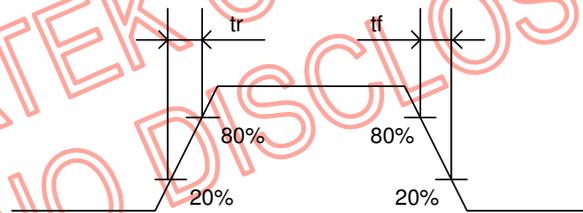
The brightness control (BC) line is sending control information to the display brightness control unit which can be a power supply for the display brightness.

The Brightness Control Line Timings are described below:



Symbol	Parameter	min	max	unit	description
tPW	Pulse Width	0.0333	8.33	ms	

Note: The signal rise and fall times (t_f , t_r) are stipulated to be equal to or less than 15ns.



5.15 INSTRUCTION DECODER & REGISTER

The instruction decoder identifies command words arriving at the interface and routes the following data type bytes to their destination. The command set can be found in “**6 INSTRUCTION DESCRIPTION**” section.

5.16 SYSTEM CLOCK GENERATOR

The timing generator produces the various signals to drive the internal circuitry. Internal chip operation is not affected by operations on the data bus.

5.17 OSCILLATOR

NT35410 has on-chip oscillator which does not require external components. This oscillator output signal is used for system clock generation for internal display operation

5.18 SOURCE DRIVER

The source driver block includes 360x640 source outputs (S1 to S1080), which should be connected directly to the TFT-LCD. The source output signals are generated in the data processing block after the data is read out of the RAM and latched, which represent the simultaneous selected rows. When less than 720 sources are required the unused source outputs should be left open-circuit.

5.19 GATE DRIVER

The gate driver block includes 640 gate outputs (G1 to G640) which should be connected directly to the TFT-LCD.

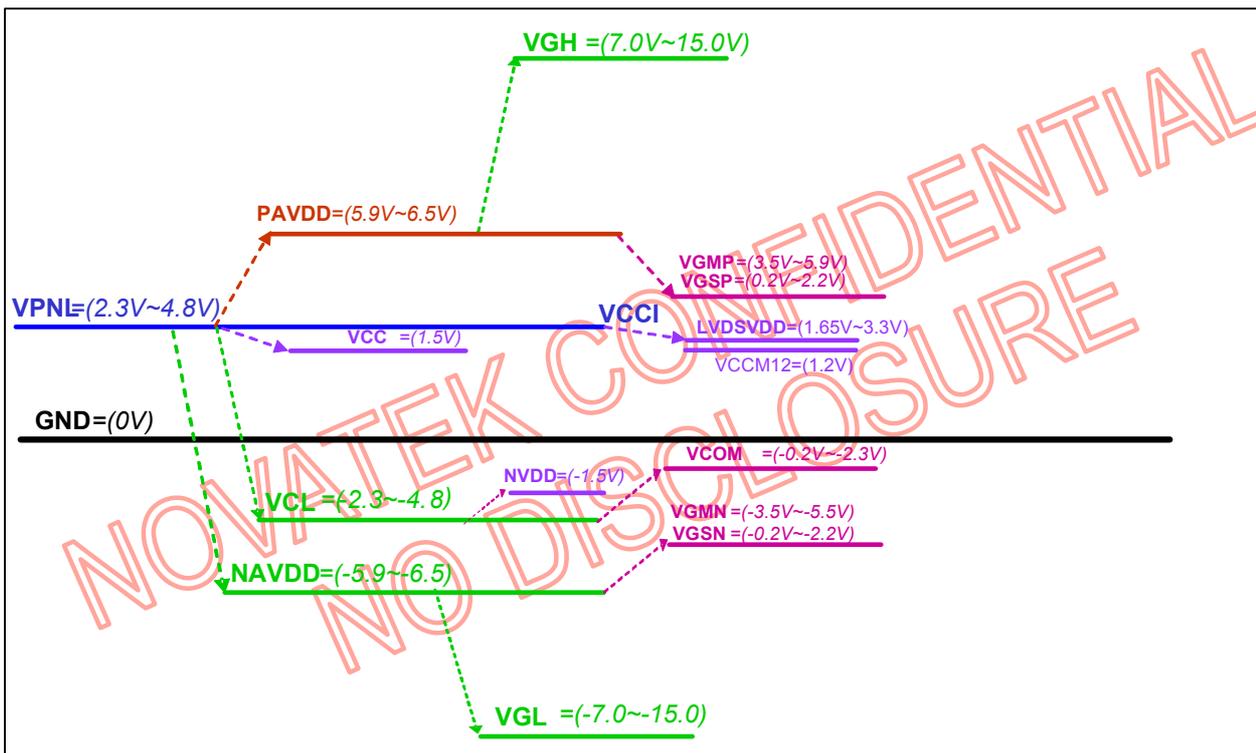
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5.20 LCD POWER GENERATION CIRCUIT

5.20.1 LCD Power Generation Scheme

The boost voltage generated in NT35410 is shown as below.

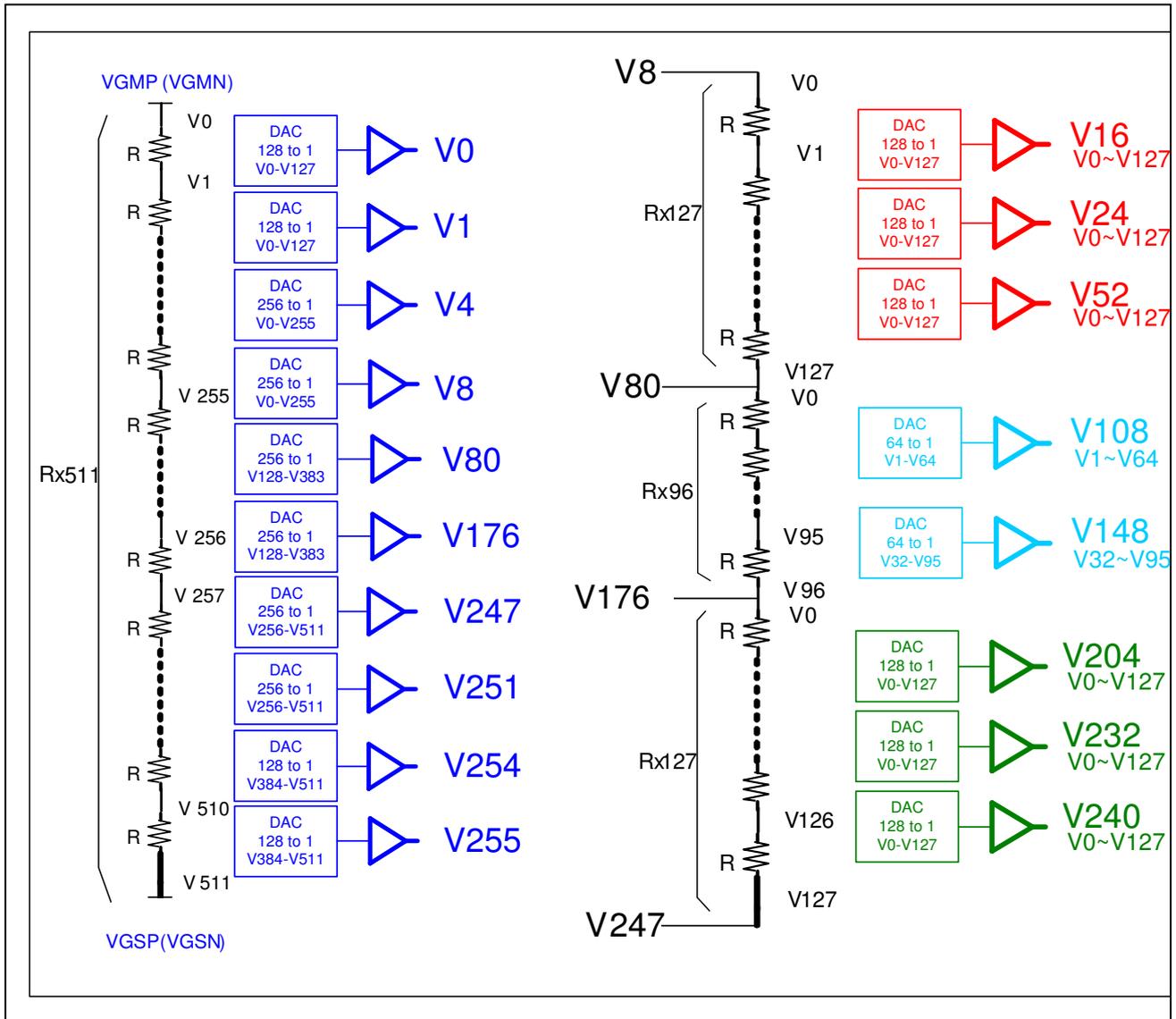
Power Architecture (Regulated Power Setting)



Note: The power generation scheme is without panel loading.

5.21 GAMMA CORRECTION FUNCTION

The structure of the grayscale amplifier is shown as below. The 13 voltage levels between VGMP/VGMN and VGSP/VGSN are determined by the gradient adjustment register, the reference adjustment register, the amplitude adjustment register and the micro-adjustment register.



5.22 Zigzag, Column, 1-Dot, 2-Dot Inversion (VCOM DC Drive)

The NT35410, in addition to the frame-inversion liquid crystal drive, supports the ZigZag, column, 1-dot and 2-dot inversion driving methods to invert the polarity of liquid crystal. The ZigZag, column, 1-dot and 2-dot inversion can provide a solution for improving display quality.

In determining the inversion drive for the inversion cycle, check the quality of display on the liquid crystal panel. Note that setting 1-dot inversion will raise the frequency of the liquid crystal polarity inversion and increase the charging/discharging current on liquid crystal cells.

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5.23 DISPLAY PANEL COLOR CHARACTERISTICS

Color characteristics of the display panel are stored on the display module that they can be read via the used interface by the engine what is using this display panel color characteristics information to adjust a color information of the image frame, what is on the engine, to match a wanted color outlook of the image on the display panel.

Used color characteristics can share 2 categories: Mandatory and Optional. The mandatory color characteristics are Black, White, Red, Green and Blue. The optional color characteristics is used if it is needed and it is called as A color (e.g. Cyan). The bits of the A color are set to '0's they are not used on the display module.

A read color characteristic value is based on 10 bit floating value where the MSB is 9th bit and the LSB is 0th bit. All power values of the bits are listed below:

- Bit 9: $2^{-1} = 0.5$,
- Bit 8: $2^{-2} = 0.25$,
- Bit 7: $2^{-3} = 0.125$,
- Bit 6: $2^{-4} = 0.0625$,
- Bit 5: $2^{-5} = 0.03125$,
- Bit 4: $2^{-6} = 0.015625$,
- Bit 3: $2^{-7} = 0.007813$,
- Bit 2: $2^{-8} = 0.003906$,
- Bit 1: $2^{-9} = 0.001953$,
- Bit 0: $2^{-10} = 0.000977$.

The wanted value is an approximation in the most of the cases when there is used binary numbers. Therefore, there is used the nearest value what can get e.g. Rx can be:

- Actual value: 0.6400, Stored value Rx[9:0] = 10 1000 1111b = 0.6396,
- Actual value: 0.3300, Stored value Rx[9:0] = 01 0101 0010b = 0.3301,
- Actual value: 0.3000, Stored value Rx[9:0] = 01 0011 0011b = 0.2998,
- Actual value: 0.6000, Stored value Rx[9:0] = 10 0110 0101b = 0.5986,
- Actual value: 0.1500, Stored value Rx[9:0] = 00 1001 1010b = 0.1504,
- Actual value: 0.0600, Stored value Rx[9:0] = 00 0011 1101b = 0.0596,
- Actual value: 0.3127, Stored value Rx[9:0] = 01 0100 0000b = 0.3125,
- Actual value: 0.3290, Stored value Rx[9:0] = 01 0101 0001b = 0.3291.

The value 0.6396 has calculated as follows:

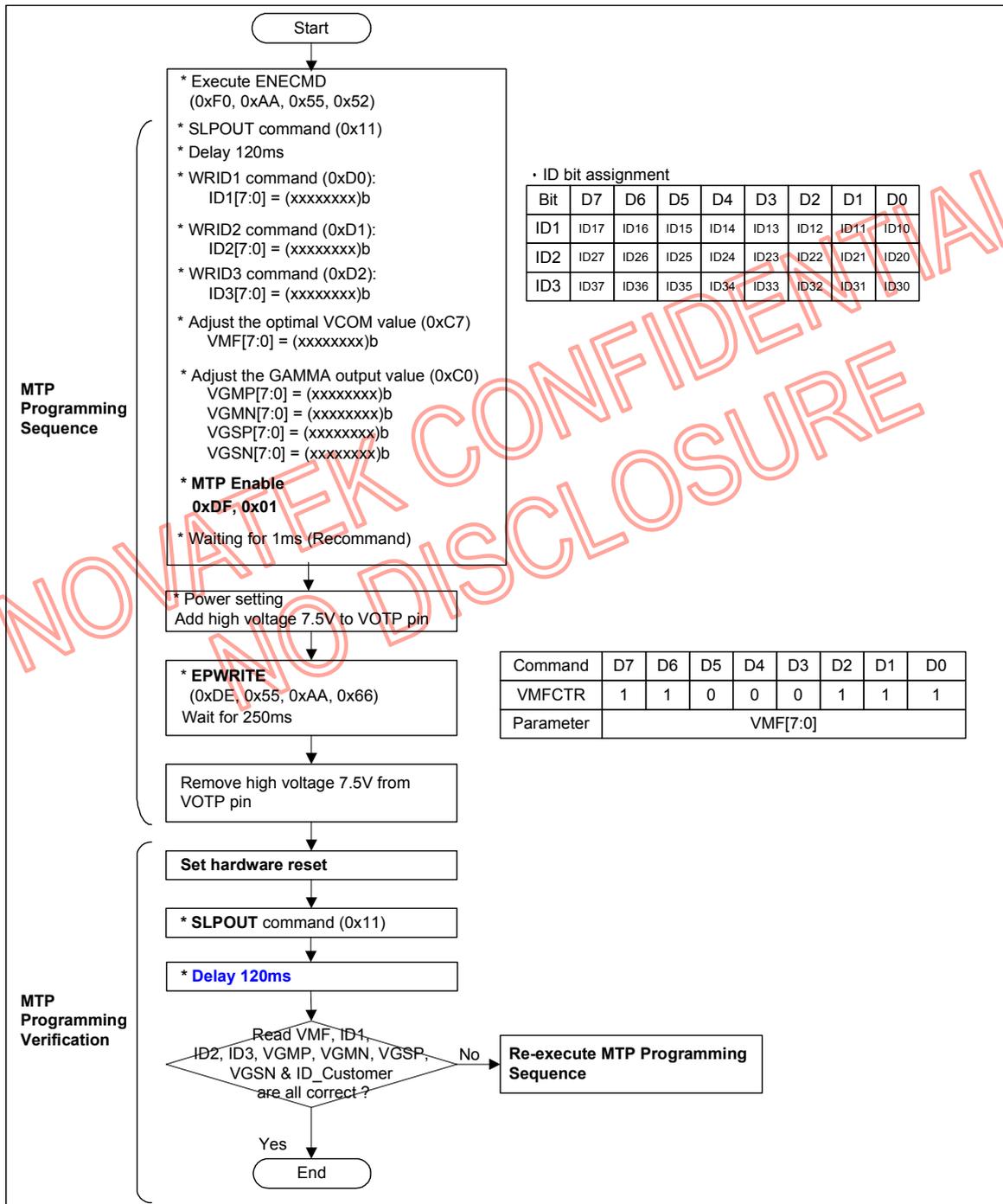
- Binary value: 10 1000 1111b
- Formula: $Rx[9] \times 0.5 + Rx[8] \times 0.25 + Rx[7] \times 0.125 + Rx[6] \times 0.0625 + Rx[5] \times 0.03125 + Rx[4] \times 0.015625 + Rx[3] \times 0.007813 + Rx[2] \times 0.003906 + Rx[1] \times 0.001953 + Rx[0] \times 0.000977$
- Use: $1 \times 0.5 + 0 \times 0.25 + 1 \times 0.125 + 0 \times 0.0625 + 0 \times 0.03125 + 0 \times 0.015625 + 1 \times 0.007813 + 1 \times 0.003906 + 1 \times 0.001953 + 1 \times 0.000977$

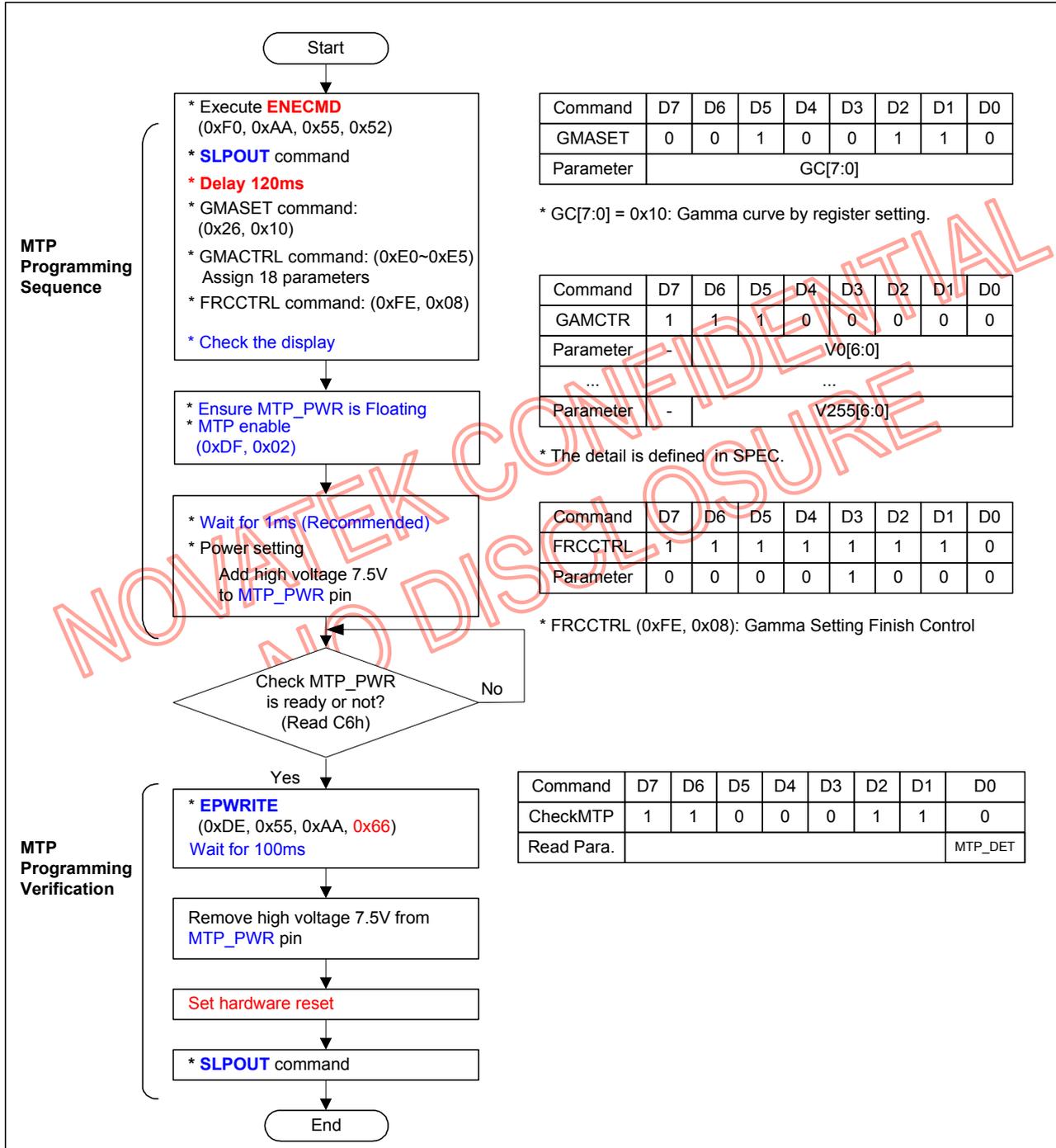
See also sections:

“Read Black/White Low Bits (70h)”, “Read Bkx (71h)”, “Read Bky (72h)”, “Read Wx (73h)”, “Read Wy (74h)”, “Read Red/Green Low bits (75h)”, “Read Rx (76h)”, “Read Ry (77h)”, “Read Gx (78h)”, “Read Gy (79h)”, “Read Blue/AColor Low Bits (7Ah)”, “Read Bx (7Bh)”, “Read By (7Ch)”, “Read Ax (7Dh)”, “Read Ay (7Eh)”.

5.24 MTP PROGRAMMING SEQUENCE

5.24.1 ID code and VCOM offset programming sequence



5.24.2 Gamma code programming sequence


6 INSTRUCTION DESCRIPTION

6.1 INSTRUCTION CODE

Table 6.1.1 Instruction Code

NO	Instruction	ACT	R/W	Address		Parameter										Function
				Others	MDDI	MDDI[15:8]	D7	D6	D5	D4	D3	D2	D1	D0		
						No Parameter										
1	NOP	Dir	W	00h	0000h	No Parameter										No Operation
2	SWRESET	Cnd1	W	01h	0100h	No Parameter										Software reset
3	RDDID	Dir	R	04h	0400h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read ID1	
					0401h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	Read ID2	
					0402h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	Read ID3	
4	RDNUMED	Dir	R	05h	x	x	P7	P6	P5	P4	P3	P2	P1	P0	Read No. of the Errors on DSI only	
5	RDRED	Dir	R	06h	x	x	R7	R6	R5	R4	R3	R2	R1	R0	Read First pixel of Red color	
6	RDGREEN	Dir	R	07h	x	x	G7	G6	G5	G4	G3	G2	G1	G0	Read First pixel of Green color	
7	RDBLUE	Dir	R	08h	x	x	B7	B6	B5	B4	B3	B2	B1	B0	Read First pixel of Blue color	
8	RDDST	Dir	R	09h	0900h	00h	ST[31:24]								Read Display Status	
					0901h	00h	ST[23:16]									
					0902h	00h	ST[15:8]									
					0903h	00h	ST[7:0]									
9	RDDPM	Dir	R	0Ah	0A00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Power Mode	
10	RDDMADCTL	Dir	R	0Bh	0B00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display MADCTL	
11	RDDCOLMOD	Dir	R	0Ch	0C00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Pixel Format	
12	RDDIM	Dir	R	0Dh	0D00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Image Mode	
13	RDDSM	Dir	R	0Eh	0E00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Signal Mode	
14	RDDSDR	Dir	R	0Fh	0F00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Self-diagnostic result	
15	SLPIN	DVS	W	10h	1000h	No Parameter										Sleep in & booster off
16	SLPOUT	Dir	W	11h	1100h	No Parameter										Sleep out & booster on
17	PTLON	DVS	W	12h	1200h	No Parameter										Partial mode on
18	NORON	DVS	W	13h	1300h	No Parameter										Partial off (Normal)
19	INVOFF	DVS	W	20h	2000h	No Parameter										Display inversion off (normal)
20	INVON	DVS	W	21h	2100h	No Parameter										Display inversion on
21	ALLPOFF	DVS	W	22h	2200h	No Parameter										All pixel off (black)
22	ALLPON	DVS	W	23h	2300h	No Parameter										All pixel on (white)
23	GAMSET	DVS	W	26h	2600h	00h	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	Gamma curve select	
24	DISPOFF	DVS	W	28h	2800h	No Parameter										Display off
25	DISPON	DVS	W	29h	2900h	No Parameter										Display on
26	CASET	Dir	W	2Ah	2A00h	00h	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	Column address set XS[15:0]: column start address XE[15:0]: column end address	
					2A01h	00h	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		
					2A02h	00h	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		
					2A03h	00h	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		
27	RASET	Dir	W	2Bh	2B00h	00h	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	Row address set YS[15:0]: row start address YE[15:0]: row end address	
					2B01h	00h	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		
					2B02h	00h	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		
					2B03h	00h	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		

Table 6.1.1 Instruction Code (Continued)

NO	Instruction	ACT	R/W	Address		Parameter										Function
				Others	MDDI	MDDI[15:8]	D7	D6	D5	D4	D3	D2	D1	D0		
28	RAMWR	Dir	W	2Ch	x	00h	D7	D6	D5	D4	D3	D2	D1	D0	Memory write	
29	RAMRD	Dir	R	2Eh	2E00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Memory read	
30	PTLAR	DVS	W	30h	3000h	00h	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	Partial start/end address set PSL[15:0]: partial start address PEL[15:0]: partial end address	
					3001h	00h	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0		
					3002h	00h	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8		
					3003h	00h	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0		
31	SCRLAR	DVS	W	33h	3300h	00h	TFA[15:8]								Scroll Area Set Top Fixed Area Vertical Scroll Area Bottom Fixed Area	
					3301h	00h	TFA[7:0]									
					3302h	00h	VSA[15:8]									
					3303h	00h	VSA[7:0]									
					3304h	00h	BFA[15:8]									
3305h	00h	BFA[7:0]														
32	TEOFF	DVS	W	34h	3400h	No Parameter										Tearing effect line off
33	TEON	DVS	W	35h	3500h	00h	-	-	-	-	-	-	M	Tearing effect mode set & on		
34	MADCTL	Cnd2	W	36h	X	X	MY	MX	MV	ML	RGB	MH	RSMX	RSMY	Memory data access control	
				X	3600h	00h	0	0	0	ML	RGB	MH				
35	VSCSAD	DVS	W	37h	3700h	00h	SSA[15:8]								Scroll Start Address of RAM	
					3701h	00h	SSA[7:0]									
36	IDMOFF	DVS	W	38h	3800h	No Parameter										Idle mode off
37	IDMON	DVS	W	39h	3900h	No Parameter										Idle mode on
38	COLMOD	Dir	W	3Ah	X	X	VIPF3	VIPF2	VIPF1	VIPF0	IFPF3	IFPF2	IFPF1	IFPF0	Interface pixel format	
39	RAMWRC	Dir	W	3Ch	X	X	D7	D6	D5	D4	D3	D2	D1	D0	Memory write Continue	
40	RAMRDC	Dir	R	3Eh	X	X	D7	D6	D5	D4	D3	D2	D1	D0	Memory read Continue	
41	STESL	DVS	W	44h	4400h	00h	N15	N14	N13	N12	N11	N10	N9	N8	Set tearing effect scan line	
					4401h	00h	N7	N6	N5	N4	N3	N2	N1	N0		
42	GSL	Dir	R	45h	4500h	00h	N15	N14	N13	N12	N11	N10	N9	N8	Get scan line	
					4501h	00h	N7	N6	N5	N4	N3	N2	N1	N0		
43	WRDISBV	DVS	W	51h	5100h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	Write display brightness	
44	RDDISBV	Dir	R	52h	5200h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	Read display brightness value	
45	WRCTRLD	DVS	W	53h	5300h	00h	-	-	BCTRL	-	DD	BL	-	-	Write control display	
46	RDCTRLD	Dir	R	54h	5400h	00h	-	-	BCTRL	-	DD	BL	-	-	Read control display value	
47	WRCABC	DVS	W	55h	5500h	00h	-	-	-	-	-	-	CABC1	CABC0	Write CABC	
48	RDCABC	Dir	R	56h	5600h	00h	-	-	-	-	-	-	CABC1	CABC0	Read CABC	
49	WRCABCMB	DVS	W	5Eh	5E00h	00h	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	Write CABC minimum brightness	
50	RDCABCMB	Dir	R	5Fh	5F00h	00h	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	Read CABC minimum brightness	
51	RDABCSDR	Dir	R	68h		00h	BCSD1	BSCSD0	-	-	-	-	-	-	Read display self-diagnostic result	

Table 6.1.1 Instruction Code (Continued)

NO	Instruction	ACT	R/W	Address		Parameter									Function
				Others	MDDI	MDDI[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	
52	RDBWLB	Dir	R	70h	7000h	00h	Bkx1	Bkx0	Bky1	Bky0	Wx1	Wx0	Wy1	Wy0	Read Black/White low bit
53	RDBkx	Dir	R	71h	7100h	00h	Bkx9	Bkx8	Bkx7	Bkx6	Bkx5	Bkx4	Bkx3	Bkx2	Read Bkx
54	RDBky	Dir	R	72h	7200h	00h	Bky9	Bky8	Bky7	Bky6	Bky5	Bky4	Bky3	Bky2	Read Bky
55	RDWx	Dir	R	73h	7300h	00h	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2	Read Wx
56	RDWy	Dir	R	74h	7400h	00h	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2	Read Wy
57	RDRGLB	Dir	R	75h	7500h	00h	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy0	Read Red/Green low bit
58	RDRx	Dir	R	76h	7600h	00h	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	Read Rx
59	RDRy	Dir	R	77h	7700h	00h	Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2	Read Ry
60	RDGx	Dir	R	78h	7800h	00h	Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2	Read Gx
61	RDGy	Dir	R	79h	7900h	00h	Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2	Read Gy
62	RDBALB	Dir	R	7Ah	7A00h	00h	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay0	Read Blue/AColor low bit
63	RDBx	Dir	R	7Bh	7B00h	00h	Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2	Read Bx
64	RDBy	Dir	R	7Ch	7C00h	00h	By9	By8	By7	By6	By5	By4	By3	By2	Read By
65	RDAX	Dir	R	7Dh	7D00h	00h	Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2	Read Ax
66	RDAY	Dir	R	7Eh	7E00h	00h	Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	Ay3	Ay2	Read Ay
67	RDDDBS	Dir	R	A1h	A100h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read DDB start
					A101h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
					A102h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	
					A103h	00h	ID417	ID416	ID415	ID414	ID413	ID412	ID411	ID410	
					A104h	00h	ID427	ID426	ID425	ID424	ID423	ID422	ID421	ID420	
					A105h	00h	ID437	ID436	ID435	ID434	ID433	ID432	ID431	ID430	
					A106h	00h	1	1	1	1	1	1	1	1	1
68	RDDDBC	Dir	R	A8h	X	X	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read DDB continue
					X	X	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
					X	X	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	
					X	X	ID417	ID416	ID415	ID414	ID413	ID412	ID411	ID410	
					X	X	ID427	ID426	ID425	ID424	ID423	ID422	ID421	ID420	
					X	X	ID437	ID436	ID435	ID434	ID433	ID432	ID431	ID430	
					X	X	1	1	1	1	1	1	1	1	1
69	RDFCS	Dir	R	AAh	AA00h	00h	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0	Read First Checksum
70	RDCCS	Dir	R	AFh	AF00h	00h	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0	Read Continue Checksum
71	RDID1	Dir	R	DAh	DA00h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read ID1
72	RDID2	Dir	R	DBh	DB00h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	Read ID2
73	RDID3	Dir	R	DCh	DC00h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	Read ID3

Notes:

1. The following description is indicates the executing time of instructions.

No.	Symbol	Executing Time	
1	Dir (Direct)	At the received a completed instruction and parameter	
2	DVS (Display Vertical Sync.)	Synchronized with the next frame	
3	DHS (Display Horizontal Sync.)	Synchronized with the next line	
4	Cnd1 (By Conditional 1)	State	Executing time
		When Sleep In	Dir
		Other	DHS
5	Cnd2 (By Conditional 2)	State	Executing time
		B7, B6, B5	Dir
		B4, B3, B2, B1, B0	DVS

2. Parameters of the command are stores onto registers when the last parameter of the command has been received. Also, parameters of the command are not stored onto registers if there has been happen a break. See more information on the section "5.5 DATA TRANSFER RECOVERY". This note is valid when a number of the parameters is equal or less than 32.

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6.1.1 NOP (00h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
NOP	Write	00h	0000h	No Parameter								

NOTE: "-" Don't care

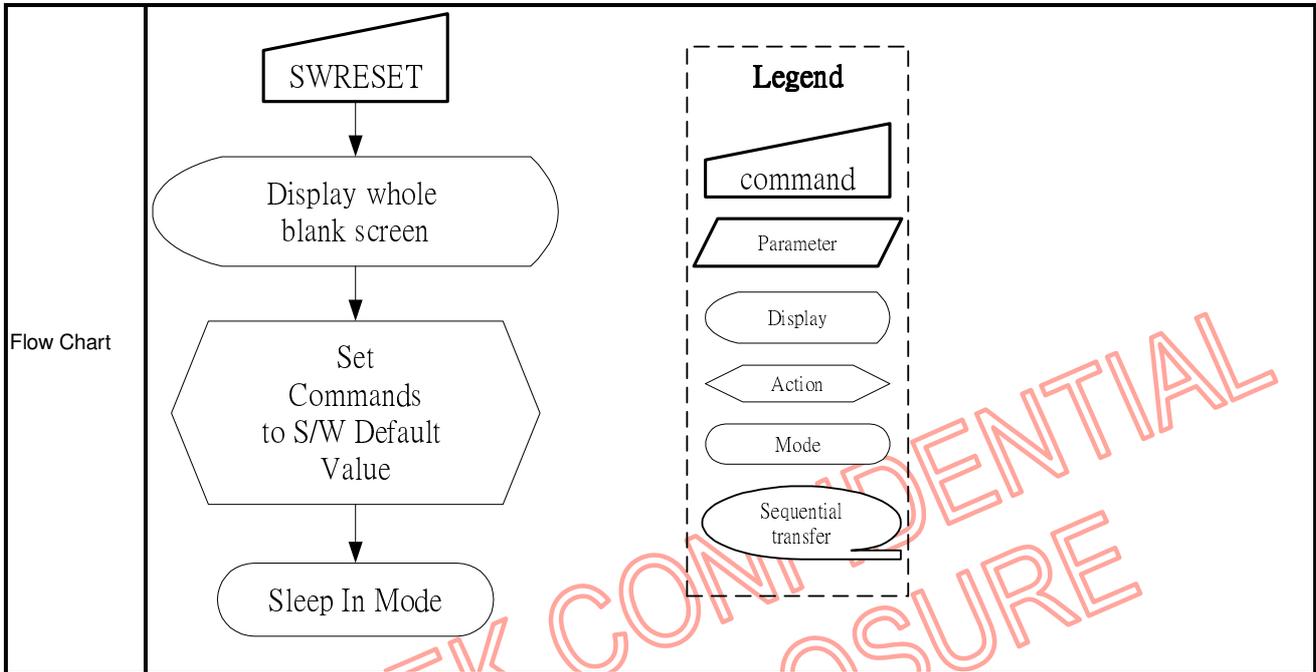
Description	This command is empty command. It does not have effect on the display module. However it can be used to terminate RAM data write or read as described in RAMWR (Memory Write), RAMRD (Memory Read) and parameter write commands.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability												
	Normal Mode On, Idle Mode Off, Sleep Out	Yes												
	Normal Mode On, Idle Mode On, Sleep Out	Yes												
	Partial Mode On, Idle Mode Off, Sleep Out	Yes												
	Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>S/W Reset</td> <td>N/A</td> </tr> <tr> <td>H/W Reset</td> <td>N/A</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A				
	Status	Default Value												
	Power On Sequence	N/A												
	S/W Reset	N/A												
H/W Reset	N/A													
Flow Chart	-													

6.1.2 SWRESET: Software Reset (01h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
SWRESET	Write	01h	0100h	No Parameter								

NOTE: "-" Don't care

Description	<p>When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and the display is blank immediately.</p> <p><i>Note: The Frame Memory contents keep or not depends on RAMKP bit on 0xC1 command.</i></p>													
Restriction	<p>It will be necessary to wait 5msec before sending new command following software reset.</p> <p>The display module loads all display suppliers' factory default values to the registers during 5msec.</p> <p>If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command.</p> <p>Software Reset command cannot be sent during Sleep Out sequence.</p>													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
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Status	Default Value													
Power On Sequence	N/A													
S/W Reset	N/A													
H/W Reset	N/A													



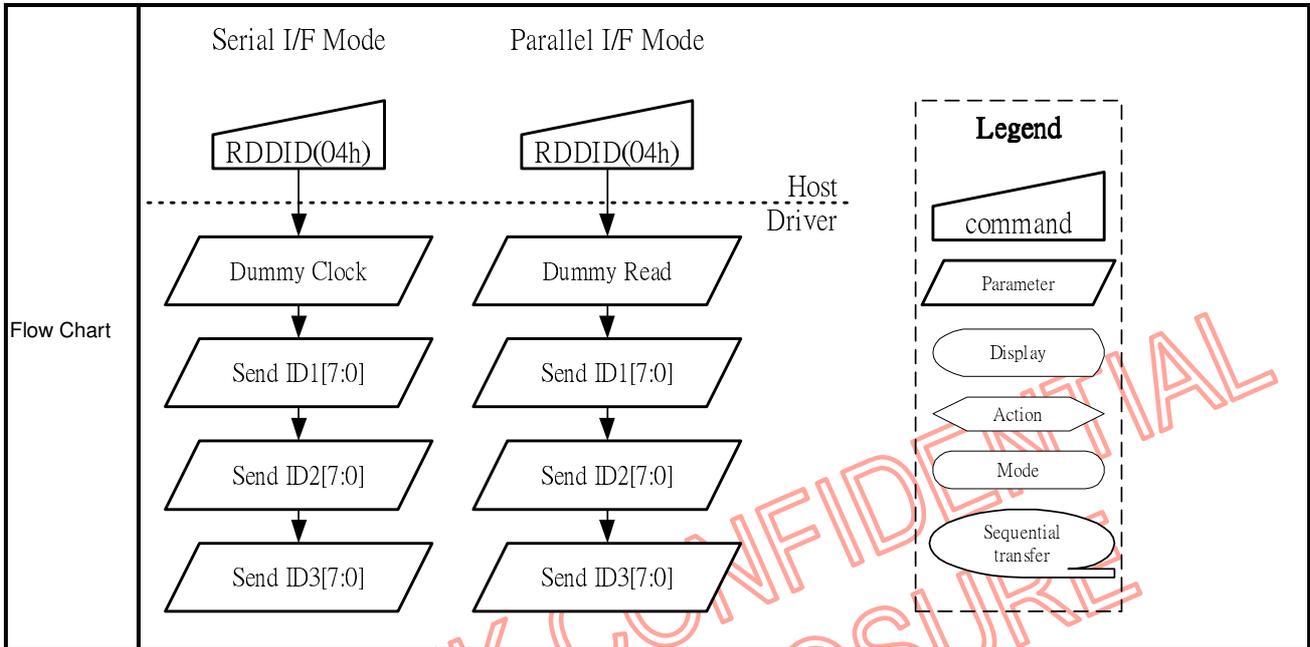
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6.1.3 RDDID: Read Display ID (04h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDID	Read	04h	0400h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10
			0401h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20
			0402h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30

NOTE: "-" Don't care

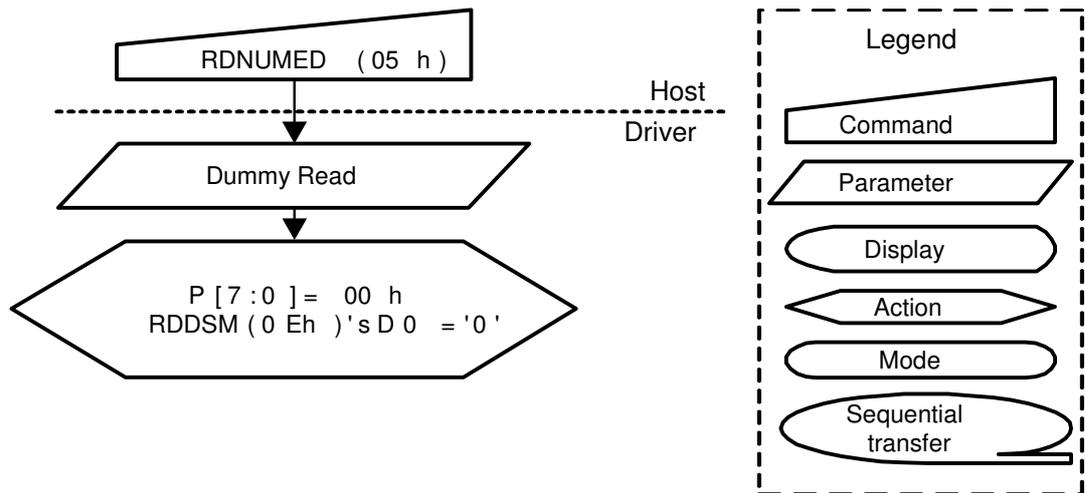
Description	<p>This read byte returns 24-bit display identification information. The 1st parameter is Dummy Read. The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID. The 3rd parameter (ID27 to ID20): LCD module/driver version ID. The 4th parameter (ID37 to UD30): LCD module/driver ID. <i>NOTE: Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.</i></p>																																						
Restriction	-																																						
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																										
Status	Availability																																						
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																																						
Sleep In	Yes																																						
Default	<p>If ID1/ID2/ID3 OTP are not yet programmed:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="3">Default Value</th> </tr> <tr> <th>ID1</th> <th>ID2</th> <th>ID3</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> <td>00h</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> <td>00h</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> <td>00h</td> <td>00h</td> </tr> </tbody> </table> <p>If ID1/ID2/ID3 OTP were programmed:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="3">Default Value</th> </tr> <tr> <th>ID1</th> <th>ID2</th> <th>ID3</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>(OTP value)</td> <td>(OTP value)</td> <td>(OTP value)</td> </tr> <tr> <td>S/W Reset</td> <td>(OTP value)</td> <td>(OTP value)</td> <td>(OTP value)</td> </tr> <tr> <td>H/W Reset</td> <td>(OTP value)</td> <td>(OTP value)</td> <td>(OTP value)</td> </tr> </tbody> </table>	Status	Default Value			ID1	ID2	ID3	Power On Sequence	00h	00h	00h	S/W Reset	00h	00h	00h	H/W Reset	00h	00h	00h	Status	Default Value			ID1	ID2	ID3	Power On Sequence	(OTP value)	(OTP value)	(OTP value)	S/W Reset	(OTP value)	(OTP value)	(OTP value)	H/W Reset	(OTP value)	(OTP value)	(OTP value)
Status	Default Value																																						
	ID1	ID2	ID3																																				
Power On Sequence	00h	00h	00h																																				
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H/W Reset	(OTP value)	(OTP value)	(OTP value)																																				



6.1.4 RDNUMED: Read Number of Errors on DSI (05h)

Inst / Para	R/W	Address			Parameter							
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDNUMED	Read	05h	X	X	P7	P6	P5	P4	P3	P2	P1	P0

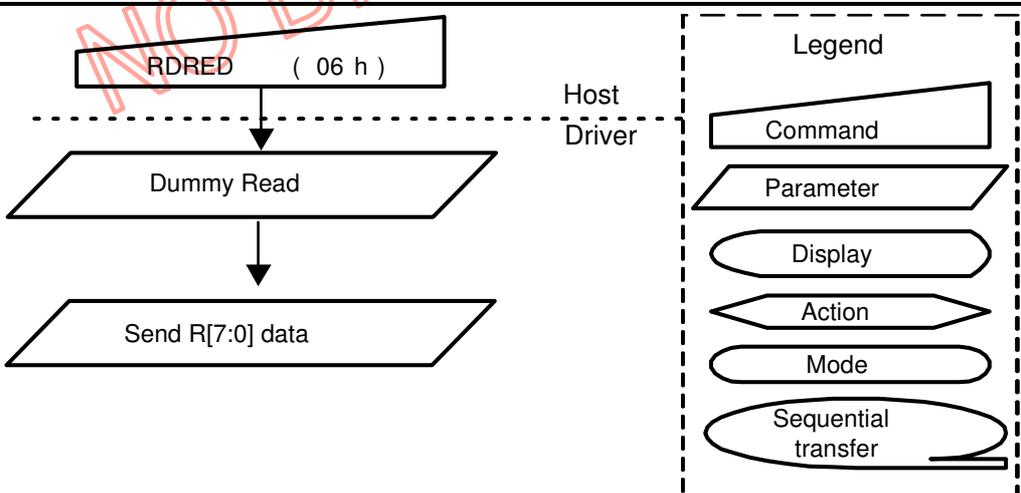
NOTE: "-" Don't care

Description	<p>The first parameter is telling a number of the parity errors on DSI. The more detailed description of the bits is below. P[6..0] bits are telling a number of the parity errors. P[7] is set to "1" if there is overflow with P[6..0] bits. P[7..0] bits are set to "0"s (as well as RDDSM(0Eh)'s D0 are set "0" at the same time) after there is sent the first parameter information (= The read function is completed). See also section "Acknowledge with Error Report (AwER)" and command RDDSM 0Eh. This command is used for MIPI DSI only. It is no function for others interface operation.</p>												
Restriction	-												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												
Flow Chart													

6.1.5 RDRED: Read Red Color (06h)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDRED	Read	06h	X	X	R7	R6	R5	R4	R3	R2	R1	R0	

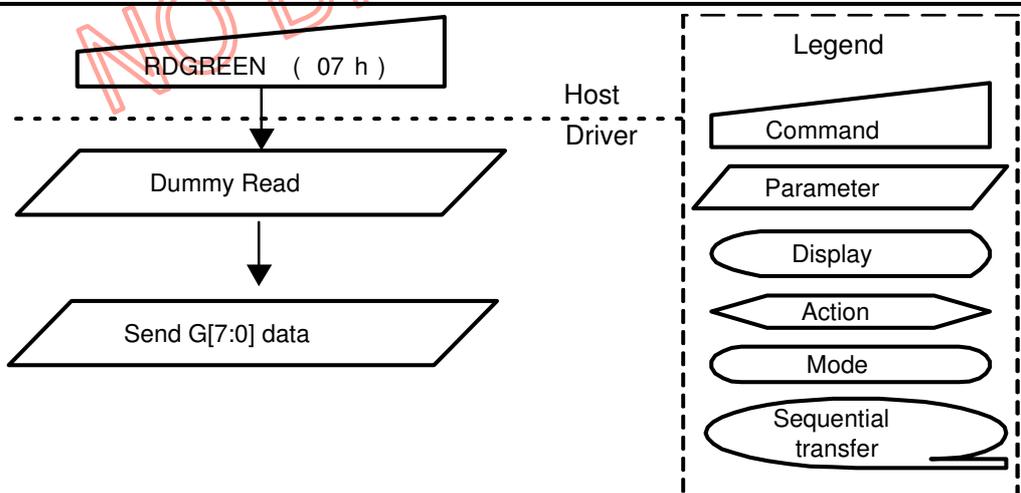
NOTE: “-“ Don't care

Description	<p>This command returns the red component value of the first pixel in the active frame. Only the relevant bits are used according to pixel format, unused bits are set to “0”.</p> <p>-16-bit format: R4 is MSB and R0 is LSB. R7, R6 and R5 are set to “0”.</p> <p>-18-bit format: R5 is MSB and R0 is LSB. R7 and R6 are set to “0”.</p> <p>-24-bit format: R7 is MSB and R0 is LSB.</p>								
Restriction	-								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Sleep Out	Yes	Partial Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability								
Normal Mode On, Sleep Out	Yes								
Partial Mode On, Sleep Out	Yes								
Sleep In	Yes								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value								
Power On Sequence	00h								
S/W Reset	00h								
H/W Reset	00h								
Flow Chart									

6.1.6 RDGREEN: Read Green Color (07h)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDGREEN	Read	07h	X	X	G7	G6	G5	G4	G3	G2	G1	G0	

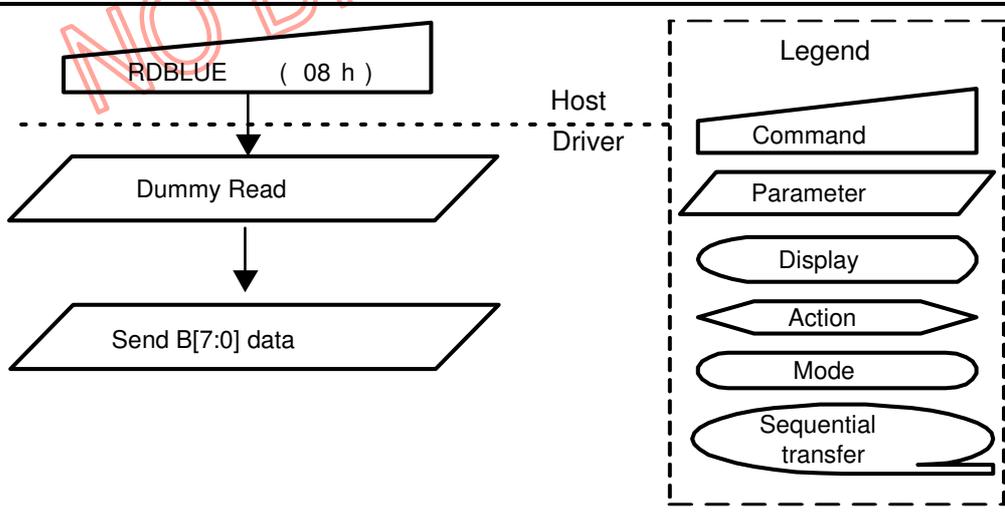
NOTE: "-“ Don't care

Description	<p>This command returns the green component value of the first pixel in the active frame. Only the relevant bits are used according to pixel format, unused bits are set to "0".</p> <p>-16-bit format: G5 is MSB and G0 is LSB. G7 and G6 are set to "0".</p> <p>-18-bit format: G5 is MSB and G0 is LSB. G7 and G6 are set to "0".</p> <p>-24-bit format: G7 is MSB and G0 is LSB.</p>								
Restriction	-								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Sleep Out	Yes	Partial Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability								
Normal Mode On, Sleep Out	Yes								
Partial Mode On, Sleep Out	Yes								
Sleep In	Yes								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value								
Power On Sequence	00h								
S/W Reset	00h								
H/W Reset	00h								
Flow Chart									

6.1.7 RDBLUE: Read Blue Color (08h)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDBLUE	Read	08h	X	X	B7	B6	B5	B4	B3	B2	B1	B0	

NOTE: "-“ Don't care

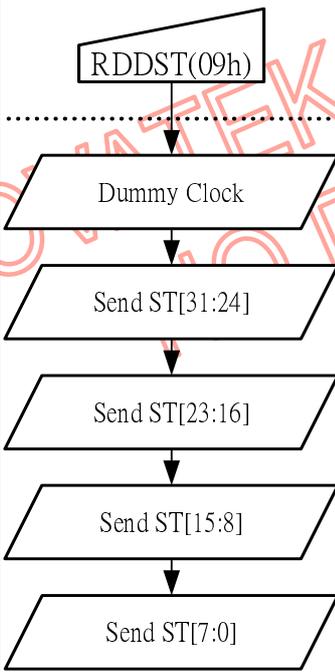
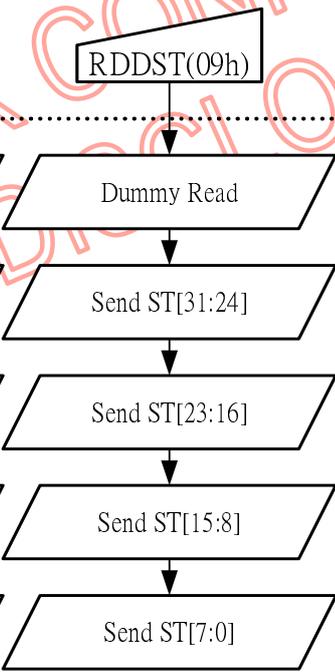
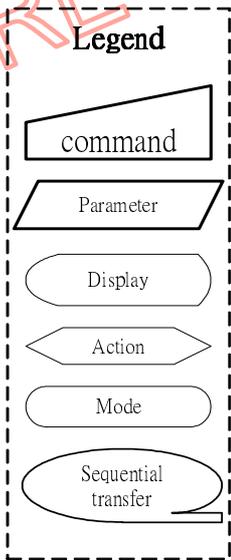
Description	<p>This command returns the blue component value of the first pixel in the active frame. Only the relevant bits are used according to pixel format, unused bits are set to "0".</p> <p>-16-bit format: B4 is MSB and R0 is LSB. B7, B6 and B5 are set to "0".</p> <p>-18-bit format: B5 is MSB and B0 is LSB. B7 and B6 are set to "0".</p> <p>-24-bit format: B7 is MSB and B0 is LSB.</p>								
Restriction	-								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Sleep Out	Yes	Partial Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability								
Normal Mode On, Sleep Out	Yes								
Partial Mode On, Sleep Out	Yes								
Sleep In	Yes								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value								
Power On Sequence	00h								
S/W Reset	00h								
H/W Reset	00h								
Flow Chart	 <p>The flow chart shows the sequence of operations for the RDBLUE command. It starts with the Host Driver sending the RDBLUE (08h) command. This is followed by a Dummy Read action, and then the data B[7:0] is sent. A legend defines symbols: Command (trapezoid), Parameter (parallelogram), Display (rounded rectangle), Action (arrowhead), Mode (oval), and Sequential transfer (oval with tail).</p>								

6.1.8 RDDST: Read Display Status (09h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDST	Read	09h	0900h	00h	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24
			0901h	00h	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16
			0902h	00h	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8
			0903h	00h	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0

NOTE: "-" Don't care

Description	This command indicates the current status of the display as described in the table below:		
	Bit	Description	Value
	ST31	Booster Voltage Status	"1" = Booster on, "0" = Off
	ST30	Row Address Order (MY)	"1" = Decrement, "0" = Increment
	ST29	Column Address Order (MX)	"1" = Decrement, "0" = Increment
	ST28	Row/Column Exchange (MV)	"1" = Row/column exchange (MV=1) "0" = Normal (MV=0)
	ST27	Vertical refresh Order (ML)	"1" = Decrement, "0" = Increment
	ST26	RGB/BGR Order (RGB)	"1" = BGR, "0" = RGB
	ST25	Horizontal refresh Order (MH)	"0"
	ST24	Not Used	"0"
	ST23	Not Used	"0"
	ST22-20	Interface Color Pixel Format Definition	"0101" = 16-bit / pixel "0110" = 18-bit / pixel "0111" = 24-bit / pixel "Others" = Not Defined
	ST19	Idle Mode On/Off	"1" = On, "0" = Off
	ST18	Partial Mode On/Off	"1" = On, "0" = Off
	ST17	Sleep In/Out	"1" = Out, "0" = In
	ST16	Display Normal Mode On/Off	"1" = Normal display on, "0" = Normal display off
	ST15	Vertical Scrolling Status	"1" = Scroll on, "0" = Scroll off
	ST14	Not Used	"0"
	ST13	Inversion Status	"1" = On, "0" = Off
	ST12	All Pixels On	"0" = Normal Display, "1" = White Display
	ST11	All Pixels Off	"0" = Normal Display, "1" = Black Display
	ST10	Display On/Off	"1" = On, "0" = Off
	ST9	Tearing effect line on/off	"1" = On, "0" = Off
	ST8-6	Gamma Curve Selection	"000" = GC0 "001" = GC1 "010" = GC2 "011" = GC3 "100" = GC4 "101" to "111" = Not defined
	ST5	Tearing effect line mode	"0" = mode1, "1" = mode2
	ST4	Not Used	"0"
	ST3	Not Used	"0"
	ST2	Not Used	"0"
	ST1	Not Used	"0"
	ST0	Not Used	"0"
Restriction	-		

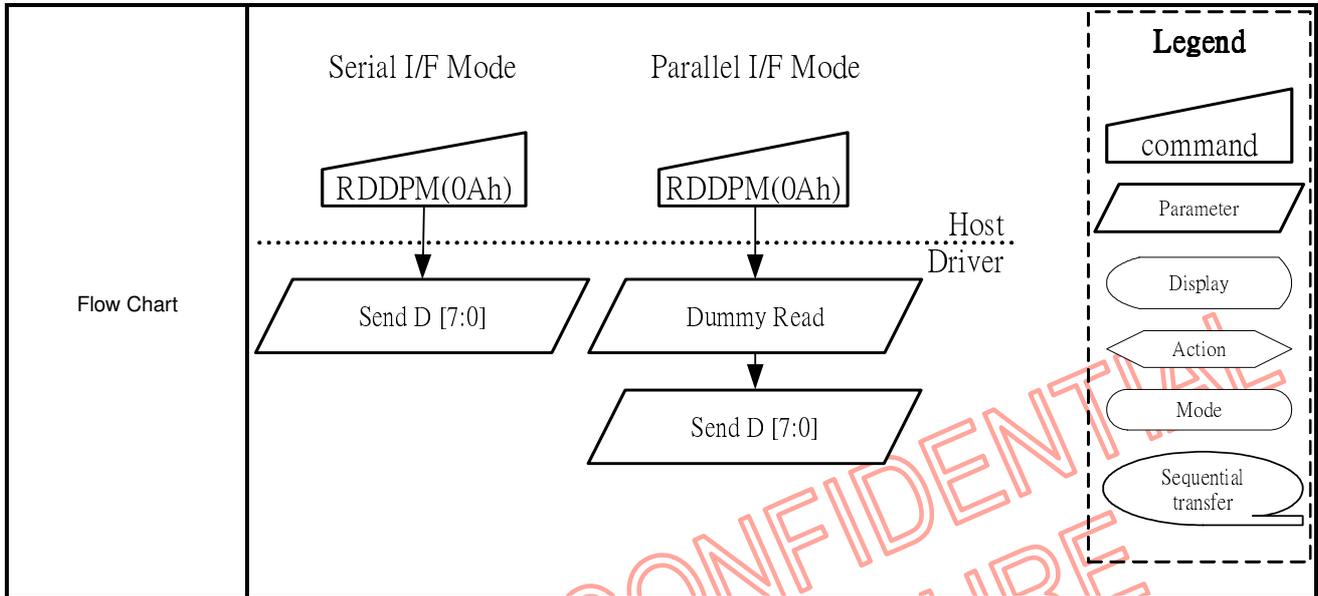
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value (ST31 to ST0):</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>0000 0000_0111 0001_0000 0000_0000 0000</td> </tr> <tr> <td>S/W Reset</td> <td>0xxx xxx0_0xxx 0001_0000 0000_0000 0000</td> </tr> <tr> <td>H/W Reset</td> <td>0000 0000_0111 0001_0000 0000_0000 0000</td> </tr> </tbody> </table>	Status	Default Value (ST31 to ST0):	Power On Sequence	0000 0000_0111 0001_0000 0000_0000 0000	S/W Reset	0xxx xxx0_0xxx 0001_0000 0000_0000 0000	H/W Reset	0000 0000_0111 0001_0000 0000_0000 0000				
Status	Default Value (ST31 to ST0):												
Power On Sequence	0000 0000_0111 0001_0000 0000_0000 0000												
S/W Reset	0xxx xxx0_0xxx 0001_0000 0000_0000 0000												
H/W Reset	0000 0000_0111 0001_0000 0000_0000 0000												
Flow Chart	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>Serial I/F Mode</p>  </div> <div style="text-align: center;"> <p>Parallel I/F Mode</p>  </div> </div> <div style="margin-top: 20px;"> <p>Host Driver</p>  </div>												

6.1.9 RDDPM: Read Display Power Mode (0Ah)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDPM	Read	0Ah	0A00h	00h	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description	This command indicates the current status of the display as described in the table below:	
	Bit	Description
	D7	Booster voltage status
	D6	Idle mode on/off
	D5	Partial mode on/off
	D4	Sleep in/out
	D3	Display normal mode on/off
	D2	Display on/off
	D1	Not used
D0	Not used	
Restriction	-	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value (D7 to D0)
	Power On Sequence	0000_1000 (08h)
	S/W Reset	0000_1000 (08h)
	H/W Reset	0000_1000 (08h)



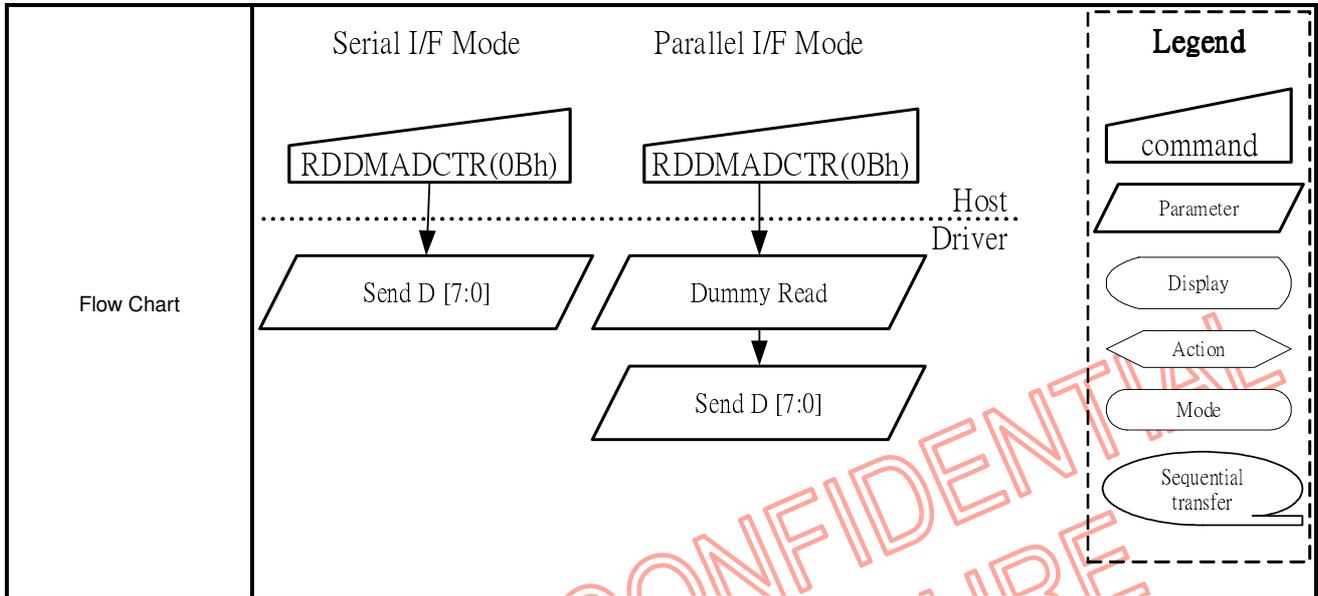
NOVATEK CONFIDENTIAL
NO DISCLOSURE

6.1.10 RDDMADCTL: Read Display MADCTL (0Bh)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDMADCTL	Read	0Bh	0B00h	00h	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description	This command indicates the current status of the display as described in the table below:	
	Bit	Description
	D7	Row Address Order
	D6	Column Address Order
	D5	Row/Column Order (MV)
	D4	Vertical fresh Order (ML)
	D3	RGB/BGR Order
	D2	Horizontal fresh Order (MH)
	D1	Flip horizontal (RSMX)
D0	Flip vertical (RSMY)	
Value	"1"=Decrement, "0"=Increment "1"=Decrement, "0"=Increment "1"=Row/column exchange (MV=1) "0"=Normal (MV=0) "1"=Decrement, "0"=Increment "1"=BGR, "0"=RGB "0" = Increment , "1" = Decrement "0" = Normal , "1" = Horizontal flip "0" = Normal , "1" = Vertical flip	
Restriction	-	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value (D7 to D0)
	Power On Sequence	0000_0000 (00h)
	S/W Reset	No change



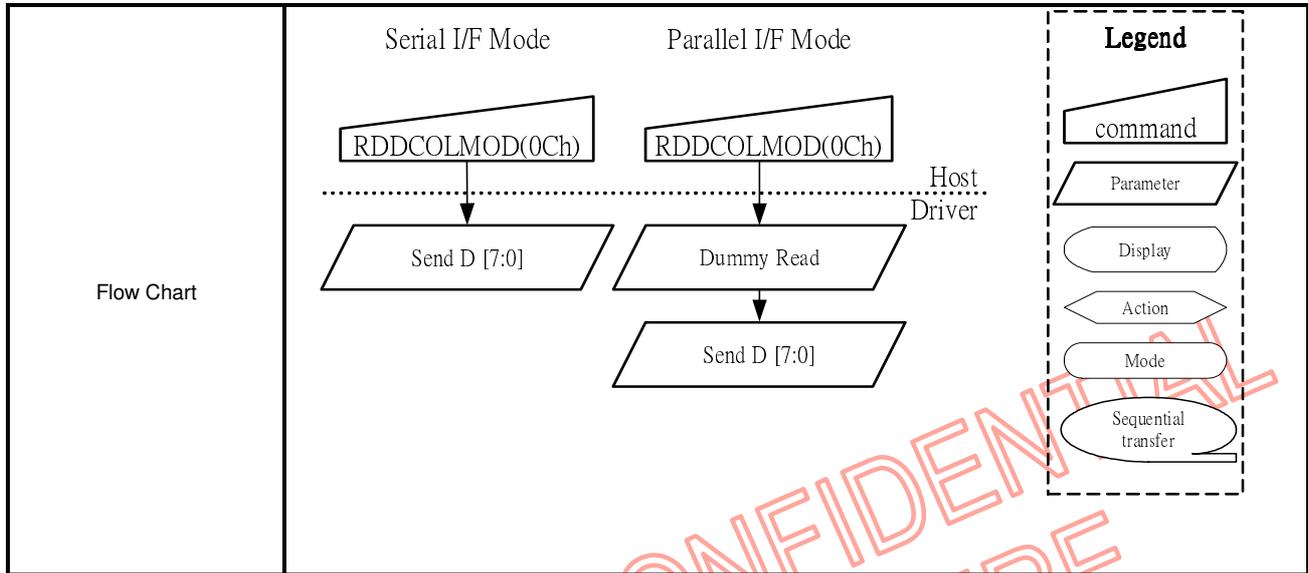
NOVATEK CONFIDENTIAL
NO DISCLOSURE

6.1.11 RDDCOLMOD: Read Display Pixel Format (0Ch)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDCOLMOD	Read	0Ch	0C00h	00h	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description	This command indicates the current status of the display as described in the table below:		
	Bit	Description	Value
	D7-4	RGB Interface Color Format	"0100" = 8-bit / pixel "0101" = 16-bit / pixel "0110" = 18-bit / pixel "0111" = 24-bit / pixel "Others" = Not Defined
D3-0	Control Interface Color Format	"0101" = 16-bit / pixel "0110" = 18-bit / pixel "0111" = 24-bit / pixel "Others" = Not Defined	
Restriction	-		
Register Availability	Status		Availability
	Normal Mode On, Idle Mode Off, Sleep Out		Yes
	Normal Mode On, Idle Mode On, Sleep Out		Yes
	Partial Mode On, Idle Mode Off, Sleep Out		Yes
	Partial Mode On, Idle Mode On, Sleep Out		Yes
	Sleep In		Yes
Default	Status		Default Value
	Power On Sequence		0111_0111 (77h)
	S/W Reset		No Change
	H/W Reset		0111_0111 (77h)



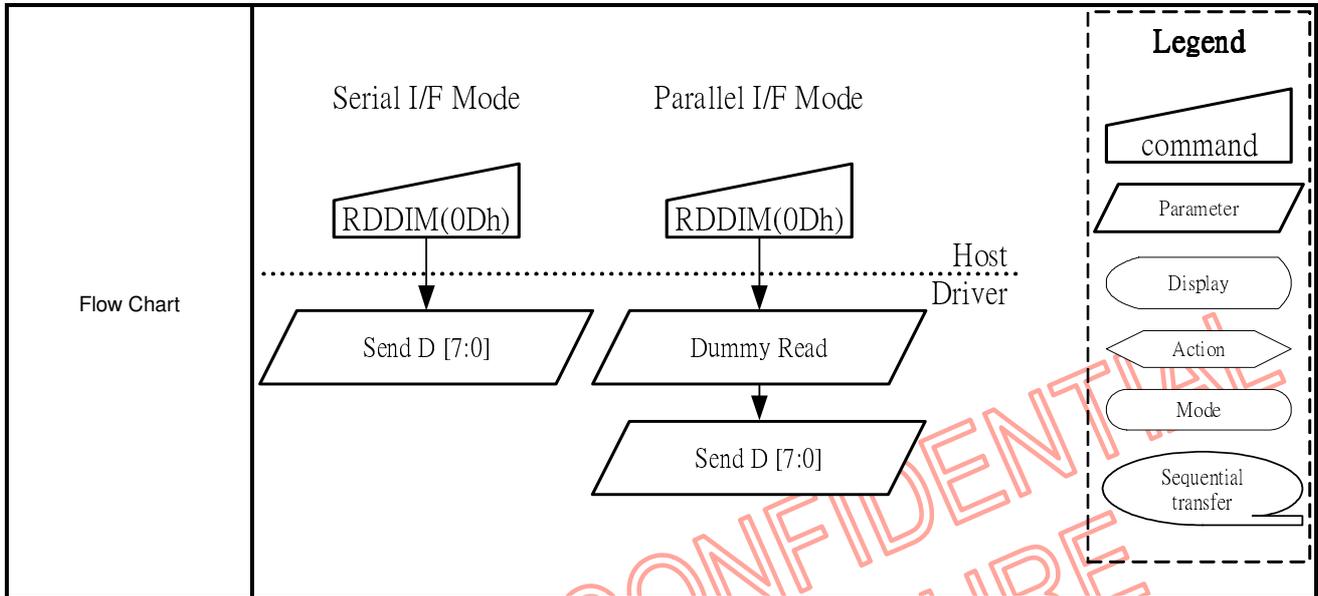
NOVATEK CONFIDENTIAL
NO DISCLOSURE

6.1.12 RDDIM: Read Display Image Mode (0Dh)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDIM	Read	0Dh	0D00h	00h	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description	This command indicates the current status of the display as described in the table below:													
	Bit	Description												
	D7	Vertical Scrolling On/Off												
	D6	Horizontal Scrolling On/Off												
	D5	Inversion On/Off												
	D4	All Pixels On												
	D3	All Pixels Off												
D2 –0	Gamma Curve Selection													
Value	"1" = Vertical Scrolling is On, "0" = Vertical Scrolling is Off. "0" (Not used) "1" = Inversion is On, "0" = Inversion is Off "0" = Normal Display, "1" = White Display "0" = Normal Display, "1" = Black Display "000" = GC0 "001" = GC1 "010" = GC2 "011" = GC3 "100" = GC4 "101" to "111" = Not defined													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability												
	Normal Mode On, Idle Mode Off, Sleep Out	Yes												
	Normal Mode On, Idle Mode On, Sleep Out	Yes												
	Partial Mode On, Idle Mode Off, Sleep Out	Yes												
	Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value (D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>0000_0000 (00h)</td> </tr> <tr> <td>S/W Reset</td> <td>0000_0000 (00h)</td> </tr> </tbody> </table>		Status	Default Value (D7 to D0)	Power On Sequence	0000_0000 (00h)	S/W Reset	0000_0000 (00h)						
	Status	Default Value (D7 to D0)												
	Power On Sequence	0000_0000 (00h)												
S/W Reset	0000_0000 (00h)													



Flow Chart

Serial I/F Mode

Parallel I/F Mode

Host
Driver

RDDIM(0Dh)

RDDIM(0Dh)

Send D [7:0]

Dummy Read

Send D [7:0]

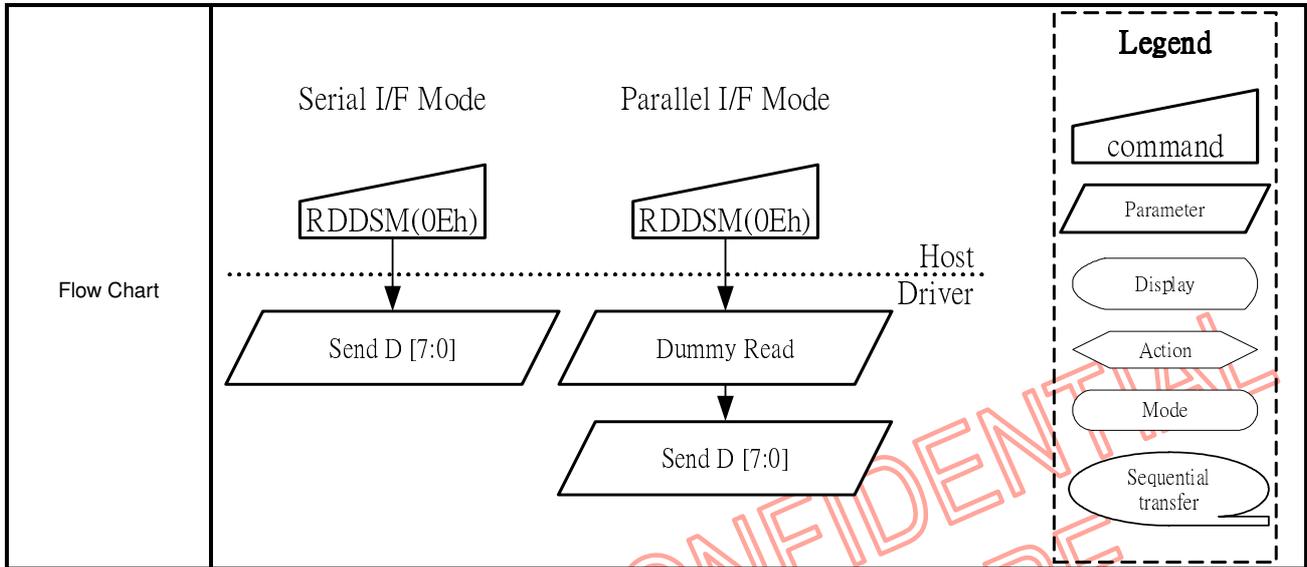
NOVATEK CONFIDENTIAL
NO DISCLOSURE

6.1.13 RDDSM: Read Display Signal Mode (0Eh)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDDSM	Read	0Eh	0E00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	

NOTE: "- " Don't care

Description	This command indicates the current status of the display as described in the table below:	
	Bit	Description
	D7	Tearing Effect Line On/Off
	D6	Tearing Effect Line Mode
	D5	Horizontal Sync. (HS, RGB I/F)On/Off
	D4	Vertical Sync. (VS, RGB I/F)On/Off
	D3	Pixel Clock (PCLK, RGB I/F)On/Off
	D2	Data Enable (DE, RGB I/F)On/Off
	D1	Not Defined
D0	Error on DSI	
Value		"1" = On, "0" = Off
Value		"1" = Mode 2, "0" = Mode 1
Value		"1" = HS bit is "1", "0" = HS bit is "0"
Value		"1" = VS bit is "1", "0" = VS bit is "0"
Value		"1" = PCLK line is On, "0" = PCLK line is Off
Value		"1" = DE bit is "1", "0" = DE bit is "0"
Value		Set to "0" (not used)
Value		"1" = Error, "0" = No Error
Note: Bit D5 to D2 indicate current status of the lines when this command has been sent.		
Restriction	-	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h



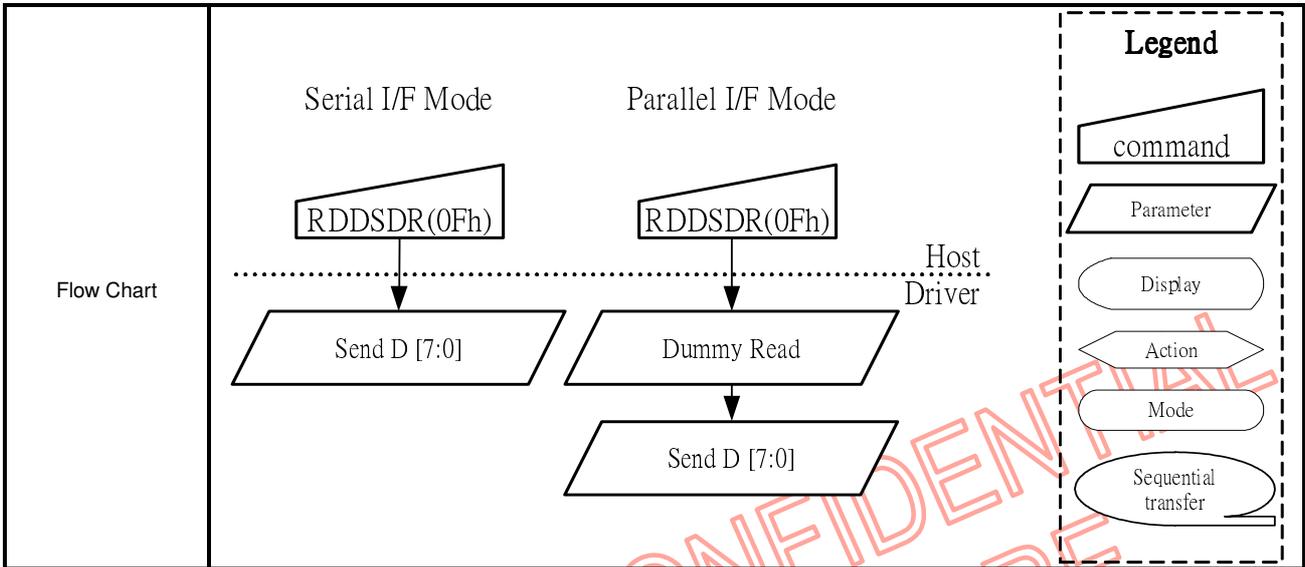
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NO DISCLOSURE

6.1.14 RDDSDR: Read Display Self-Diagnostic Result (0Fh)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDDSDR	Read	0Fh	0F00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	

NOTE: "-“ Don't care

Description	This command indicates the current status of the display as described in the table below:	
	Bit	Description
	D7	Register Loading Detection
	D6	Functionality Detection
	D5	Not Defined
	D4	Not Defined
	D3	Not Defined
	D2	Not Defined
	D1	Not Defined
D0	Not Defined	
Restriction	-	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes	
Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h

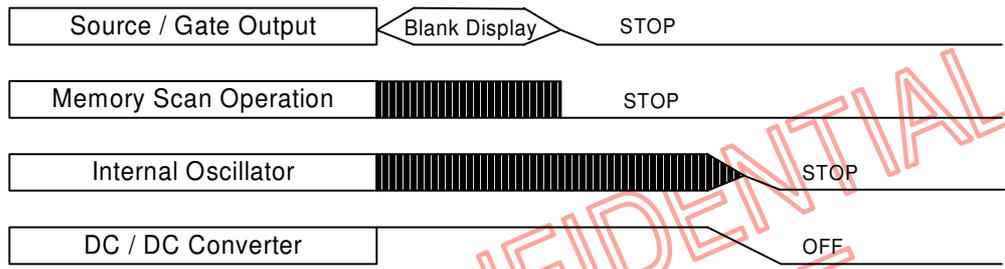


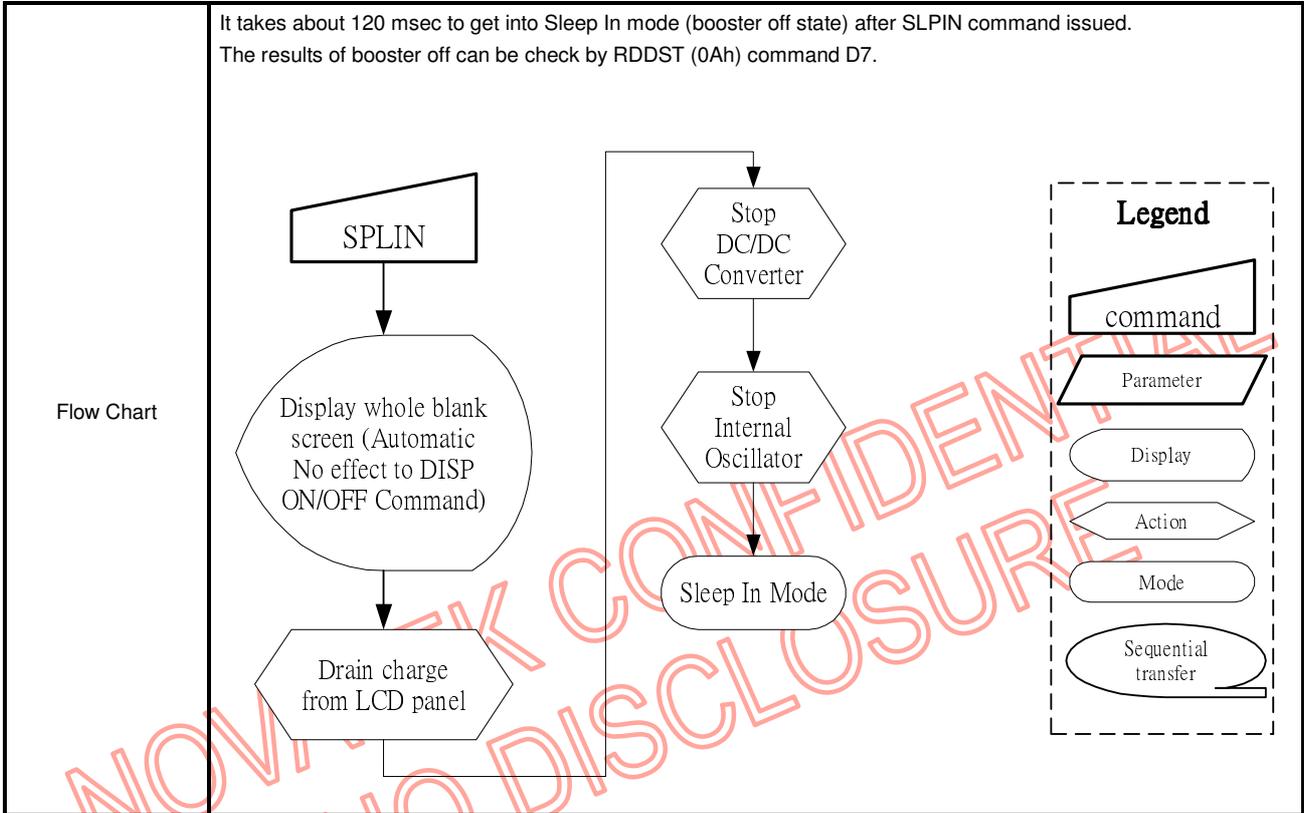
NOVATEK CONFIDENTIAL
NO DISCLOSURE

6.1.15 SLPIN: Sleep In (10h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
SLPIN	Write	10h	1000h	No Parameter								

NOTE: “-“ Don't care

Description	<p>This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.</p>  <p>Control Interface as well as memory and registers are still working and the memory keeps its contents. User can send PCLK, HS and VS information on RGB I/F for blank display after Sleep In command and this information is valid during 2 frames after Sleep In command if there is used Normal Mode On in Sleep Out-mode. Dimming function does not work when there is changing mode from Sleep Out to Sleep In. There is used an internal oscillator for blank display.</p>												
Restriction	<p>This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).</p> <p>It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.</p> <p>It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</p>												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep In Mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep In Mode</td> </tr> <tr> <td>H/W Reset</td> <td>Sleep In Mode</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Sleep In Mode	S/W Reset	Sleep In Mode	H/W Reset	Sleep In Mode				
Status	Default Value												
Power On Sequence	Sleep In Mode												
S/W Reset	Sleep In Mode												
H/W Reset	Sleep In Mode												

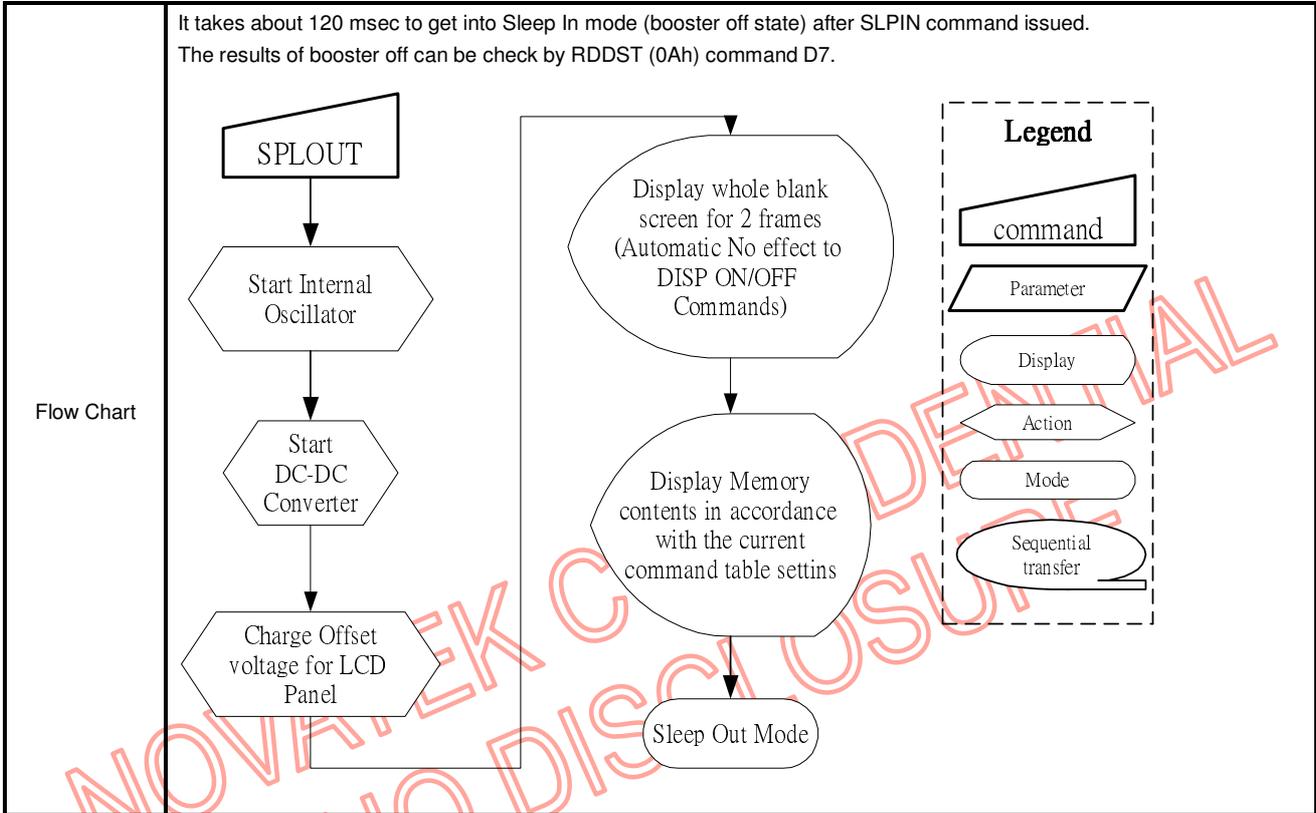


6.1.16 SLPOUT: Sleep Out (11h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
SLPOUT	Write	11h	1100h	No Parameter								

NOTE: “-“ Don't care

Description	<p>This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.</p>  <p>User can start to send PCLK, HS and VS information on RGB I/F before Sleep Out command and this information is valid at least 2 frames before Sleep Out command, if there is left Sleep In-mode to Sleep Out-mode in Normal Mode On. There is used an internal oscillator for blank display.</p>												
Restriction	<p>Sleep Out Mode can only be exit by the Sleep In Command (10h), SW reset or HW reset. It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. NT35410 loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the NT35410 is already Sleep Out –mode. NT35410 is doing self-diagnostic functions during this 5msec. See also section 5.12. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</p>												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep In Mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep In Mode</td> </tr> <tr> <td>H/W Reset</td> <td>Sleep In Mode</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Sleep In Mode	S/W Reset	Sleep In Mode	H/W Reset	Sleep In Mode				
Status	Default Value												
Power On Sequence	Sleep In Mode												
S/W Reset	Sleep In Mode												
H/W Reset	Sleep In Mode												



6.1.17 PTLON: Partial Display Mode On (12h)

Inst / Para	R/W	Address		Parameter							
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1
PTLON	Write	12h	1200h	No Parameter							

NOTE: "-" Don't care

Description	<p>This command turns on Partial mode. The partial mode window is described by the Partial Area command (30H)</p> <p>To leave Partial mode, the Normal Display Mode On command (13H) should be written.</p> <p>There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On.</p>												
Restriction	This command has no effect when Partial mode is active.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power-On Sequence</td> <td>Normal Mode On</td> </tr> <tr> <td>S/W Reset</td> <td>Normal Mode On</td> </tr> <tr> <td>H/W Reset</td> <td>Normal Mode On</td> </tr> </tbody> </table>	Status	Default Value	Power-On Sequence	Normal Mode On	S/W Reset	Normal Mode On	H/W Reset	Normal Mode On				
Status	Default Value												
Power-On Sequence	Normal Mode On												
S/W Reset	Normal Mode On												
H/W Reset	Normal Mode On												
Flow Chart	See Partial Area (30h)												

6.1.18 NORON: Normal Display Mode On (13h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
NORON	Write	13h	1300h	No Parameter								

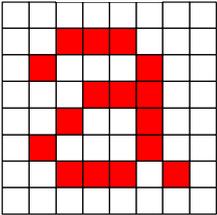
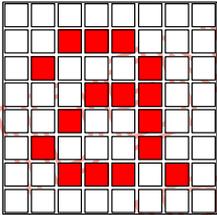
NOTE: "-" Don't care

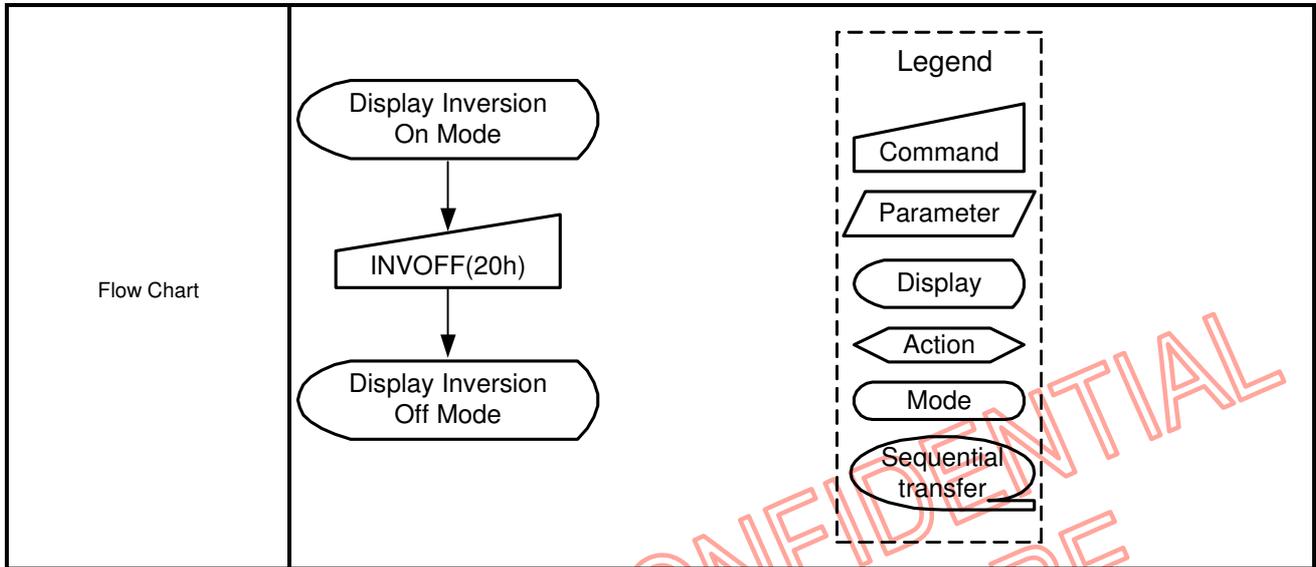
Description	<p>This command returns the display to normal mode. Normal display mode on means Partial mode off. Exit from NORON by the Partial mode On command (12h) There is no abnormal visual effect during mode change from Normal mode On to Partial mode On.</p>												
Restriction	<p>This command has no effect when Normal Display mode is active.</p>												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Default Value	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Default Value												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal Mode On</td> </tr> <tr> <td>S/W Reset</td> <td>Normal Mode On</td> </tr> <tr> <td>H/W Reset</td> <td>Normal Mode On</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Normal Mode On	S/W Reset	Normal Mode On	H/W Reset	Normal Mode On				
Status	Default Value												
Power On Sequence	Normal Mode On												
S/W Reset	Normal Mode On												
H/W Reset	Normal Mode On												
Flow Chart	<p>See Partial Area Definition Descriptions for details of when to use this command</p>												

6.1.19 INVOFF: Display Inversion Off (20h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
INVOFF	Write	20h	2000h	No Parameter								

NOTE: "-" Don't care

Description	<p>This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. (Example)</p> <div style="display: flex; align-items: center; justify-content: center;"> <div style="text-align: center;"> <p>Memory</p>  </div> <div style="margin: 0 20px; font-size: 2em;">→</div> <div style="text-align: center;"> <p>Display</p>  </div> </div>												
Restriction	<p>This command has no effect when module is already inversion off mode.</p>												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 60%;">Status</th> <th style="width: 40%;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 60%;">Status</th> <th style="width: 40%;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td style="text-align: center;">Display Inversion off</td> </tr> <tr> <td>S/W Reset</td> <td style="text-align: center;">Display Inversion off</td> </tr> <tr> <td>H/W Reset</td> <td style="text-align: center;">Display Inversion off</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Display Inversion off	S/W Reset	Display Inversion off	H/W Reset	Display Inversion off				
Status	Default Value												
Power On Sequence	Display Inversion off												
S/W Reset	Display Inversion off												
H/W Reset	Display Inversion off												

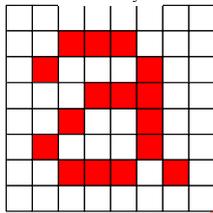
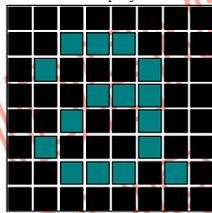


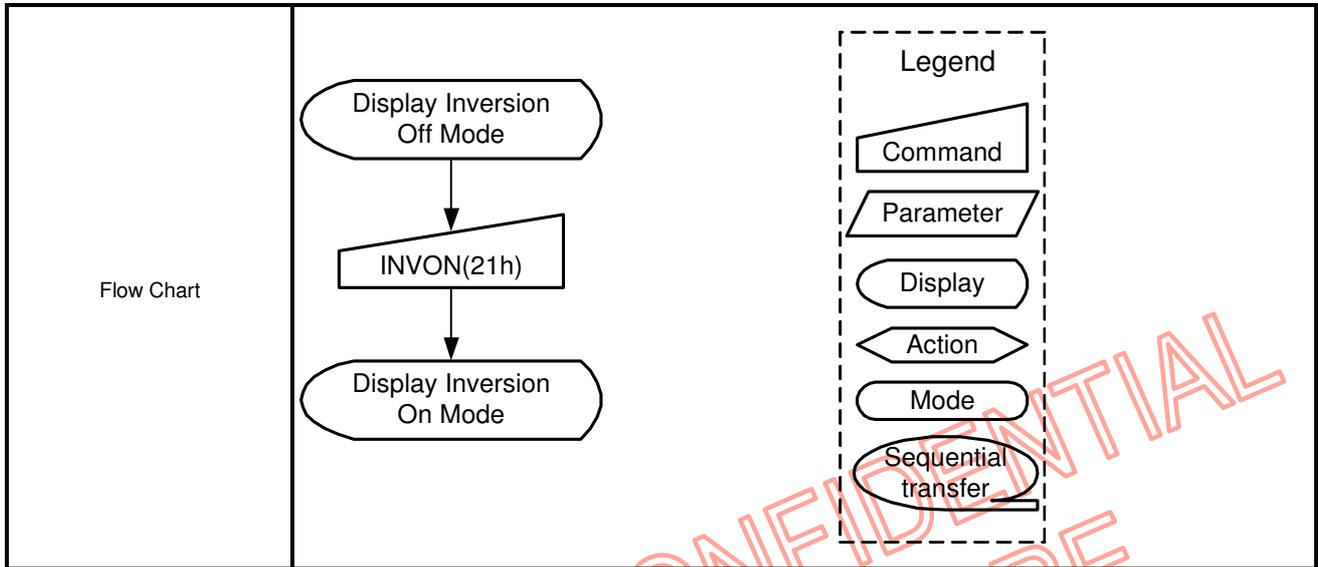
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NO DISCLOSURE

6.1.20 INVON: Display Inversion On (21h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
INVON	Write	21h	2100h	No Parameter								

NOTE: "-" Don't care

Description	<p>This command is used to enter display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. To exit from Display Inversion On, the Display Inversion Off command (20h) should be written. (Example)</p> <div style="display: flex; align-items: center; justify-content: center;"> <div style="text-align: center;"> <p>Memory</p>  </div> <div style="margin: 0 20px; font-size: 2em;">→</div> <div style="text-align: center;"> <p>Display</p>  </div> </div>												
Restriction	This command has no effect when module is already Inversion On mode.												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 60%;">Status</th> <th style="width: 40%;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 60%;">Status</th> <th style="width: 40%;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td style="text-align: center;">Display Inversion off</td> </tr> <tr> <td>S/W Reset</td> <td style="text-align: center;">Display Inversion off</td> </tr> <tr> <td>H/W Reset</td> <td style="text-align: center;">Display Inversion off</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Display Inversion off	S/W Reset	Display Inversion off	H/W Reset	Display Inversion off				
Status	Default Value												
Power On Sequence	Display Inversion off												
S/W Reset	Display Inversion off												
H/W Reset	Display Inversion off												

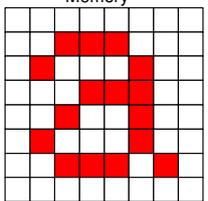
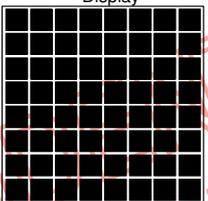


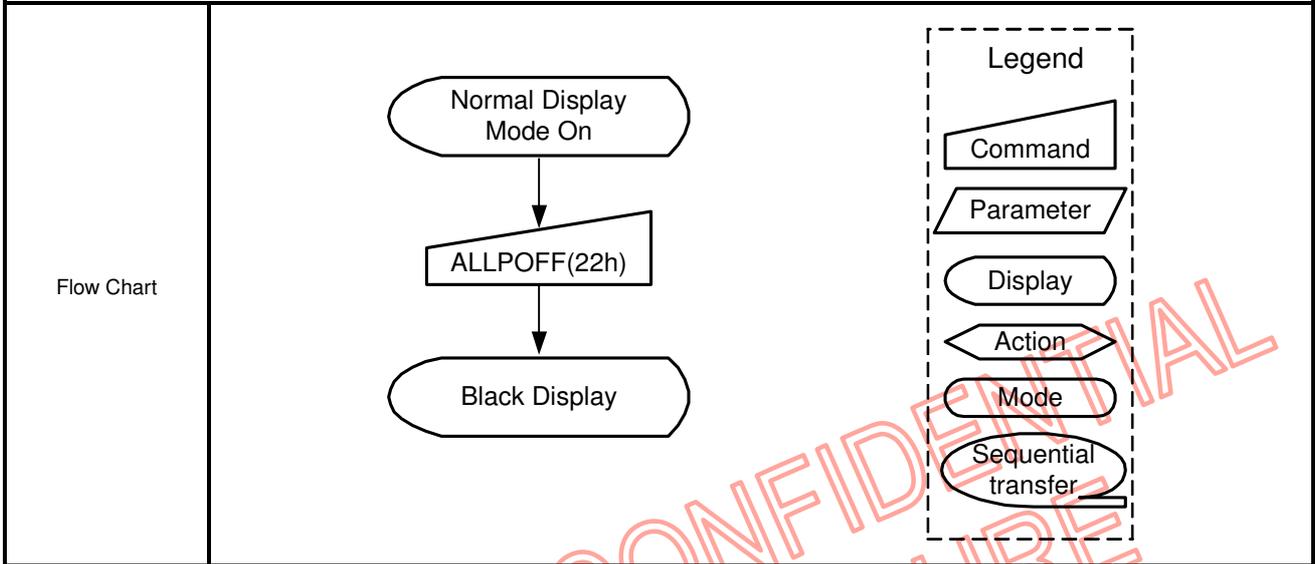
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6.1.21 ALLPOFF: All Pixel Off (22h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
ALLPOFF	Write	22h	2200h	No Parameter								

NOTE: “-“ Don't care

Description	<p>This command turns the display panel black in Sleep Out mode and a status of the Display On/Off register can be on or off.</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p> <div style="display: flex; align-items: center; justify-content: center;"> <div style="text-align: center;"> <p>Memory</p>  </div> <div style="margin: 0 20px; font-size: 2em;">→</div> <div style="text-align: center;"> <p>Display</p>  <p>(Example)</p> </div> </div> <p>“All Pixels On”, “Normal Display Mode On” or “Partial Mode On” commands are used to leave this mode. The display panel is showing the content of the frame memory after “Normal Display On” and “Partial Mode On” commands.</p>												
Restriction	This command has no effect when module is already inversion off mode.												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>All pixel off</td> </tr> <tr> <td>S/W Reset</td> <td>All pixel off</td> </tr> <tr> <td>H/W Reset</td> <td>All pixel off</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	All pixel off	S/W Reset	All pixel off	H/W Reset	All pixel off				
Status	Default Value												
Power On Sequence	All pixel off												
S/W Reset	All pixel off												
H/W Reset	All pixel off												

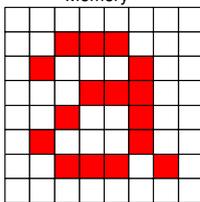
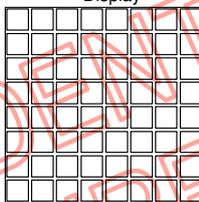


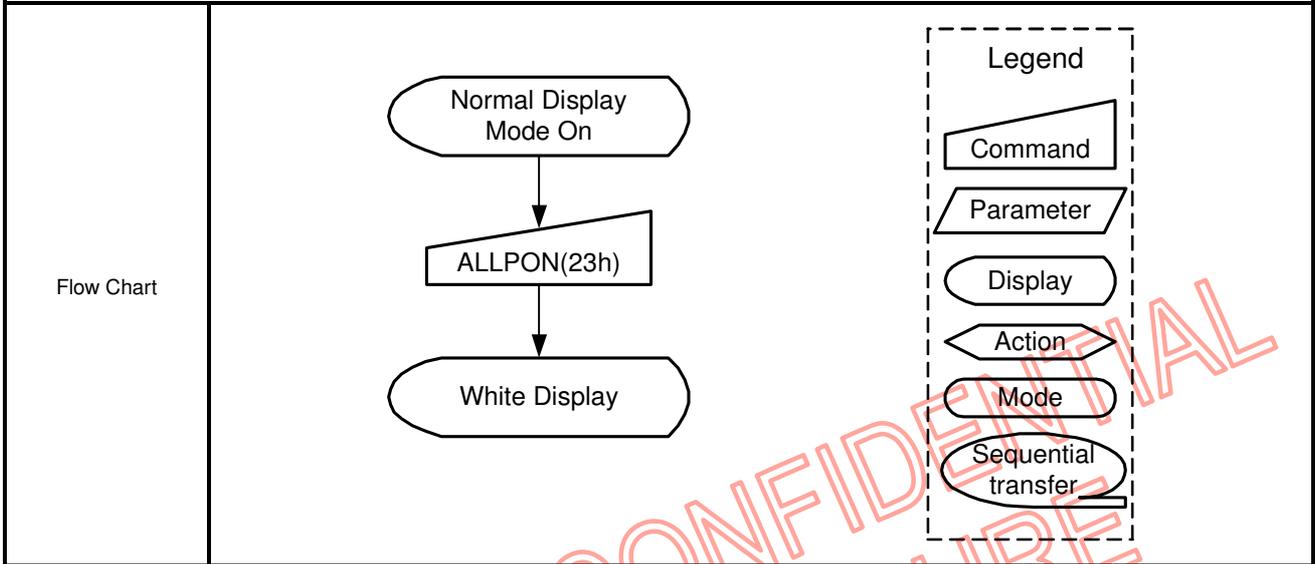
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6.1.22 ALLPON: All Pixel On (23h)

Inst / Para	R/W	Address		Parameter							
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1
ALLPON	Write	23h	2300h	No Parameter							

NOTE: "- " Don't care

Description	<p>This command turns the display panel white in Sleep Out mode and a status of the Display On/Off register can be on or off.</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p> <p>(Example)</p> <div style="display: flex; align-items: center; justify-content: center;"> <div style="text-align: center;"> <p>Memory</p>  </div> <div style="font-size: 2em; margin: 0 20px;">→</div> <div style="text-align: center;"> <p>Display</p>  </div> </div> <p>"All Pixels Off", "Normal Display Mode On" or "Partial Mode On" commands are used to leave this mode. The display panel is showing the content of the frame memory after "Normal Display On" and "Partial Mode On" commands.</p>												
Restriction	This command has no effect when module is already in all pixel on mode.												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>All pixel off</td> </tr> <tr> <td>S/W Reset</td> <td>All pixel off</td> </tr> <tr> <td>H/W Reset</td> <td>All pixel off</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	All pixel off	S/W Reset	All pixel off	H/W Reset	All pixel off				
Status	Default Value												
Power On Sequence	All pixel off												
S/W Reset	All pixel off												
H/W Reset	All pixel off												



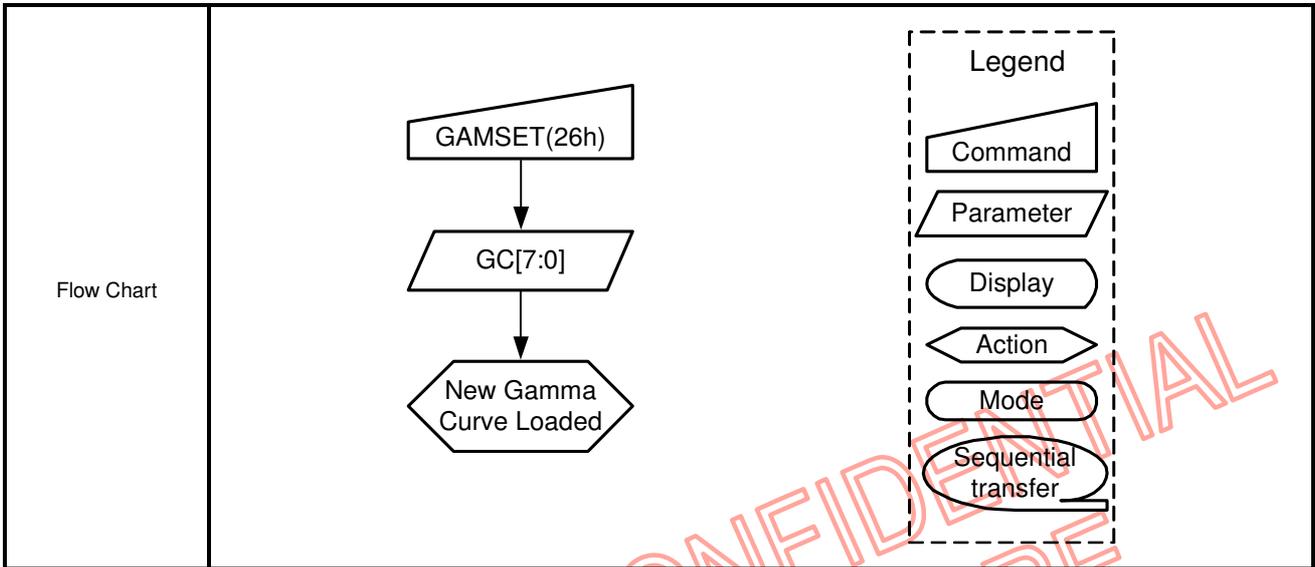
NOVATEK CONFIDENTIAL
NO DISCLOSURE

6.1.23 GAMSET: Gamma Set (26h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
GAMSET	Write	26h	2600h	00h	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0

NOTE: “-“ Don't care

Description	This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curves are defined in Fig 5.21.1 The curve is selected by setting the appropriate bit in the parameter as described in the Table.													
	GC[7:0]	Parameter												
	01h	GC0												
	02h	GC1												
	04h	GC2												
	08h	GC3												
	10h	GC4												
	<i>Note: All other values are undefined.</i>													
Restriction	Values of GC [7:0] not shown in table above are invalid and will not change the current selected gamma curve until valid is received.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>01h</td> </tr> <tr> <td>S/W Reset</td> <td>01h</td> </tr> <tr> <td>H/W Reset</td> <td>01h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	01h	S/W Reset	01h	H/W Reset	01h				
Status	Default Value													
Power On Sequence	01h													
S/W Reset	01h													
H/W Reset	01h													

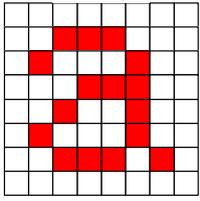
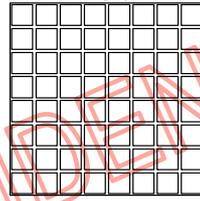


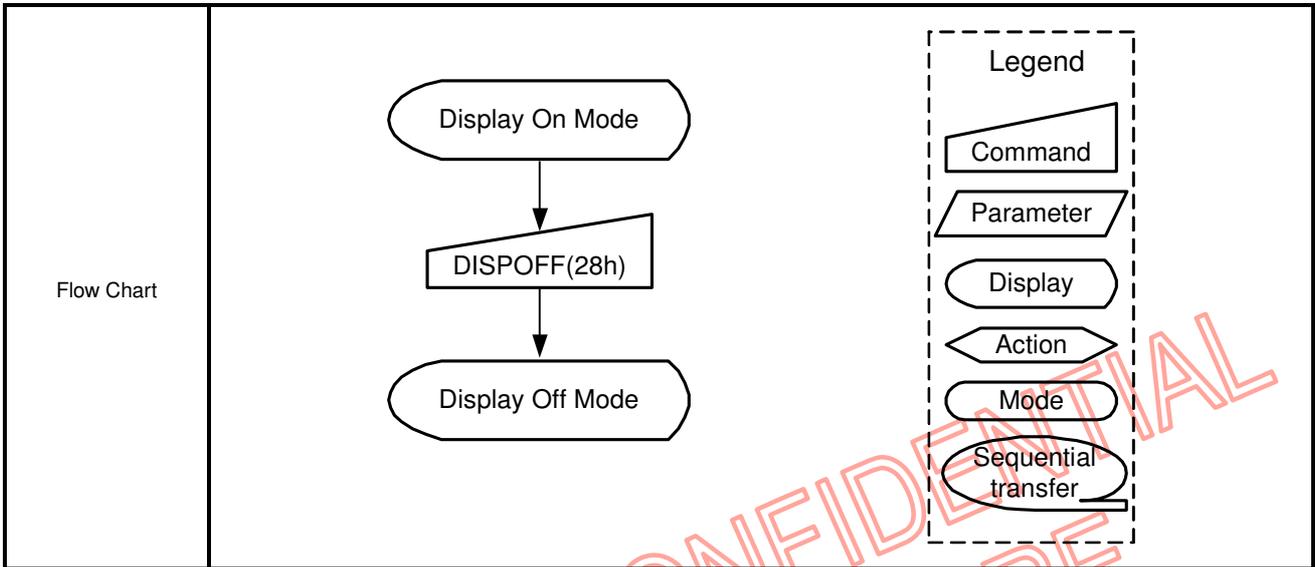
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NO DISCLOSURE

6.1.24 DISPOFF: Display Off (28h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
DISPOFF	Write	28h	2800h	No Parameter								

NOTE: “-“ Don't care

Description	<p>This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.</p> <p>This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display.</p> <p>(Example)</p> <div style="display: flex; align-items: center; justify-content: center;"> <div style="text-align: center;"> <p>Memory</p>  </div> <div style="margin: 0 20px;">→</div> <div style="text-align: center;"> <p>Display</p>  </div> </div>												
Restriction	This command has no effect when module is already in Display Off mode.												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display off</td> </tr> <tr> <td>S/W Reset</td> <td>Display off</td> </tr> <tr> <td>H/W Reset</td> <td>Display off</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off				
Status	Default Value												
Power On Sequence	Display off												
S/W Reset	Display off												
H/W Reset	Display off												

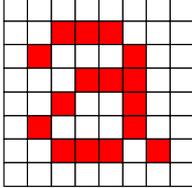
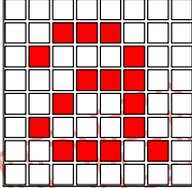


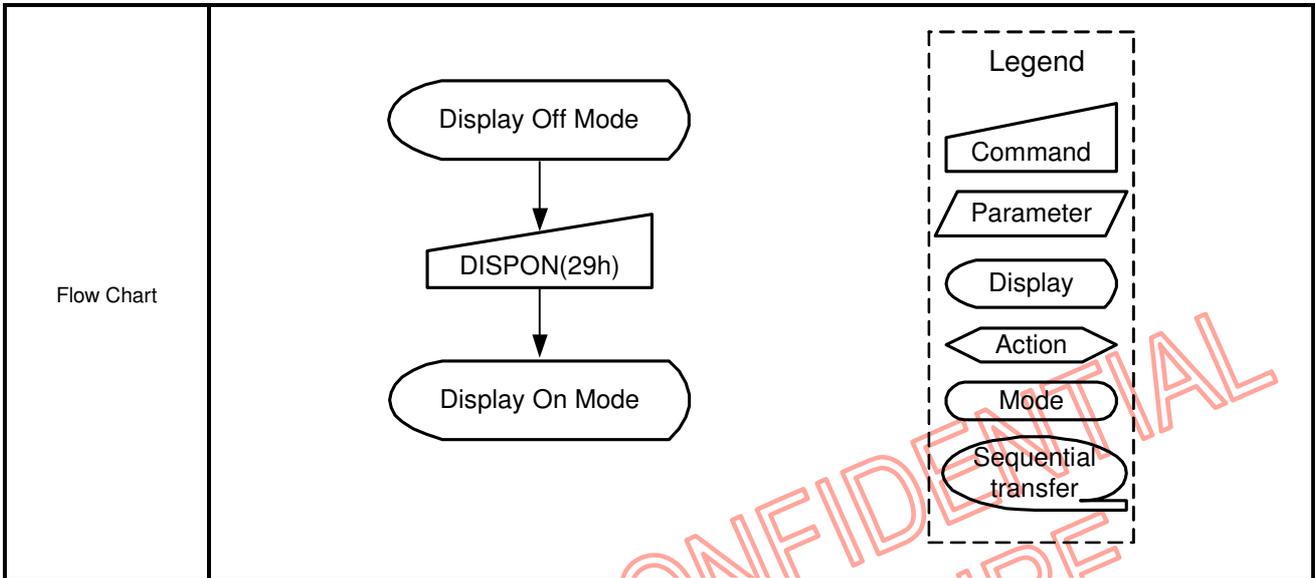
NOVATEK CONFIDENTIAL
NO DISCLOSURE

6.1.25 DISPON: Display On (29h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
DISPON	Write	29h	2900h	No Parameter								

NOTE: “-“ Don't care

Description	<p>This command is used to recover from DISPLAY OFF mode. Output from Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. (Example)</p> <div style="display: flex; align-items: center; justify-content: center;"> <div style="text-align: center;"> <p>Memory</p>  </div> <div style="margin: 0 20px;">→</div> <div style="text-align: center;"> <p>Display</p>  </div> </div>												
Restriction	This command has no effect when module is already in Display On mode.												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Status</th> <th style="width: 50%;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Status</th> <th style="width: 50%;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display off</td> </tr> <tr> <td>S/W Reset</td> <td>Display off</td> </tr> <tr> <td>H/W Reset</td> <td>Display off</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off				
Status	Default Value												
Power On Sequence	Display off												
S/W Reset	Display off												
H/W Reset	Display off												

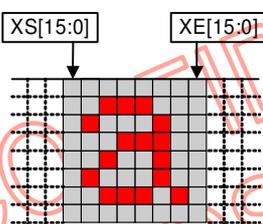


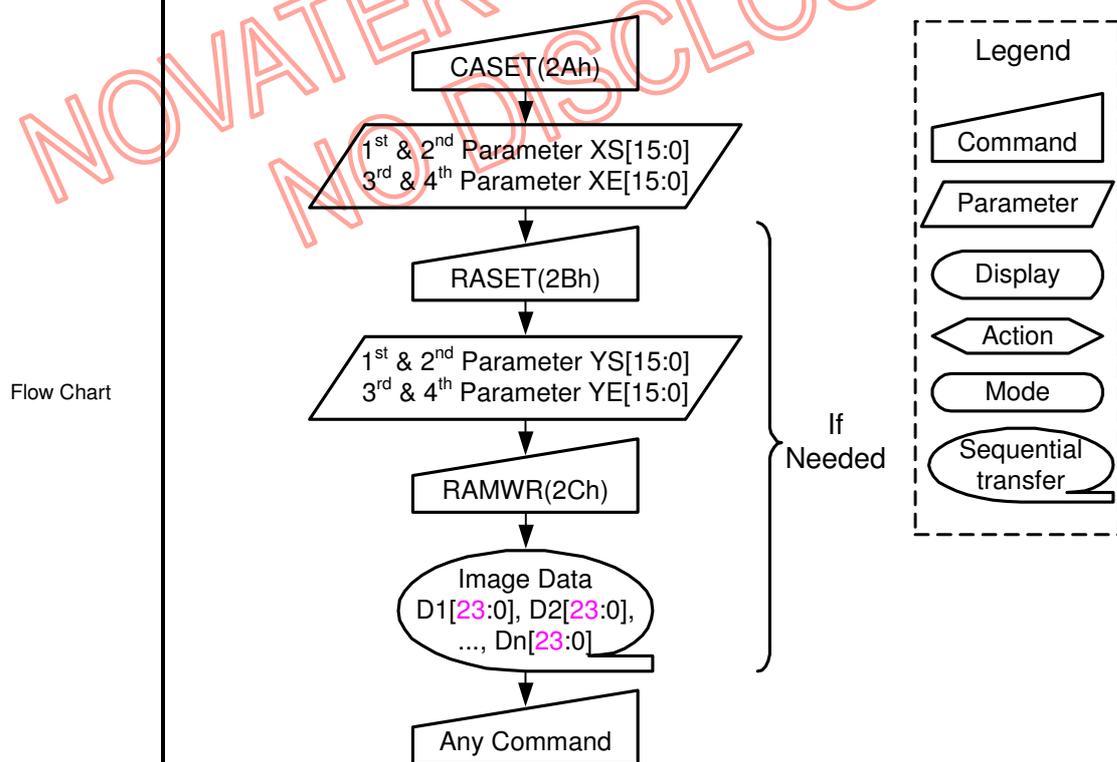
NOVATEK CONFIDENTIAL
NO DISCLOSURE

6.1.26 CASET: Column Address Set (2Ah)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
CASET	Write	2Ah	2A00h	00h	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8
			2A01h	00h	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0
			2A02h	00h	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8
			2A03h	00h	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0

NOTE: "-" Don't care

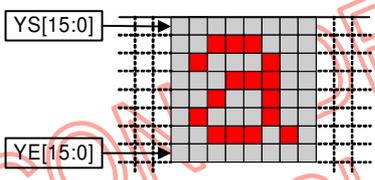
Description	<p>This command is used to define area of frame memory where MPU can access. This command makes no change on the other driver status. Each value represents one column line in the Frame Memory. (Example)</p> 												
Restriction	<p>XS[15:0] always must be equal to or less than XE[15:0] When XS[15:0] or XE[15:0] is greater than maximum address like below, data of out of range will be ignored. For DISP[1:0] = "00" (360 x 640 resolution) MV = "0": Parameter range $0 \leq XS[15:0] \leq XE[15:0] \leq 359$ (0167h) MV = "1": Parameter range $0 \leq XS[15:0] \leq XE[15:0] \leq 639$ (027Fh) For DISP[1:0] = "01" (360 x 480 resolution) MV = "0": Parameter range $0 \leq XS[15:0] \leq XE[15:0] \leq 359$ (0167h) MV = "1": Parameter range $0 \leq XS[15:0] \leq XE[15:0] \leq 479$ (01DFh) For DISP[1:0] = "10" (320 x 480 resolution) MV = "0": Parameter range $0 \leq XS[15:0] \leq XE[15:0] \leq 319$ (013Fh) MV = "1": Parameter range $0 \leq XS[15:0] \leq XE[15:0] \leq 479$ (01DFh)</p>												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												

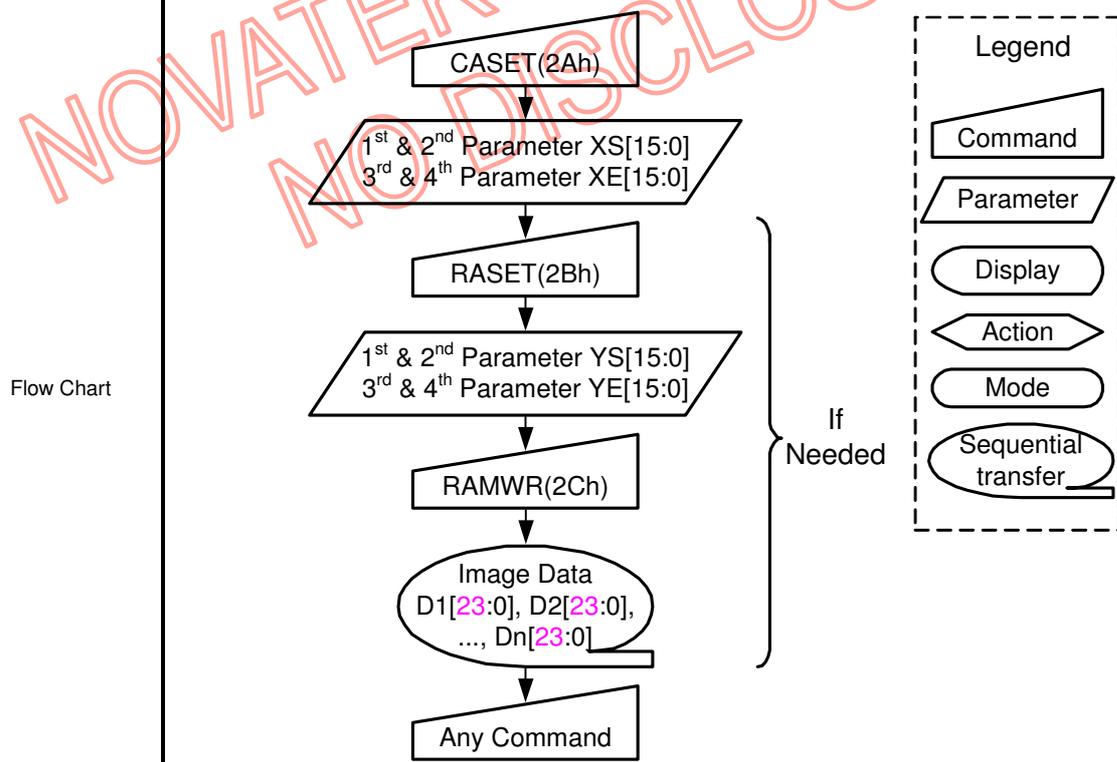
Default	For DISP [1:0] = "00" (360x640 resolution)			
	Status	Default Value		
		XS[15:0]	XE[15:0] (MV="0")	XE[15:0] (MV="1")
	Power On Sequence	0000h	0167h (359d)	
	S/W Reset	0000h	0167h (359d)	027Fh (639d)
	H/W Reset	0000h	0167h (359d)	
	For DISP [1:0] = "01" (360x480 resolution)			
	Status	Default Value		
		XS[15:0]	XE[15:0] (MV="0")	XE[15:0] (MV="1")
	Power On Sequence	0000h	0167h (359d)	
S/W Reset	0000h	0167h (359d)	01DFh (479d)	
H/W Reset	0000h	0167h (359d)		
For DISP [1:0] = "10" (320x480 resolution)				
Status	Default Value			
	XS[15:0]	XE[15:0] (MV="0")	XE[15:0] (MV="1")	
Power On Sequence	0000h	013Fh (319d)		
S/W Reset	0000h	013Fh (319d)	01DFh (479d)	
H/W Reset	0000h	013Fh (319d)		
Flow Chart	 <pre> graph TD CASET[CASET(2Ah)] --> Param1[/1st & 2nd Parameter XS[15:0] 3rd & 4th Parameter XE[15:0]/] Param1 --> RASET[RASET(2Bh)] RASET --> Param2[/1st & 2nd Parameter YS[15:0] 3rd & 4th Parameter YE[15:0]/] Param2 --> RAMWR[RAMWR(2Ch)] RAMWR --> ImageData([Image Data D1[23:0], D2[23:0], ..., Dn[23:0]]) ImageData --> AnyCommand[/Any Command/] subgraph Legend direction TB Command[Command] Parameter[/Parameter/] Display[Display] Action[Action] Mode[Mode] Sequential[Sequential transfer] end subgraph IfNeeded [If Needed] RAMWR ImageData end </pre>			

6.1.27 RASET: Row Address Set (2Bh)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RASET	Write	2Bh	2B00h	00h	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8
			2B01h	00h	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0
			2B02h	00h	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8
			2B03h	00h	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0

NOTE: “-“ Don't care

Description	<p>This command is used to define area of frame memory where MPU can access. This command makes no change on the other driver status. Each value represents one row line in the Frame Memory. (Example)</p> 												
Restriction	<p>YS[15:0] always must be equal to or less than YE[15:0] When YS[15:0] or YE[15:0] is greater than maximum address like below, data of out of range will be ignored. For DISP [1:0] = “00” (360 x 640 resolution) MV = “0”: Parameter range $0 \leq YS[15:0] \leq YE[15:0] \leq 639$ (027Fh) MV = “1”: Parameter range $0 \leq YS[15:0] \leq YE[15:0] \leq 359$ (0167h) For DISP [1:0] = “01” (360 x 480 resolution) MV = “0”: Parameter range $0 \leq YS[15:0] \leq YE[15:0] \leq 479$ (01DFh) MV = “1”: Parameter range $0 \leq YS[15:0] \leq YE[15:0] \leq 359$ (0167h) For DISP [1:0] = “10” (320 x 480 resolution) MV = “0”: Parameter range $0 \leq YS[15:0] \leq YE[15:0] \leq 479$ (01DFh) MV = “1”: Parameter range $0 \leq YS[15:0] \leq YE[15:0] \leq 319$ (013Fh)</p>												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												

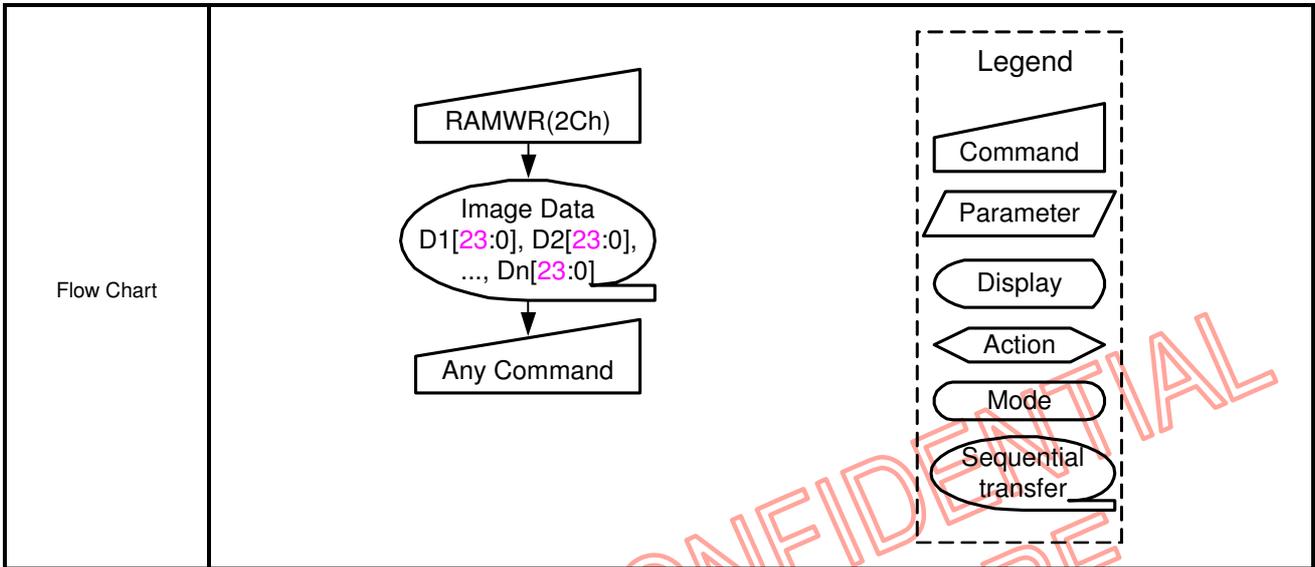
Default	For DISP [1:0] = "00" (360 x 640 resolution)			
	Status	Default Value		
		YS[15:0]	YE[15:0] (MV="0")	YE[15:0] (MV="1")
	Power On Sequence	0000h	027Fh (639d)	
	S/W Reset	0000h	027Fh (639d)	167h (359d)
	H/W Reset	0000h	027Fh (639d)	
	For DISP [1:0] = "01" (360 x 480 resolution)			
	Status	Default Value		
		YS[15:0]	YE[15:0] (MV="0")	YE[15:0] (MV="1")
Power On Sequence	0000h	01DFh (479d)		
S/W Reset	0000h	01DFh (479d)	167h (359d)	
H/W Reset	0000h	01DFh (479d)		
For DISP [1:0] = "10" (320 x 480 resolution)				
Status	Default Value			
	YS[15:0]	YE[15:0] (MV="0")	YE[15:0] (MV="1")	
Power On Sequence	0000h	01DFh (479d)		
S/W Reset	0000h	01DFh (479d)	013Fh (319d)	
H/W Reset	0000h	01DFh (479d)		
Flow Chart	 <pre> graph TD CASET[CASET(2Ah)] --> P1[/1st & 2nd Parameter XS[15:0] 3rd & 4th Parameter XE[15:0]/] P1 --> RASET[RASET(2Bh)] RASET --> P2[/1st & 2nd Parameter YS[15:0] 3rd & 4th Parameter YE[15:0]/] P2 --> RAMWR[RAMWR(2Ch)] RAMWR --> ID([Image Data D1[23:0], D2[23:0], ..., Dn[23:0]]) ID --> AC[Any Command] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command (trapezoid) Parameter (parallelogram) Display (rounded rectangle) Action (arrow) Mode (oval) Sequential transfer (oval with arrow) <p>If Needed</p>			

6.1.28 RAMWR: Memory Write (2Ch)

Inst / Para	R/W	Address			Parameter							
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RAMWR	Write	2Ch	X	X	D7	D6	D5	D4	D3	D2	D1	D0
					:	:	:	:	:	:	:	:
					D7	D6	D5	D4	D3	D2	D1	D0

NOTE: “-“ Don't care

Description	<p>This command is used to transfer data from MPU interface to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. The Start Column/Start Row positions are different in accordance with MADCTL setting Then D[23:0] is stored in frame memory and the column register and the row register incremented. Sending any other command can stop Frame Write.</p>												
Restriction	There is no restriction on length of parameters. No access in the frame memory in Sleep In mode												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>SRAM data keep or not depends on RAMKP bit in 0XC1</td> </tr> <tr> <td>H/W Reset</td> <td>SRAM data keep or not depends on RAMKP bit in 0XC1</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	SRAM data keep or not depends on RAMKP bit in 0XC1	H/W Reset	SRAM data keep or not depends on RAMKP bit in 0XC1				
Status	Default Value												
Power On Sequence	Contents of memory is set randomly												
S/W Reset	SRAM data keep or not depends on RAMKP bit in 0XC1												
H/W Reset	SRAM data keep or not depends on RAMKP bit in 0XC1												



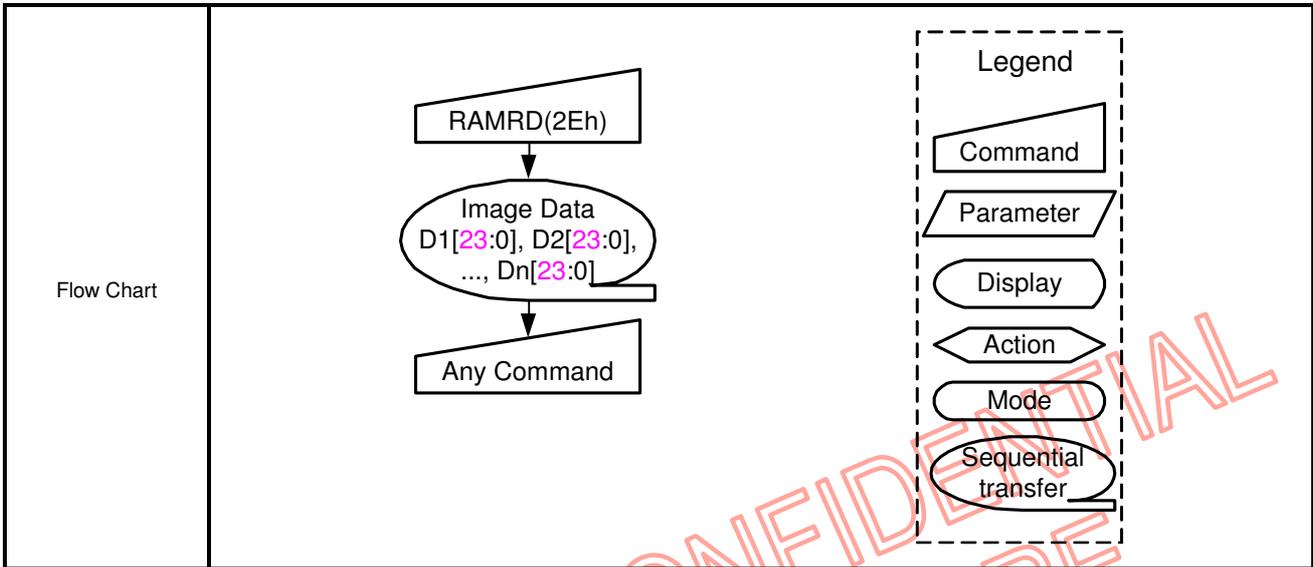
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6.1.29 RAMRD: Memory Read (2Eh)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RAMRD	Read	2Eh	2E00h	00h	D7	D6	D5	D4	D3	D2	D1	D0
			X	X	:	:	:	:	:	:	:	:
			X	X	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: “-“ Don't care

Description	<p>This command is used to transfer data from frame memory to MPU interface.</p> <p>This command makes no change to the other driver status.</p> <p>When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.</p> <p>The Start Column/Start Row positions are different in accordance with MADCTL setting.</p> <p>Then D[23:0] is read back from the frame memory and the column register and the row register incremented</p> <p>Frame Read can be canceled by sending any other command.</p>												
Restriction	There is no restriction on length of parameters. No access in the frame memory in Sleep In mode												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of memory is not cleared</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is not cleared</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset	Contents of memory is not cleared				
Status	Default Value												
Power On Sequence	Contents of memory is set randomly												
S/W Reset	Contents of memory is not cleared												
H/W Reset	Contents of memory is not cleared												

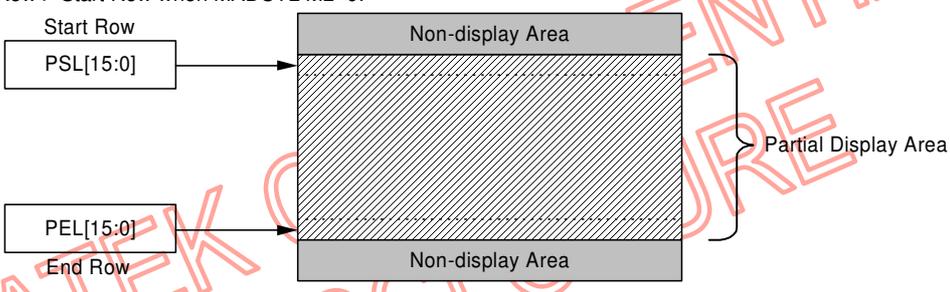
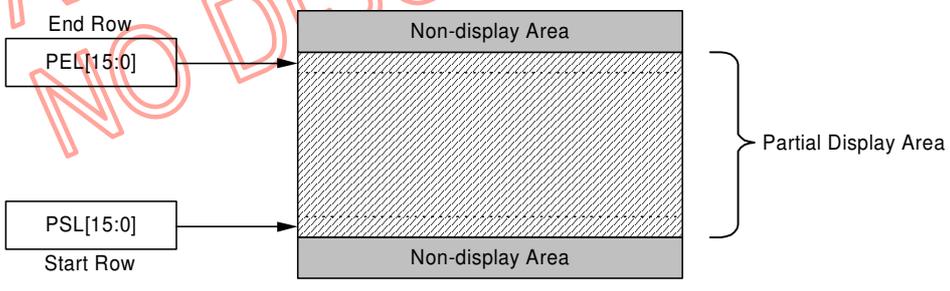
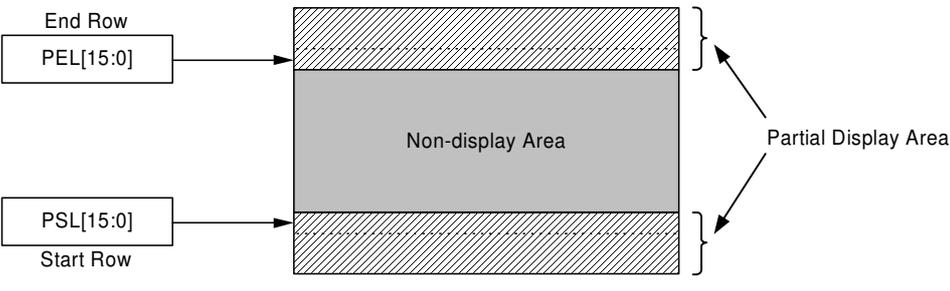


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6.1.30 PTLAR: Partial Area (30h)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
PTLAR	Write	30h	3000h	00h	PSL[15:8]								
			3001h	00h	PSL[7:0]								
			3002h	00h	PEL[15:8]								
			3003h	00h	PEL[7:0]								

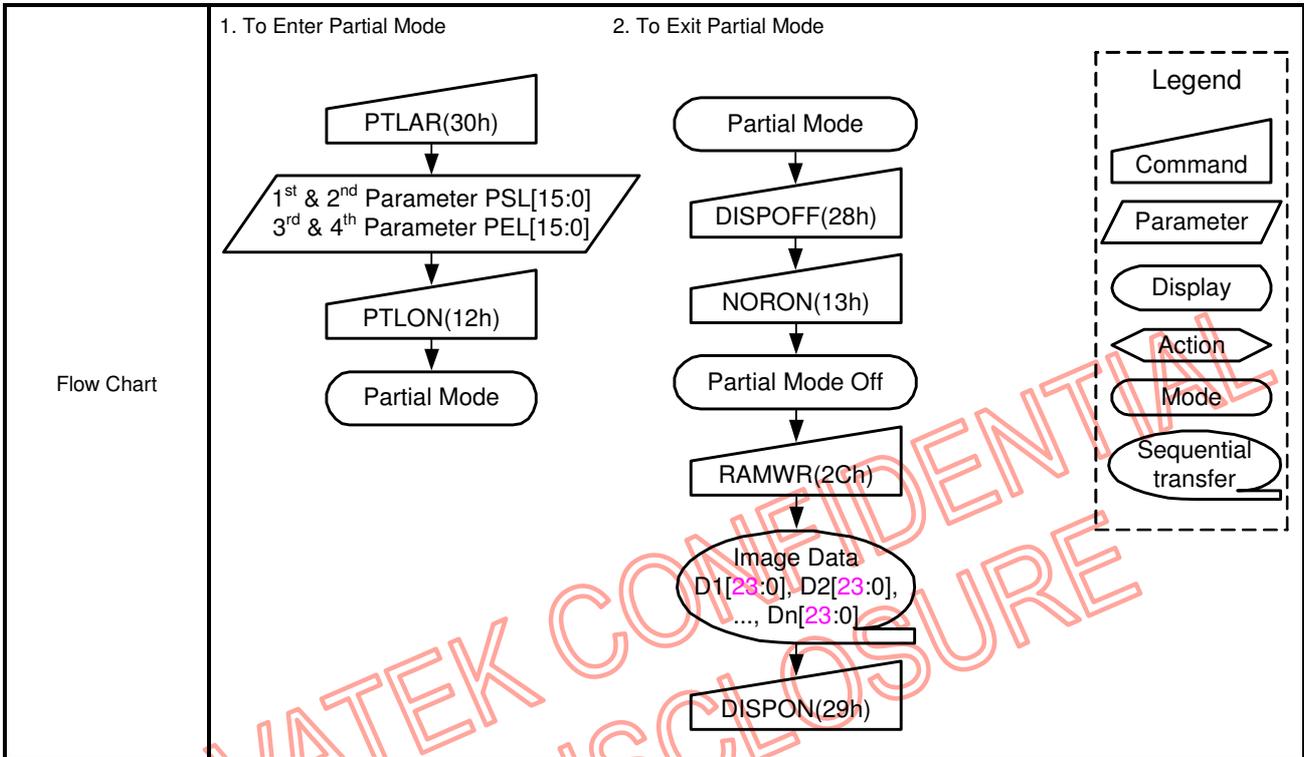
NOTE: “-“ Don't care

Description	<p>This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.</p> <p>If End Row > Start Row when MADCTL ML=0:</p>  <p>If End Row > Start Row when MADCTL ML=1:</p>  <p>If End Row < Start Row when MADCTL ML=0:</p>  <p>If End Row = Start Row then the Partial Area will be one row deep.</p>
-------------	--

Restriction	PSL[15:0] and PEL[15:0] should have below range DISP[1:0] = "00" (360 x 640): $0 \leq \text{PSL}[15:0], \text{PEL}[15:0] \leq 639$ (027Fh), $ \text{PEL}-\text{PSL} \leq 639$ (027Fh). DISP[1:0] = "01" (360 x 480): $0 \leq \text{PSL}[15:0], \text{PEL}[15:0] \leq 479$ (01DFh), $ \text{PEL}-\text{PSL} \leq 479$ (01DFh). DISP[1:0] = "10" (320 x 480): $0 \leq \text{PSL}[15:0], \text{PEL}[15:0] \leq 479$ (01DFh), $ \text{PEL}-\text{PSL} \leq 479$ (01DFh).
-------------	--

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default Value	
		PSL[15:0]	PEL[15:0]
	Power On Sequence	0000h	027Fh (639d) when DISP [1:0] = "00" 01DFh (479d) when DISP [1:0] = "01" 01DFh (479d) when DISP [1:0] = "10"
	S/W Reset	0000h	027Fh (639d) when DISP [1:0] = "00" 01DFh (479d) when DISP [1:0] = "01" 01DFh (479d) when DISP [1:0] = "10"
	H/W Reset	0000h	027Fh (639d) when DISP [1:0] = "00" 01DFh (479d) when DISP [1:0] = "01" 01DFh (479d) when DISP [1:0] = "10"



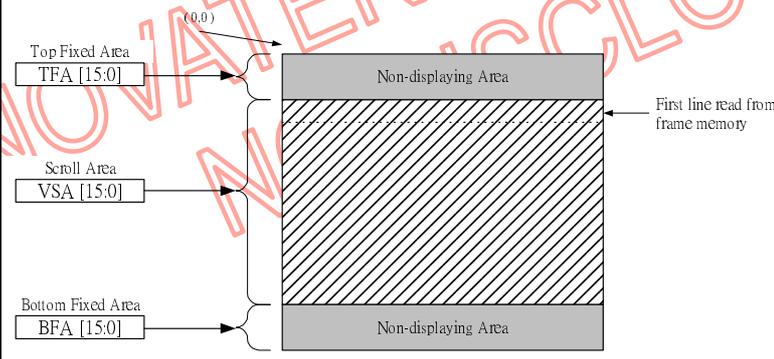
6.1.31 SCRLAR: Scroll Area (33h)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
SCRLAR	Write	33h	3300h	00h	TFA[15:8]								
			3301h	00h	TFA[7:0]								
			3302h	00h	VSA[15:8]								
			3303h	00h	VSA[7:0]								
			3304h	00h	BFA[15:8]								
			3305h	00h	BFA[7:0]								

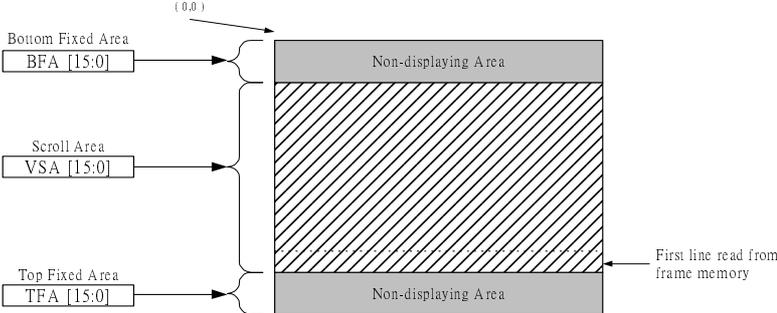
NOTE: “-“ Don't care

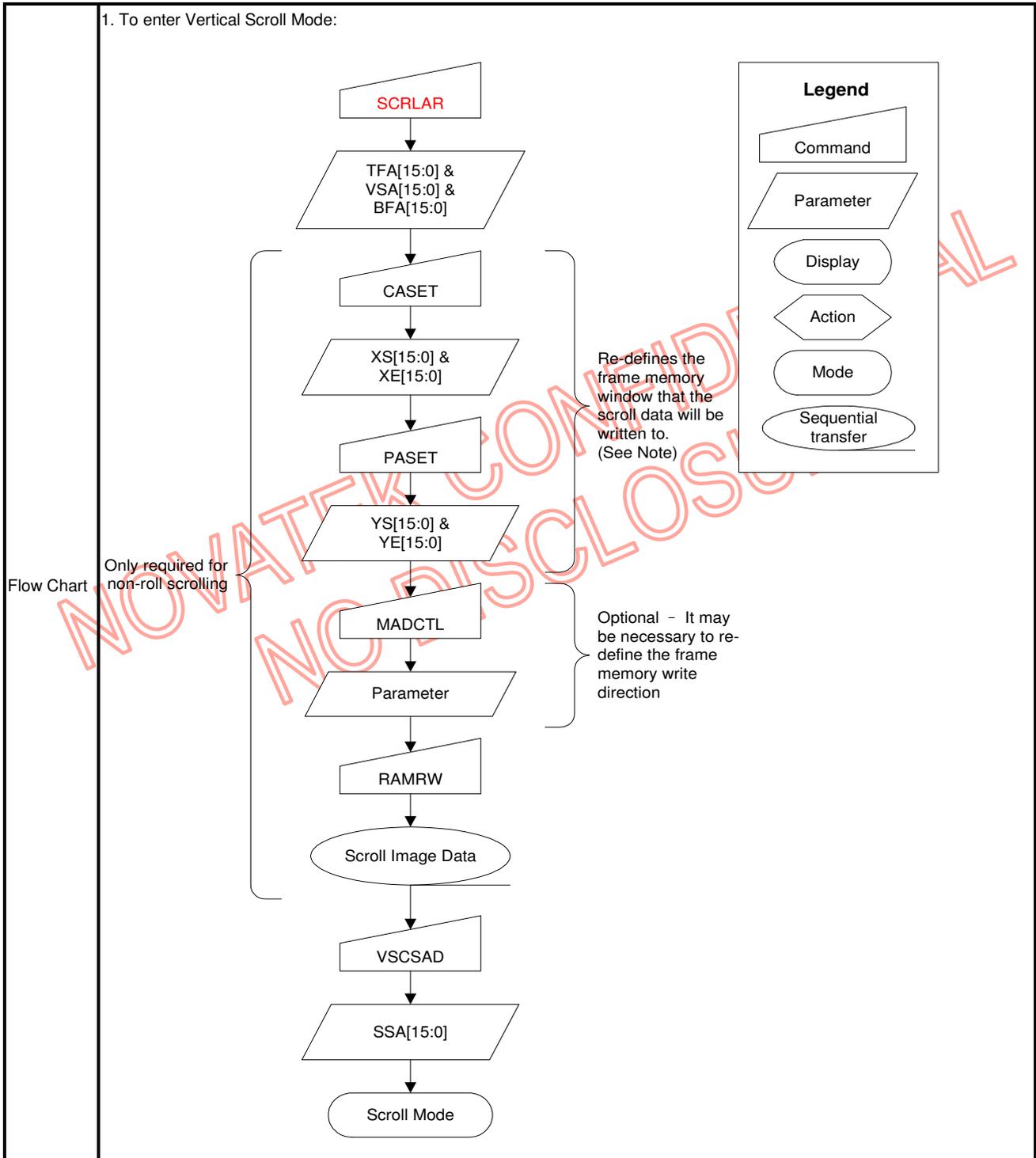
This command defines the Vertical Scrolling Area of the display.

When MADCTL ML=0
TFA [15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).
VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)
The first line appears immediately after the bottom most line of the Top Fixed Area.
BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
TFA, VSA and BFA refer to the Frame Memory row address.

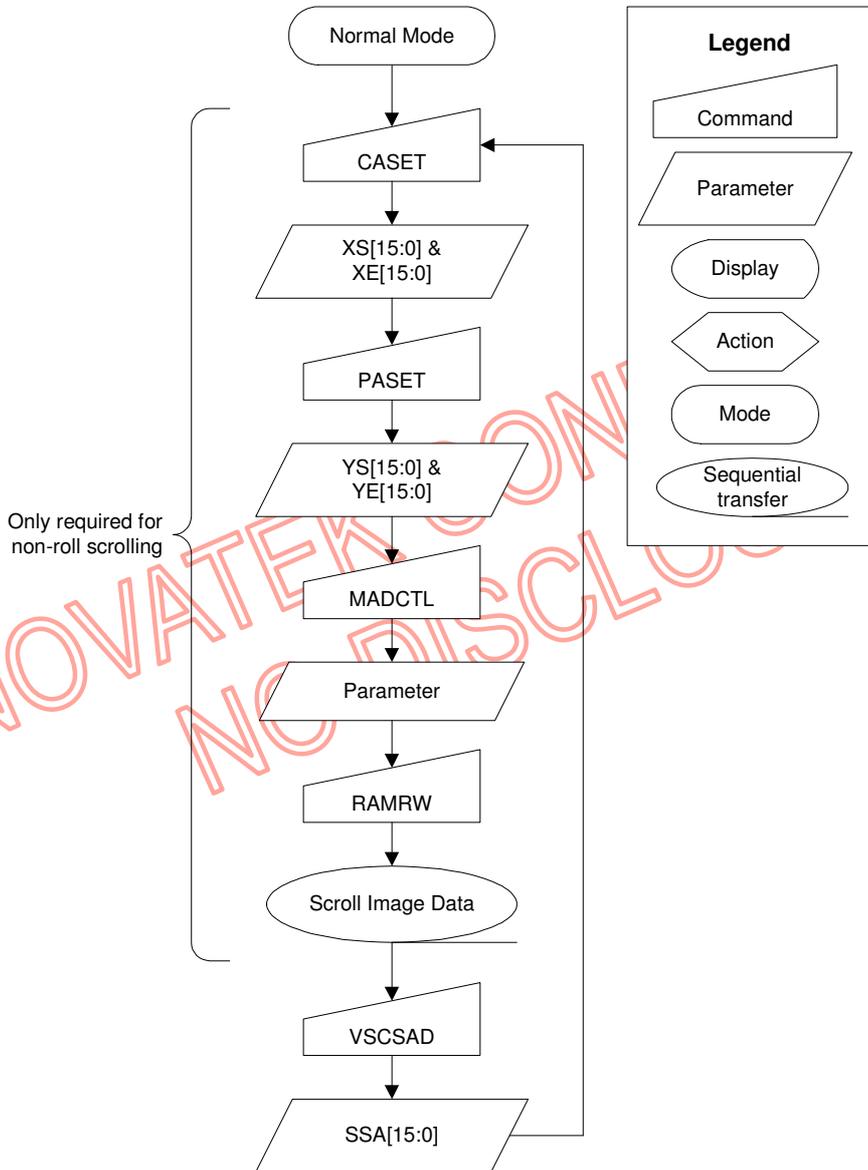


When MADCTL ML=1
TFA [15:0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)
The first line appears immediately after the top most line of the Top Fixed Area.

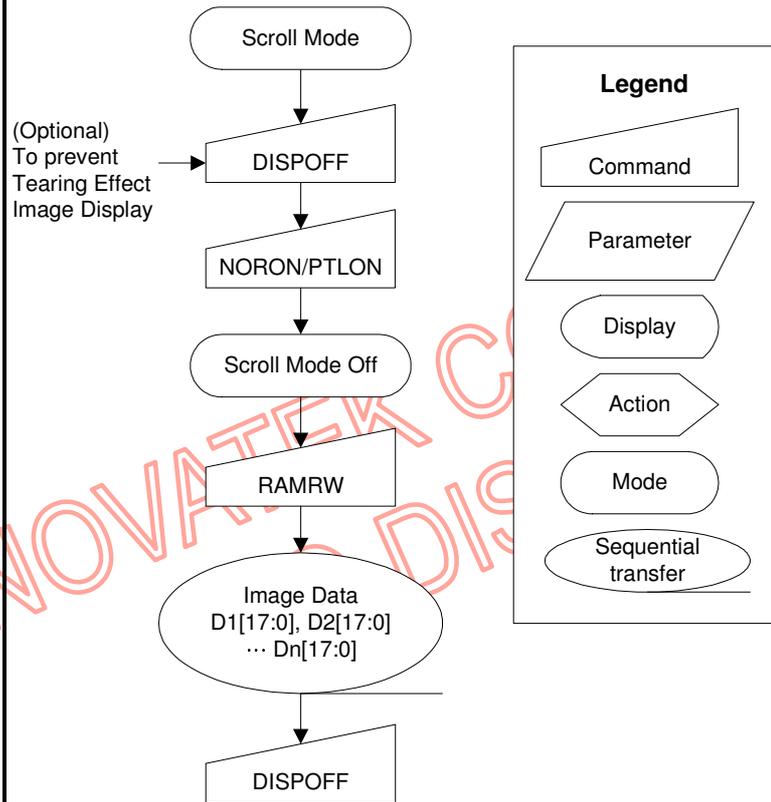
	<p>BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).</p>  <p>See Section 5.2.6 for details of the Memory to Display Mapping.</p>																			
Restriction	<p>The condition is DISP[1:0] = "00" (360 x 640): (TFA+VSA+BFA) = 640, otherwise Scrolling mode is undefined. DISP[1:0] = "01" (360 x 480): (TFA+VSA+BFA) = 480, otherwise Scrolling mode is undefined. DISP[1:0] = "10" (320 x 480): (TFA+VSA+BFA) = 480, otherwise Scrolling mode is undefined. In Vertical Scroll Mode, MADCTL parameter MV should be set to '0'-this only affects the Frame Memory Write.</p>																			
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																			
Normal Mode On, Idle Mode Off, Sleep Out	Yes																			
Normal Mode On, Idle Mode On, Sleep Out	Yes																			
Partial Mode On, Idle Mode Off, Sleep Out	Yes																			
Partial Mode On, Idle Mode On, Sleep Out	Yes																			
Sleep In	Yes																			
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="3">Default Value</th> </tr> <tr> <th>TFA [15:0]</th> <th>VSA [15:0]</th> <th>BFA [15:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>0000h</td> <td>0280h (640d) when DISP [1:0] = "00" 01E0h (480d) when DISP [1:0] = "01" 01E0h (480d) when DISP [1:0] = "10"</td> <td>0000h</td> </tr> <tr> <td>S/W Reset</td> <td>0000h</td> <td>0280h (640d) when DISP [1:0] = "00" 01E0h (480d) when DISP [1:0] = "01" 01E0h (480d) when DISP [1:0] = "10"</td> <td>0000h</td> </tr> <tr> <td>H/W Reset</td> <td>0000h</td> <td>0280h (640d) when DISP [1:0] = "00" 01E0h (480d) when DISP [1:0] = "01" 01E0h (480d) when DISP [1:0] = "10"</td> <td>0000h</td> </tr> </tbody> </table>	Status	Default Value			TFA [15:0]	VSA [15:0]	BFA [15:0]	Power On Sequence	0000h	0280h (640d) when DISP [1:0] = "00" 01E0h (480d) when DISP [1:0] = "01" 01E0h (480d) when DISP [1:0] = "10"	0000h	S/W Reset	0000h	0280h (640d) when DISP [1:0] = "00" 01E0h (480d) when DISP [1:0] = "01" 01E0h (480d) when DISP [1:0] = "10"	0000h	H/W Reset	0000h	0280h (640d) when DISP [1:0] = "00" 01E0h (480d) when DISP [1:0] = "01" 01E0h (480d) when DISP [1:0] = "10"	0000h
Status	Default Value																			
	TFA [15:0]	VSA [15:0]	BFA [15:0]																	
Power On Sequence	0000h	0280h (640d) when DISP [1:0] = "00" 01E0h (480d) when DISP [1:0] = "01" 01E0h (480d) when DISP [1:0] = "10"	0000h																	
S/W Reset	0000h	0280h (640d) when DISP [1:0] = "00" 01E0h (480d) when DISP [1:0] = "01" 01E0h (480d) when DISP [1:0] = "10"	0000h																	
H/W Reset	0000h	0280h (640d) when DISP [1:0] = "00" 01E0h (480d) when DISP [1:0] = "01" 01E0h (480d) when DISP [1:0] = "10"	0000h																	



Note: The frame memory window size must be defined correctly otherwise undesirable image will be displayed.
 2. Continuous Scroll:



3. To Exit Vertical Scroll Mode:



NOTE: Scroll Mode can be exit by both the Normal Display Mode On(13h) and Partial Mode On(12h) commands.

6.1.32 TEOFF: Tearing Effect Line OFF (34h)

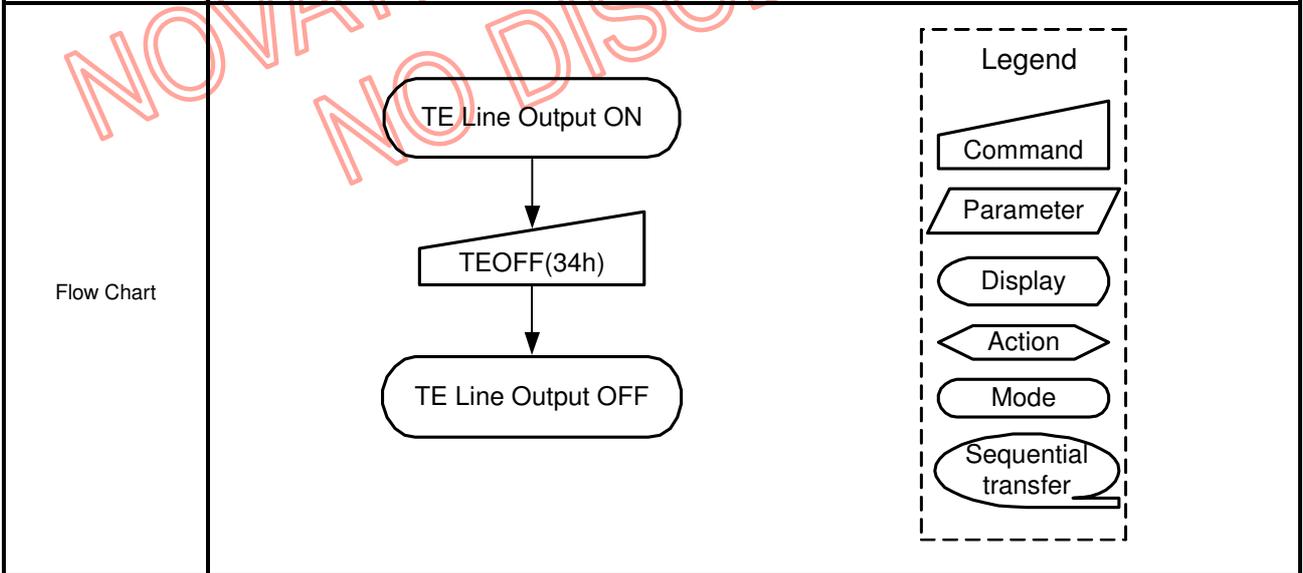
Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
TEOFF	Write	34h	3400h	No Parameter								

NOTE: "-“ Don't care

Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
Restriction	This command has no effect when Tearing Effect output is already OFF.

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

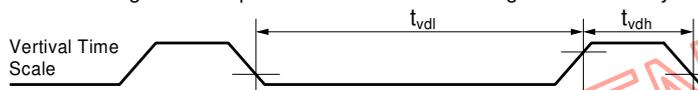
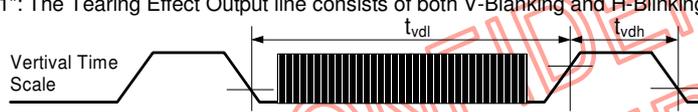
Default	Status	Default Value
	Power On Sequence	Tearing Effect off
	S/W Reset	Tearing Effect off
	H/W Reset	Tearing Effect off

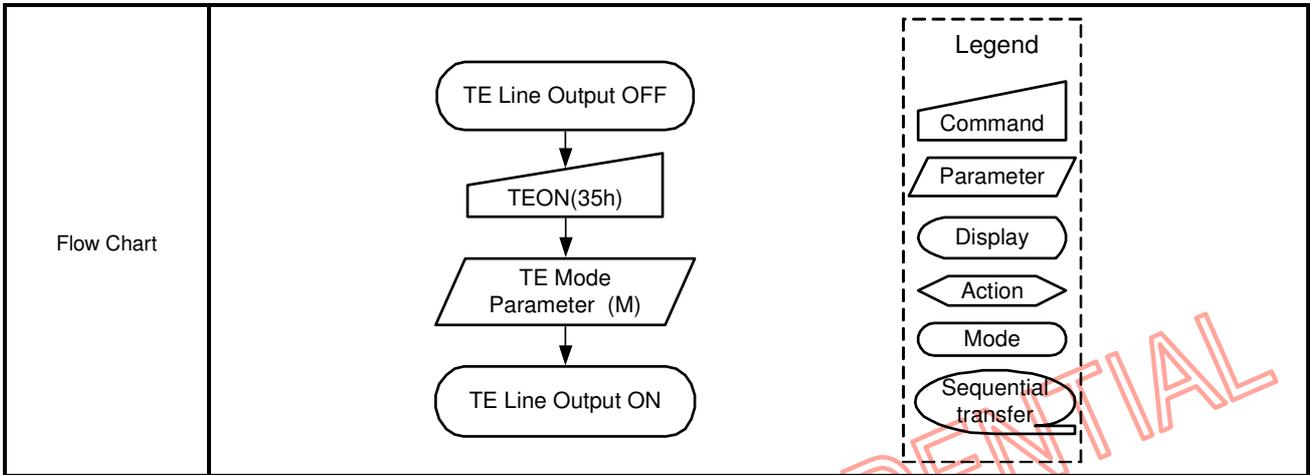


6.1.33 TEON: Tearing Effect Line ON (35h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
TEON	Write	35h	3500h	00h	-	-	-	-	-	-	-	M

NOTE: “-“ Don't care

Description	<p>This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit ML.</p> <p>The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. (“-“ = Don't Care).</p> <p>When M = “0”: The Tearing Effect Output line consists of V-Blanking information only.</p>  <p>When M = “1”: The Tearing Effect Output line consists of both V-Blanking and H-Blanking information.</p>  <p>Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Lofw.</p>												
Restriction	This command has no effect when Tearing Effect output is already ON.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Tearing Effect off</td> </tr> <tr> <td>S/W Reset</td> <td>Tearing Effect off</td> </tr> <tr> <td>H/W Reset</td> <td>Tearing Effect off</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Tearing Effect off	S/W Reset	Tearing Effect off	H/W Reset	Tearing Effect off				
Status	Default Value												
Power On Sequence	Tearing Effect off												
S/W Reset	Tearing Effect off												
H/W Reset	Tearing Effect off												



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6.1.34 MADCTL: Memory Data Access Control (36h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
MADCTL	Write	36h	X	X	MY	MX	MV	ML	RGB	MH	RSMX	RSMY
		X	3600h	00h	0	0	0	ML	RGB	MH	-	-

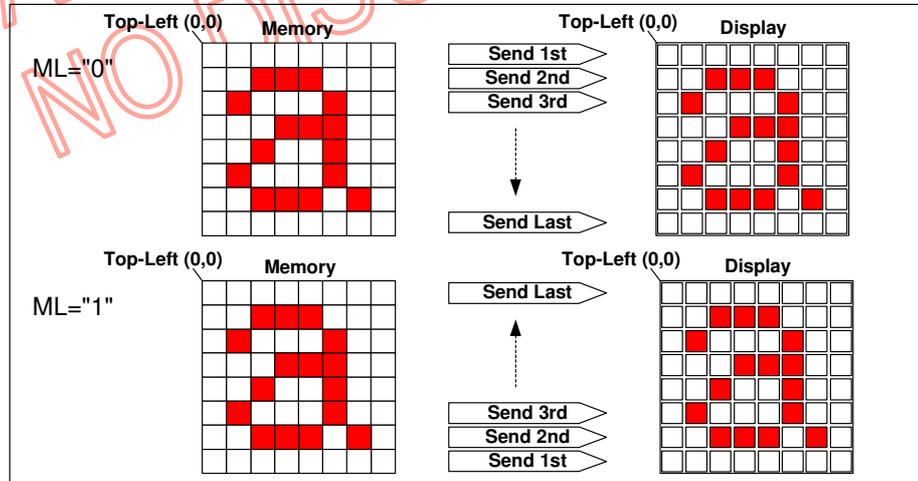
NOTE: "-" Don't care

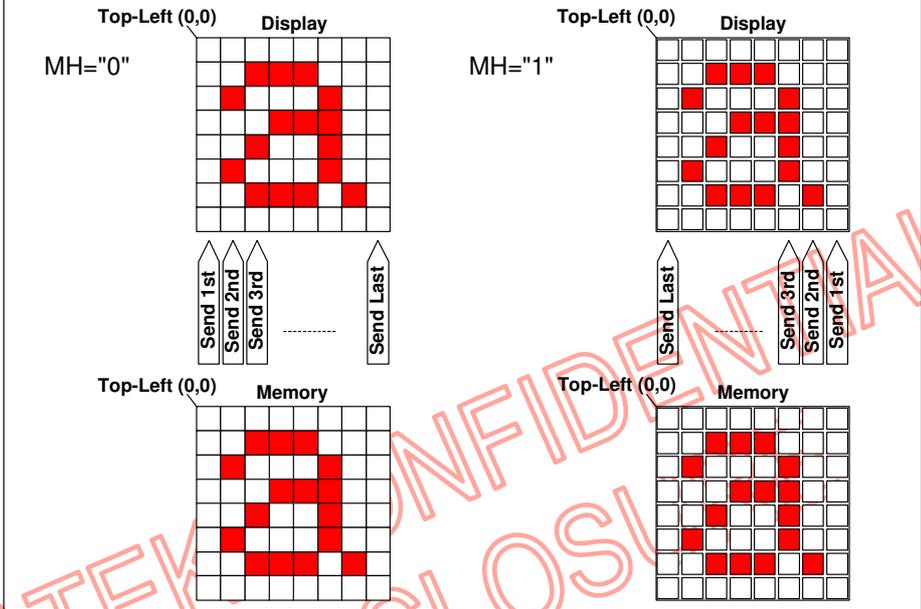
This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.

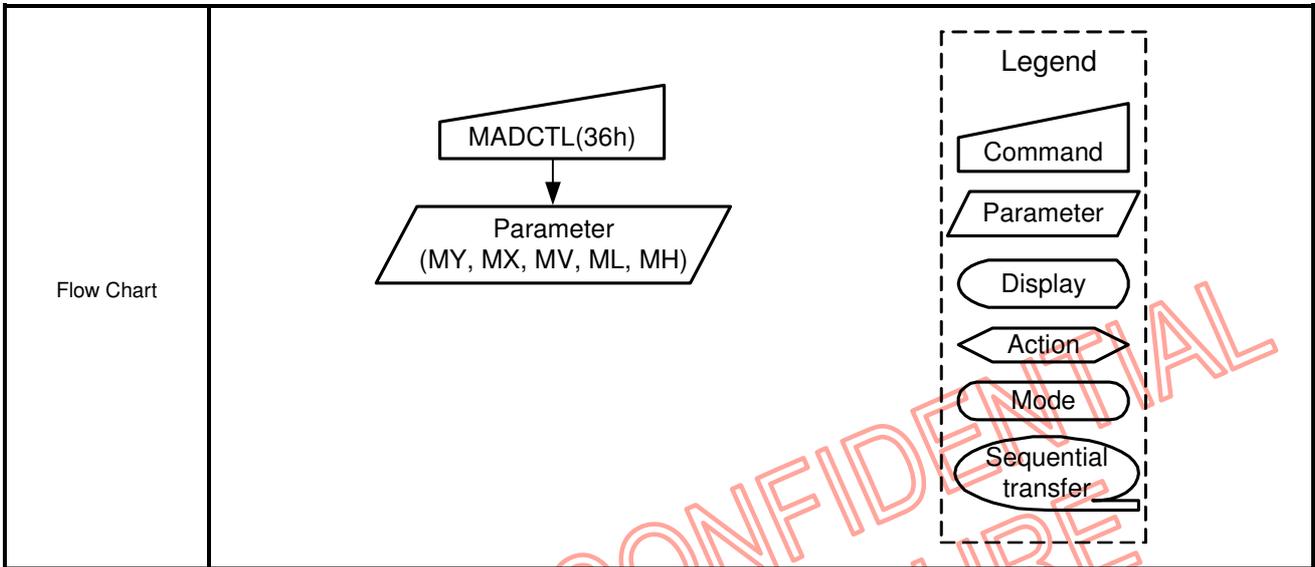
Bit	NAME	DESCRIPTION
MY	Row Address Order	These 3 bits controls interface to memory write/read direction. The behavior on display after pattern changed.
MX	Column Address Order	
MV	Row/Column Exchange	
ML	Vertical Refresh Order	LCD Vertical refresh direction control. Immediately behavior on display.
RGB	RGB-BGR Order	Color selector switch control "0" = RGB color sequence, "1" = BGR color sequence The behavior on display after pattern changed.
MH	Horizontal Refresh Order	LCD Horizontal refresh direction control. Immediately behavior on display.
RSMX	Flip horizontal	"0" = Normal, "1" = Horizontal flip
RSMY	Flip vertical	"0" = Normal, "1" = Vertical flip

Description

ML: Vertical Refresh Order



<p>Description</p>	<p style="text-align: center;">MH: Horizontal Refresh Order</p> 												
<p>Restriction</p>													
<p>Register Availability</p>	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
<p>Default</p>	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>No change</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	No change	H/W Reset	00h				
Status	Default Value												
Power On Sequence	00h												
S/W Reset	No change												
H/W Reset	00h												

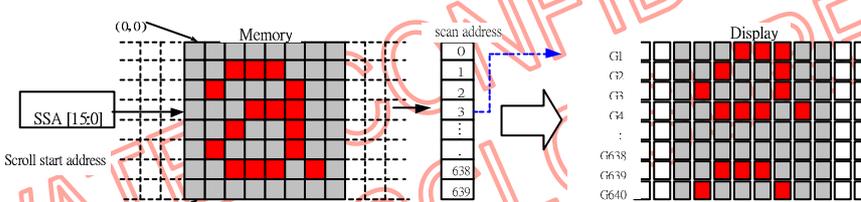
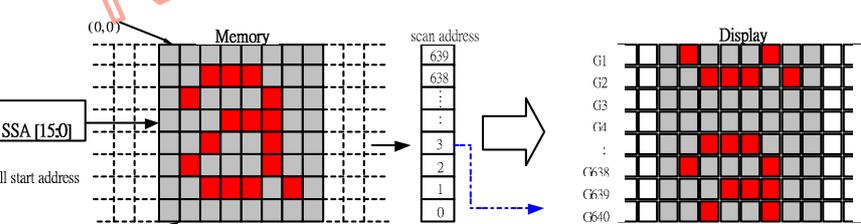


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6.1.35 VSCSAD: Vertical Scroll Start Address SRAM (37h)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
VSCSAD	Write	36h	3700h	00h	SSA[15:8]								
			3701h	00h	SSA[7:0]								

NOTE: "-" Don't care

Description	<p>This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.</p> <p>The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:</p> <p>This command Start the scrolling.</p> <p>Exit from V-scrolling mode by commands Partial mode On (12h) or Normal mode On (13h).</p> <p>When MADCTL ML=0</p> <p>Example: When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=640 and Vertical Scrolling Pointer SSA='3'.</p>  <p>When MADCTL ML =1</p> <p>Example: When Top Fixed Area= Bottom Fixed Area=00, Vertical Scrolling Area=640 and SSA='3'</p>  <p>NOTE: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. SSA refers to the Frame Memory scan address.</p>
-------------	---

Restriction	<p>Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)-otherwise undesirable image will be displayed on the Panel. SSA[15:0] is based on 1-line unit.</p> <p>DISP[1:0] = 00, SSA[15:0] = 0000h, 0001h, 0002h, 0003h, ... , 027Fh DISP[1:0] = 01, SSA[15:0] = 0000h, 0001h, 0002h, 0003h, ... , 01DFh DISP[1:0] = 10, SSA[15:0] = 0000h, 0001h, 0002h, 0003h, ... , 01DFh</p>												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>No</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>No</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	No	Partial Mode On, Idle Mode On, Sleep Out	No	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	No												
Partial Mode On, Idle Mode On, Sleep Out	No												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>0000h</td> </tr> <tr> <td>S/W Reset</td> <td>0000h</td> </tr> <tr> <td>H/W Reset</td> <td>0000h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	0000h	S/W Reset	0000h	H/W Reset	0000h				
Status	Default Value												
Power On Sequence	0000h												
S/W Reset	0000h												
H/W Reset	0000h												
Flow Chart	See Vertical Scrolling Definition (33h) description.												

6.1.36 IDMOFF: Idle Mode Off (38h)

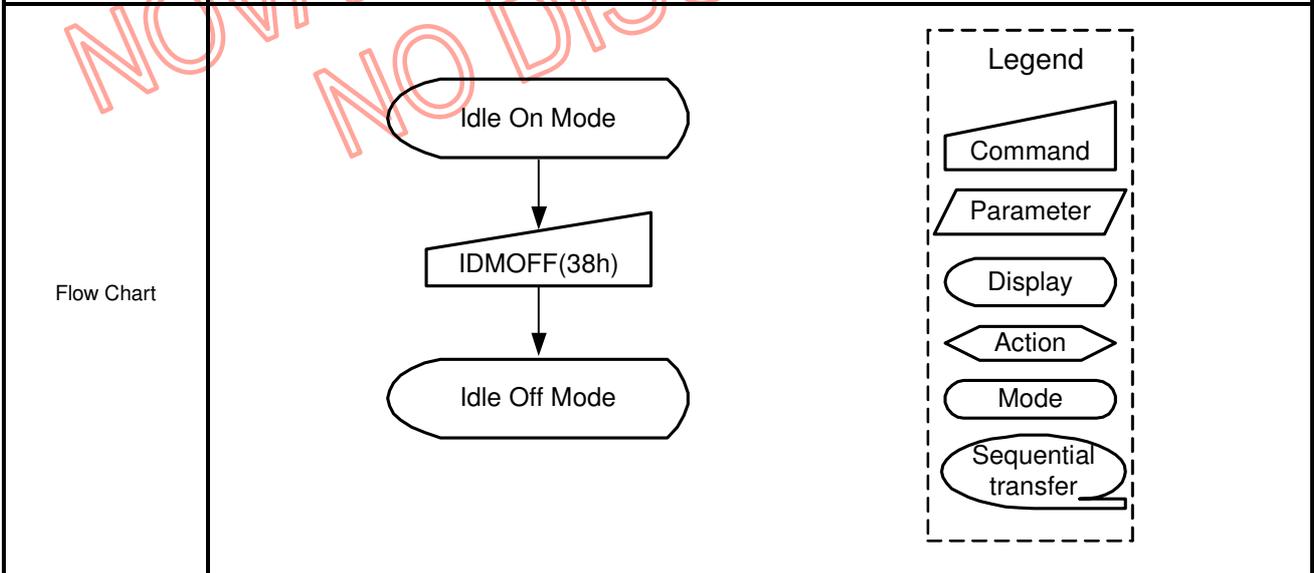
Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
IDMOFF	Write	38h	3800h	No Parameter								

NOTE: “-“ Don't care

Description	This command is used to recover from Idle mode on In the idle off mode, display panel can display maximum 16.7M colors.
Restriction	This command has no effect when module is already in idle off mode.

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

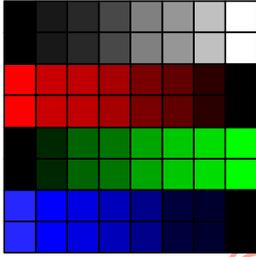
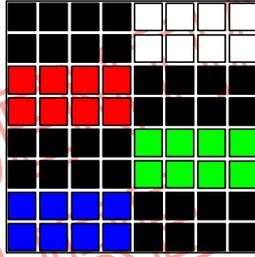
Default	Status	Default Value
	Power On Sequence	Idle Mode off
	S/W Reset	Idle Mode off
	H/W Reset	Idle Mode off

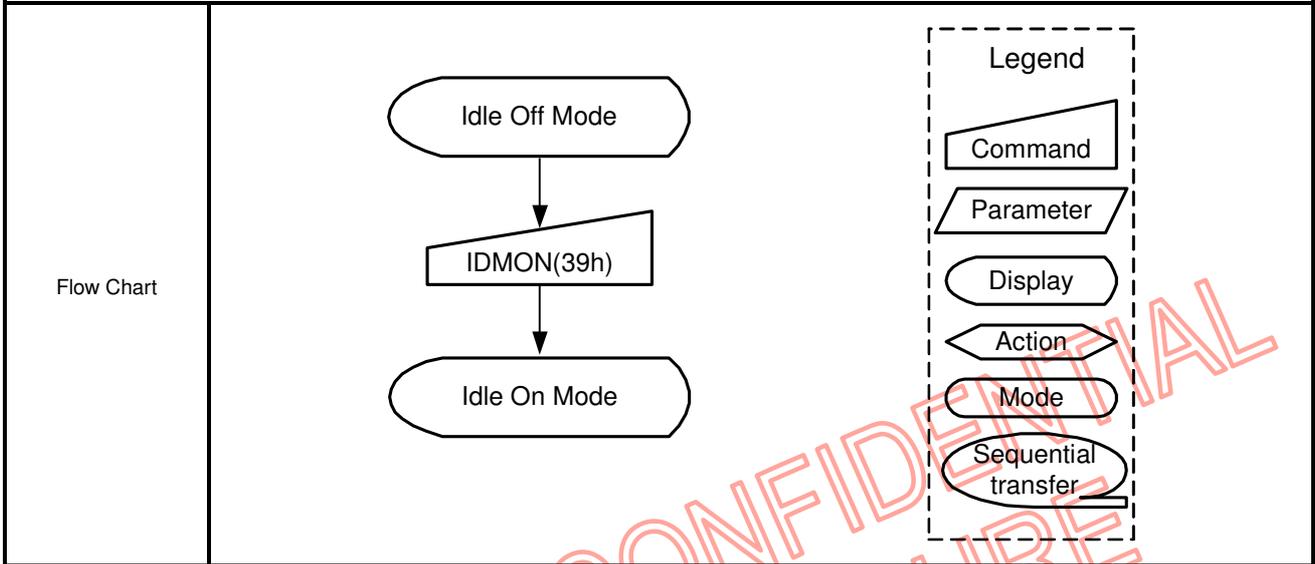


6.1.37 IDMON: Idle Mode On (39h)

Inst / Para	R/W	Address		Parameter							
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1
IDMON	Write	39h	3900h	No Parameter							

NOTE: “-“ Don't care

Description	<p>This command is used to enter into Idle mode on. In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G, and B in Frame Memory, 8 color depth data is displayed.</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Memory</p>  </div> <div style="font-size: 2em; margin: 0 20px;">→</div> <div style="text-align: center;"> <p>Display</p>  </div> </div>																																							
	<table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th colspan="4">Memory Contents vs. Display Colors</th> </tr> <tr> <th></th> <th>R₇R₆R₅R₄R₃R₂R₁R₀</th> <th>R₇G₆G₅G₄G₃G₂G₁G₀</th> <th>B₇B₆B₅B₄B₃B₂B₁B₀</th> </tr> </thead> <tbody> <tr> <td>Black</td> <td>0XXXXXXXX</td> <td>0XXXXXXXX</td> <td>0XXXXXXXX</td> </tr> <tr> <td>Blue</td> <td>0XXXXXXXX</td> <td>0XXXXXXXX</td> <td>1XXXXXXXX</td> </tr> <tr> <td>Red</td> <td>1XXXXXXXX</td> <td>0XXXXXXXX</td> <td>0XXXXXXXX</td> </tr> <tr> <td>Magenta</td> <td>1XXXXXXXX</td> <td>0XXXXXXXX</td> <td>1XXXXXXXX</td> </tr> <tr> <td>Green</td> <td>0XXXXXXXX</td> <td>1XXXXXXXX</td> <td>0XXXXXXXX</td> </tr> <tr> <td>Cyan</td> <td>0XXXXXXXX</td> <td>1XXXXXXXX</td> <td>1XXXXXXXX</td> </tr> <tr> <td>Yellow</td> <td>1XXXXXXXX</td> <td>1XXXXXXXX</td> <td>0XXXXXXXX</td> </tr> <tr> <td>White</td> <td>1XXXXXXXX</td> <td>1XXXXXXXX</td> <td>1XXXXXXXX</td> </tr> </tbody> </table>	Memory Contents vs. Display Colors					R ₇ R ₆ R ₅ R ₄ R ₃ R ₂ R ₁ R ₀	R ₇ G ₆ G ₅ G ₄ G ₃ G ₂ G ₁ G ₀	B ₇ B ₆ B ₅ B ₄ B ₃ B ₂ B ₁ B ₀	Black	0XXXXXXXX	0XXXXXXXX	0XXXXXXXX	Blue	0XXXXXXXX	0XXXXXXXX	1XXXXXXXX	Red	1XXXXXXXX	0XXXXXXXX	0XXXXXXXX	Magenta	1XXXXXXXX	0XXXXXXXX	1XXXXXXXX	Green	0XXXXXXXX	1XXXXXXXX	0XXXXXXXX	Cyan	0XXXXXXXX	1XXXXXXXX	1XXXXXXXX	Yellow	1XXXXXXXX	1XXXXXXXX	0XXXXXXXX	White	1XXXXXXXX	1XXXXXXXX
Memory Contents vs. Display Colors																																								
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Black	0XXXXXXXX	0XXXXXXXX	0XXXXXXXX																																					
Blue	0XXXXXXXX	0XXXXXXXX	1XXXXXXXX																																					
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Restriction	This command has no effect when module is already in idle off mode																																							
Register Availability	<table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																											
Status	Availability																																							
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Status	Default Value																																							
Power On Sequence	Idle Mode off																																							
S/W Reset	Idle Mode off																																							
H/W Reset	Idle Mode off																																							



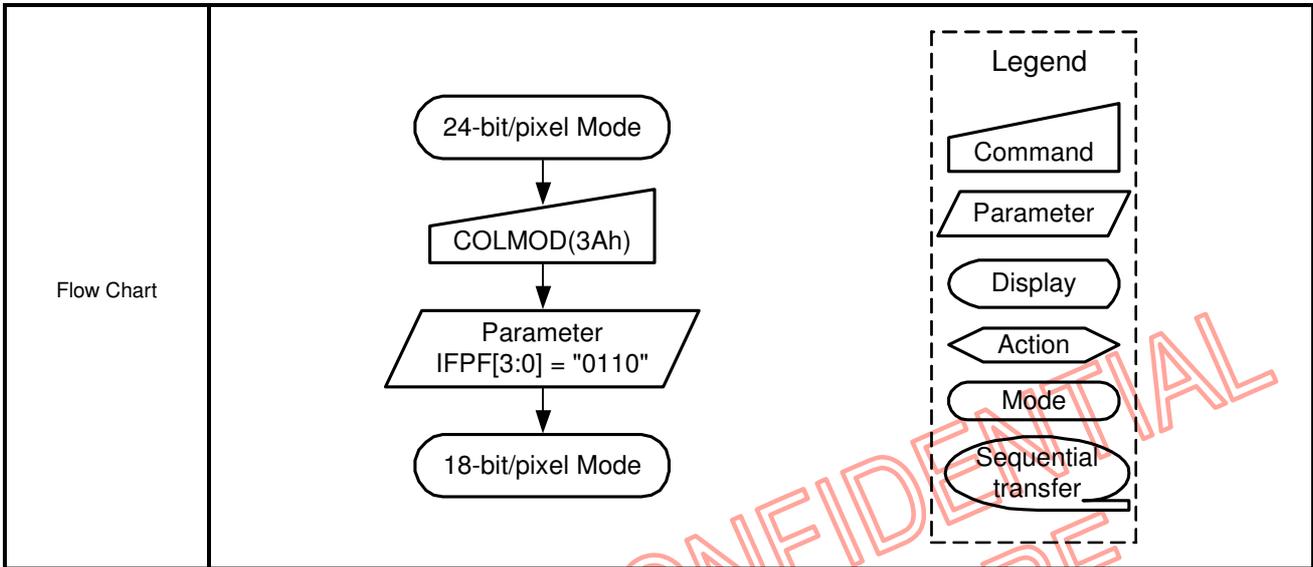
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6.1.38 COLMOD: Interface Pixel Format (3Ah)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
COLMOD	Write	3Ah	X	X	VIPF3	VIPF2	VIPF1	VIPF0	IFPF3	IFPF2	IFPF1	IFPF0	

NOTE: “-“ Don't care

Description	This command is used to define the format of RGB picture data, which is to be transferred via the RGB interface. The formats are shown in the table:	
	Bit	NAME
	VIPF3	Pixel Format for RGB Interface
	VIPF2	
	VIPF1	
	VIPF0	
	IFPF3	Pixel Format for Control Interface
	IFPF2	
	IFPF1	
	IFPF0	
DESCRIPTION		
“0101” = 16-bit/pixel		
“0110” = 18-bit/pixel		
“0111” = 24-bit/pixel		
The others = not defined		
“0101” = 16-bit/pixel		
“0110” = 18-bit/pixel		
“0111” = 24-bit/pixel		
The others = not defined		
Restriction	There is no visible effect until the Frame Memory is written to.	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	77h
	S/W Reset	77h
	H/W Reset	77h



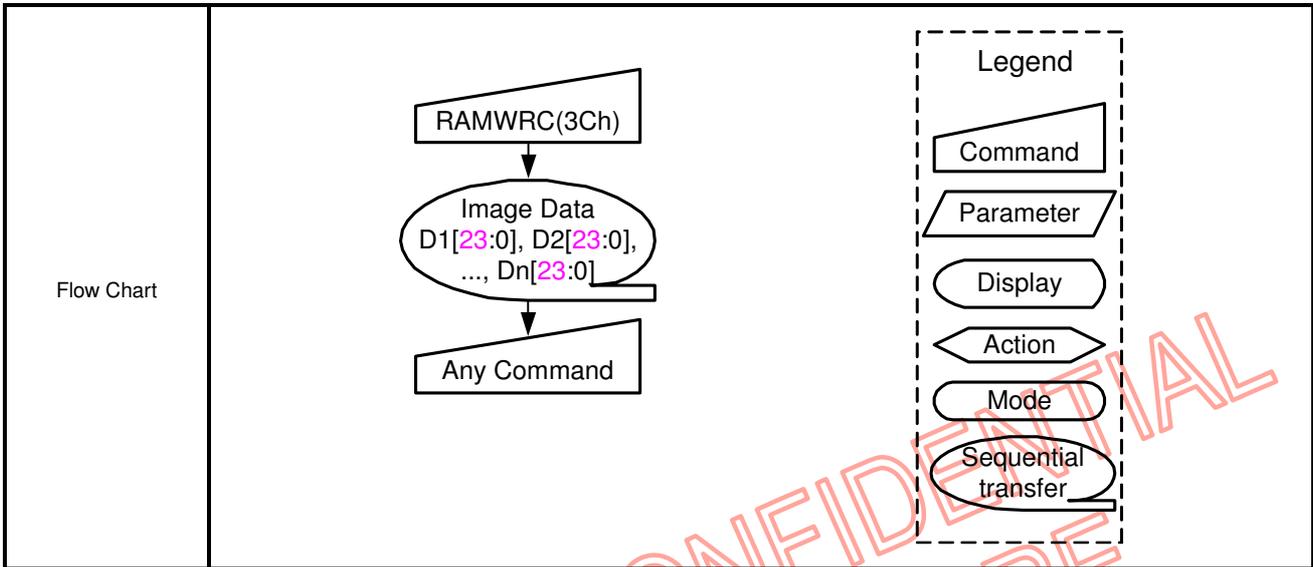
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NO DISCLOSURE

6.1.39 RAMWRC: Memory Write Continue (3Ch)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RAMWRC	Write	3Ch	X	X	D7	D6	D5	D4	D3	D2	D1	D0
					:	:	:	:	:	:	:	:
					D7	D6	D5	D4	D3	D2	D1	D0

NOTE: “-“ Don't care

Description	<p>This command is used to transfer data from MPU interface to frame memory, if there is wanted to continue memory write after “RAMWR Memory Write (2Ch)” command.</p> <p>This command makes no change to the other driver status.</p> <p>When this command is accepted, the column register and the row register are not reset to the Start Column/Start Row positions.</p> <p>The Start Column/Start Row positions are different in accordance with MADCTL setting</p> <p>Then D[23:0] is stored in frame memory and the column register and the row register incremented.</p> <p>Sending any other command can stop Frame Write.</p>												
Restriction	There is no restriction on length of parameters. No access in the frame memory in Sleep In mode												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Set randomly (RAMKP=0) Not cleared (RAMKP=1)</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is set randomly</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Set randomly (RAMKP=0) Not cleared (RAMKP=1)	H/W Reset	Contents of memory is set randomly				
Status	Default Value												
Power On Sequence	Contents of memory is set randomly												
S/W Reset	Set randomly (RAMKP=0) Not cleared (RAMKP=1)												
H/W Reset	Contents of memory is set randomly												



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6.1.40 RAMRDC: Memory Read Continue (3Eh)

Inst / Para	R/W	Address			Parameter							
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RAMRDC	Read	3Eh	X	X	D7	D6	D5	D4	D3	D2	D1	D0
			X	X	:	:	:	:	:	:	:	:
			X	X	D7	D6	D5	D4	D3	D2	D1	D0

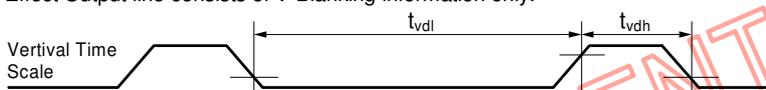
NOTE: “-“ Don't care

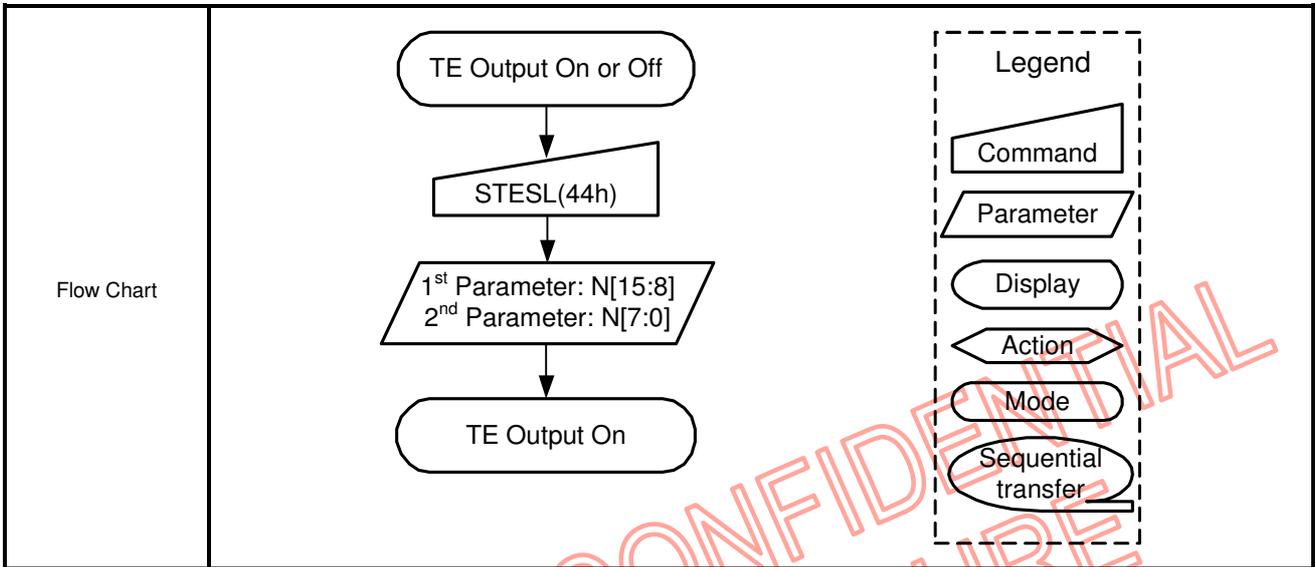
Description	<p>This command is used to transfer data from frame memory to MPU interface, if there is wanted to continue memory read after “RAMRD Memory Read (2Eh)” command.</p> <p>This command makes no change to the other driver status.</p> <p>When this command is accepted, the column register and the row register are not reset to the Start Column/Start Row positions.</p> <p>The Start Column/Start Row positions are different in accordance with MADCTL setting.</p> <p>Then D[23:0] is read back from the frame memory and the column register and the row register incremented</p> <p>Frame Read can be canceled by sending any other command.</p>												
Restriction	There is no restriction on length of parameters. No access in the frame memory in Sleep In mode												
Register Availability	<table border="1" style="width: 100%;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Set randomly (RAMKP=0) Not cleared (RAMKP=1)</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is set randomly</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Set randomly (RAMKP=0) Not cleared (RAMKP=1)	H/W Reset	Contents of memory is set randomly				
Status	Default Value												
Power On Sequence	Contents of memory is set randomly												
S/W Reset	Set randomly (RAMKP=0) Not cleared (RAMKP=1)												
H/W Reset	Contents of memory is set randomly												
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <pre> graph TD A[RAMWRC(3Ch)] --> B([Image Data D1[23:0], D2[23:0], ..., Dn[23:0]]) B --> C[Any Command] </pre> </div> <div style="flex: 1; border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>												

6.1.41 STESL: Set Tearing Effect Scan Line (44h)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
STESL	Write	44h	4400h	00h	N[15:8]								
			4401h	00h	N[7:0]								

NOTE: "-" Don't care

Description	<p>This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing MADCTL bit ML.</p> <p>The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line mode. The Tearing Effect Output line consists of V-Blanking information only.</p>  <p>Note that STESL with N[15:0]="000h" is equivalent to TEON with M="0"</p> <p>The Tearing Effect Output line shall be active low when the display module is in Sleep in mode.</p> <p>This command takes affect on the frame following the current frame. Therefore, if the TE output is already on, the TE output shall continue to operate as programmed by the previous "TEON (35h)" or "STESL (44h) command" until the end of the frame.</p>												
Restriction	<p>When N[15:0] is greater than maximum scanning line like below, data of out of range will be ignored.</p> <p>For DISP[1:0] = "00" (360 x 640 resolution) Parameter range $0 \leq N[15:0] \leq 640$ (0280h)</p> <p>For DISP [1:0] = "01" (360 x 480 resolution) Parameter range $0 \leq N[15:0] \leq 480$ (01E0h)</p> <p>For DISP [1:0] = "10" (320 x 480 resolution) Parameter range $0 \leq N[15:0] \leq 480$ (01E0h)</p>												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
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Status	Default Value												
Power On Sequence	0000h												
S/W Reset	0000h												
H/W Reset	0000h												

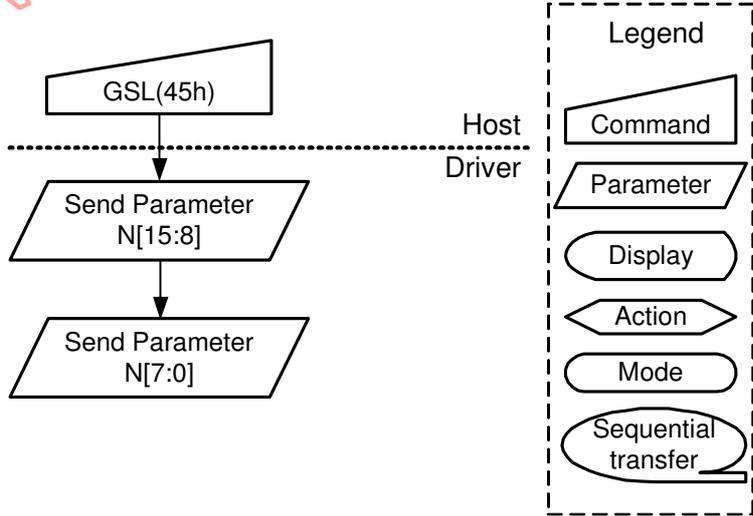


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6.1.42 GSL: Get Scan Line (45h)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
GSL	Read	45h	4500h	00h	N[15:8]								
			4501h	00h	N[7:0]								

NOTE: "- Don't care

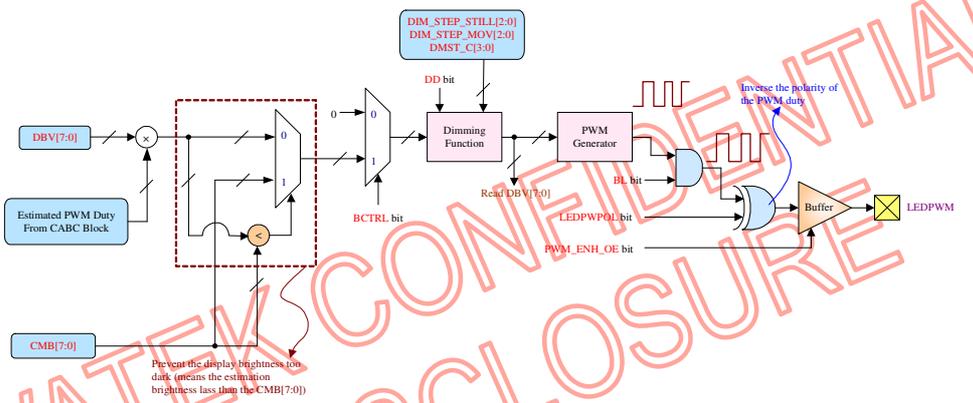
Description	<p>This command returns the current scan line, N, used to update the display module. The total number of scan lines on display is defined as VSYNC + VBP + VADR + VFP. The first scan line is defined as the first line of V Sync and is denoted as Line 0.</p> <p>When in Sleep in mode, the returned value is undefined.</p>												
Restriction	-												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>XXXXh</td> </tr> <tr> <td>S/W Reset</td> <td>XXXXh</td> </tr> <tr> <td>H/W Reset</td> <td>XXXXh</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	XXXXh	S/W Reset	XXXXh	H/W Reset	XXXXh				
Status	Default Value												
Power On Sequence	XXXXh												
S/W Reset	XXXXh												
H/W Reset	XXXXh												
Flow Chart													

6.1.43 WRDISBV: Write Display Brightness (51h)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
WRDISBV	Write	51h	5100h	00h	DBV[7:0]								

NOTE: "-" Don't care

This command is used to adjust the brightness value of the display.
 It should be checked what relationship between value and output brightness of the display.
 This relationship is defined on the display module specification.
 In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.



Prevent the display brightness too dark (means the estimation brightness less than the CMB[7:0])

DBV[7:0]	PWM Duty
00	Off (Default)
01	2/256
02	3/256
03	4/256
:	
:	
:	
FE	255/256
FF	1

Restriction	The display supplier cannot use this command for tuning. (e.g. factory tuning, etc.)	
Register Available	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h

6.1.44 RDISBV: Read Display Brightness (52h)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDISBV	Read	52h	5200h	00h	DBV[7:0]								

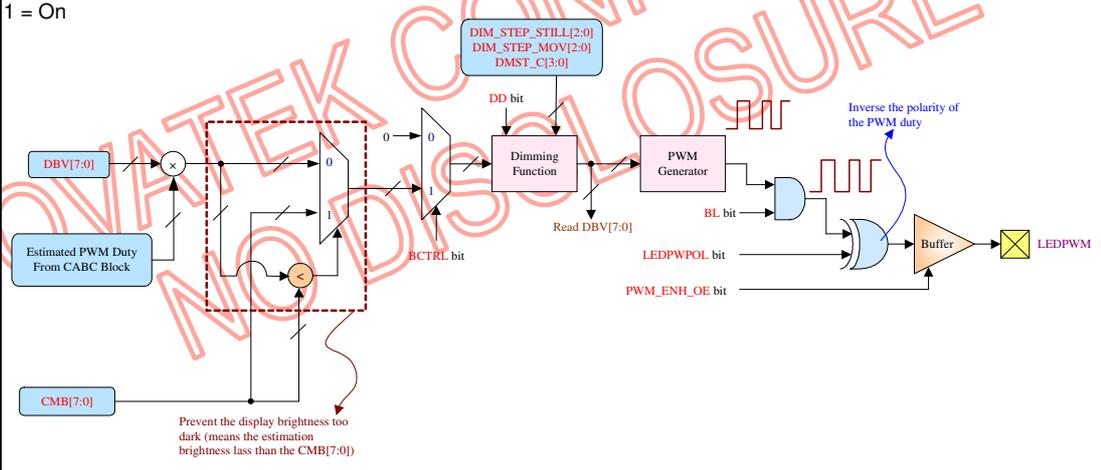
NOTE: “-“ Don't care

Description	<p>This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification.</p> <p>In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p> <p>This command can be used to read the brightness value of the display also when display brightness control is in automatic mode. See the chapter “6.1.37 Write CTRL Display (53h)” bit BCTRL = “1”.</p> <p>DBV[7:0] is reset when display is in sleep-in mode.</p> <p>DBV[7:0] is ‘FFh’ when bit BCTRL of “6.1.37 Write CTRL Display (53h)” command is ‘0’.</p> <p>DBV[7:0] is manual set brightness specified with “6.1.37 Write CTRL Display (53h)” command when bit BCTRL is ‘1’</p>												
Restriction													
Register Available	<table border="1" style="width: 100%;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												
Flow Chart	-												

6.1.45 WRCTRLD: Write CTRL Display (53h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
WRCTRLD	Write	53h	5300h	00h	-	-	BCTRL	-	DD	BL	-	-

NOTE: “-“ Don't care

Description	<p>This command is used to set back-light control mechanism.</p> <p>BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off (Default) 1 = Brightness registers are active, according to the other parameters.</p> <p>DD : Display Dimming: DD = 0: Display Dimming is Off (Default) DD = 1: Display Dimming is On</p> <p>BL: Backlight Control On/Off 0 = Completely turn off backlight circuit. Control lines must be low. (default) 1 = On</p>  <p style="font-size: small;">Prevent the display brightness too dark (means the estimation brightness less than the CMB[7:0])</p>												
Restriction													
Register Available	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

6.1.46 RDCTRLD: Read CTRL Display Value (54h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDCTRLD	Read	54h	5400h	00h	-	-	BCTRL	-	DD	BL	-	-

NOTE: "- "Don't care"

Description	<p>This command returns ambient light and brightness control values, see chapter: "5.1.45 Write CTRL Display (53h)".</p> <p>BCTRL: Brightness Control Block ON/OFF. This bit is always used to switch brightness for display. 0 = OFF (Brightness registers are 00h, DBV[7..0]) 1 = ON (Brightness registers are active, according to the other parameters.)</p> <p>Display Dimming (DD): DD = 0: Display Dimming is off DD = 1: Display Dimming is on</p> <p>BL: Backlight Control On/Off 0 = OFF (Completely turn off backlight circuit. Control lines must be low.) 1 = ON</p> <p>Dimming function is adapted to the brightness registers for display and keyboard when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0.</p> <p>When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.</p>												
Restriction													
Register Available	<table border="1" style="width: 100%;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												
Flow Chart	-												

6.1.47 WRCABC: Write Content Adaptive Brightness Control (55h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
WRCABC	Write	55h	5500h	00h	-	-	-	-	-	-	CABC1	CABC0

NOTE: "- " Don't care

Description	<p>This command is used to set parameters for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality which are defined on a table below.</p> <table border="1"> <thead> <tr> <th>CABC1</th> <th>CABC0</th> <th>Function Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>OFF (Default)</td> </tr> <tr> <td>0</td> <td>1</td> <td>UI (User Interface Image)</td> </tr> <tr> <td>1</td> <td>0</td> <td>Still Picture</td> </tr> <tr> <td>1</td> <td>1</td> <td>Moving Image</td> </tr> </tbody> </table> <p>A Content Adaptive Brightness Control function can be used to reduce the power consumption of the luminance source. Content adaptation means that content grey level scale can be increased while simultaneously lowering brightness of the backlight to achieve same perceived brightness. The adjusted grey level scale and thus the power consumption reduction depends on the content of the image.</p> <p>Definition of Modes and target power reduction ratio:</p> <p>OFF mode: Content Adaptive Brightness Control functionality is totally off.</p> <p>UI [User interface] image mode: Optimized for UI image. It is kept image quality as much as possible. Target power consumption reduction ratio: 10% or less.</p> <p>Still picture mode: Optimized for still picture. Some image quality degradation would be acceptable. Target power consumption reduction ratio: more than 30%.</p> <p>Moving image mode: Optimized for moving image. It is focused on the biggest power reduction with image quality degradation. Target power consumption reduction ratio: more than 30%.</p>	CABC1	CABC0	Function Description	0	0	OFF (Default)	0	1	UI (User Interface Image)	1	0	Still Picture	1	1	Moving Image
	CABC1	CABC0	Function Description													
0	0	OFF (Default)														
0	1	UI (User Interface Image)														
1	0	Still Picture														
1	1	Moving Image														
Restriction	<ul style="list-style-type: none"> - Limits of image degradation are needed to agree with system and module suppliers. - CABC is only used for normal mode. 															
Register Available	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes			
Status	Availability															
Normal Mode On, Idle Mode Off, Sleep Out	Yes															
Normal Mode On, Idle Mode On, Sleep Out	Yes															
Partial Mode On, Idle Mode Off, Sleep Out	Yes															
Partial Mode On, Idle Mode On, Sleep Out	Yes															
Sleep In	Yes															

Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
	Status	Default Value								
	Power On Sequence	00h								
	S/W Reset	00h								
H/W Reset	00h									
Flow Chart	-									

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6.1.48 RDCABC: Read Content Adaptive Brightness Control (56h)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDCABC	Read	56h	5600h	00h	-	-	-	-	-	-	-	CABC1	CABC0

NOTE: “-“ Don't care

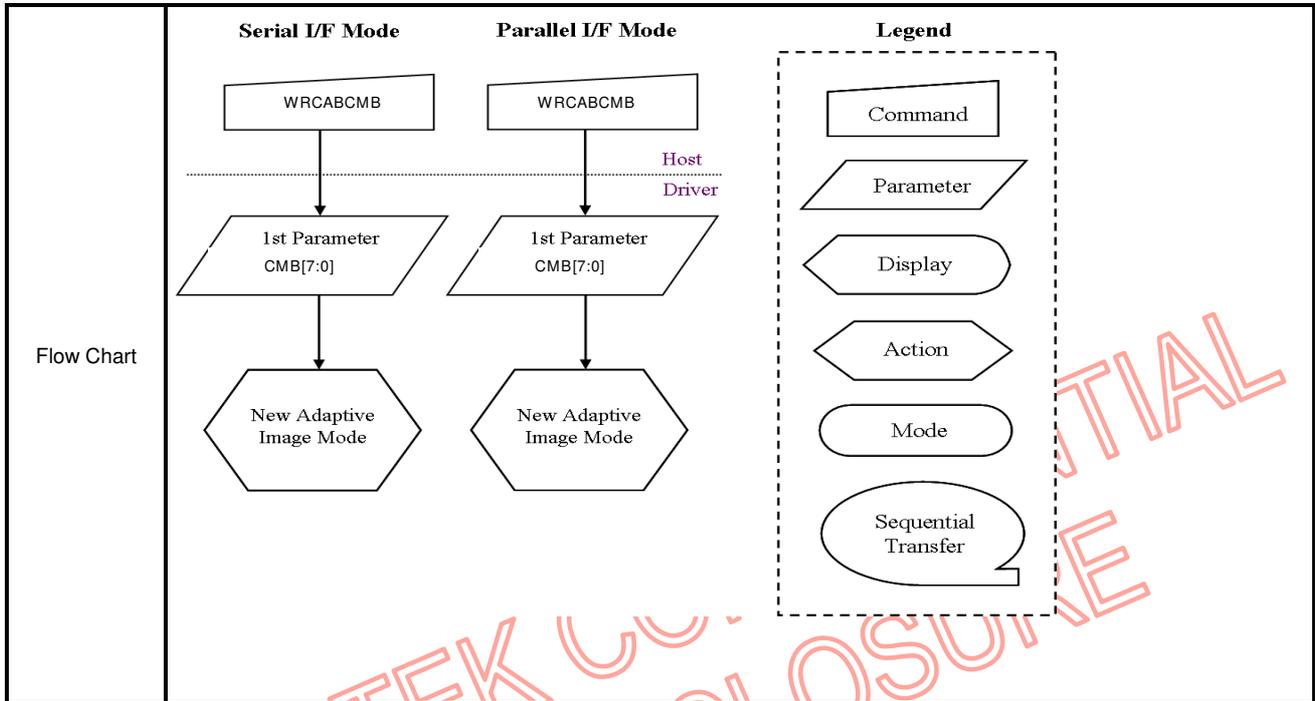
Description	<p>This command is used to read the settings for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality which are defined on a table below.</p> <table border="1"> <thead> <tr> <th>CABC1</th> <th>CABC0</th> <th>Function Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>OFF</td> </tr> <tr> <td>0</td> <td>1</td> <td>User Interface Image</td> </tr> <tr> <td>1</td> <td>0</td> <td>Still Picture</td> </tr> <tr> <td>1</td> <td>1</td> <td>Moving Image</td> </tr> </tbody> </table> <p>A Content Adaptive Brightness Control function can be used to reduce the power consumption of the luminance source. Content adaptation means that content grey level scale can be increased while simultaneously lowering brightness of the backlight to achieve same perceived brightness. The adjusted grey level scale and thus the power consumption reduction depends on the content of the image.</p> <p>Definition of Modes and target power reduction ratio:</p> <p>OFF mode: Content Adaptive Brightness Control functionality is totally off.</p> <p>UI [User interface] image mode: Optimized for UI image. It is kept image quality as much as possible. Target power consumption reduction ratio: 10% or less.</p> <p>Still picture mode: Optimized for still picture. Some image quality degradation would be acceptable. Target power consumption reduction ratio: more than 30%.</p> <p>Moving image mode: Optimized for moving image. It is focused on the biggest power reduction with image quality degradation. Target power consumption reduction ratio: more than 30%.</p>		CABC1	CABC0	Function Description	0	0	OFF	0	1	User Interface Image	1	0	Still Picture	1	1	Moving Image
	CABC1	CABC0	Function Description														
0	0	OFF															
0	1	User Interface Image															
1	0	Still Picture															
1	1	Moving Image															
Restriction	-																
Register Available	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes			
	Status	Availability															
	Normal Mode On, Idle Mode Off, Sleep Out	Yes															
	Normal Mode On, Idle Mode On, Sleep Out	Yes															
	Partial Mode On, Idle Mode Off, Sleep Out	Yes															
Partial Mode On, Idle Mode On, Sleep Out	Yes																
Sleep In	Yes																
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h							
	Status	Default Value															
	Power On Sequence	00h															
	S/W Reset	00h															
H/W Reset	00h																

6.1.49 WRCABCMB: Write CABC minimum brightness (5Eh)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
WRCABCMB	Write	5Eh	5E00h	00h	CMB[7:0]								

NOTE: "-“ Don't care

Description	<p>This command is used to set the minimum brightness value of the display for CABC function. Because the CABC function can reduce the backlight brightness automatically based on different image contents. In some application of the combination with manual brightness setting, display brightness is too dark. So it is necessary to avoid apparently image quality degradation.</p> <p>CABC minimum brightness setting is to avoid too much brightness reduction. In other words, CABC can not reduce the display brightness to less than CABC minimum brightness setting. This function does not affect to the other function manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal. When display brightness is turned off ("BCTRL" = '0'), CABC minimum brightness setting is ignored.</p> <p>In principle relationship, the 00h value means the lowest brightness for CABC, and FFh value means the highest brightness for CABC.</p>												
Restriction	The display supplier does not need to use this command for tuning..												
Register Available	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>CMB[7:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	CMB[7:0]	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	CMB[7:0]												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												



6.1.50 RDCABCMB: Read CABC minimum brightness (5Fh)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDCABCMB	Read	5Fh	5F00h	00h	CMB[7:0]								

NOTE: "-" Don't care

Description	This command returns the minimum brightness value of CABC function. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. CMB[7:0] is CABC minimum brightness specified with CABC minimum brightness (5Eh) command													
Restriction	-													
Register Available	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
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Partial Mode On, Idle Mode Off, Sleep Out	Yes													
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Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>CMB[7:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	CMB[7:0]	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h					
Status	CMB[7:0]													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	-													

6.1.51 RDABCSDR: Read Automatic Brightness Control Self-Diagnostic Result (68h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDABCSDR	Read	68h	6800h	00h	D7	D6	0	0	0	0	0	0

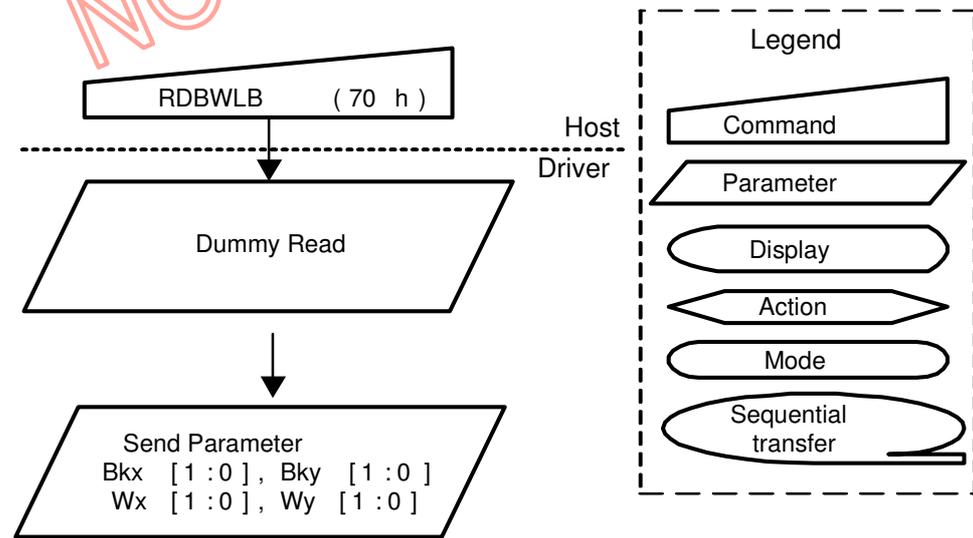
NOTE: "-" Don't care

Description	This command indicates the current status of the display self-diagnostic results for automatic brightness control after Sleep Out –command as described in the table below:																											
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>Register Loading Detection</td> <td>See section 5.12</td> </tr> <tr> <td>D6</td> <td>Functionality Detection</td> <td></td> </tr> <tr> <td>D5</td> <td>Not Used</td> <td>"0"</td> </tr> <tr> <td>D4</td> <td>Not Used</td> <td>"0"</td> </tr> <tr> <td>D3</td> <td>Not Used</td> <td>"0"</td> </tr> <tr> <td>D2</td> <td>Not Used</td> <td>"0"</td> </tr> <tr> <td>D1</td> <td>Not Used</td> <td>"0"</td> </tr> <tr> <td>D0</td> <td>Not Used</td> <td>"0"</td> </tr> </tbody> </table>	Bit	Description	Value	D7	Register Loading Detection	See section 5.12	D6	Functionality Detection		D5	Not Used	"0"	D4	Not Used	"0"	D3	Not Used	"0"	D2	Not Used	"0"	D1	Not Used	"0"	D0	Not Used	"0"
Bit	Description	Value																										
D7	Register Loading Detection	See section 5.12																										
D6	Functionality Detection																											
D5	Not Used	"0"																										
D4	Not Used	"0"																										
D3	Not Used	"0"																										
D2	Not Used	"0"																										
D1	Not Used	"0"																										
D0	Not Used	"0"																										
Restriction	-																											
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes														
	Status	Availability																										
Normal Mode On, Idle Mode Off, Sleep Out	Yes																											
Normal Mode On, Idle Mode On, Sleep Out	Yes																											
Partial Mode On, Idle Mode Off, Sleep Out	Yes																											
Partial Mode On, Idle Mode On, Sleep Out	Yes																											
Sleep In	Yes																											
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value (D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>0000_0000 (00h)</td> </tr> <tr> <td>S/W Reset</td> <td>0000_0000 (00h)</td> </tr> <tr> <td>H/W Reset</td> <td>0000_0000 (00h)</td> </tr> </tbody> </table>		Status	Default Value (D7 to D0)	Power On Sequence	0000_0000 (00h)	S/W Reset	0000_0000 (00h)	H/W Reset	0000_0000 (00h)																		
Status	Default Value (D7 to D0)																											
Power On Sequence	0000_0000 (00h)																											
S/W Reset	0000_0000 (00h)																											
H/W Reset	0000_0000 (00h)																											
Flow Chart																												

6.1.52 RDBWLB: Read Black/White Low Bits (70h)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDBWLB	Read	70h	7000h	00h	Bkx1	Bkx0	Bky1	Bky0	Wx1	Wx0	Wy1	Wy0	

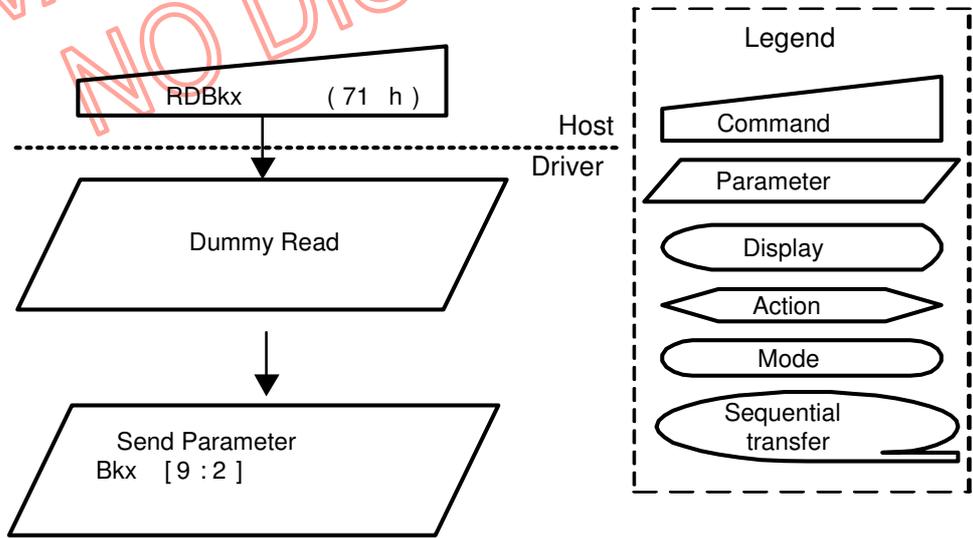
NOTE: “-“ Don't care

Description	This command returns the lowest bits of black and white color characteristic. Black: Bkx and Bky White: Wx and Wy													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>70h</td> </tr> <tr> <td>S/W Reset</td> <td>No Change</td> </tr> <tr> <td>H/W Reset</td> <td>70h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	70h	S/W Reset	No Change	H/W Reset	70h				
Status	Default Value													
Power On Sequence	70h													
S/W Reset	No Change													
H/W Reset	70h													
Flow Chart														

6.1.53 RDBkx: Read Bkx (71h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBkx	Read	71h	7100h	00h	Bkx9	Bkx8	Bkx7	Bkx6	Bkx5	Bkx4	Bkx3	Bkx2

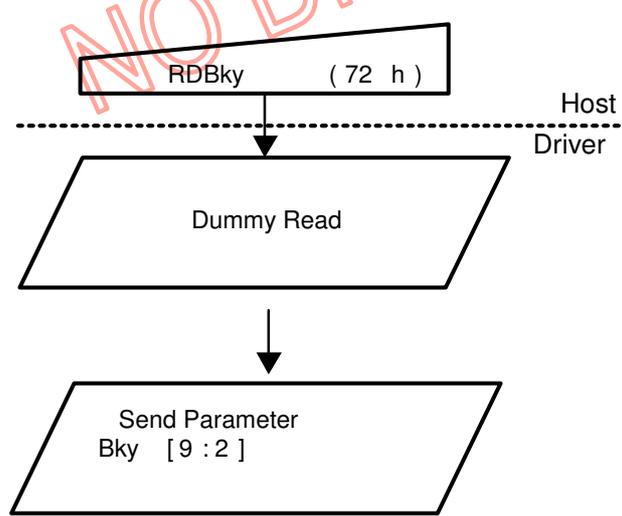
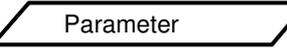
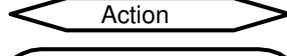
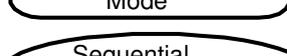
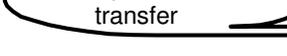
NOTE: "- Don't care

Description	This command returns the Bkx bit (Bkx[9:2]) of black color characteristic.	
Restriction	-	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	71h
	S/W Reset	No Change
	H/W Reset	71h
Flow Chart		

6.1.54 RDBky: Read Bky (72h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBky	Read	72h	7200h	00h	Bky9	Bky8	Bky7	Bky6	Bky5	Bky4	Bky3	Bky2

NOTE: “-“ Don't care

Description	This command returns the Bky bit (Bky[9:2]) of black color characteristic.	
Restriction	-	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	72h
	S/W Reset	No Change
	H/W Reset	72h
Flow Chart		
	<div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none">  Command  Parameter  Display  Action  Mode  Sequential transfer </div>	

6.1.55 RDWx: Read Wx (73h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDWx	Read	73h	7300h	00h	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2

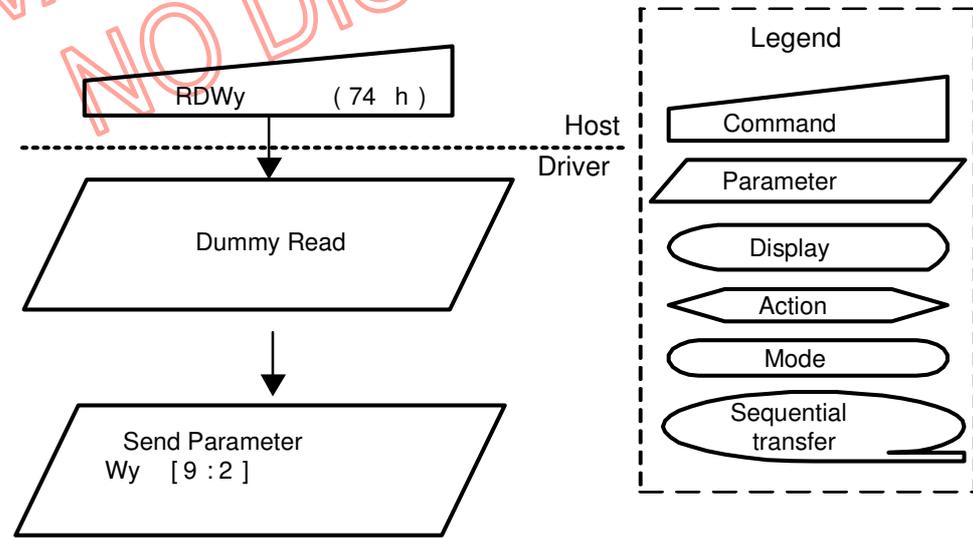
NOTE: “-“ Don't care

Description	This command returns the Wx bit (Wx[9:2]) of white color characteristic.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>36h</td> </tr> <tr> <td>S/W Reset</td> <td>No Change</td> </tr> <tr> <td>H/W Reset</td> <td>36h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	36h	S/W Reset	No Change	H/W Reset	36h				
Status	Default Value													
Power On Sequence	36h													
S/W Reset	No Change													
H/W Reset	36h													
Flow Chart														

6.1.56 RDWy: Read Wy (74h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDWy	Read	74h	7400h	00h	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2

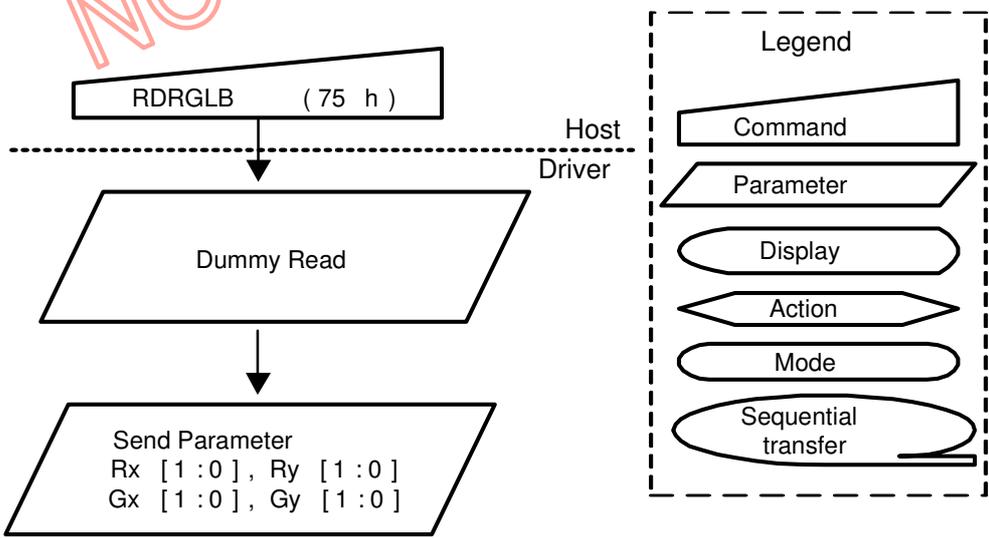
NOTE: “-“ Don't care

Description	This command returns the Wy bit (Wy[9:2]) of white color characteristic.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>4Ah</td> </tr> <tr> <td>S/W Reset</td> <td>No Change</td> </tr> <tr> <td>H/W Reset</td> <td>4Ah</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	4Ah	S/W Reset	No Change	H/W Reset	4Ah				
Status	Default Value													
Power On Sequence	4Ah													
S/W Reset	No Change													
H/W Reset	4Ah													
Flow Chart														

6.1.57 RDRGLB: Read Red/Green Low Bits (75h)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDRGLB	Read	75h	7500h	00h	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy0	

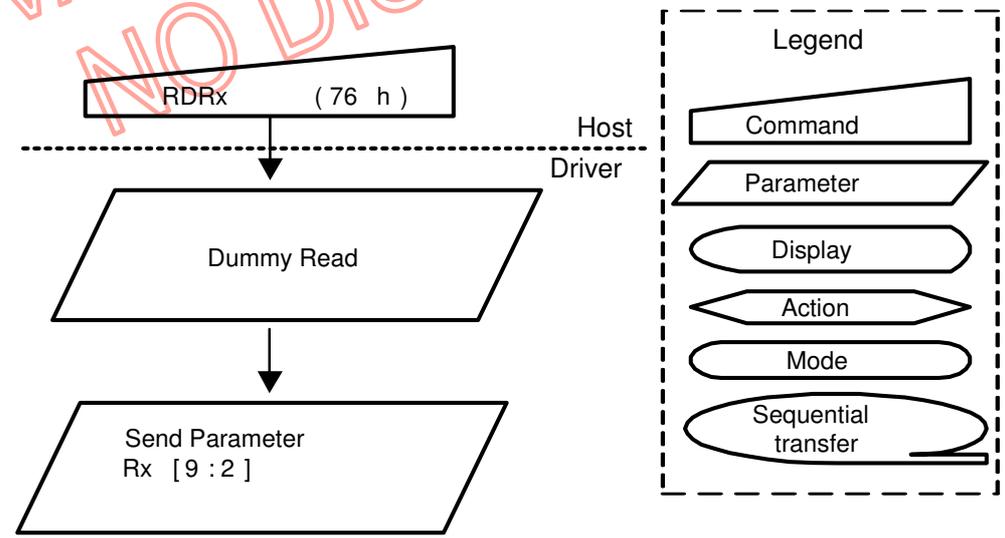
NOTE: "-“ Don't care

Description	This command returns the lowest bits of red and green color characteristic. Red: Rx and Ry Green: Gx and Gy													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>75h</td> </tr> <tr> <td>S/W Reset</td> <td>No Change</td> </tr> <tr> <td>H/W Reset</td> <td>75h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	75h	S/W Reset	No Change	H/W Reset	75h				
Status	Default Value													
Power On Sequence	75h													
S/W Reset	No Change													
H/W Reset	75h													
Flow Chart														

6.1.58 RDRx: Read Rx (76h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDRx	Read	76h	7600h	00h	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2

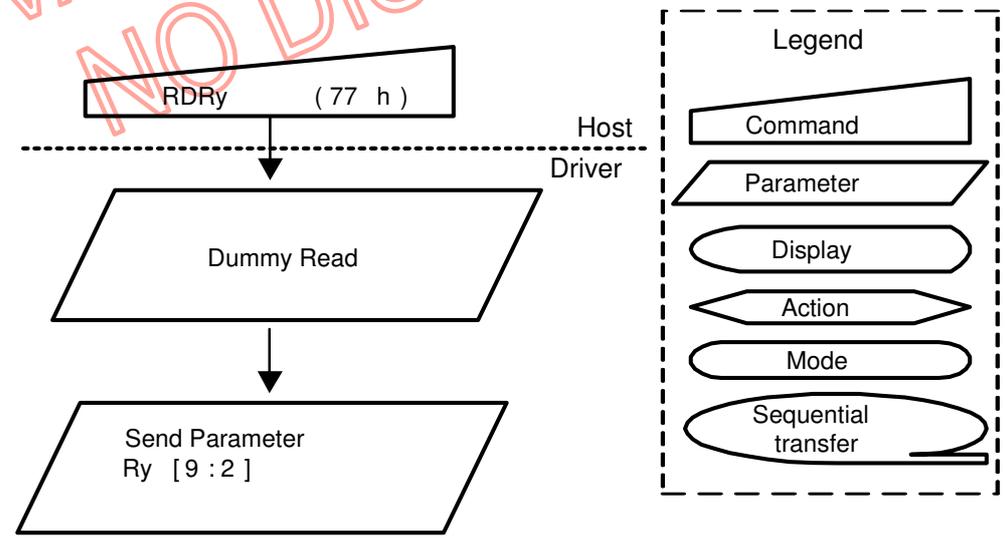
NOTE: "-“ Don't care

Description	This command returns the Rx bit (Rx[9:2]) of red color characteristic.	
Restriction	-	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	80h
	S/W Reset	No Change
	H/W Reset	80h
Flow Chart		

6.1.59 RDRy: Read Ry (77h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDRy	Read	77h	7700h	00h	Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2

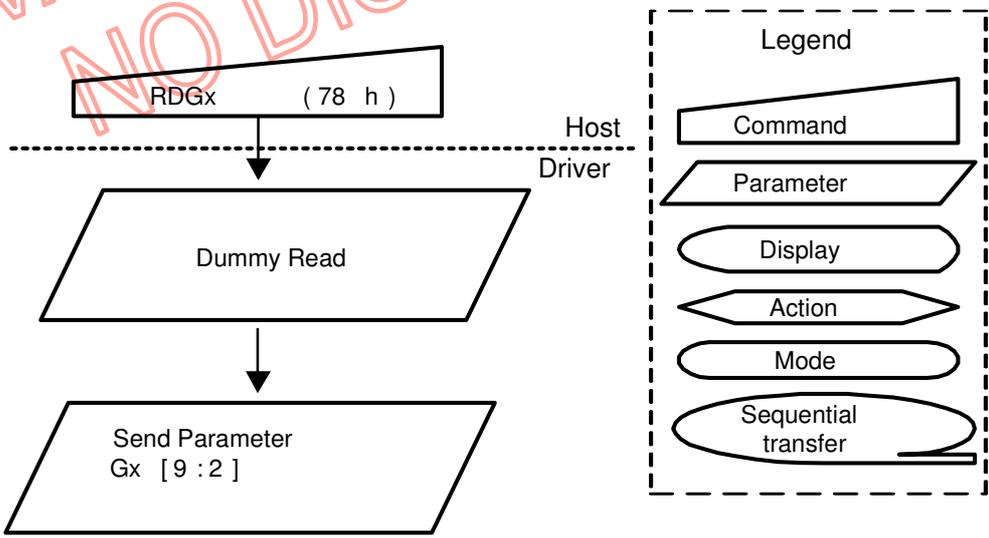
NOTE: “-“ Don't care

Description	This command returns the Ry bit (Ry[9:2]) of red color characteristic.	
Restriction	-	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	4Ah
	S/W Reset	No Change
	H/W Reset	4Ah
Flow Chart		

6.1.60 RDGx: Read Gx (78h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDGx	Read	78h	7800h	00h	Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2

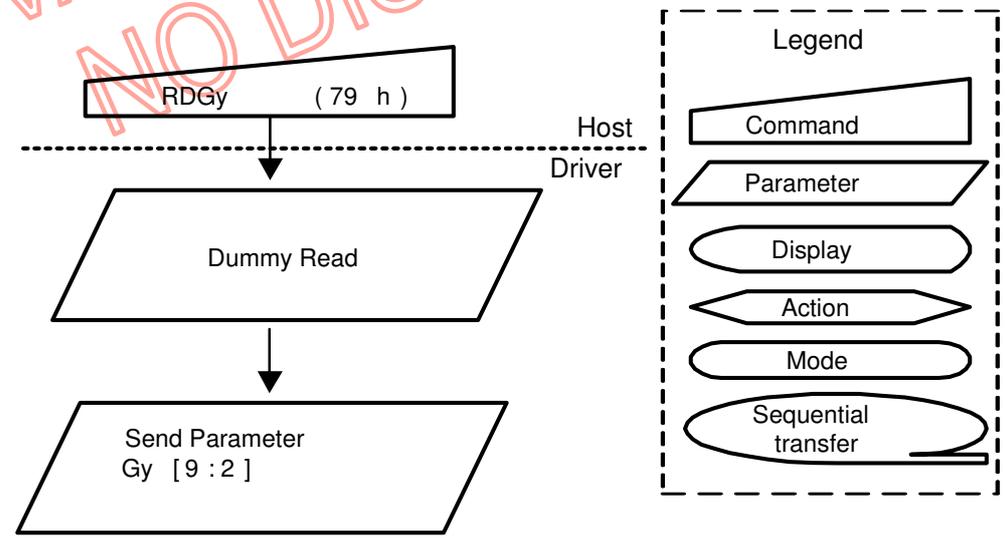
NOTE: "- Don't care"

Description	This command returns the Gx bit (Gx[9:2]) of green color characteristic.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>2Ch</td> </tr> <tr> <td>S/W Reset</td> <td>No Change</td> </tr> <tr> <td>H/W Reset</td> <td>2Ch</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	2Ch	S/W Reset	No Change	H/W Reset	2Ch				
Status	Default Value													
Power On Sequence	2Ch													
S/W Reset	No Change													
H/W Reset	2Ch													
Flow Chart	 <p>The flow chart illustrates the sequence of operations for the RDGx (78 h) command. It starts with a Host sending a Command (RDGx (78 h)) to the Driver. This is followed by a Dummy Read (Parameter) and then the Send Parameter Gx [9 : 2] (Parameter). A legend on the right defines the symbols used: Command (trapezoid), Parameter (parallelogram), Display (rounded rectangle), Action (arrowhead), Mode (oval), and Sequential transfer (oval with a tail).</p>													

6.1.61 RDGy: Read Gy (79h)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDGy	Read	79h	7900h	00h	Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2	

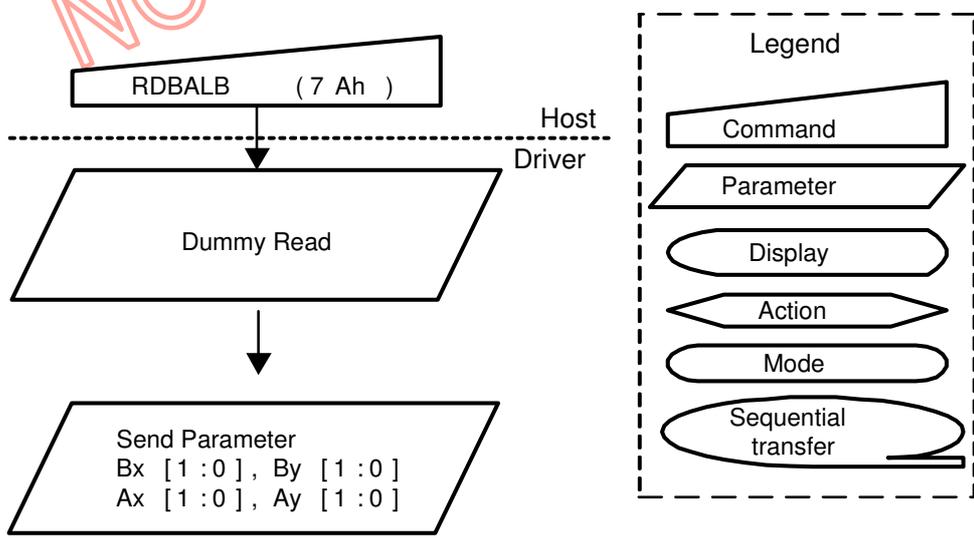
NOTE: "-“ Don't care

Description	This command returns the Gy bit (Gy[9:2]) of green color characteristic.	
Restriction	-	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	58h
	S/W Reset	No Change
	H/W Reset	58h
Flow Chart		

6.1.62 RDBALB: Read Blue/AColor Low Bits (7Ah)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBALB	Read	7Ah	7A00h	00h	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay0

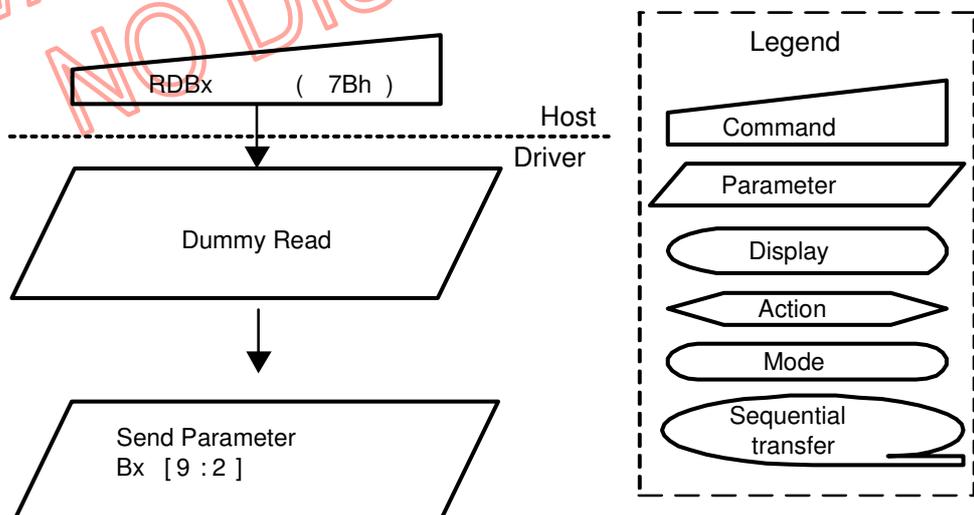
NOTE: “-“ Don't care

Description	This command returns the lowest bits of blue and A color characteristic. Blue: Bx and By A: Ax and Ay													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>70h</td> </tr> <tr> <td>S/W Reset</td> <td>No Change</td> </tr> <tr> <td>H/W Reset</td> <td>70h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	70h	S/W Reset	No Change	H/W Reset	70h				
Status	Default Value													
Power On Sequence	70h													
S/W Reset	No Change													
H/W Reset	70h													
Flow Chart														

6.1.63 RDBx: Read Bx (7Bh)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBx	Read	7Bh	7B00h	00h	Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2

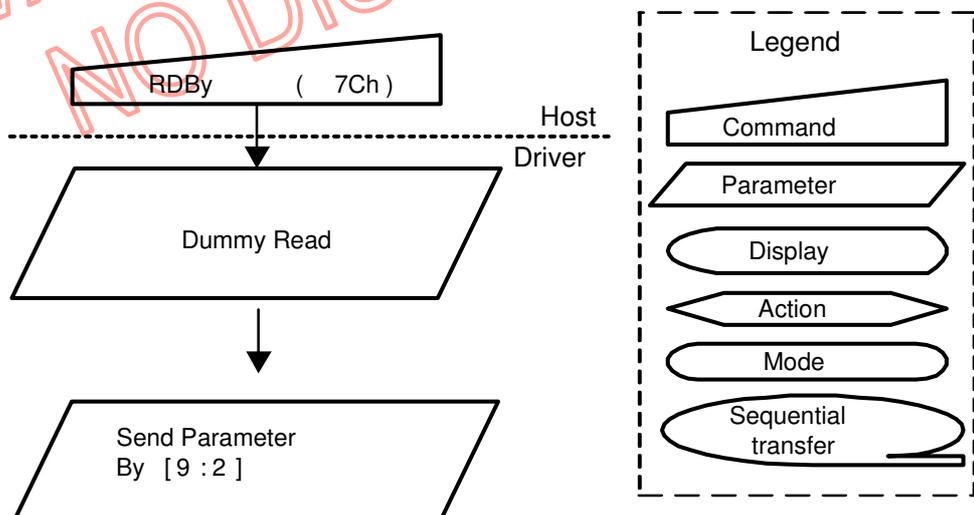
NOTE: “-“ Don't care

Description	This command returns the Bx bit (Bx[9:2]) of blue color characteristic.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>96h</td> </tr> <tr> <td>S/W Reset</td> <td>No Change</td> </tr> <tr> <td>H/W Reset</td> <td>96h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	96h	S/W Reset	No Change	H/W Reset	96h				
Status	Default Value													
Power On Sequence	96h													
S/W Reset	No Change													
H/W Reset	96h													
Flow Chart														

6.1.64 RDBy: Read By (7Ch)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBy	Read	7Ch	7C00h	00h	By9	By8	By7	By6	By5	By4	By3	By2

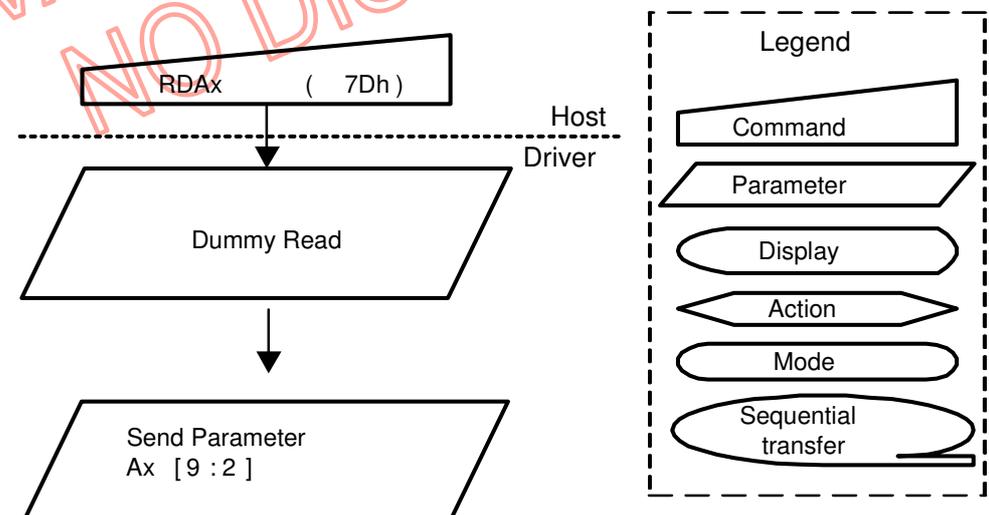
NOTE: “-“ Don't care

Description	This command returns the By bit (By[9:2]) of blue color characteristic.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>3Ch</td> </tr> <tr> <td>S/W Reset</td> <td>No Change</td> </tr> <tr> <td>H/W Reset</td> <td>3Ch</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	3Ch	S/W Reset	No Change	H/W Reset	3Ch				
Status	Default Value													
Power On Sequence	3Ch													
S/W Reset	No Change													
H/W Reset	3Ch													
Flow Chart														

6.1.65 RDAx: Read Ax (7Dh)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDAx	Read	7Dh	7D00h	00h	Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2

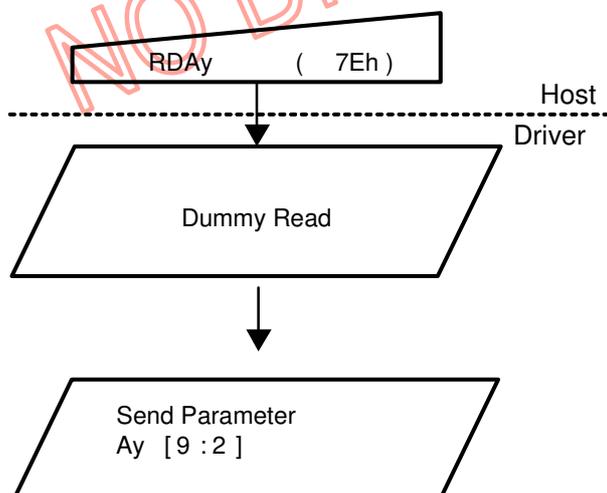
NOTE: "- Don't care

Description	This command returns the Ax bit (Ax[9:2]) of A color characteristic.	
Restriction	-	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	No Change
	H/W Reset	00h
Flow Chart		

6.1.66 RDAy: Read Ay (7Eh)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDAy	Read	7Eh	7E00h	00h	Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	Ay3	Ay2

NOTE: “-“ Don't care

Description	This command returns the Ay bit (Ay[9:2]) of A color characteristic.														
Restriction	-														
Register Availability	Status	Availability													
	Normal Mode On, Idle Mode Off, Sleep Out	Yes													
	Normal Mode On, Idle Mode On, Sleep Out	Yes													
	Partial Mode On, Idle Mode Off, Sleep Out	Yes													
	Partial Mode On, Idle Mode On, Sleep Out	Yes													
	Sleep In	Yes													
Default	Status	Default Value													
	Power On Sequence	00h													
	S/W Reset	No Change													
	H/W Reset	00h													
Flow Chart															
	<table border="1"> <thead> <tr> <th colspan="2">Legend</th> </tr> </thead> <tbody> <tr> <td></td> <td>Command</td> </tr> <tr> <td></td> <td>Parameter</td> </tr> <tr> <td></td> <td>Display</td> </tr> <tr> <td></td> <td>Action</td> </tr> <tr> <td></td> <td>Mode</td> </tr> <tr> <td></td> <td>Sequential transfer</td> </tr> </tbody> </table>		Legend			Command		Parameter		Display		Action		Mode	
Legend															
	Command														
	Parameter														
	Display														
	Action														
	Mode														
	Sequential transfer														

6.1.67 RDDDBS: Read DDB Start (A1h)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDDDBS	Read	A1h	A100h	00h	SID[7:0]								
			A101h	00h	SID[15:8]								
			A102h	00h	MRID[7:0]								
			A103h	00h	MRID[15:8]								
			A104h	00h	1	1	1	1	1	1	1	1	1

NOTE: "-" Don't care

Description	<p>This command returns the supplier identification and display module mode/revision information. <i>Note: This information is not the same what "Read ID1 (DAh)", "Read ID2 (DBh)" and "Read ID3 (DCh)" commands are returning.</i></p> <p>Parameter 1 : (SID[7:0]) : LCD module's manufacturer ID. Parameter 2 : (SID[15:8]) : LCD module/driver version ID. Parameter 3 : (MRID[7:0]) : LCD module/driver ID. Parameter 4 : (MRID[15:8]) : IC version code. Parameter 5 : FFh - Exit code – there is no more data in the Descriptor Block</p> <p>This read sequence can be interrupted by any command and it can be continued by "Read DDB Continue (A8h)" command when the first parameter, what has been transferred, is the parameter, which has not been sent e.g. RDDDBS => 1st parameter has been sent => 2nd parameter has been sent=> interrupt => RDDDBC => 3rd parameter of the RDDDBS has been sent.</p>																													
Restriction	-																													
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																	
Status	Availability																													
Normal Mode On, Idle Mode Off, Sleep Out	Yes																													
Normal Mode On, Idle Mode On, Sleep Out	Yes																													
Partial Mode On, Idle Mode Off, Sleep Out	Yes																													
Partial Mode On, Idle Mode On, Sleep Out	Yes																													
Sleep In	Yes																													
Default	<p>If SID[15:0] & MRID[15:0] MTP are not yet programmed :</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="5">Default Value</th> </tr> <tr> <th>1st Para</th> <th>2nd Para</th> <th>3rd Para</th> <th>4th Para</th> <th>5th Para</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> <td>00h</td> <td>00h</td> <td>00h</td> <td>FFh</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> <td>00h</td> <td>00h</td> <td>00h</td> <td>FFh</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> <td>00h</td> <td>00h</td> <td>00h</td> <td>FFh</td> </tr> </tbody> </table>	Status	Default Value					1 st Para	2 nd Para	3 rd Para	4 th Para	5 th Para	Power On Sequence	00h	00h	00h	00h	FFh	S/W Reset	00h	00h	00h	00h	FFh	H/W Reset	00h	00h	00h	00h	FFh
Status	Default Value																													
	1 st Para	2 nd Para	3 rd Para	4 th Para	5 th Para																									
Power On Sequence	00h	00h	00h	00h	FFh																									
S/W Reset	00h	00h	00h	00h	FFh																									
H/W Reset	00h	00h	00h	00h	FFh																									

	<p>If SID[15:0] & MRID[15:0] MTP were programmed :</p> <table border="1"> <thead> <tr> <th>Status</th> <th colspan="5">Default Value</th> </tr> <tr> <th></th> <th>1st Para</th> <th>2nd Para</th> <th>3rd Para</th> <th>4th Para</th> <th>5th Para</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>(MTP value)</td> <td>(MTP value)</td> <td>(MTP value)</td> <td>(MTP value)</td> <td>FFh</td> </tr> <tr> <td>S/W Reset</td> <td>(MTP value)</td> <td>(MTP value)</td> <td>(MTP value)</td> <td>(MTP value)</td> <td>FFh</td> </tr> <tr> <td>H/W Reset</td> <td>(MTP value)</td> <td>(MTP value)</td> <td>(MTP value)</td> <td>(MTP value)</td> <td>FFh</td> </tr> </tbody> </table> <p><i>Note : SID[15:0] & MRID[15:0] can be programmed by MTP</i></p>	Status	Default Value						1 st Para	2 nd Para	3 rd Para	4 th Para	5 th Para	Power On Sequence	(MTP value)	(MTP value)	(MTP value)	(MTP value)	FFh	S/W Reset	(MTP value)	(MTP value)	(MTP value)	(MTP value)	FFh	H/W Reset	(MTP value)	(MTP value)	(MTP value)	(MTP value)	FFh
Status	Default Value																														
	1 st Para	2 nd Para	3 rd Para	4 th Para	5 th Para																										
Power On Sequence	(MTP value)	(MTP value)	(MTP value)	(MTP value)	FFh																										
S/W Reset	(MTP value)	(MTP value)	(MTP value)	(MTP value)	FFh																										
H/W Reset	(MTP value)	(MTP value)	(MTP value)	(MTP value)	FFh																										
Flow Chart																															

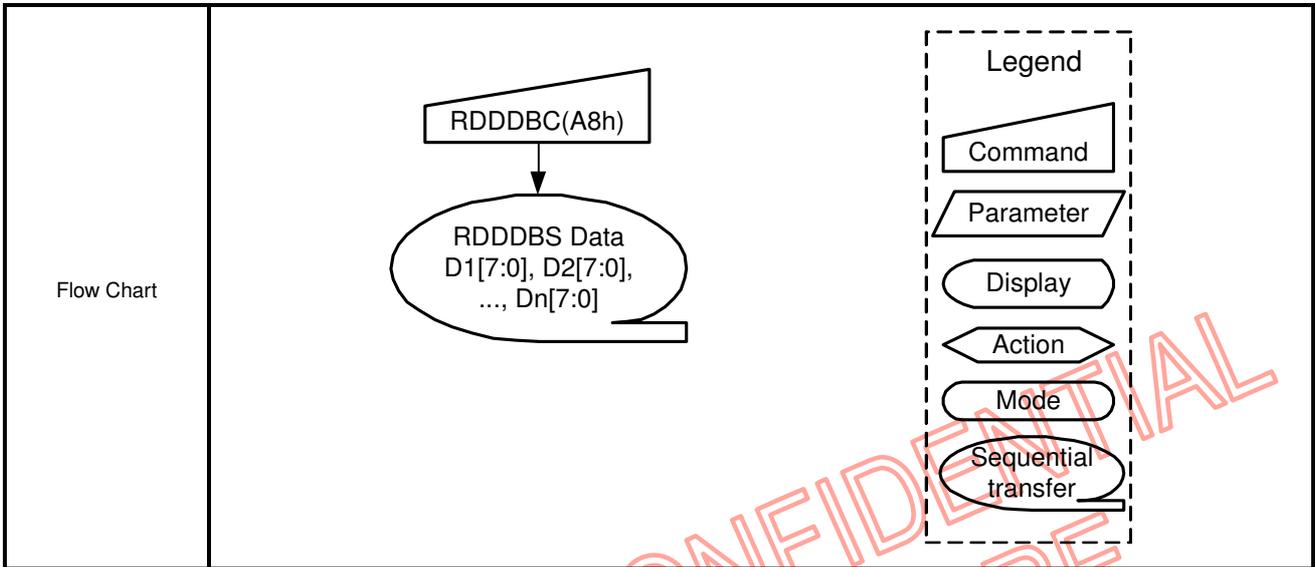
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6.1.68 RDDDBC: Read DDB Continue (A8h)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDDDBS	Read	A8h	A800h	00h	SID[7:0]								
			A801h	00h	SID[15:8]								
			A802h	00h	MRID[7:0]								
			A803h	00h	MRID[15:8]								
			A804h	00h	1	1	1	1	1	1	1	1	1

NOTE: "-" Don't care

Description	A read_DDB_start command should be executed at least once before a read_DDB_continue command to define the read location. Otherwise, data read with a read_DDB_continue command is undefined.													
Restriction														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>XXh</td> </tr> <tr> <td>S/W Reset</td> <td>No Change</td> </tr> <tr> <td>H/W Reset</td> <td>XXh</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	XXh	S/W Reset	No Change	H/W Reset	XXh				
Status	Default Value													
Power On Sequence	XXh													
S/W Reset	No Change													
H/W Reset	XXh													

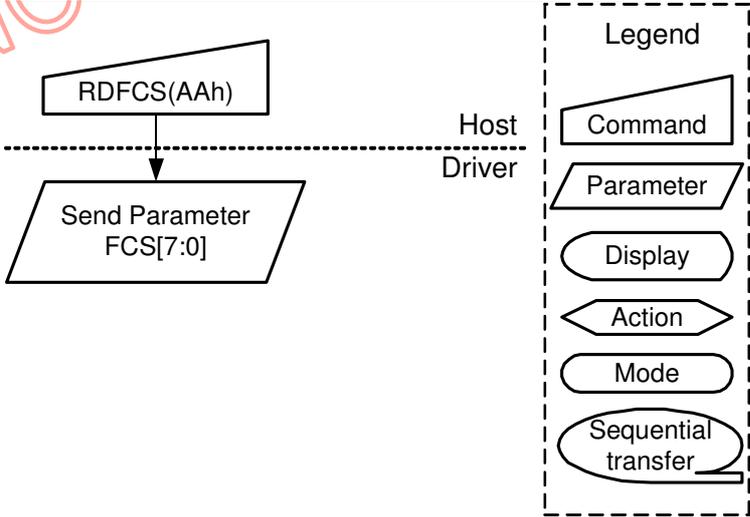


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6.1.69 RDFCS: Read First Checksum (AAh)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDFCS	Read	AAh	AA00h	00h	FCS[7:0]								

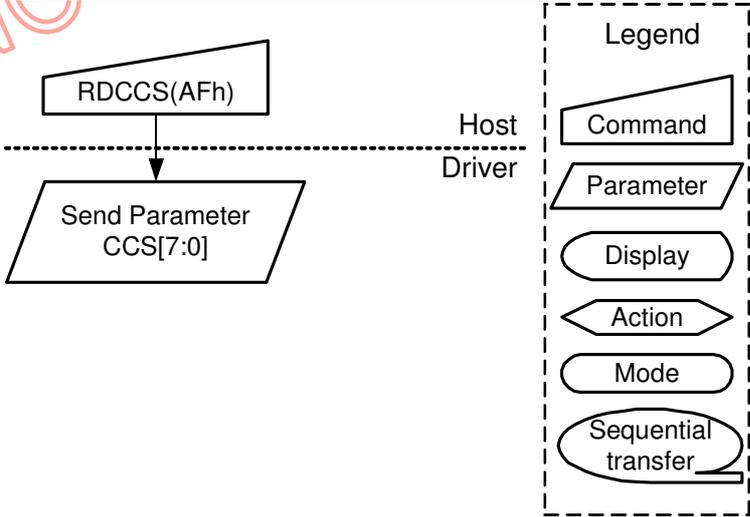
NOTE: “-“ Don't care

Description	This command returns the first checksum what has been calculated from “Instruction Code” area registers (not include “Extended Instruction Code) and the frame memory after the write access to those registers and/or frame memory has been done.												
Restriction	It will be necessary to wait 150ms after there is the last write access on “Instruction Code” area registers before there can read this checksum value.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												
Flow Chart													

6.1.70 RDCCS: Read Continue Checksum (AFh)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDCCS	Read	AFh	AF00h	00h	CCS[7:0]							

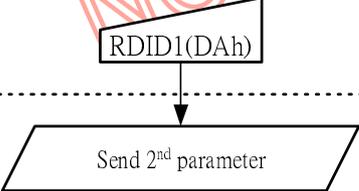
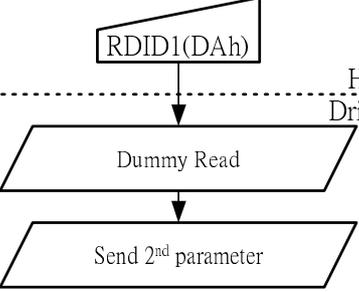
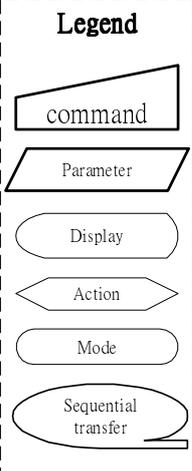
NOTE: "-" Don't care

Description	This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from "Instruction Code" area registers and the frame memory after the write access to those registers and/or frame memory has been done.												
Restriction	It will be necessary to wait 300ms after there is the last write access on "Instruction Code" area registers before there can read this checksum value in the first time.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												
Flow Chart													

6.1.71 RDID1: Read ID1 Value (DAh)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDID1	Read	DAh	DA00h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10

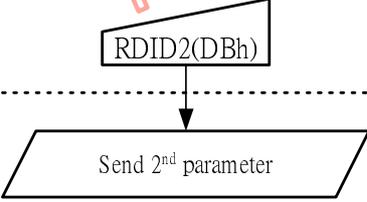
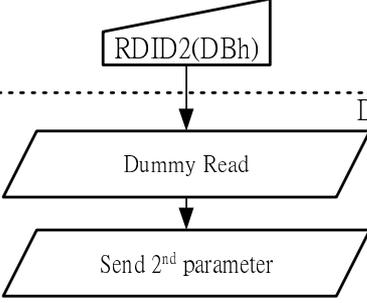
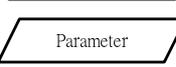
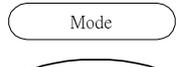
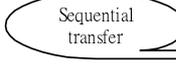
NOTE: “-“ Don't care

Description	This read byte identifies the LCD module's manufacture ID.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>ID1 = "00h"</td> </tr> <tr> <td>S/W Reset</td> <td>No Change</td> </tr> <tr> <td>H/W Reset</td> <td>ID1 = "00h"</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	ID1 = "00h"	S/W Reset	No Change	H/W Reset	ID1 = "00h"				
Status	Default Value													
Power On Sequence	ID1 = "00h"													
S/W Reset	No Change													
H/W Reset	ID1 = "00h"													
Flow Chart	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>Serial I/F Mode</p>  </div> <div style="text-align: center;"> <p>Parallel I/F Mode</p>  </div> </div> <div style="margin-top: 20px;"> <p style="text-align: right;">Host Driver</p>  </div>													

6.1.72 RDID2: Read ID2 Value (DBh)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDID2	Read	DBh	DB00h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20

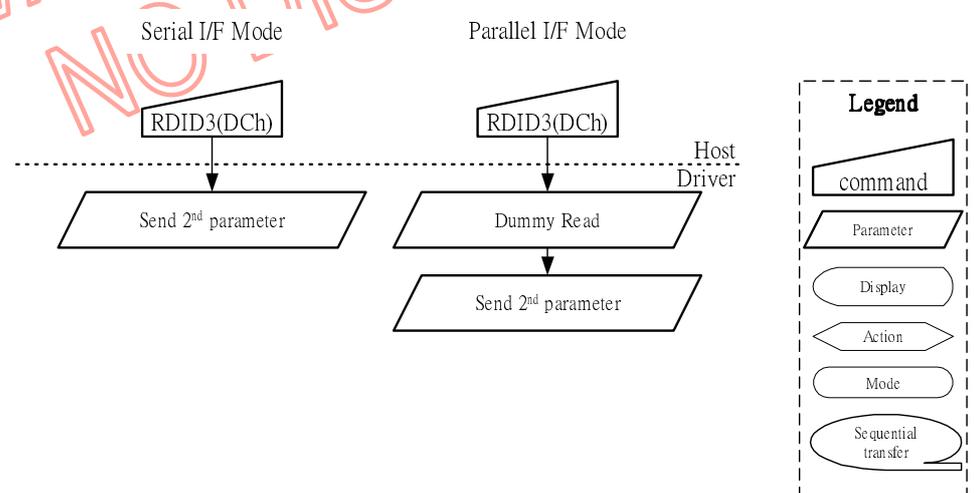
NOTE: “-“ Don't care

Description	This read byte is used to track the LCD module/driver version. It is changed each time a version is made to the display, material or construction specifications. Parameter Range: ID2 = 00h to FFh													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>ID2 = “00h”</td> </tr> <tr> <td>S/W Reset</td> <td>No Change</td> </tr> <tr> <td>H/W Reset</td> <td>ID2 = “00h”</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	ID2 = “00h”	S/W Reset	No Change	H/W Reset	ID2 = “00h”				
Status	Default Value													
Power On Sequence	ID2 = “00h”													
S/W Reset	No Change													
H/W Reset	ID2 = “00h”													
Flow Chart	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>Serial I/F Mode</p>  </div> <div style="text-align: center;"> <p>Parallel I/F Mode</p>  </div> </div> <div style="margin-top: 20px;"> <p style="text-align: right;">Host Driver</p> <div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none">  command  Parameter  Display  Action  Mode  Sequential transfer </div> </div>													

6.1.73 RDID3: Read ID3 Value (DCh)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDID3	Read	DCh	DC00h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	

NOTE: “-“ Don't care

Description	This parameter read byte identifies the LCD module/driver.												
Restriction	-												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>ID3 = "00h"</td> </tr> <tr> <td>S/W Reset</td> <td>No Change</td> </tr> <tr> <td>H/W Reset</td> <td>ID3 = "00h"</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	ID3 = "00h"	S/W Reset	No Change	H/W Reset	ID3 = "00h"				
Status	Default Value												
Power On Sequence	ID3 = "00h"												
S/W Reset	No Change												
H/W Reset	ID3 = "00h"												
Flow Chart	 <p>The flow chart illustrates the RDID3(DCh) command sequence for two interface modes. In Serial I/F Mode, the command RDID3(DCh) is sent, followed by the 2nd parameter. In Parallel I/F Mode, the command RDID3(DCh) is sent, followed by a Dummy Read, and then the 2nd parameter. A dashed line separates the Host and Driver components. The legend defines symbols: a trapezoid for 'command', a parallelogram for 'Parameter', a rounded rectangle for 'Display', a diamond for 'Action', a rounded rectangle for 'Mode', and a rounded rectangle with a tail for 'Sequential transfer'.</p>												

6.2 EXTENDED INSTRUCTION CODE

Note: 1. For LV2 command, please fill the complete parameters for application.

2. Set 0xFF,0xAA,0x55,0x52 first before executing LV2 command.

3. For SPI I/F, can't read LV2 register.

6.2.1 IFMODE: Set Display Interface Mode (B0h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
IFMODE	Write	B0h	B000h	00h	RCM	-	-	ICM	DP	EP	HSP	VSP
			B001h	00h	-	DIS_EO TP_HS	DSIM	DSIG	DSITE	-	IOPT_MIPI[1:0]	

NOTE: "-" Don't care

Description	<p>Sets the operation status of the display interface. The setting becomes effective as soon as the command is received.</p> <p>DP: PCLK polarity set ("0"=data fetched at the rising time, "1"=data fetched at the falling time)</p> <p>EP: DE polarity ("0"= High enable for RGB interface, "1"=Low enable for RGB interface)</p> <p>HSP: HSYNC polarity ("0"=Low level sync clock, "1"=High level sync clock)</p> <p>VSP: VSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock)</p> <p>ICM: RGB Interface clock selection ("0"=PCLK, "1"=internal clock)</p> <p>RCM: The selection for mode RGB interface is decided by RCM described as below:</p> <table border="1"> <thead> <tr> <th>RCM</th> <th>Mode selection</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>RGB Mode 1</td> </tr> <tr> <td>1</td> <td>RGB Mode 2</td> </tr> </tbody> </table> <p>IOPT_MIPI[1:0]: HS-RX bias current option</p> <table border="1"> <thead> <tr> <th>IOPT_MIPI[1:0]</th> <th>Bias Current</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>150uA</td> </tr> <tr> <td>01</td> <td>225uA</td> </tr> <tr> <td>10</td> <td>300uA</td> </tr> <tr> <td>11</td> <td>375uA</td> </tr> </tbody> </table> <p>DSITE: TE line enable/disable. ("0": TE line is disabled, "1": TE line is enabled)</p> <p>DSIG: Generic read/write data type enable/disable for MIPI DSI. ("0": Generic read/write disable, "1": Generic read/write enable)</p> <p>DSIM: Video mode data type enable/disable for MIPI DSI. ("0": Video mode data type disable, "1": Video mode data type enable)</p> <p>DIS_EOTP_HS: EoT packet enable/disable control. ("1": EoT packet is supported. "0": EoT packet is unsupported, the MIPI interface will report "Protocol Violation Error" when EoTp not received.)</p>	RCM	Mode selection	0	RGB Mode 1	1	RGB Mode 2	IOPT_MIPI[1:0]	Bias Current	00	150uA	01	225uA	10	300uA	11	375uA
	RCM	Mode selection															
0	RGB Mode 1																
1	RGB Mode 2																
IOPT_MIPI[1:0]	Bias Current																
00	150uA																
01	225uA																
10	300uA																
11	375uA																
Restriction	-																
Register Available	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes				
Status	Availability																
Normal Mode On, Idle Mode Off, Sleep Out	Yes																
Normal Mode On, Idle Mode On, Sleep Out	Yes																
Partial Mode On, Idle Mode Off, Sleep Out	Yes																
Partial Mode On, Idle Mode On, Sleep Out	Yes																
Sleep In	Yes																

Default	Status	Default Value		
		RCM/ICM/DP/EP/HSP/VSP	DIS_EOTP_HS/DSIM/DSIG/DSITE	IOPT_MIPI[1:0]
	Power On sequence	0/0/0/0/0/0	1/0/1/1	02
	S/W Reset	0/0/0/0/0/0	1/0/1/1	02
	H/W Reset	0/0/0/0/0/0	1/0/1/1	02

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6.2.2 FRMCTR1: Set Division ratio for internal clocks of Normal mode (B1h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
FRMCTR1	Write	B1h	B100h	00h	DIVA[7:0]							
			B101h	00h	0	0	0	0	0	0	DIVA9	DIVA8
			B102h	00h	VPA[7:0]							
			B103h	00h	0	0	0	0	0	0	VPA9	VPA8
			B104h	00h	0	0	0	0	0	0	PSELA[1:0]	

NOTE: "-" Don't care

Description	Sets the division ratio for internal clocks of normal mode at CPU interface mode. DIVA[9:0]: Division ratio for internal clocks when normal mode.(Note: DIVA[9:0]=0d, PCLK=1) VPA[9:0]: Vsync porch for internal clocks when normal mode. PSELA[1:0]: PCLK selection when normal mode.																									
	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>PSELA{1:0}</th> <th>Divisor Condition</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>2</td> </tr> <tr> <td>2</td> <td>4</td> </tr> <tr> <td>3</td> <td>4</td> </tr> </tbody> </table> $\text{Frame rate} = \frac{14\text{MHz}}{\text{DIVA}[9:0] \times (\text{Line} + \text{VPA}[9:0])}$	PSELA{1:0}	Divisor Condition	0	1	1	2	2	4	3	4															
PSELA{1:0}	Divisor Condition																									
0	1																									
1	2																									
2	4																									
3	4																									
Restriction	Without CABC function: <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>DISP[1:0]</th> <th>Resolution</th> <th>Line</th> <th>DIVA</th> <th>VPA</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>360x640</td> <td>640</td> <td>300~1023</td> <td>30~1023</td> </tr> <tr> <td>01</td> <td>360x480</td> <td>480</td> <td>300~1023</td> <td>30~1023</td> </tr> <tr> <td>10</td> <td>320x480</td> <td>480</td> <td>300~1023</td> <td>30~1023</td> </tr> <tr> <td>11</td> <td>reserved</td> <td>-</td> <td>-</td> <td>-</td> </tr> </tbody> </table>	DISP[1:0]	Resolution	Line	DIVA	VPA	00	360x640	640	300~1023	30~1023	01	360x480	480	300~1023	30~1023	10	320x480	480	300~1023	30~1023	11	reserved	-	-	-
	DISP[1:0]	Resolution	Line	DIVA	VPA																					
00	360x640	640	300~1023	30~1023																						
01	360x480	480	300~1023	30~1023																						
10	320x480	480	300~1023	30~1023																						
11	reserved	-	-	-																						
With CABC function: <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>DISP[1:0]</th> <th>Resolution</th> <th>Line</th> <th>DIVA</th> <th>VPA</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>360x640</td> <td>640</td> <td>300~1023</td> <td>30~1023</td> </tr> <tr> <td>01</td> <td>360x480</td> <td>480</td> <td>300~1023</td> <td>30~1023</td> </tr> <tr> <td>10</td> <td>320x480</td> <td>480</td> <td>300~1023</td> <td>30~1023</td> </tr> <tr> <td>11</td> <td>reserved</td> <td>-</td> <td>-</td> <td>-</td> </tr> </tbody> </table>	DISP[1:0]	Resolution	Line	DIVA	VPA	00	360x640	640	300~1023	30~1023	01	360x480	480	300~1023	30~1023	10	320x480	480	300~1023	30~1023	11	reserved	-	-	-	
DISP[1:0]	Resolution	Line	DIVA	VPA																						
00	360x640	640	300~1023	30~1023																						
01	360x480	480	300~1023	30~1023																						
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Default	<table border="1"> <thead> <tr> <th>Status</th> <th colspan="3">Default Value</th> </tr> <tr> <th rowspan="2">DISP</th> <th colspan="3">"00" (360X640)</th> </tr> <tr> <th>DIVA[9:0]</th> <th>VPA[9:0]</th> <th>PSELA[1:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td style="text-align: center;">341</td> <td style="text-align: center;">48</td> <td style="text-align: center;">0</td> </tr> <tr> <td>S/W Reset</td> <td style="text-align: center;">341</td> <td style="text-align: center;">48</td> <td style="text-align: center;">0</td> </tr> <tr> <td>H/W Reset</td> <td style="text-align: center;">341</td> <td style="text-align: center;">48</td> <td style="text-align: center;">0</td> </tr> </tbody> </table>	Status	Default Value			DISP	"00" (360X640)			DIVA[9:0]	VPA[9:0]	PSELA[1:0]	Power On Sequence	341	48	0	S/W Reset	341	48	0	H/W Reset	341	48	0
	Status	Default Value																						
	DISP	"00" (360X640)																						
		DIVA[9:0]	VPA[9:0]	PSELA[1:0]																				
	Power On Sequence	341	48	0																				
S/W Reset	341	48	0																					
H/W Reset	341	48	0																					
Note: Normal mode default frame rate ~ = 60Hz																								

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6.2.3 FRMCTR2: Set Division ratio for internal clocks of Idle mode (B2h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
FRMCTR2	Write	B2h	B200h	00h	DIVB[7:0]							
			B201h	00h	0	0	0	0	0	0	DIVB9	DIVB8
			B202h	00h	VPB[7:0]							
			B203h	00h	0	0	0	0	0	0	VPB9	VPB8
			B204h	00h	0	0	0	0	0	0	PSELB[1:0]	

NOTE: "-" Don't care

Description	<p>Sets the division ratio for internal clocks of Idle mode at CPU interface mode. DIVB[9:0]: Division ratio for internal clocks when Idle mode. (Note: DIVB[9:0]=0d, PCLK=1) VPB[9:0]: Vsync porch for internal clocks when Idle mode. PSELB[1:0]: PCLK selection when Idle mode.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>PSELB[1:0]</th> <th>Divisor Condition</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>2</td> </tr> <tr> <td>2</td> <td>4</td> </tr> <tr> <td>3</td> <td>4</td> </tr> </tbody> </table> $\text{Frame rate} = \frac{14\text{MHz}}{\text{DIVB}[9:0] \times (\text{Line} + \text{VPB}[9:0])}$	PSELB[1:0]	Divisor Condition	0	1	1	2	2	4	3	4																																								
PSELB[1:0]	Divisor Condition																																																		
0	1																																																		
1	2																																																		
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DISP[1:0]	Resolution	Line	DIVB	VPB																																															
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Sleep In	Yes																																																		

Default	Status	Default Value		
	DISP	"00" (360X640)		
		DIVB[9:0]	VPB[9:0]	PSELB[1:0]
	Power On Sequence	341	48	0
	S/W Reset	341	48	0
H/W Reset	341	48	0	

Note: Idle mode default frame rate ~ = 60Hz

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6.2.4 FRMCTR3: Set Division ratio for internal clocks of Partial mode (Idle mode off) (B3h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
FRMCTR3	Write	B3h	B300h	00h	DIVC[7:0]							
			B301h	00h	0	0	0	0	0	0	DIVC9	DIVC8
			B302h	00h	VPC[7:0]							
			B303h	00h	0	0	0	0	0	0	VPC9	VPC8
			B304h	00h	0	0	0	0	0	0	PSEL[1:0]	

NOTE: "-" Don't care

Description	<p>Sets the division ratio for internal clocks of Partial mode at CPU interface mode. DIVC[9:0]: Division ratio for internal clocks when Partial mode. (Note: DIVC[9:0]=0d, PCLK=1) VPC[9:0]: Vsync porch for internal clocks when Partial mode. PSEL[1:0]: PCLK selection when Partial mode.</p> <table border="1"> <thead> <tr> <th>PSEL[1:0]</th> <th>Divisor Condition</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>2</td> </tr> <tr> <td>2</td> <td>4</td> </tr> <tr> <td>3</td> <td>4</td> </tr> </tbody> </table> $\text{Frame rate} = \frac{14\text{MHz}}{\text{PSEL} \times \text{DIVC}[9:0] \times (\text{Line} + \text{VPC}[9:0])}$	PSEL[1:0]	Divisor Condition	0	1	1	2	2	4	3	4																																								
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Sleep In	Yes																																																		

Default	Status	Default Value		
	DISP	"00" (360X640)		
		DIVC[9:0]	VPC[9:0]	PSEL
	Power On Sequence	341	48	0
	S/W Reset	341	48	0
	H/W Reset	341	48	0
Note: Partial mode default frame rate ~ = 60Hz				

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6.2.5 INVCTR: Inversion Control (B4h)

Inst / Para	R/W	Address			Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
INVCTR	Write	B4h	B400h	00h	-	-	-	-	-	-	-	NLA1	NLA0
			B401h	00h	-	-	-	-	-	-	-	NLB1	NLB0
			B402h	00h	-	-	-	-	-	-	-	NLC1	NLC0

NOTE: "-" Don't care

Description	Display inversion mode set NLA : Inversion setting in full colors normal mode (Normal mode on) NLB : Inversion setting in Idle mode (Idle mode on) NLC : Inversion setting in full colors partial mode (Partial mode on / Idle mode off)																			
	<table border="1"> <thead> <tr> <th>NLA / NLB / NLC [1:0]</th> <th>Inversion</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1dot inversion</td> </tr> <tr> <td>1</td> <td>2dot inversion</td> </tr> <tr> <td>2</td> <td>column inversion</td> </tr> <tr> <td>3</td> <td>zigzag inversion</td> </tr> </tbody> </table>	NLA / NLB / NLC [1:0]	Inversion	0	1dot inversion	1	2dot inversion	2	column inversion	3	zigzag inversion									
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Restriction	-																			
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Status	Default Value																			
	NLA[1:0]	NLB[1:0]	NLC[1:0]																	
Power On Sequence	01d	02d	01d																	
S/W Reset	01d	02d	01d																	
H/W Reset	01d	02d	01d																	

6.2.6 RGBBPCTR: RGB Interface Blanking Porch Setting (B5h)

Inst / Para	R/W	Address				Parameter						
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RGBBPCTR	Write	B5h	B500h	00h	-	-	VBPA5	VBPA4	VBPA3	VBPA2	VBPA1	VBPA0
			B501h	00h	-	-	HBPA5	HBPA4	HBPA3	HBPA2	HBPA1	HBPA0

NOTE: “-“ Don't care

Description	This command is used to set the no. of clock for back and front porch of V-Sync and H-Sync in RGB mode 2 RCM = “1”). The vertical (horizontal) back porch hasn't to include the vertical (horizontal) pulse width. The setting value “00h” is invalid for all of the registers.															
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>VBPA[5:0]</td> <td>V-Sync Back Porch in Normal Mode</td> <td>“01h” to “3Fh” = 1 to 63 H-Sync clocks</td> </tr> <tr> <td>HBPA[5:0]</td> <td>H-Sync Back Porch in Normal Mode</td> <td>“01h” to “3Fh” = 1 to 63 PCLK clocks</td> </tr> </tbody> </table>	Bit	Description	Value	VBPA[5:0]	V-Sync Back Porch in Normal Mode	“01h” to “3Fh” = 1 to 63 H-Sync clocks	HBPA[5:0]	H-Sync Back Porch in Normal Mode	“01h” to “3Fh” = 1 to 63 PCLK clocks						
Bit	Description	Value														
VBPA[5:0]	V-Sync Back Porch in Normal Mode	“01h” to “3Fh” = 1 to 63 H-Sync clocks														
HBPA[5:0]	H-Sync Back Porch in Normal Mode	“01h” to “3Fh” = 1 to 63 PCLK clocks														
Restriction	VBPA[5:0] ≥ “04h” HBPA[5:0] ≥ “0Eh”															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes		
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Status	Default Value															
	VBPA	HBPA														
Power On Sequence	28h (40d)	16h (22d)														
S/W Reset	No Change															
H/W Reset	28h (40d)	16h (22d)														

6.2.7 DISSET: Display Function set (B6h)

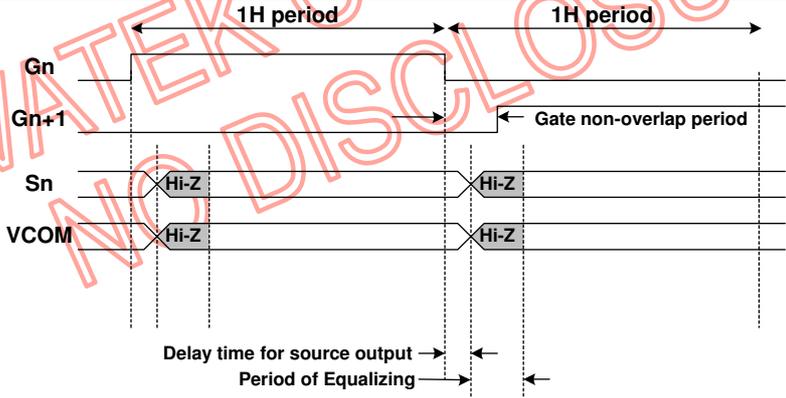
Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
DISSET	Write	B6h	B600h	00h	NO[2:0]			0	0	EQ[2:0]		
			B601h	00h	SDT[5:0]						PT_NonDSP_Source [1:0]	
			B602h	00h	0	ISOPA[2:0]			0	IGOPA[2:0]		
			B603h	00h	0	0	0	0	IGOPB[2:0]			
			B604h	00h	0	ISOPC[2:0]			0	IGOPC[2:0]		

NOTE: "-" Don't care

Description	NO[2:0]: Set amount of non-overlap of the gate output.				
	NO[2:0]	Sclk cycle	Amount of non-overlap of the gate output time (us)		
			PSEL[1:0] = 0	PSEL[1:0] = 1	PSEL[1:0] = 2
	000	4	0.284	0.568	1.136
	001	8	0.568	1.136	2.272
	010	12	0.852	1.704	3.408
	011	16	1.136	2.272	4.544
	100	20	1.42	2.84	5.68
	101	24	1.704	3.408	6.816
	110	28	1.988	3.976	7.952
111	32	2.272	4.544	9.088	
Description	EQ[2:0]: Sets the equalizing period (For 1 / 2 Dot inversion only)				
	EQ[2:0]	Sclk cycle	EQ time (us)		
			PSEL[1:0] = 0	PSEL[1:0] = 1	PSEL[1:0] = 2
	000	0	0	0	0
	001	10	0.71	1.42	2.84
	010	20	1.42	2.84	5.68
	011	30	2.13	4.26	8.52
	100	40	2.84	5.68	11.36
	101	50	3.55	7.1	14.2
	110	60	4.26	8.52	17.04
111	70	4.97	9.94	19.88	

Description	SDT[5:0]: Set delay amount from the gate output signal falling edge of the source outputs.				
	SDT[5:0]	Sclk cycle	Amount of non-overlap of the gate output time (us)		
			PSEL[1:0] = 0	PSEL[1:0] = 1	PSEL[1:0] = 2
	000000	0	0	0	0
	000001	7	0.35	0.70	1.39
	000010	14	0.70	1.39	2.78
	000011	21	1.04	2.09	4.17
	000100	28	1.39	2.78	5.57
	000101	35	1.74	3.48	6.96

	111101	427	21.22	42.44	84.89
	111110	434	21.57	43.14	86.28
	111111	441	21.92	43.84	87.67
	PT_NonDSP_Source[1:0]: Source setting in non-display area at partial mode.				
	PT_NonDSP_Source[1:0]	Source (Positive/Negative)			
0	Blanking				
1	Anti-Blanking				
2	VSS(only used when GOAX=1)				
3	Hi-Z				

	<p>ISOPA[2:0]: Source OP Bias Current selection for Normal Mode. ISOPC[2:0]: Source OP Bias Current selection for Partial Mode.</p> <table border="1"> <thead> <tr> <th>ISOPA[2:0] / ISOPC[2:0]</th> <th>Source OP Bias Current select</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Very Small</td> </tr> <tr> <td>1</td> <td>Small</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>7</td> <td>Big</td> </tr> </tbody> </table> <p>IGOPA[2:0]: Gamma OP Bias Current selection for Normal Mode. IGOPB[2:0]: Gamma OP Bias Current selection for Idle Mode. IGOPC[2:0]: Gamma OP Bias Current selection for Partial Mode.</p> <table border="1"> <thead> <tr> <th>IGOPA[2:0] / IGOPB[2:0] / IGOPC[2:0]</th> <th>Gamma OP Bias Current select</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Very Small</td> </tr> <tr> <td>1</td> <td>Small</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>7</td> <td>Big</td> </tr> </tbody> </table> 	ISOPA[2:0] / ISOPC[2:0]	Source OP Bias Current select	0	Very Small	1	Small	:	:	7	Big	IGOPA[2:0] / IGOPB[2:0] / IGOPC[2:0]	Gamma OP Bias Current select	0	Very Small	1	Small	:	:	7	Big
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H/W Reset	2d	4d	2d	4d	4d																														

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6.2.8CTRLLEDPWM: Set the States for LED Control (B7h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
CTRLLEDPWM	Write	B7h	B700h	00h	-	-	-	PWM_ENH_OE	0	LEDPWPOL	-	-

NOTE: "-" Don't care

Description	<p>This command is used to set states for LED control pin. PWM_ENH_OE: the enable control for LEDPWM pins.</p> <table border="1"> <thead> <tr> <th rowspan="2">WRCABC(55h)</th> <th colspan="2">PWM_ENH_OE=1</th> <th rowspan="2">PWM_ENH_OE =0</th> </tr> <tr> <th>LEDPWMPOL=0</th> <th>LEDPWMPOL=1</th> </tr> </thead> <tbody> <tr> <td>00, CABC off</td> <td>Low (100% duty)</td> <td>High (100% duty)</td> <td>Hi-Z</td> </tr> <tr> <td>01, UI mode</td> <td rowspan="2">PWM waveform (active high)</td> <td rowspan="2">PWM waveform (active low)</td> <td rowspan="2">Hi-Z</td> </tr> <tr> <td>10, Still mode</td> </tr> <tr> <td>11, Moving mode</td> <td></td> <td></td> <td></td> </tr> </tbody> </table>			WRCABC(55h)	PWM_ENH_OE=1		PWM_ENH_OE =0	LEDPWMPOL=0	LEDPWMPOL=1	00, CABC off	Low (100% duty)	High (100% duty)	Hi-Z	01, UI mode	PWM waveform (active high)	PWM waveform (active low)	Hi-Z	10, Still mode	11, Moving mode			
	WRCABC(55h)	PWM_ENH_OE=1			PWM_ENH_OE =0																	
		LEDPWMPOL=0	LEDPWMPOL=1																			
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<p>LEDPWPOL: Set the PWM active polarity for external LED driver control, In other words, LEDPWPOL=1 is suitable setting for "Low-Active" LED driver IC.</p> <table border="1"> <thead> <tr> <th rowspan="2">LEDPWPOL</th> <th colspan="2">Polarity of BC(=LEDPWM) Pin</th> </tr> <tr> <th>Lit period</th> <th>Non-lit-period</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>High</td> <td>Low</td> </tr> <tr> <td>1</td> <td>Low</td> <td>High</td> </tr> </tbody> </table>			LEDPWPOL	Polarity of BC(=LEDPWM) Pin		Lit period	Non-lit-period	0	High	Low	1	Low	High									
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6.2.9 Display Function Selection(B8h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
DFS	Write	B8h	B800h	00h	-	-	DISP[1:0]		REV	SRGB	SMY	SMX
			B801h	00h	0	0	0		0	0	1	0

NOTE: "-" Don't care

Description	When REV, SRGB, SMX, SMY bit set, display will change immediately. These register are used for different panel. DISP[1:0]: Display Resolution Select.					
	DISP[1:0]	SMY	Resolution	Gate Scan Line	Source output	Non-used Gate and their level
	00	0	360x640	G1→G640	S1→S1080	Non
		1		G640→G1	S1→S1080	Non
	01	0	360x480	G1→G480	S1→S1080	G481-G640, fix VGL
		1		G480→G1	S1→S1080	G481-G640, fix VGL
	10	0	320x480	G1→G480	S1→S480, S601→S1080	G481-G640, fix VGL
		1		G480→G1	S1→S480, S601→S1080	G481-G640, fix VGL
	REV: Normally White or Normally Black Select					
	REV	Panel	data	color	Source	
	0	NW	0x00	Black	V0+/V0-	
			0xFF	White	V255+/V255	
	1	NB	0x00	Black	V255+/V255	
			0xFF	White	V0+/V0-	
	SRGB: RGB Order Select					
	SRGB	Order	Gamma			
	0	RGB	Normal			
	1	BGR	RB swap			
	SMY: Gate Scan Direction Select					
	SMY	Gate				
	0	G1→G640 (or G480)				
	1	G640 (or G480)→G1				
	SMX: Source Scan Direction Select					
	SMX	Source				
	0	SDUM0,SDUM1,S1→S1080(or S1→S480, S601→S1080),SDUM2,SDUM3				
	1	SDUM3,SDUM2,S1080→S1(or S1080→S601, S480→S1),SDUM1,SDUM0				
Restriction	-					

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H/W Reset	0000_1000													

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6.2.10 CTRLDMSP: Set the Total Dimming for CABC (B9h)

Inst / Para	R/W	Address			Parameter							
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
CTRLDMSP	Write	B9h	B900h	00h	-	DIM_STEP_CTRL[2:0]			-	DIM_STEP_OFF[2:0]		
			B901h	00h	-	-	-	-	-	DIM_STEP_STILL[2:0]		
			B902h	00h	-	-	-	-	-	DIM_STEP_MOV[2:0]		
			B903h	00h	-	-	-	-	DMST_C[3:0]			

NOTE: "-" Don't care

This command is used to set total dimming steps for CABC.

DIM_STEP_CTRL[2:0] :

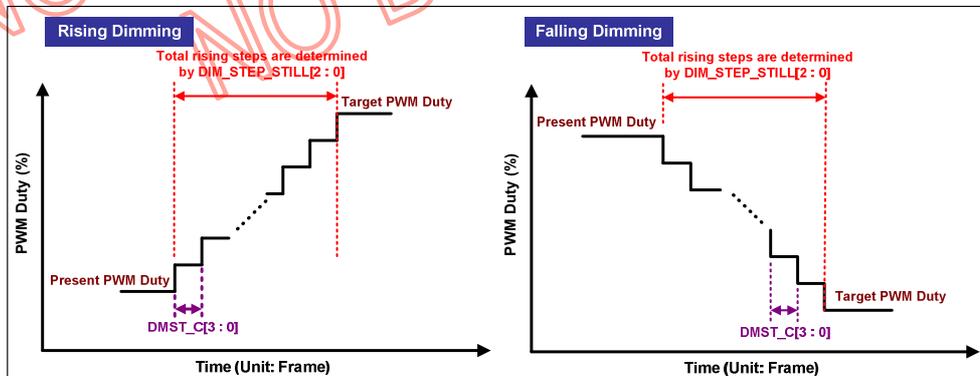
DIM_STEP_OFF[2:0] :

DIM_STEP_STILL[2 : 0]: Set the total dimming steps for Still-Mode

DIM_STEP_STILL[2 : 0]	Total Steps Per Dimming Procedure
000	2
001	4
010	8
011	16
100	32
101	64
110	128
111	256

Backlight dimming in Still-Mode:

Description



Note:

Rising dimming and falling dimming for Still-Mode of CABC are using the same registers (DIM_STEP_STILL[2:0] and DMST_C[3:0]) to set the total dimming steps and each dimming step time.

For example:

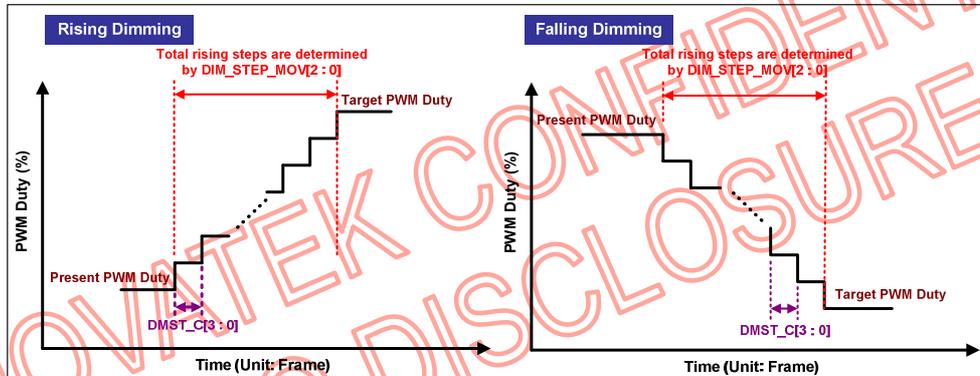
DIM_STEP_STILL[2:0] is set 0x06, this means that the total dimming steps are 128 steps

DMST_C[3:0] is set 0x01, this means that each dimming step time length of falling dimming is 2 frames. So, the total dimming time length is 256 frames (= 128 x 2)

DIM_STEP_MOV[2:0]: Set the total dimming steps for Moving-Mode

DIM_STEP_MOV[2 : 0]	Total Steps Per Dimming Procedure
000	2
001	4
010	8
011	16
100	32
101	64
110	128
111	256

Backlight dimming in Moving-Mode:



Note:

Rising dimming and falling dimming for Moving-Mode of CABC are using the same registers (DIM_STEP_MOV[2:0] and DMST_C[3:0]) to set the total dimming steps and each dimming step time.

For example:

DIM_STEP_MOV[2:0] is set 0x01, this means that the total dimming steps are 4 steps

DMST_C[3:0] is set 0x05, this means that each dimming step time length of falling dimming is 6 frames. So, the total dimming time length is 24 frames (= 4 x 6)

DMST_C[3:0]: Set the dimming step time for Still-Mode and Moving-Mode of CABC.

DMST_C[3 : 0]	Total Steps Per Dimming Procedure
0000	1
0001	2
0010	3
0011	4
0100	5
0101	6
0110	7
0111	8
1xxx	Reserved

	<p>Note: Rising dimming and falling dimming in Still-mode / Moving Mode of CABG are use the same register, DMST_C[3:0], to set the dimming step time.</p>																																		
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S/W Reset	4d	4d	4d	4d	0d																														
H/W Reset	4d	4d	4d	4d	0d																														

6.2.11 PWCTR1: Power Control 1 (C0h)

Inst / Para	R/W	Address				Parameter							
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
PWCTR1	Write	C0h	C000h	00h	VGMP[7:0]								
			C001h	00h	VGMN[7:0]								
			C002h	00h	VGSP[7:0]								
			C003h	00h	VGSN[7:0]								
			C004h	00h	SID[7:0]								
			C005h	00h	SID[15:8]								
			C006h	00h	MRID[7:0]								
			C007h	00h	MRID[15:8]								

NOTE: "-" Don't care

Description	Set the gamma regulator output voltage VGMP[7:0]: set the gamma VGMP regulator output voltage. VGMN[7:0]: set the gamma VGMN regulator output voltage.																																																																								
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	<p>VGSP[7:0]: set the gamma VGSP regulator output voltage. VGSN[7:0]: set the gamma VGSN regulator output voltage.</p> <table border="1"> <thead> <tr> <th>VGSP[7:0]</th> <th>Output voltage</th> <th>VGSN[7:0]</th> <th>Output voltage</th> </tr> </thead> <tbody> <tr> <td>00d</td> <td>0.200V</td> <td>00d</td> <td>-0.200V</td> </tr> <tr> <td>01d</td> <td>0.210V</td> <td>01d</td> <td>-0.210V</td> </tr> <tr> <td>02d</td> <td>0.220V</td> <td>02d</td> <td>-0.220V</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>:</td> <td>(STEP=10mV)</td> <td>:</td> <td>(STEP=10mV)</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>100d</td> <td>1.200V</td> <td>100d</td> <td>-1.200V</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>:</td> <td>(STEP=10mV)</td> <td>:</td> <td>(STEP=10mV)</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>180d</td> <td>1.500V</td> <td>180d</td> <td>-1.500V</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>:</td> <td>(STEP=10mV)</td> <td>:</td> <td>(STEP=10mV)</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>200d</td> <td>2.200V</td> <td>200d</td> <td>-2.200V</td> </tr> <tr> <td>201d</td> <td rowspan="2">NOT USE</td> <td>201d</td> <td rowspan="2">NOT USE</td> </tr> <tr> <td>:</td> </tr> <tr> <td>255d</td> <td></td> <td>255d</td> <td></td> </tr> </tbody> </table> <p>SID[15:0] & MRID[15:0]: These commands return supplier identification and display module model & revision information.</p>	VGSP[7:0]	Output voltage	VGSN[7:0]	Output voltage	00d	0.200V	00d	-0.200V	01d	0.210V	01d	-0.210V	02d	0.220V	02d	-0.220V	:	:	:	:	:	(STEP=10mV)	:	(STEP=10mV)	:	:	:	:	100d	1.200V	100d	-1.200V	:	:	:	:	:	(STEP=10mV)	:	(STEP=10mV)	:	:	:	:	180d	1.500V	180d	-1.500V	:	:	:	:	:	(STEP=10mV)	:	(STEP=10mV)	:	:	:	:	200d	2.200V	200d	-2.200V	201d	NOT USE	201d	NOT USE	:	255d		255d	
VGSP[7:0]	Output voltage	VGSN[7:0]	Output voltage																																																																							
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180d	1.500V	180d	-1.500V																																																																							
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200d	2.200V	200d	-2.200V																																																																							
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255d		255d																																																																								
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Voltage	00H	00H	00H	00H																																																																						

6.2.12 PWCTR2: Power Control 2 (C1h)

Inst / Para	R/W	Address				Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0		
PWCTR2	Write	C1h	C100h	00h	0	PCK45_A[2:0]		BT4_A[1:0]		BT5_A[1:0]				
			C101h	00h	0	PCK45_B[2:0]		BT4_B[1:0]		BT5_B[1:0]				
			C102h	00h	0	PCK45_C[2:0]		BT4_C[1:0]		BT5_C[1:0]				
			C103h	00h	VBH[3:0]			VBL[3:0]						
			C104h	00h	0	0	GOS[1:0]		0		GOT[2:0]			
			C105h	00h	FORCE_EN _VCOM_BUF _O	0	TE_PWR_SEL	RAMKP	GDSTB_SEL	0	0	GD_E2O		

NOTE: “-“ Don't care

Description	<p>PCK45_A[2:0]: VGH/VGL booster clock selection in Normal Mode. Synchronize to H sync. PCK45_B[2:0]: VGH/VGL booster clock selection in Idle Mode. Synchronize to H sync. PCK45_C[2:0]: VGH/VGL booster clock selection in Partial Mode. Synchronize to H sync.</p> <table border="1"> <thead> <tr> <th>PCK45_A[2:0] / PCK45_B[2:0] / PCK45_C[2:0]</th> <th>Frequency (KHz)</th> </tr> </thead> <tbody> <tr><td>000</td><td>H / 16</td></tr> <tr><td>001</td><td>H / 8</td></tr> <tr><td>010</td><td>H / 4</td></tr> <tr><td>011</td><td>H/2</td></tr> <tr><td>100</td><td>H (default)</td></tr> <tr><td>101</td><td>2H</td></tr> <tr><td>110</td><td>4H</td></tr> <tr><td>111</td><td>8H</td></tr> </tbody> </table> <p>BT4_A[1:0]: VGH booster voltage output selection in Normal Mode. BT4_B[1:0]: VGH booster voltage output selection in Idle Mode. BT4_C[1:0]: VGH booster voltage output selection in Partial Mode.</p> <table border="1"> <thead> <tr> <th>BT4_A[1:0] / BT4_B[1:0] / BT4_C[1:0]</th> <th>VGH</th> </tr> </thead> <tbody> <tr><td>00</td><td>PAVDD+VPNL</td></tr> <tr><td>01</td><td>PAVDD-NAVDD</td></tr> <tr><td>10</td><td>PAVDD-NAVDD+VPNL</td></tr> <tr><td>11</td><td>2*PAVDD-NAVDD</td></tr> </tbody> </table> <p>BT5_A[1:0]: VGL booster voltage output selection in Normal Mode. BT5_B[1:0]: VGL booster voltage output selection in Idle Mode. BT5_C[1:0]: VGL booster voltage output selection in Partial Mode.</p> <table border="1"> <thead> <tr> <th>BT5_A[1:0] / BT5_B[1:0] / BT5_C[1:0]</th> <th>VGL</th> </tr> </thead> <tbody> <tr><td>00</td><td>NAVDD-VPNL</td></tr> <tr><td>01</td><td>NAVDD-PAVDD</td></tr> <tr><td>10</td><td>2*NAVDD -VPNL</td></tr> <tr><td>11</td><td>2*NAVDD-PAVDD</td></tr> </tbody> </table>	PCK45_A[2:0] / PCK45_B[2:0] / PCK45_C[2:0]	Frequency (KHz)	000	H / 16	001	H / 8	010	H / 4	011	H/2	100	H (default)	101	2H	110	4H	111	8H	BT4_A[1:0] / BT4_B[1:0] / BT4_C[1:0]	VGH	00	PAVDD+VPNL	01	PAVDD-NAVDD	10	PAVDD-NAVDD+VPNL	11	2*PAVDD-NAVDD	BT5_A[1:0] / BT5_B[1:0] / BT5_C[1:0]	VGL	00	NAVDD-VPNL	01	NAVDD-PAVDD	10	2*NAVDD -VPNL	11	2*NAVDD-PAVDD
	PCK45_A[2:0] / PCK45_B[2:0] / PCK45_C[2:0]	Frequency (KHz)																																					
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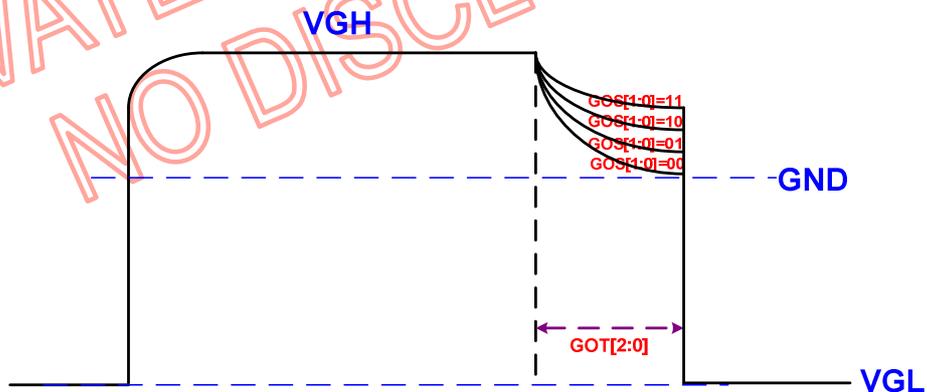
VBH[3:0]: Clamp Voltage Setting for VGH / VBL[3:0]: Clamp Voltage Setting for VCL

VBH[3:0]	VGH (V)	VBL[3:0]	VCL (V)
0x00	15	0x00	-1.5
0x01	14	0x01	-2
0x02	13	0x02	-2.5
0x03	12	0x03	-3
0x04	11	0x04	-3.5
0x05	10	0x05	-4
0x06	9	0x06	Clamp off
0x07	8	0x07	Clamp off
0x08	7	0x08	Clamp off
0x0F	Clamp off	0x0F	Clamp off

GOS[1:0]: Set the VGH 2nd level output slope

GOS[1:0]	Sclk cycle	VGH 2 nd level output slope		
		PSEL[1:0]=0	PSEL[1:0]=1	PSEL[1:0]=2
00	0	0	0	0
01	2	Small	Small	Small
10	7	Medium	Medium	Medium
11	12	Large	Large	Large

Description



GOT[2:0]: Set the VGH 2nd level output time range

GOT[2:0]	Sclk cycle	VGH 2nd level output timing range(uS)		
		PSEL[1:0]=0	PSEL[1:0]=1	PSEL[1:0]=2
000	0	0.00	0.00	0.00
001	2	0.14	0.29	0.57
010	7	0.50	1.00	2.00
011	12	0.86	1.71	3.43
100	17	1.21	2.43	4.86
101	22	1.57	3.14	6.29
110	27	1.93	3.86	7.71
111	32	2.29	4.57	9.14

	GDSTB_SEL: In sleep in mode, gate output level.						
	<table border="1"> <thead> <tr> <th>GDSTB_SEL</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Gate output =VGH</td> </tr> <tr> <td>1</td> <td>Gate output =VGL</td> </tr> </tbody> </table>	GDSTB_SEL	Function	0	Gate output =VGH	1	Gate output =VGL
	GDSTB_SEL	Function					
	0	Gate output =VGH					
	1	Gate output =VGL					
GD_E2O: Gate driver							
<table border="1"> <thead> <tr> <th>GD_E2O</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>G1~G639 at IC left side;G2~G640 at IC right side(bump on the top view)</td> </tr> <tr> <td>1</td> <td>G2~G640 at IC left side;G1~G639 at IC right side(bump on the top view)</td> </tr> </tbody> </table>	GD_E2O	Function	0	G1~G639 at IC left side;G2~G640 at IC right side(bump on the top view)	1	G2~G640 at IC left side;G1~G639 at IC right side(bump on the top view)	
GD_E2O	Function						
0	G1~G639 at IC left side;G2~G640 at IC right side(bump on the top view)						
1	G2~G640 at IC left side;G1~G639 at IC right side(bump on the top view)						
RAMKP: Set the RAM data keep/loss in Sleep in mode.							
<table border="1"> <thead> <tr> <th>RAMKP</th> <th>RAM data statue in Sleep in Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>RAM loss in Sleep in (For Saving Power)</td> </tr> <tr> <td>1</td> <td>RAM Keep in Sleep in mode</td> </tr> </tbody> </table>	RAMKP	RAM data statue in Sleep in Mode	0	RAM loss in Sleep in (For Saving Power)	1	RAM Keep in Sleep in mode	
RAMKP	RAM data statue in Sleep in Mode						
0	RAM loss in Sleep in (For Saving Power)						
1	RAM Keep in Sleep in mode						
FORCE_EN_VCOM_BUF_O: Set VCOM level							
<table border="1"> <thead> <tr> <th>FORCE_EN_VCOM_BUF_O</th> <th>VCOM Level setting</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>VCOM</td> </tr> <tr> <td>1</td> <td>VCOM forced to GND (for saving power)</td> </tr> </tbody> </table>	FORCE_EN_VCOM_BUF_O	VCOM Level setting	0	VCOM	1	VCOM forced to GND (for saving power)	
FORCE_EN_VCOM_BUF_O	VCOM Level setting						
0	VCOM						
1	VCOM forced to GND (for saving power)						
	Note: When setting FORCE_EN_VCOM_BUF_O=1, VCOM will be forced to GND. And set GMF[7:0] (C7h) to adjust gamma offset.						
Restriction							

Default	Status		Default Value				
		PCK45_A[2:0]	PCK45_B[2:0]	PCK45_C[2:0]	GOS[1:0]	GOT[2:0]	
	Power On Sequence	4	4	4	0	0	
	S/W Reset	4	4	4	0	0	
	H/W Reset	4	4	4	0	0	
	Status		Default Value				
		BT4_A[1:0]	BT4_B[1:0]	BT4_C[1:0]	BT5_A[1:0]	BT5_B[1:0]	BT5_C[1:0]
	Power On Sequence	1	1	1	1	1	1
	S/W Reset	1	1	1	1	1	1
	H/W Reset	1	1	1	1	1	1
	Status		Default Value				
		RAMKP	GDSTB_SEL	GD_E2O	TE_PWR_S EL	FORCE_EN_V COM_BUF_O	
Power On Sequence	0	0	0	0	0		
S/W Reset	0	0	0	0	0		
H/W Reset	0	0	0	0	0		

6.2.13 PWCTR3: Power Control 3 (in Normal mode/ Full colors) (C2h)

Inst / Para	R/W	Address				Parameter						
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
PWCTR3	Write	C2h	C200h	00h	-	VBP_A[2:0]			-	-	BT1_A[1:0]	
			C201h	00h	-	-	-	-	PCK1_A[2:0]			
			C202h	00h	-	VBN_A[2:0]			-	-	BT2_A[1:0]	
			C203h	00h	-	PCK3_A[2:0]			-	PCK2_A[2:0]		

NOTE: "-" Don't care

Description	<p>VBP_A[2:0]: Set the PAVDD booster clamp voltage in normal mode/full colors. VBN_A[2:0]: Set the NAVDD booster clamp voltage in normal mode/full colors.</p> <table border="1"> <thead> <tr> <th>VBP_A[2:0]</th> <th>PAVDD Clamp voltage</th> <th>VBN_A[2:0]</th> <th>NAVDD Clamp voltage</th> </tr> </thead> <tbody> <tr><td>00d</td><td>6.5</td><td>00d</td><td>-6.5</td></tr> <tr><td>01d</td><td>6.4</td><td>01d</td><td>-6.4</td></tr> <tr><td>02d</td><td>6.3</td><td>02d</td><td>-6.3</td></tr> <tr><td>03d</td><td>6.2</td><td>03d</td><td>-6.2</td></tr> <tr><td>04d</td><td>6.1</td><td>04d</td><td>-6.1</td></tr> <tr><td>05d</td><td>6</td><td>05d</td><td>-6</td></tr> <tr><td>06d</td><td>5.9</td><td>06d</td><td>-5.9</td></tr> <tr><td>07d</td><td>Clamp off</td><td>07d</td><td>Clamp off</td></tr> </tbody> </table>				VBP_A[2:0]	PAVDD Clamp voltage	VBN_A[2:0]	NAVDD Clamp voltage	00d	6.5	00d	-6.5	01d	6.4	01d	-6.4	02d	6.3	02d	-6.3	03d	6.2	03d	-6.2	04d	6.1	04d	-6.1	05d	6	05d	-6	06d	5.9	06d	-5.9	07d	Clamp off	07d	Clamp off											
	VBP_A[2:0]	PAVDD Clamp voltage	VBN_A[2:0]	NAVDD Clamp voltage																																															
	00d	6.5	00d	-6.5																																															
	01d	6.4	01d	-6.4																																															
	02d	6.3	02d	-6.3																																															
	03d	6.2	03d	-6.2																																															
	04d	6.1	04d	-6.1																																															
	05d	6	05d	-6																																															
	06d	5.9	06d	-5.9																																															
	07d	Clamp off	07d	Clamp off																																															
<p>BT1_A[2:0]: Set the PAVDD booster multiple in normal mode/full colors. BT2_A[2:0]: Set the NAVDD booster multiple in normal mode/full colors.</p> <table border="1"> <thead> <tr> <th>BT1_A[1:0]</th> <th>Multiple</th> <th>BT2_A[1:0]</th> <th>Multiple</th> </tr> </thead> <tbody> <tr><td>00d</td><td>X2</td><td>00d</td><td>X2</td></tr> <tr><td>01d</td><td>X2.5</td><td>01d</td><td>X3</td></tr> <tr><td>02d</td><td>X3</td><td>02d</td><td>X3</td></tr> <tr><td>03d</td><td>X4</td><td>03d</td><td>X3</td></tr> </tbody> </table>				BT1_A[1:0]	Multiple	BT2_A[1:0]	Multiple	00d	X2	00d	X2	01d	X2.5	01d	X3	02d	X3	02d	X3	03d	X4	03d	X3																												
BT1_A[1:0]	Multiple	BT2_A[1:0]	Multiple																																																
00d	X2	00d	X2																																																
01d	X2.5	01d	X3																																																
02d	X3	02d	X3																																																
03d	X4	03d	X3																																																
<p>PCK1_A[2:0]: PAVDD Booster Clock Selection in Normal mode. Synchronize to H sync. PCK2_A[2:0]: NAVDD Booster Clock Selection in Normal mode. Synchronize to H sync. PCK3_A[2:0]: VCL Booster Clock Selection in Normal mode. Synchronize to H sync.</p> <table border="1"> <thead> <tr> <th>PCK1_A[2:0]</th> <th>Frequency (KHz)</th> <th>PCK2_A[2:0]</th> <th>Frequency (KHz)</th> <th>PCK3_A[2:0]</th> <th>Frequency (KHz)</th> </tr> </thead> <tbody> <tr><td>00d</td><td>H / 16</td><td>00d</td><td>H / 16</td><td>00d</td><td>H / 16</td></tr> <tr><td>01d</td><td>H / 8</td><td>01d</td><td>H / 8</td><td>01d</td><td>H / 8</td></tr> <tr><td>02d</td><td>H / 4</td><td>02d</td><td>H / 4</td><td>02d</td><td>H / 4</td></tr> <tr><td>03d</td><td>H/2</td><td>03d</td><td>H/2</td><td>03d</td><td>H/2</td></tr> <tr><td>04d</td><td>H</td><td>04d</td><td>H</td><td>04d</td><td>H</td></tr> <tr><td>05d</td><td>2H</td><td>05d</td><td>2H</td><td>05d</td><td>2H</td></tr> <tr><td>06d</td><td>4H</td><td>06d</td><td>4H</td><td>06d</td><td>4H</td></tr> </tbody> </table>				PCK1_A[2:0]	Frequency (KHz)	PCK2_A[2:0]	Frequency (KHz)	PCK3_A[2:0]	Frequency (KHz)	00d	H / 16	00d	H / 16	00d	H / 16	01d	H / 8	01d	H / 8	01d	H / 8	02d	H / 4	02d	H / 4	02d	H / 4	03d	H/2	03d	H/2	03d	H/2	04d	H	04d	H	04d	H	05d	2H	05d	2H	05d	2H	06d	4H	06d	4H	06d	4H
PCK1_A[2:0]	Frequency (KHz)	PCK2_A[2:0]	Frequency (KHz)	PCK3_A[2:0]	Frequency (KHz)																																														
00d	H / 16	00d	H / 16	00d	H / 16																																														
01d	H / 8	01d	H / 8	01d	H / 8																																														
02d	H / 4	02d	H / 4	02d	H / 4																																														
03d	H/2	03d	H/2	03d	H/2																																														
04d	H	04d	H	04d	H																																														
05d	2H	05d	2H	05d	2H																																														
06d	4H	06d	4H	06d	4H																																														

Restriction	-			
Default	Default Value			
	Status	VBP_A[2:0]	VBN_A[2:0]	BT1_A[1:0]
	Power On Sequence	6	6	1
	S/W Reset	6	6	1
	H/W Reset	6	6	1
	Default Value			
	Status	PCK1_A[2:0]	PCK2_A[2:0]	PCK3_A[2:0]
	Power On Sequence	4	3	5
	S/W Reset	4	3	5
	H/W Reset	4	3	5

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NO DISCLOSURE

6.2.14 PWCTR4: Power Control 4 (in Idle mode/ 8-colors) (C3h)

Inst / Para	R/W	Address				Parameter						
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
PWCTR4	Write	C3h	C300h	00h	-	VBP_B[2:0]			-	-	BT1_B[1:0]	
			C301h	00h	-	-	-	-	PCK1_B[2:0]			
			C302h	00h	-	VBN_B[2:0]			-	-	BT2_B[1:0]	
			C303h	00h	-	PCK3_B[2:0]			-	PCK2_B[2:0]		

NOTE: "-" Don't care

Description	<p>VBP_B[2:0]: Set the PAVDD booster clamp voltage in Idle mode. VBN_B[2:0]: Set the NAVDD booster clamp voltage in Idle mode.</p> <table border="1"> <thead> <tr> <th>VBP_B[2:0]</th> <th>PAVDD Clamp voltage</th> <th>VBN_B[2:0]</th> <th>NAVDD Clamp voltage</th> </tr> </thead> <tbody> <tr><td>00d</td><td>6.5</td><td>00d</td><td>-6.5</td></tr> <tr><td>01d</td><td>6.4</td><td>01d</td><td>-6.4</td></tr> <tr><td>02d</td><td>6.3</td><td>02d</td><td>-6.3</td></tr> <tr><td>03d</td><td>6.2</td><td>03d</td><td>-6.2</td></tr> <tr><td>04d</td><td>6.1</td><td>04d</td><td>-6.1</td></tr> <tr><td>05d</td><td>6</td><td>05d</td><td>-6</td></tr> <tr><td>06d</td><td>5.9</td><td>06d</td><td>-5.9</td></tr> <tr><td>07d</td><td>Clamp off</td><td>07d</td><td>Clamp off</td></tr> </tbody> </table>								VBP_B[2:0]	PAVDD Clamp voltage	VBN_B[2:0]	NAVDD Clamp voltage	00d	6.5	00d	-6.5	01d	6.4	01d	-6.4	02d	6.3	02d	-6.3	03d	6.2	03d	-6.2	04d	6.1	04d	-6.1	05d	6	05d	-6	06d	5.9	06d	-5.9	07d	Clamp off	07d	Clamp off											
	VBP_B[2:0]	PAVDD Clamp voltage	VBN_B[2:0]	NAVDD Clamp voltage																																																			
	00d	6.5	00d	-6.5																																																			
	01d	6.4	01d	-6.4																																																			
	02d	6.3	02d	-6.3																																																			
	03d	6.2	03d	-6.2																																																			
	04d	6.1	04d	-6.1																																																			
	05d	6	05d	-6																																																			
	06d	5.9	06d	-5.9																																																			
	07d	Clamp off	07d	Clamp off																																																			
<p>BT1_B[2:0]: Set the PAVDD booster multiple in Idle mode. BT2_B[2:0]: Set the NAVDD booster multiple in Idle mode.</p> <table border="1"> <thead> <tr> <th>BT1_B[1:0]</th> <th>Multiple</th> <th>BT2_B[1:0]</th> <th>Multiple</th> </tr> </thead> <tbody> <tr><td>00d</td><td>X2</td><td>00d</td><td>X2</td></tr> <tr><td>01d</td><td>X2.5</td><td>01d</td><td>X3</td></tr> <tr><td>02d</td><td>X3</td><td>02d</td><td>X3</td></tr> <tr><td>03d</td><td>X4</td><td>03d</td><td>X3</td></tr> </tbody> </table>								BT1_B[1:0]	Multiple	BT2_B[1:0]	Multiple	00d	X2	00d	X2	01d	X2.5	01d	X3	02d	X3	02d	X3	03d	X4	03d	X3																												
BT1_B[1:0]	Multiple	BT2_B[1:0]	Multiple																																																				
00d	X2	00d	X2																																																				
01d	X2.5	01d	X3																																																				
02d	X3	02d	X3																																																				
03d	X4	03d	X3																																																				
<p>PCK1_B[2:0]: PAVDD Booster Clock Selection in Idle mode. Synchronize to H sync. PCK2_B[2:0]: NAVDD Booster Clock Selection in Idle mode. Synchronize to H sync. PCK3_B[2:0]: VCL Booster Clock Selection in Idle mode. Synchronize to H sync.</p> <table border="1"> <thead> <tr> <th>PCK1_B[2:0]</th> <th>Frequency (KHz)</th> <th>PCK2_B[2:0]</th> <th>Frequency (KHz)</th> <th>PCK3_B[2:0]</th> <th>Frequency (KHz)</th> </tr> </thead> <tbody> <tr><td>00d</td><td>H / 16</td><td>00d</td><td>H / 16</td><td>00d</td><td>H / 16</td></tr> <tr><td>01d</td><td>H / 8</td><td>01d</td><td>H / 8</td><td>01d</td><td>H / 8</td></tr> <tr><td>02d</td><td>H / 4</td><td>02d</td><td>H / 4</td><td>02d</td><td>H / 4</td></tr> <tr><td>03d</td><td>H/2</td><td>03d</td><td>H/2</td><td>03d</td><td>H/2</td></tr> <tr><td>04d</td><td>H</td><td>04d</td><td>H</td><td>04d</td><td>H</td></tr> <tr><td>05d</td><td>2H</td><td>05d</td><td>2H</td><td>05d</td><td>2H</td></tr> <tr><td>06d</td><td>4H</td><td>06d</td><td>4H</td><td>06d</td><td>4H</td></tr> </tbody> </table>								PCK1_B[2:0]	Frequency (KHz)	PCK2_B[2:0]	Frequency (KHz)	PCK3_B[2:0]	Frequency (KHz)	00d	H / 16	00d	H / 16	00d	H / 16	01d	H / 8	01d	H / 8	01d	H / 8	02d	H / 4	02d	H / 4	02d	H / 4	03d	H/2	03d	H/2	03d	H/2	04d	H	04d	H	04d	H	05d	2H	05d	2H	05d	2H	06d	4H	06d	4H	06d	4H
PCK1_B[2:0]	Frequency (KHz)	PCK2_B[2:0]	Frequency (KHz)	PCK3_B[2:0]	Frequency (KHz)																																																		
00d	H / 16	00d	H / 16	00d	H / 16																																																		
01d	H / 8	01d	H / 8	01d	H / 8																																																		
02d	H / 4	02d	H / 4	02d	H / 4																																																		
03d	H/2	03d	H/2	03d	H/2																																																		
04d	H	04d	H	04d	H																																																		
05d	2H	05d	2H	05d	2H																																																		
06d	4H	06d	4H	06d	4H																																																		

Restriction	-				
Default	Default Value				
	Status	VBP_B[2:0]	VBN_B[2:0]	BT1_B[1:0]	BT2_B[1:0]
	Power On Sequence	6	6	1	1
	S/W Reset	6	6	1	1
	H/W Reset	6	6	1	1
	Default Value				
	Status	PCK1_B[2:0]	PCK2_B[2:0]	PCK3_B[2:0]	
	Power On Sequence	4	3	5	
	S/W Reset	4	3	5	
	H/W Reset	4	3	5	

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6.2.15 PWCTR5: Power Control 5 (in Partial mode/ Full-colors) (C4h)

Inst / Para	R/W	Address				Parameter						
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
PWCTR5	Write	C4h	C400h	00h	-	VBP_C[2:0]			-	-	BT1_C[1:0]	
			C401h	00h	-	-	-	-	PCK1_C[2:0]			
			C402h	00h	-	VBN_C[2:0]			-	-	BT2_C[1:0]	
			C403h	00h	-	PCK3_C[2:0]			-	PCK2_C[2:0]		

NOTE: "-" Don't care

Description	VBP_C[2:0]: Set the PAVDD booster clamp voltage in Partial mode. VBN_C[2:0]: Set the NAVDD booster clamp voltage in Partial mode.										
	VBP_C[2:0]		PAVDD Clamp voltage		VBN_C[2:0]		NAVDD Clamp voltage				
	00d	6.5	00d	-6.5							
	01d	6.4	01d	-6.4							
	02d	6.3	02d	-6.3							
	03d	6.2	03d	-6.2							
	04d	6.1	04d	-6.1							
	05d	6	05d	-6							
	06d	5.9	06d	-5.9							
	07d	Clamp off	07d	Clamp off							
BT1_C[2:0]: Set the PAVDD booster multiple in Partial mode. BT2_C[2:0]: Set the NAVDD booster multiple in Partial mode.											
BT1_C[1:0]		Multiple		BT2_C[1:0]		Multiple					
00d	X2	00d	X2								
01d	X2.5	01d	X3								
02d	X3	02d	X3								
03d	X4	03d	X3								
PCK1_C[2:0]: PAVDD Booster Clock Selection in Partial mode. Synchronize to H sync. PCK2_C[2:0]: NAVDD Booster Clock Selection in Partial mode. Synchronize to H sync. PCK3_C[2:0]: VCL Booster Clock Selection in Partial mode. Synchronize to H sync.											
PCK1_C[2:0]		Frequency (KHz)		PCK2_C[2:0]		Frequency (KHz)		PCK3_C[2:0]		Frequency (KHz)	
00d	H / 16	00d	H / 16	00d	H / 16						
01d	H / 8	01d	H / 8	01d	H / 8						
02d	H / 4	02d	H / 4	02d	H / 4						
03d	H/2	03d	H/2	03d	H/2						
04d	H	04d	H	04d	H						
05d	2H	05d	2H	05d	2H						
06d	4H	06d	4H	06d	4H						

Restriction	-			
Default	Default Value			
	Status	VBP_C[2:0]	VBN_C[2:0]	BT1_C[1:0]
	Power On Sequence	6	6	1
	S/W Reset	6	6	1
	H/W Reset	6	6	1
	Default Value			
	Status	PCK1_C[2:0]	PCK2_C[2:0]	PCK3_C[2:0]
	Power On Sequence	4	3	5
	S/W Reset	4	3	5
	H/W Reset	4	3	5

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6.2.16 nVM: MTP reload or no-reload selection (C5h)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
nVM	Write	C5h	C500h	00h	-	-	-	-	-	-	-	-	nVM

NOTE: "-" Don't care

Description	<p>nVM is a controlled bit for user to select the registers reloaded from MTP or set by command setting</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>nVM</th> <th>E7h, E8h, E9h, EBh, & ECh controlled by nVM bit</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Reload from MTP</td> </tr> <tr> <td>1</td> <td>Set by command setting</td> </tr> </tbody> </table> <p>Notes: 1. If the user doesn't program any MTP, these above description MTP registers default value equal to NT35410 Driver IC default value as Specification definition. 2. If the user has programmed MTP bits, these above description registers default value are equal to MTP values after hardware reset or software reset again. 3. When the NT35410 exit sleep mode, the driver IC will reload MTP or register default value to the above description MTP registers to change these registers contents. 4. The user can set the nVM bit to "H" to keep current register value by user's software setting, before the driver IC Exit sleep mode .</p>	nVM	E7h, E8h, E9h, EBh, & ECh controlled by nVM bit	0	Reload from MTP	1	Set by command setting
	nVM	E7h, E8h, E9h, EBh, & ECh controlled by nVM bit					
0	Reload from MTP						
1	Set by command setting						

Restriction	-								
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>01h</td> </tr> <tr> <td>S/W Reset</td> <td>01h</td> </tr> <tr> <td>H/W Reset</td> <td>01h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	01h	S/W Reset	01h	H/W Reset	01h
Status	Default Value								
Power On Sequence	01h								
S/W Reset	01h								
H/W Reset	01h								

6.2.16 MTPDET: MTP Power Detect (C6h)

Inst / Para	R/W	Address			Parameter							
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
MTPDET	Read	C6h	C600h	00h	-	-	-	-	-	-	-	MTP_DET
		C6h	C601h	00h	CheckSum_LV2[7:0]							

NOTE: "-" Don't care

Description	<p>MTPDET Command is used to check the external power for MTP programming which is ready or not. When the pad "VOTP" is floating or connected to ground, the read out value of MTP_DET register is "0". When the external power 7.5v is connected to the pad "VOTP", the read out value of MTP_DET register is "1"</p> <p>CheckSum_LV2[7:0]: Including B0h, B1h, B2h, B3h, B4h, B5h, B7h, B8h, B9h, C1h, C2h, C3h, C4h, C7h & E7h, for customer check MTP total sum value.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr style="background-color: yellow;"> <td style="text-align: center;">Total sum</td> </tr> <tr> <td style="text-align: center;">BCh</td> </tr> </table>	Total sum	BCh
Total sum			
BCh			

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 NO DISCLOSURE

6.2.17 VMFCTR: VCOM Offset Control & Gamma Offset Control (C7h)

Inst / Para	R/W	Address			Parameter							
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
VMFCTR	Write	C7h	C700h	00h	VMF[7:0]							
			C701h	00h	GMF[7:0]							

NOTE: "-" Don't care

Description	VMF[7:0]: set the VCOM offset voltage.		VMF[7:0]		VMF[7:0]	
	VMF[7:0]	VCOM	VMF[7:0]	VCOM	VMF[7:0]	VCOM
	0	-0.2	51	-0.71	101	-1.21
	1	-0.21	52	-0.72	102	-1.22
	2	-0.22	53	-0.73	103	-1.23
	3	-0.23	54	-0.74	104	-1.24
	4	-0.24	55	-0.75	105	-1.25
	5	-0.25	56	-0.76	106	-1.26
	6	-0.26	57	-0.77	107	-1.27
	7	-0.27	58	-0.78	108	-1.28
	8	-0.28	59	-0.79	109	-1.29
	9	-0.29	60	-0.8	110	-1.3
	10	-0.3	61	-0.81	111	-1.31
	11	-0.31	62	-0.82	112	-1.32
	12	-0.32	63	-0.83	113	-1.33
	13	-0.33	64	-0.84	114	-1.34
	14	-0.34	65	-0.85	115	-1.35
	15	-0.35	66	-0.86	116	-1.36
	16	-0.36	67	-0.87	117	-1.37
	17	-0.37	68	-0.88	118	-1.38
	18	-0.38	69	-0.89	119	-1.39
	19	-0.39	70	-0.9	120	-1.4
	20	-0.4	71	-0.91	121	-1.41
	21	-0.41	72	-0.92	122	-1.42
	22	-0.42	73	-0.93	123	-1.43
	23	-0.43	74	-0.94	124	-1.44
	24	-0.44	75	-0.95	125	-1.45
	25	-0.45	76	-0.96	126	-1.46
	26	-0.46	77	-0.97	127	-1.47
	27	-0.47	78	-0.98	128	-1.48
	28	-0.48	79	-0.99	129	-1.49
	29	-0.49	80	-1	130	-1.5
	30	-0.5	81	-1.01	131	-1.51
	31	-0.51	82	-1.02	132	-1.52
	32	-0.52	83	-1.03	133	-1.53
	33	-0.53	84	-1.04	134	-1.54
	34	-0.54	85	-1.05	135	-1.55
	35	-0.55	86	-1.06	136	-1.56
	36	-0.56	87	-1.07	137	-1.57
	37	-0.57	88	-1.08	138	-1.58
	38	-0.58	89	-1.09	139	-1.59
	39	-0.59	90	-1.1	140	-1.6
	40	-0.6	91	-1.11	141	-1.61
	41	-0.61	92	-1.12	142	-1.62
	42	-0.62	93	-1.13	143	-1.63
	43	-0.63	94	-1.14	144	-1.64
	44	-0.64	95	-1.15	145	-1.65
	45	-0.65	96	-1.16	146	-1.66
	46	-0.66	97	-1.17	147	-1.67
	47	-0.67	98	-1.18	148	-1.68
	48	-0.68	99	-1.19	149	-1.69
	49	-0.69	100	-1.2	150	-1.7
	50	-0.7				

VMF[7:0]	VCOM	VMF[7:0]	VCOM
151	-1.71	201	-2.21
152	-1.72	202	-2.22
153	-1.73	203	-2.23
154	-1.74	204	-2.24
155	-1.75	205	-2.25
156	-1.76	206	-2.26
157	-1.77	207	-2.27
158	-1.78	208	-2.28
159	-1.79	209	-2.29
160	-1.8	210	-2.3
161	-1.81	211	
162	-1.82		
163	-1.83	:	no use
164	-1.84		
165	-1.85	255	
166	-1.86		
167	-1.87		
168	-1.88		
169	-1.89		
170	-1.9		
171	-1.91		
172	-1.92		
173	-1.93		
174	-1.94		
175	-1.95		
176	-1.96		
177	-1.97		
178	-1.98		
179	-1.99		
180	-2		
181	-2.01		
182	-2.02		
183	-2.03		
184	-2.04		
185	-2.05		
186	-2.06		
187	-2.07		
188	-2.08		
189	-2.09		
190	-2.1		
191	-2.11		
192	-2.12		
193	-2.13		
194	-2.14		
195	-2.15		
196	-2.16		
197	-2.17		
198	-2.18		
199	-2.19		
200	-2.2		

-The step voltage is 10mV
 -The VCOM Voltage Range = -0.2V ~ -2.3V

	<p>GMF[7:0]: Use to adjust the gamma voltage (VGMP/VGMN/VGSP/VGSN) offset.</p> <table border="1"> <thead> <tr> <th>GMF[7:0]</th> <th>VGMP (V)</th> <th>VGMN (V)</th> <th>VGSP (V)</th> <th>VGSN (V)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>VGMP</td> <td>VGMN</td> <td>VGSP</td> <td>VGSN</td> </tr> <tr> <td>1</td> <td>VGMP + 0.01V</td> <td>VGMN + 0.01V</td> <td>VGSP + 0.01V</td> <td>VGSN + 0.01V</td> </tr> <tr> <td>2</td> <td>VGMP + 0.02V</td> <td>VGMN + 0.02V</td> <td>VGSP + 0.02V</td> <td>VGSN + 0.02V</td> </tr> <tr> <td>3</td> <td>VGMP + 0.03V</td> <td>VGMN + 0.03V</td> <td>VGSP + 0.03V</td> <td>VGSN + 0.03V</td> </tr> <tr> <td>4</td> <td>VGMP + 0.04V</td> <td>VGMN + 0.04V</td> <td>VGSP + 0.04V</td> <td>VGSN + 0.04V</td> </tr> <tr> <td>5</td> <td>VGMP + 0.05V</td> <td>VGMN + 0.05V</td> <td>VGSP + 0.05V</td> <td>VGSN + 0.05V</td> </tr> <tr> <td>:</td> <td>Step = 10 mV</td> <td>Step = 10 mV</td> <td>Step = 10 mV</td> <td>Step = 10 mV</td> </tr> <tr> <td>127</td> <td>VGMP + 1.27V</td> <td>VGMN + 1.27V</td> <td>VGSP + 1.27V</td> <td>VGSN + 1.27V</td> </tr> <tr> <td>128</td> <td>VGMP</td> <td>VGMN</td> <td>VGSP</td> <td>VGSN</td> </tr> <tr> <td>129</td> <td>VGMP - 0.01V</td> <td>VGMN - 0.01V</td> <td>VGSP - 0.01V</td> <td>VGSN - 0.01V</td> </tr> <tr> <td>130</td> <td>VGMP - 0.02V</td> <td>VGMN - 0.02V</td> <td>VGSP - 0.02V</td> <td>VGSN - 0.02V</td> </tr> <tr> <td>131</td> <td>VGMP - 0.03V</td> <td>VGMN - 0.03V</td> <td>VGSP - 0.03V</td> <td>VGSN - 0.03V</td> </tr> <tr> <td>:</td> <td>Step = -10 mV</td> <td>Step = -10 mV</td> <td>Step = -10 mV</td> <td>Step = -10 mV</td> </tr> <tr> <td>252</td> <td>VGMP - 1.24V</td> <td>VGMN - 1.24V</td> <td>VGSP - 1.24V</td> <td>VGSN - 1.24V</td> </tr> <tr> <td>253</td> <td>VGMP - 1.25V</td> <td>VGMN - 1.25V</td> <td>VGSP - 1.25V</td> <td>VGSN - 1.25V</td> </tr> <tr> <td>254</td> <td>VGMP - 1.26V</td> <td>VGMN - 1.26V</td> <td>VGSP - 1.26V</td> <td>VGSN - 1.26V</td> </tr> <tr> <td>255</td> <td>VGMP - 1.27V</td> <td>VGMN - 1.27V</td> <td>VGSP - 1.27V</td> <td>VGSN - 1.27V</td> </tr> </tbody> </table> <p>Note:</p> <ol style="list-style-type: none"> When use GMF[7:0], it need to set C1h- FORCE_EN_VCOM_BUF_O to 'H' (VCOM force to VSS), then set GMF to adjust the offset voltage. The ranges of gamma voltage are as below even GMF[7:0] is adjusted. $3.5V < VGMP < 5.9V$, $-3.5V < VGMN < -5.5V$, $0.2V < VGSP < 2.2V$, $-0.2V < VGSN < -2.2V$. 	GMF[7:0]	VGMP (V)	VGMN (V)	VGSP (V)	VGSN (V)	0	VGMP	VGMN	VGSP	VGSN	1	VGMP + 0.01V	VGMN + 0.01V	VGSP + 0.01V	VGSN + 0.01V	2	VGMP + 0.02V	VGMN + 0.02V	VGSP + 0.02V	VGSN + 0.02V	3	VGMP + 0.03V	VGMN + 0.03V	VGSP + 0.03V	VGSN + 0.03V	4	VGMP + 0.04V	VGMN + 0.04V	VGSP + 0.04V	VGSN + 0.04V	5	VGMP + 0.05V	VGMN + 0.05V	VGSP + 0.05V	VGSN + 0.05V	:	Step = 10 mV	127	VGMP + 1.27V	VGMN + 1.27V	VGSP + 1.27V	VGSN + 1.27V	128	VGMP	VGMN	VGSP	VGSN	129	VGMP - 0.01V	VGMN - 0.01V	VGSP - 0.01V	VGSN - 0.01V	130	VGMP - 0.02V	VGMN - 0.02V	VGSP - 0.02V	VGSN - 0.02V	131	VGMP - 0.03V	VGMN - 0.03V	VGSP - 0.03V	VGSN - 0.03V	:	Step = -10 mV	252	VGMP - 1.24V	VGMN - 1.24V	VGSP - 1.24V	VGSN - 1.24V	253	VGMP - 1.25V	VGMN - 1.25V	VGSP - 1.25V	VGSN - 1.25V	254	VGMP - 1.26V	VGMN - 1.26V	VGSP - 1.26V	VGSN - 1.26V	255	VGMP - 1.27V	VGMN - 1.27V	VGSP - 1.27V	VGSN - 1.27V						
GMF[7:0]	VGMP (V)	VGMN (V)	VGSP (V)	VGSN (V)																																																																																							
0	VGMP	VGMN	VGSP	VGSN																																																																																							
1	VGMP + 0.01V	VGMN + 0.01V	VGSP + 0.01V	VGSN + 0.01V																																																																																							
2	VGMP + 0.02V	VGMN + 0.02V	VGSP + 0.02V	VGSN + 0.02V																																																																																							
3	VGMP + 0.03V	VGMN + 0.03V	VGSP + 0.03V	VGSN + 0.03V																																																																																							
4	VGMP + 0.04V	VGMN + 0.04V	VGSP + 0.04V	VGSN + 0.04V																																																																																							
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128	VGMP	VGMN	VGSP	VGSN																																																																																							
129	VGMP - 0.01V	VGMN - 0.01V	VGSP - 0.01V	VGSN - 0.01V																																																																																							
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S/W Reset	64h	00h																																																																																									
H/W Reset	64h	00h																																																																																									

6.2.18 RDVMF: Read VCOM offset value (C8h)

Inst / Para	R/W	Address			Parameter							
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
RDVMF	Read	C8h	C800h	00h	C8_P1_REG[7:0]							

NOTE: "-" Don't care

Description	Read VCOM offset value.																														
Restriction	-																														
Register Available	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																	
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	Status	Default Value																													
		C8_P1_REG[7:0]																													
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		H/W Reset	MTP value																												
Power On Sequence		64h																													
S/W Reset		64h																													
H/W Reset		64h																													

6.2.19 RDMP: Read MTP value (C9h)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDMP	Read	C9h	C900h	00h	-	-	-	-	MTP[3:0]				
			C901h	00h	VMF1[7:0]								
			C902h	00h	ID11[7:0]								
			C903h	00h	ID21[7:0]								
			C904h	00h	ID31[7:0]								
			C905h	00h	GMF1[7:0]								

NOTE: “-“ Don't care

Description	Read MTP value. MTP[3:0]: MTP programming time flag. (000: No programmed, 001: Programmed 1 time, 010: programmed 2 times, 011: programmed 3 times, 100: programmed 4 times)																																				
	<table border="1"> <thead> <tr> <th>MTP program times</th> <th>MTP[3]</th> <th>MTP[2]</th> <th>MTP[1]</th> <th>MTP[0]</th> <th>Hex</th> </tr> </thead> <tbody> <tr> <td>MTP 0 time</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0x00</td> </tr> <tr> <td>MTP 1st time</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>0x09</td> </tr> <tr> <td>MTP 2nd time</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>0x0A</td> </tr> <tr> <td>MTP 3rd time</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>0x0B</td> </tr> <tr> <td>MTP 4th time</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>0x0C</td> </tr> </tbody> </table>	MTP program times	MTP[3]	MTP[2]	MTP[1]	MTP[0]	Hex	MTP 0 time	0	0	0	0	0x00	MTP 1 st time	1	0	0	1	0x09	MTP 2 nd time	1	0	1	0	0x0A	MTP 3 rd time	1	0	1	1	0x0B	MTP 4 th time	1	1	0	0	0x0C
	MTP program times	MTP[3]	MTP[2]	MTP[1]	MTP[0]	Hex																															
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	MTP 1 st time	1	0	0	1	0x09																															
	MTP 2 nd time	1	0	1	0	0x0A																															
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MTP 4 th time	1	1	0	0	0x0C																																
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Sleep In	Yes																																				

Default	Status	Default Value					
		MTP[3:0]	VMF1[7:0]	ID11[7:0]	ID21[7:0]	ID31[7:0]	GMF1[7:0]
	Power On Sequence	0000	00h 00h	00h 00h	00h 00h	00h 00h	00h 00h
	S/W Reset	0000	00h 00h	00h 00h	00h 00h	00h 00h	00h 00h
	H/W Reset	0000	00h 00h	00h 00h	00h 00h	00h 00h	00h 00h

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6.2.20 WRID1: Write ID1 for MTP program (D0h)

Inst / Para	R/W	Address			Parameter							
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
WRID1	Write	D0h	D000h	00h	ID1[7:0]							

NOTE: "-" Don't care

Description	Write 8-bit LCD module's manufacturer ID to save it to MTP. ID1[7:0]: LCD module's manufacturer ID.													
Restriction	-													
Register Available	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
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Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>ID1[7:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>C1h</td> </tr> <tr> <td>S/W Reset</td> <td>C1h</td> </tr> <tr> <td>H/W Reset</td> <td>C1h</td> </tr> </tbody> </table>		Status	ID1[7:0]	Power On Sequence	C1h	S/W Reset	C1h	H/W Reset	C1h				
Status	ID1[7:0]													
Power On Sequence	C1h													
S/W Reset	C1h													
H/W Reset	C1h													

6.2.21 WRID2: Write ID2 for MTP program (D1h)

Inst / Para	R/W	Address			Parameter							
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
WRID2	Write	D1h	D100h	00h	ID2[7:0]							

NOTE: "-" Don't care

Description	Write 7-bit LCD module/driver version ID to save it to MTP. ID2[7:0]: LCD module/driver version ID (specified by module supplier).													
Restriction	-													
Register Available	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
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Sleep In	Yes													
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Status	Default Value													
Power On Sequence	80h													
S/W Reset	80h													
H/W Reset	80h													

6.2.22 WRID3: Write ID3 for MTP program (D2h)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
WRID3	Write	D2h	D200h	00h	ID3[7:0]								
			D201h	00h	0	0	0	0	ID_Customer[3:0]				

NOTE: "-" Don't care

Description	Write 8-bit project ID to save it to MTP. ID3[7:0]: project ID (specified by handset company). ID_Customer[3:0]: for manufacturer used.														
Restriction	-														
Register Available	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes		
Status	Availability														
Normal Mode On, Idle Mode Off, Sleep Out	Yes														
Normal Mode On, Idle Mode On, Sleep Out	Yes														
Partial Mode On, Idle Mode Off, Sleep Out	Yes														
Partial Mode On, Idle Mode On, Sleep Out	Yes														
Sleep In	Yes														
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>ID3[7:0]</th> <th>ID_Customer[3:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>9Bh</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>9Bh</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>9Bh</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value		ID3[7:0]	ID_Customer[3:0]	Power On Sequence	9Bh	00h	S/W Reset	9Bh	00h	H/W Reset	9Bh	00h
Status	Default Value														
	ID3[7:0]	ID_Customer[3:0]													
Power On Sequence	9Bh	00h													
S/W Reset	9Bh	00h													
H/W Reset	9Bh	00h													

6.2.23 RDID4: Read ID4 for IC Vender Code (D3h)

Inst / Para	R/W	Address		Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDID4	Read	D3h	D300h	00h	0	0	0	0	0	0	0	0	1
			D301h	00h	0	1	0	1	0	1	0	0	0
			D302h	00h	0	0	0	1	0	0	0	0	0
			D303h	00h	0	0	0	0	0	ID4[3:0]			

NOTE: "-" Don't care

Description	Read IC vender code. 1 st parameter: Dummy read 2 nd parameter: Vender ID code. "01" means <i>Novatek</i> . 3 rd / 4 th parameter: Chip ID code. "5410h" means NT35410. ID4[3:0]: Chip version code.													
Restriction	-													
Register Available	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>01 / 54 / 10/ X</td> </tr> <tr> <td>S/W Reset</td> <td>01 / 54 / 10/ X</td> </tr> <tr> <td>H/W Reset</td> <td>01 / 54 / 10/ X</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	01 / 54 / 10/ X	S/W Reset	01 / 54 / 10/ X	H/W Reset	01 / 54 / 10/ X					
Status	Default Value													
Power On Sequence	01 / 54 / 10/ X													
S/W Reset	01 / 54 / 10/ X													
H/W Reset	01 / 54 / 10/ X													

6.2.24 RDID5: Read ID5 Value (D4h)

Inst / Para	R/W	Address		Parameter										
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0		
RDID5	Read	D4h	D400h	00h	-	-	ID51[5:0]							
			D401h	00h	-	-	ID52[5:0]							
			D402h	00h	-	-	ID53[5:0]							
			D403h	00h	-	-	-	ID54[4:0]						
			D404h	00h	ID55[7:0]									
			D405h	00h	-	-	-	-	-	-	-	-	ID55[9:8]	
			D406h	00h	-	-	-	-	ID56[3:0]					

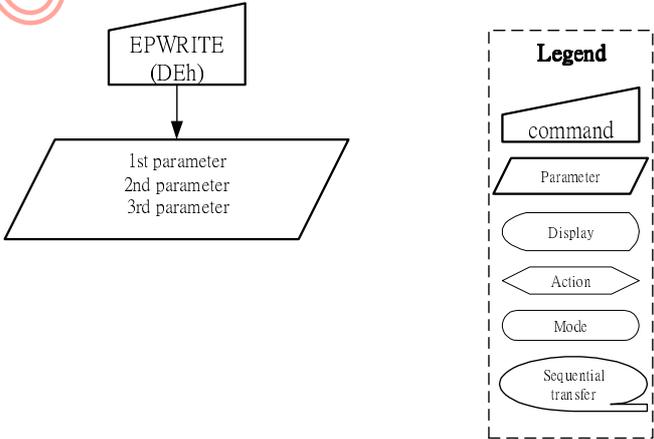
NOTE: "-" Don't care

Description	This command is used to read the chip information. - ID51[5:0]: The third code of lot ID (0~9, A~Z) - ID52[5:0]: The fourth code of lot ID (0~9, A~Z) - ID53[5:0]: The fifth code of lot ID (0~9, A~Z) - ID54[4:0]: The wafer number of this chip (0d~25d) - ID55[9:0]: The X-axis coordinate in the wafer map - ID56[3:0]: The Y-axis coordinate in the wafer map												
Restriction	-												
Register Available	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
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Sleep In	Yes												
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Status	Default Value												
Power On Sequence	-												
S/W Reset	-												
H/W Reset	-												

6.2.25 EPWRITE: MTP Write Command (DEh)

Inst / Para	R/W	Address			Parameter							
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
EPWRITE	Write	DEh	DE00h	00h	0	1	0	1	0	1	0	1
			DE01h	00h	1	0	1	0	1	0	1	0
			DE02h	00h	0	1	1	0	0	1	1	0

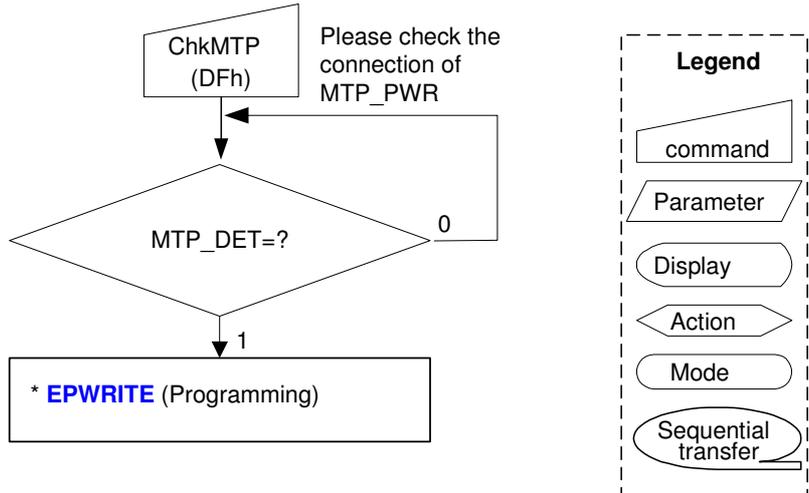
NOTE: "-" Don't care

Description	MTP write command. Please see MTP Access sequence for program (Data write) for more detail.												
Restriction	-												
Register Available	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
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Status	Default Value												
Power On Sequence	-												
S/W Reset	-												
H/W Reset	-												
Flow Chart													

6.2.26 EN_MTP: Enable MTP Write Mode (DFh)

Inst / Para	R/W	Address			Parameter							
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
EN_MTP	Read	DFh	DF00h	00h	0	0	EN_MTP [5]	EN_MTP [4]	EN_MTP [3]	EN_MTP [2]	EN_MTP [1]	EN_MTP [0]

NOTE: "-" Don't care

Description	<p>Enable MTP Write</p> <p>D0: ID (ID1(0xD0), ID2(0xD1), ID3(0xD2), VCOM voltage(0xC7), Gamma voltage(0xC0)→4 times programmed D1: Gamma code (0xE0~0xE5)→ 1 time programmed D2: Timing→1 time programmed D3: CABC Gamma→1 time programmed D4: Trim(LV2) →1 time programmed D5: Inhouse→1 time programmed</p>												
Restriction	-												
Register Available	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
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Status	Default Value												
Power On Sequence	-												
S/W Reset	-												
H/W Reset	-												
Flow Chart													

6.2.27 GAMCTRLPR: Set Gamma Correction Characteristics For Positive "R" (E0h)

Inst / Para	R/W	Address		Parameter										
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0		
GAMCTRLPR	Write	E0h	E000h	00h	-	V0RP[6:0]								
			E001h	00h	-	V1RP[6:0]								
			E002h	00h	V4RP[7:0]									
			E003h	00h	V8RP[7:0]									
			E004h	00h	-	V16RP[6:0]								
			E005h	00h	-	V24RP[6:0]								
			E006h	00h	-	V52RP[6:0]								
			E007h	00h	V80RP[7:0]									
			E008h	00h	-	-	V108RP[5:0]							
			E009h	00h	-	-	V148RP[5:0]							
			E00Ah	00h	V176RP[7:0]									
			E00Bh	00h	-	V204RP[6:0]								
			E00Ch	00h	-	V232RP[6:0]								
			E00Dh	00h	-	V240RP[6:0]								
			E00Eh	00h	V247RP[7:0]									
			E00Fh	00h	V251RP[7:0]									
			E010h	00h	-	V254RP[6:0]								
E011h	00h	-	V255RP[6:0]											

6.2.28 GAMCTRLNR: Set Gamma Correction Characteristics For Negative "R" (E1h)

Inst / Para	R/W	Address			Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0		
GAMCTRLNR	Write	E1h	E100h	00h	-	V0RN[6:0]								
			E101h	00h	-	V1RN[6:0]								
			E102h	00h	V4RN[7:0]									
			E103h	00h	V8RN[7:0]									
			E104h	00h	-	V16RN[6:0]								
			E105h	00h	-	V24RN[6:0]								
			E106h	00h	-	V52RN[6:0]								
			E107h	00h	V80RN[7:0]									
			E108h	00h	-	-	V108RN[5:0]							
			E109h	00h	-	-	V148RN[5:0]							
			E10Ah	00h	V176RN[7:0]									
			E10Bh	00h	-	V204RN[6:0]								
			E10Ch	00h	-	V232RN[6:0]								
			E10Dh	00h	-	V240RN[6:0]								
			E10Eh	00h	V247RN[7:0]									
			E10Fh	00h	V251RN[7:0]									
			E110h	00h	-	V254RN[6:0]								
E111h	00h	-	V255RN[6:0]											

6.2.29 GAMCTRLPG: Set Gamma Correction Characteristics For Positive "G" (E2h)

Inst / Para	R/W	Address			Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0		
GAMCTRLNR	Write	E2h	E200h	00h	-	V0GP[6:0]								
			E201h	00h	-	V1GP[6:0]								
			E202h	00h	V4GP[7:0]									
			E203h	00h	V8GP[7:0]									
			E204h	00h	-	V16GP[6:0]								
			E205h	00h	-	V24GP[6:0]								
			E206h	00h	-	V52GP[6:0]								
			E207h	00h	V80GP[7:0]									
			E208h	00h	-	-	V108GP[5:0]							
			E209h	00h	-	-	V148GP[5:0]							
			E20Ah	00h	V176GP[7:0]									
			E20Bh	00h	-	V204GP[6:0]								
			E20Ch	00h	-	V232GP[6:0]								
			E20Dh	00h	-	V240GP[6:0]								
			E20Eh	00h	V247GP[7:0]									
			E20Fh	00h	V251GP[7:0]									
			E210h	00h	-	V254GP[6:0]								
			E211h	00h	-	V255GP[6:0]								

6.2.30 GAMCTRLNG: Set Gamma Correction Characteristics For Negative "G" (E3h)

Inst / Para	R/W	Address		Parameter										
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0		
GAMCTRLNG	Write	E3h	E300h	00h	-	V0GN[6:0]								
			E301h	00h	-	V1GN[6:0]								
			E302h	00h	V4GN[7:0]									
			E303h	00h	V8GN[7:0]									
			E304h	00h	-	V16GN[6:0]								
			E305h	00h	-	V24GN[6:0]								
			E306h	00h	-	V52GN[6:0]								
			E307h	00h	V80GN[7:0]									
			E308h	00h	-	-	V108GN[5:0]							
			E309h	00h	-	-	V148GN[5:0]							
			E30Ah	00h	V176GN[7:0]									
			E30Bh	00h	-	V204GN[6:0]								
			E30Ch	00h	-	V232GN[6:0]								
			E30Dh	00h	-	V240GN[6:0]								
			E30Eh	00h	V247GN[7:0]									
			E30Fh	00h	V251GN[7:0]									
			E310h	00h	-	V254GN[6:0]								
E311h	00h	-	V255GN[6:0]											

6.2.31 GAMCTRLPB: Set Gamma Correction Characteristics For Positive "B" (E4h)

Inst / Para	R/W	Address			Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0		
GAMCTRLPB	Write	E4h	E400h	00h	-	V0BP[6:0]								
			E401h	00h	-	V1BP[6:0]								
			E402h	00h	V4BP[7:0]									
			E703h	00h	V8BP[7:0]									
			E404h	00h	-	V16BP[6:0]								
			E405h	00h	-	V24BP[6:0]								
			E406h	00h	-	V52BP[6:0]								
			E407h	00h	V80BP[7:0]									
			E408h	00h	-	-	V108BP[5:0]							
			E409h	00h	-	-	V148BP[5:0]							
			E40Ah	00h	V176BP[7:0]									
			E40Bh	00h	-	V204BP[6:0]								
			E40Ch	00h	-	V232BP[6:0]								
			E40Dh	00h	-	V240BP[6:0]								
			E40Eh	00h	V247BP[7:0]									
			E40Fh	00h	V251BP[7:0]									
			E410h	00h	-	V254BP[6:0]								
E411h	00h	-	V255BP[6:0]											

6.2.32 GAMCTRLNB: Set Gamma Correction Characteristics For Negative "B" (E5h)

Inst / Para	R/W	Address			Parameter									
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0		
GAMCTBLNB	Write	E5h	E500h	00h	-	V0BN[6:0]								
			E501h	00h	-	V1BN[6:0]								
			E502h	00h	V4BN[7:0]									
			E503h	00h	V8BN[7:0]									
			E504h	00h	-	V16BN[6:0]								
			E505h	00h	-	V24BN[6:0]								
			E506h	00h	-	V52BN[6:0]								
			E507h	00h	V80BN[7:0]									
			E508h	00h	-	-	V108BN[5:0]							
			E509h	00h	-	-	V148BN[5:0]							
			E50Ah	00h	V176BN[7:0]									
			E50Bh	00h	-	V204BN[6:0]								
			E50Ch	00h	-	V232BN[6:0]								
			E50Dh	00h	-	V240BN[6:0]								
			E50Eh	00h	V247BN[7:0]									
			E50Fh	00h	V251BN[7:0]									
			E510h	00h	-	V254BN[6:0]								
E511h	00h	-	V255BN[6:0]											

6.2.33 DSTB: Enter Deep Standby Mode (E8h)

Inst / Para	R/W	Address			Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0	
DSTB	Write	E8h	E800h	00h	0	0	0	0	0	0	0	0	DSTB

NOTE: "-" Don't care

Description	DSTB=1, Enter Deep standby mode - DSTB can be executed in normal, partial & sleep in mode - After executing DSTB, RAM data & registers won't be kept - Set RESET to exit deep standby mode													
Restriction	-													
Register Available	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability													
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
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Sleep In	Yes													
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Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart														

6.2.34 ENECMD: Enable Extend Command (F0h)

Inst / Para	R/W	Address		Parameter								
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
ENECMD	Write	F0h	F000h	00h	1	0	1	0	1	0	1	0
			F001h	00h	0	1	0	1	0	1	0	1
			F002h	00h	0	1	0	1	0	0	1	0

NOTE: "-" Don't care

Description	Enable extend command Set extend command first when executing the LV2 command.													
Restriction	-													
Register Available	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													

6.2.35 GMACMD: GAMMA Write & Read Command (FEh)

Inst / Para	R/W	Address			Parameter							
		Others	MDDI	D[15:8] (MDDI)	D7	D6	D5	D4	D3	D2	D1	D0
GMACMD	Write	FEh	FE00h	00h	-	-	-	GMA_RD	GMA_WR	-	-	-

NOTE: "-" Don't care

Description	<p>GMA_WR: Write GAMMA code. GMA_RD: Read GAMMA code</p> <p>Ex: Gamma code write sequence</p> <ol style="list-style-type: none"> 1. 0xF0, 0xAA, 0x55, 0x52 2. 0x11 3. Delay 120ms 4. 0x26, 0x10 5. 0xE0~0xE5 (set Gamma code what you want) 6. 0xFE, 0x08 7. Delay 120ms 8. 0x29 <p>Ex: Gamma code read sequence</p> <ol style="list-style-type: none"> 1. 0xF0, 0xAA, 0x55, 0x52 2. 0x11 3. Delay 120ms 4. 0x26, 0x10 5. 0xE0~0xE5 (set Gamma code what you want) 6. 0xFE, 0x08 7. Delay 120ms 8. Read 0xE0~0xE5 (Read Gamma code) 												
Restriction													
Register Available	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												

6.3 INSTRUCTION SETUP FLOW

6.3.1 Initializing with the Built-in Power Supply Circuits

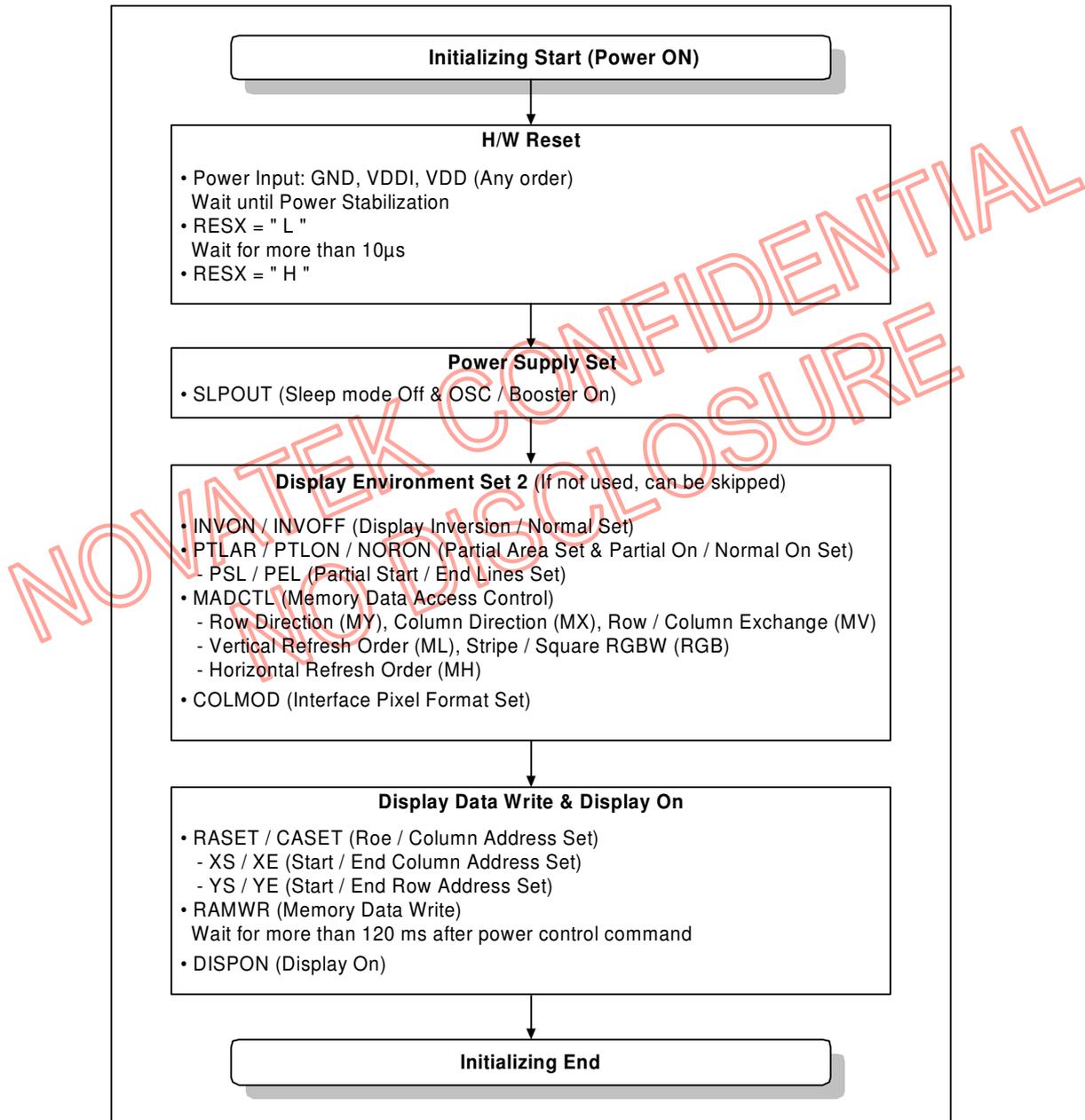


Fig. 6.3.1 Initializing with the built-in power supply circuit

The initializing sequence does not have any effect on the display. The display is in its normal background color during the initializing.

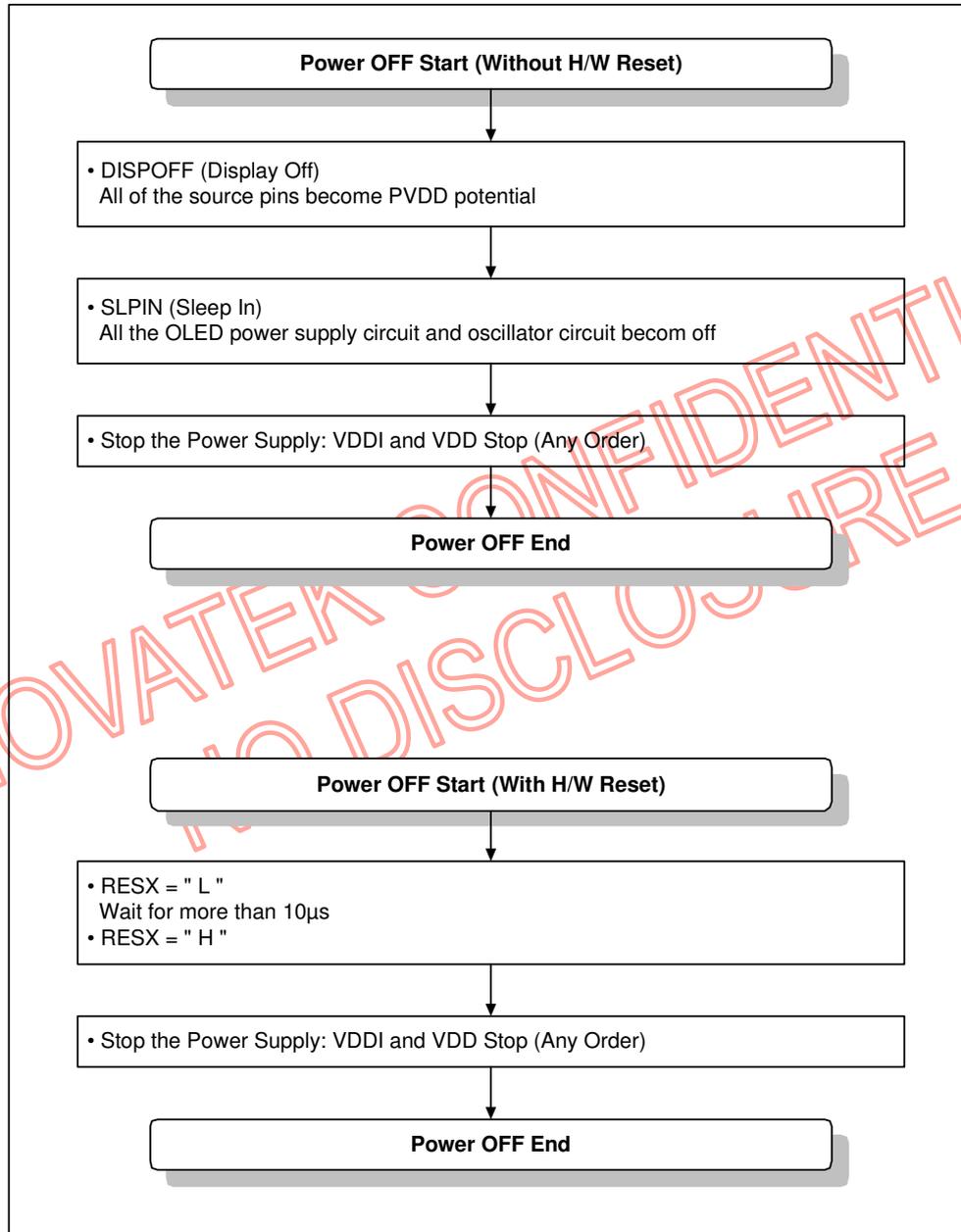
6.3.2 Power OFF Sequence


Fig. 6.3.2 Power off sequence

7 SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply voltage	VDDI, LVDSVDD	-0.3 ~ +5.5	V
Supply voltage	VPNL, VPNLR	- 0.3 ~ +5.5	V
Supply voltage (Digital)	VCC	-0.3 ~ +1.8	V
Driver supply Voltage	PAVDD	-0.3 ~ +6.5	V
Driver supply Voltage	VGH-VGL	-0.3 ~ +32.0	V
Operating temperature range	TOPR	-30 ~ +70	°C
Storage Temperature range	TSTG	-55 ~ +125	°C
Logic Input voltage range	V _{IN}	-0.3 ~ VDDI+0.3	V
Logic Input voltage range	V _O	-0.3 ~ VDDI+0.3	V
Supply voltage (MTP)	VOTP	- 0.3 ~ 7.8	V
Humidity	-	5% to 95%	%

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

7.2 ESD PROTECTION LEVEL

Table 7.2.1 ESD models.

Model	Test Condition	Protection Level	Unit
Human Body Model	C = 100 pF, R = 1.5 kΩ	> 3000	V
Machine Model	C = 200 pF, R = 0.0 Ω	> 300	V
Air ESD discharge	C=150 pF, R = 330 Ω	±6000	V
Contact ESD discharge		±6000	V

7.3 LATCH-UP PROTECTION LEVEL

The device will not latch up at trigger current levels less than ±100 mA.

7.4 LIGHT SENSITIVITY

The operation of the IC will not be materially altered by incident light.

7.5 MAXIMUM SERIES RESISTANCE

The driver will operate in "Chip on Glass" applications with series resistances (due to ITO track resistance). Voltages are specified at module I/O assuming maximum values as in **Table 7.5.1**.

Table 7.5.1 Maximum series resistance on module.

Name	Type	Maximum Series Resistance	Unit
VDDI/VDDIL	Power supply	10	Ω
VPNL, LVDSVDD, VPNL_DET, VREF	Power supply	5	Ω
VSS, AVSS, LVDSVSS	Ground	5	Ω
CVSS	Ground	5	Ω
IM3, IM2, IM1, IM0	Input	50	Ω
RESX, CSX, DCX, WRX/SCL, RDX, SDI, SDO, TE, HS, VS, DE, ERR D23 to D0, VSEL	Input	50	Ω
PCLK	Input	50	Ω
D0_P, D0_N, CLK_P, CLK_N	Input	5	Ω
BC_R, BC_L, TE_R, TE_L	Output	50	Ω
VCCM12, LVDSVDD	Capacitor connection	10	Ω
VCOM	Capacitor connection	5	Ω
VGH, VGL	Capacitor connection	20	Ω
PAVDD, NAVDD, VCL	Capacitor connection	5	Ω
C11P, C11N, C12P, C12N, C13P, C13N, C21P, C21N, C22P, C22N, C23P, C23N, C31P, C31N,	Capacitor connection	5	Ω
C41P, C41N, C51P, C51N	Capacitor connection	5	Ω
VOTP	Power supply	15	Ω
DIOPWR, NVDDI	Power supply	10	Ω
VCC, VCCI	Power supply	5	Ω

7.6 DC CHARACTERISTICS

7.6.1 Basic Characteristics

Parameter	Symbol	Conditions	Specification			Unit	Related Pins
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	VPNL	Operating Voltage	2.3	2.8	4.8	V	Note 1, 2
Logic Operating voltage	VDDI	I/O supply voltage	1.65	1.8	4.8	V	Note 1, 2
Panel Power Supply Voltage Noise	VPNL_noise	Noise Range, 0 to 100MHz, Sinusoidal Wave	-	-	100	mV, peak to peak	
		Noise Range, 0 to 30KHz, Pulse Wave with Duty Cycle(50%/50%)	-	-	500	mV, peak to peak	
Panel Power Supply Voltage (Logic) Noise	VDDI_noise	Noise Range, 0 to 100MHz, Sinusoidal Wave	-	-	100	mV, peak to peak	
Input / Output							
Logic High level input voltage	VIH	-	0.7 VDDI	-	VDDI	V	Note 1, 2,
Logic Low level input voltage	VIL	-	VSS	-	0.3 VDDI	V	Note 1, 2,
Logic High level output voltage	VOH	IOH = -1.0mA	0.8 VDDI	-	VDDI	V	Note 1, 2
Logic Low level output voltage	VOL	IOL = +1.0mA	VSS	-	0.2 VDDI	V	Note 1, 2
Logic High level leakage	ILIH	-	-	-	1	μA	Note 1, 2
Logic Low level leakage	ILIL	-	-1	-	-	μA	Note 1, 2
VCOM Operation							
VCOM voltage	VCOM	Operating Voltage	-2.3	-	-0.2	V	Note 6
Source Driver							
Source output range	VSout		0.1		PAVDD-0.1	V	Note 3
			NAVDD+0.1		-0.1	V	Note 3
Positive Gamma high voltage	VGMP		3.5		5.9	V	Note 5
Negative Gamma low voltage	VGMN		-5.5		-3.5	V	Note 5
Positive Gamma low voltage	VGSP		0.5		2.5	V	Note 5
Negative Gamma high voltage	VGSN		-2.5		-0.5	V	Note 5
Source output settling time	Tr	Below with 99% precision		15	20	μS	60Hz Fig.7.6.2
Positive Output deviation voltage	V, dev	Sout>=4.2V,Sout<=0.8V			20	mV	Fig.7.6.3 Note 3
	V, dev	4.2V>Sout>0.8V			6	mV	Note 3
Negative Output deviation voltage	V, dev	Sout<=-4.2V,Sout<=-0.8V			20	mV	Fig.7.6.3 Note 3
	V, dev	-4.2V<Sout<-0.8V			6	mV	Note 3
Output offset voltage	VOFSET				35	mV	Note 4
Booster Operation							
1 st Booster voltage	PAVDD				6.5	V	Note 4
2 nd Booster voltage	NAVDD		-6.5			V	Note 4

3 rd Booster voltage	VCL			-VPNL		V	Note 4
4 th Booster voltage	VGH		PAVDD+ VPNL	-	2*PAVDD- NAVDD	V	-
5 th Booster voltage	VGL		2*NAVDD- PAVDD	-	VCL+NAVDD D	V	-
Oscillator tolerance	OSC	25°C	-5	-	+5	%	
Oscillator tolerance	OSC	70°C ~ -30°C	-8	-	+8	%	

Note 1: VDDI=1.65 to 4.8V, VPNL=2.3 to 4.8V, AVSS=VSS=VSSR=0V, Ta=-30 to 70 °C (to +85 °C no damage)

Note 2, When the measurements are performed with LCD module, measurement points are like below.

CSX, RDX, WRX, D[23:0], DCX, RESX, SDI, SDO, IM[3:0] and Test pins

Note 3: Source channel loading = 40pF/channel

Note 4: VPNL=2.85V, Ta=25°C, No load on the panel, booster multiple =2.5x or 3x

Note 5: PAVDD=6.5V, NAVDD=-6.5V

Note 6: VPNL>=2.8V

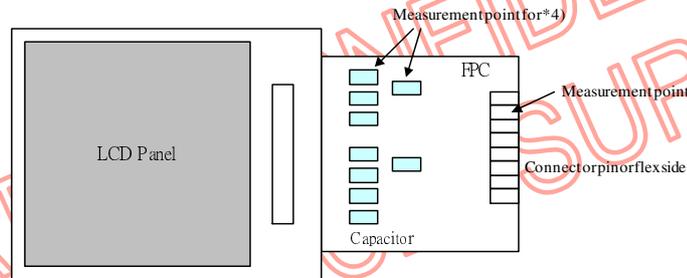


Fig. 7.6.1 Measurement Points for All Characteristics.

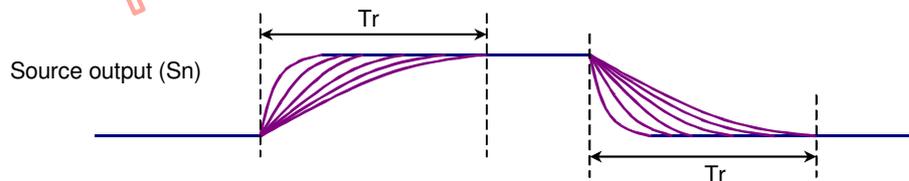


Fig. 7.6.2 Tr: Source output stable timing

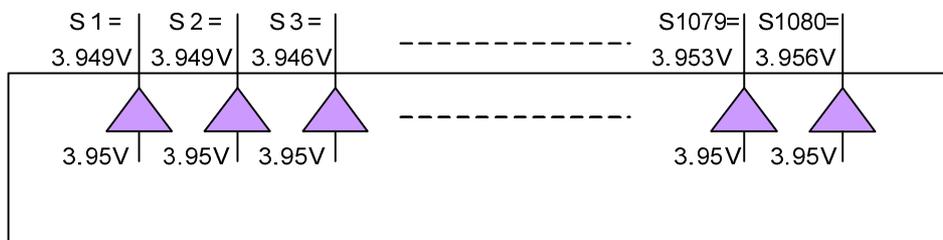


Fig. 7.6.3 Source output deviation (Channel by Channel)

- When $S_{out} \geq 4.2V$, $S_{out} \leq 0.8V$
 $\text{Max}(S1, S2, S3, \dots, S1080) - \text{Min}(S1, S2, S3, \dots, S1080) \leq 20mV$
- When $4.2V > S_{out} > 0.8V$
 $\text{Max}(S1, S2, S3, \dots, S1080) - \text{Min}(S1, S2, S3, \dots, S1080) \leq 6mV$
- Example
 When S_{out} level is 3.95V (Gray scale voltage)
 $\text{Max}(S1, S2, S3, \dots, S1080) = 3.956V$
 $\text{Min}(S1, S2, S3, \dots, S1080) = 3.946V$
 S_{out} deviation =
 $\text{Max}(S1, S2, S3, \dots, S1080) - \text{Min}(S1, S2, S3, \dots, S1080) = 10mV$ <- Out Spec

7.6.2 Current Consumption

16.7Mcolors, nHD, 3.5"Transmissive, Normally Black, $T_a=25^\circ C$, $V_{DDI}=1.8V$, $V_{PNL}=2.78V$, MCU interface, No Access				
Mode Of Operation	Condition	Image	Power Consumption	
			IDD1(μA)	IPNL (mA)
Normal Mode on	Column inversion 60Hz	White	2	20
Partial Mode off		Black	2	18
Idle Mode off		Check 1x1	2	21.5
Sleep out mode				
Normal Mode off	Column inversion 30Hz	White	2	8
Partial Mode off		Black	2	8
Idle Mode on		Check 4x4	2	10
Sleep out mode				
Sleep in mode	RAM Power Off MIPI LP mode	-	2	0.1
Sleep in mode	RAM Power Off MIPI ULPM	-	2	0.06
Deep standby mode	DSTB_SEL=0		1	0.005

7.6.3 MIPI Characteristics
7.6.3.1 DC Characteristics for DSI LP Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Logic high level input voltage	VIHLPCD	LP-CD	450	-	1350	mV
Logic low level input voltage	VILLPCD	LP-CD	0	-	200	mV
Logic high level input voltage	VIHLPRX	LP-RX (CLK, D0)	880	-	1350	mV
Logic low level input voltage	VILLPRX	LP-RX (CLK, D0)	0	-	550	mV
Logic low level input voltage	VILLPRX ULP	LP-RX (CLK ULP mode)	0	-	300	mV
Logic high level output voltage	VOHLPT X	LP-TX (D0)	1.1	-	1.3	V
Logic low level output voltage	VOLLPT X	LP-TX (D0)	-50	-	50	mV
Logic high level input current	I _{IH}	LP-CD, LP-RX	-	-	10	μA
Logic low level input current	I _{IL}	LP-CD, LP-RX	-10	-	-	μA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-D0+/- (Note 3)	-	-	300	Vps

Note 1) $V_{DDI}=1.65\sim 4.8V$, $V_{PNL}=2.3$ to $4.8V$, $V_{SS}=0V$, $T_a=30$ to 70 °C (to $+85$ °C no damage).

Note 2) DSI high speed is off.

Note 3) Peak interference amplitude max. 200mV and interference frequency min. 450MHz.

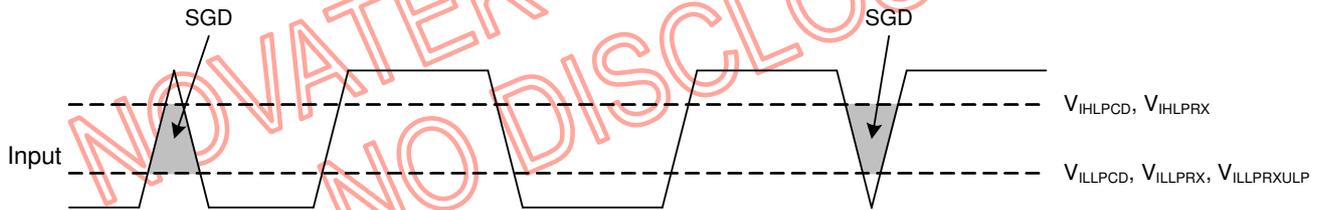


Fig. 7.6.5 Spike/Glitch rejection-DSI

7.6.3.2 DC CHARACTERISTICS FOR DSI HS MODE

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Input voltage common mode range	VCMCLK VCMDATA	DSI-CLK+/-, DSI-D0+/- (Note2, 3)	70	-	330	mV
Input voltage common mode variation ($\leq 450\text{MHz}$)	VCMRCLKL VCMRDATAL	DSI-CLK+/-, DSI-D0+/- (Note 4)	-50	-	50	mV
Input voltage common mode variation ($\geq 450\text{MHz}$)	VCMRCLKM VCMRDATAM	DSI-CLK+/-, DSI-D0+/-	-	-	100	mV
Low-level differential input voltage threshold	VTHLCLK VTHLDATA	DSI-CLK+/-, DSI-D0+/-	-70	-	-	mV
High-level differential input voltage threshold	VTHHCLK VTHHDATA	DSI-CLK+/-, DSI-D0+/-	-	-	70	mV
Single-ended input low voltage	VILHS	DSI-CLK+/-, DSI-D0+/- (Note 3)	-40	-	-	mV
Single-ended input high voltage	VIHHS	DSI-CLK+/-, DSI-D0+/- (Note 3)	-	-	460	mV
Differential input termination resistor	RTERM	DSI-CLK+/-, DSI-D0+/-	80	100	125	Ω
Single-ended threshold voltage for termination enable	VTERM-EN	DSI-CLK+/-, DSI-D0+/-	-	-	450	mV
Termination capacitor	CTERM	DSI-CLK+/-, DSI-D0+/-	-	-	14	pF

Note 1) $V_{DDI}=1.65\sim 4.8\text{V}$, $V_{PNL}=2.3$ to 4.8V , $V_{SS}=0\text{V}$, $T_a=-30$ to 70°C (to $+85^\circ\text{C}$ no damage).

Note 2) Includes 50mV (-50mV to 50mV) ground difference.

Note 3) Without $V_{CMRCLKM}$ / $V_{CMRDATAM}$.

Note 4) Without 50mV (-50mV to 50mV) ground difference.

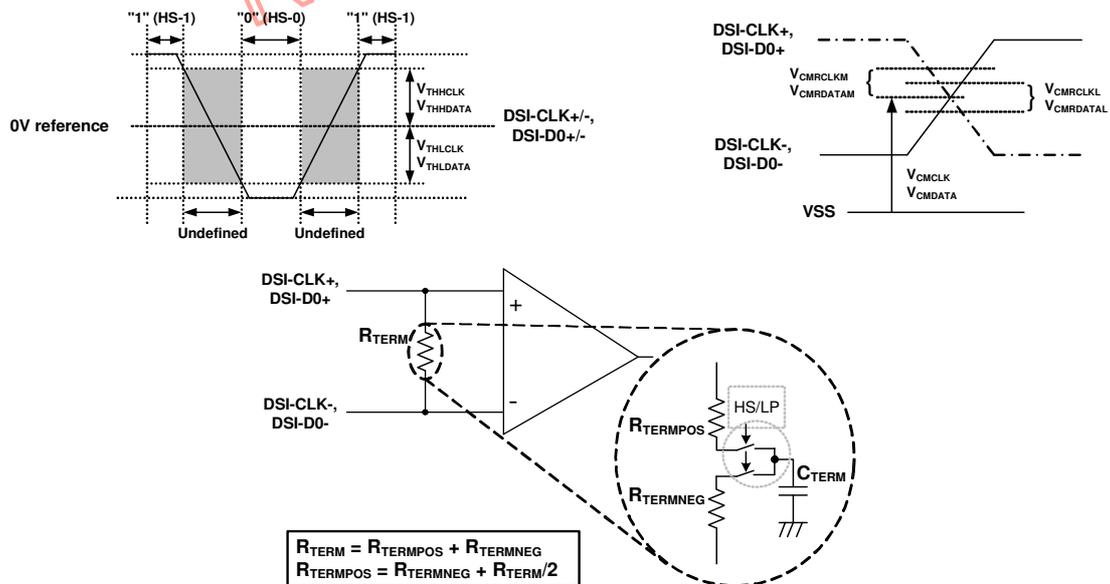


Fig. 7.6.6 Differential voltage range, termination resistor and Common mode voltage

7.6.4 MDDI Characteristics

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Differential input "High" level voltage (hibernation wake up)	$V_{IT+offset}$	$V_T=125mV$ (MDDI_DATA_P/M)	-	100	125	mV
Differential input "Low" level voltage (hibernation wake up)	$V_{IT-offset}$	$V_T=125mV$ (MDDI_DATA_P/M)	75	100	-	mV
Differential input "High" level voltage	V_{IT+}	$V_T=0mV$ (MDDI_STB_P/M, MDDI_DATA_P/M)	-	0	50	mV
Differential input "Low" level voltage	V_{IT-}	$V_T=0mV$ (MDDI_STB_P/M, MDDI_DATA_P/M)	-50	0	-	mV
Terminal impedance	Z_t	-	80	-	125	ohm

Note 1) $V_{DDI}=1.65\sim 4.8V$, $V_{PNL}=2.3$ to $4.8V$, $V_{SS}=LVDSV_{SS}=0V$, $T_a=-30$ to $70^\circ C$ (to $+85^\circ C$ no damage).

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7.7 AC CHARACTERISTICS

7.7.1 Parallel Interface Characteristics (80-Series MCU)

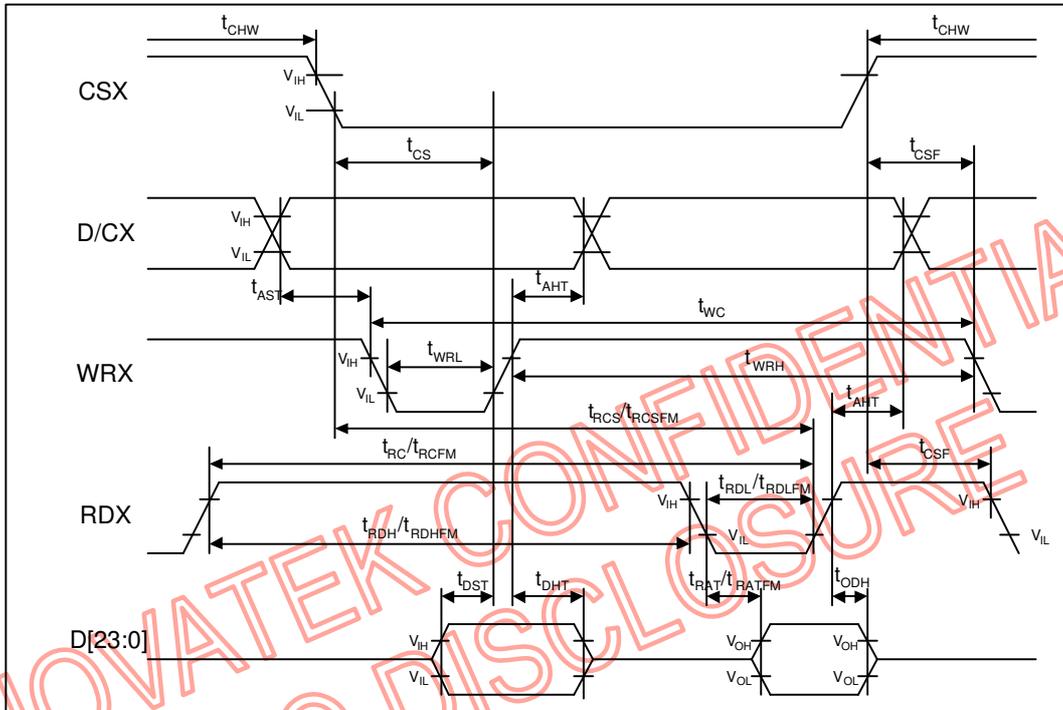
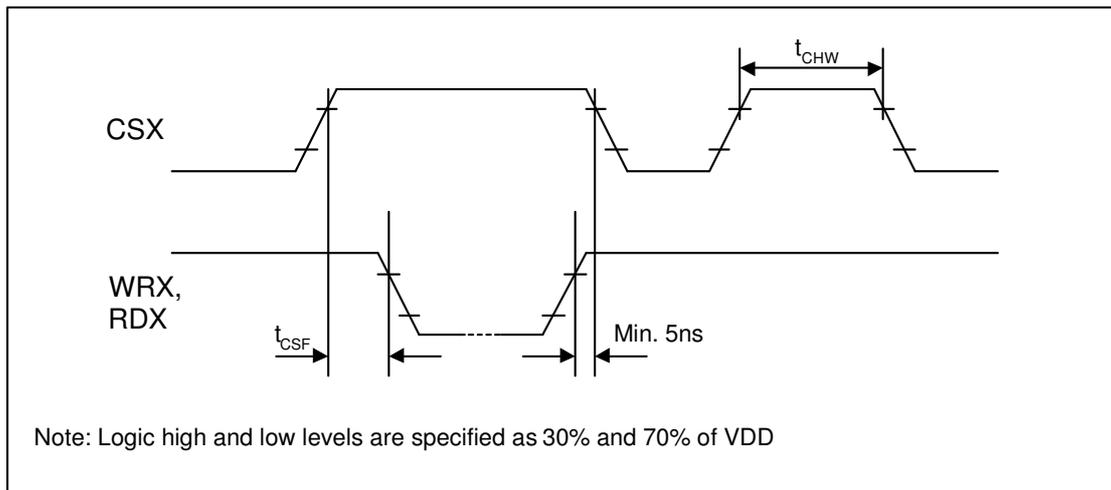


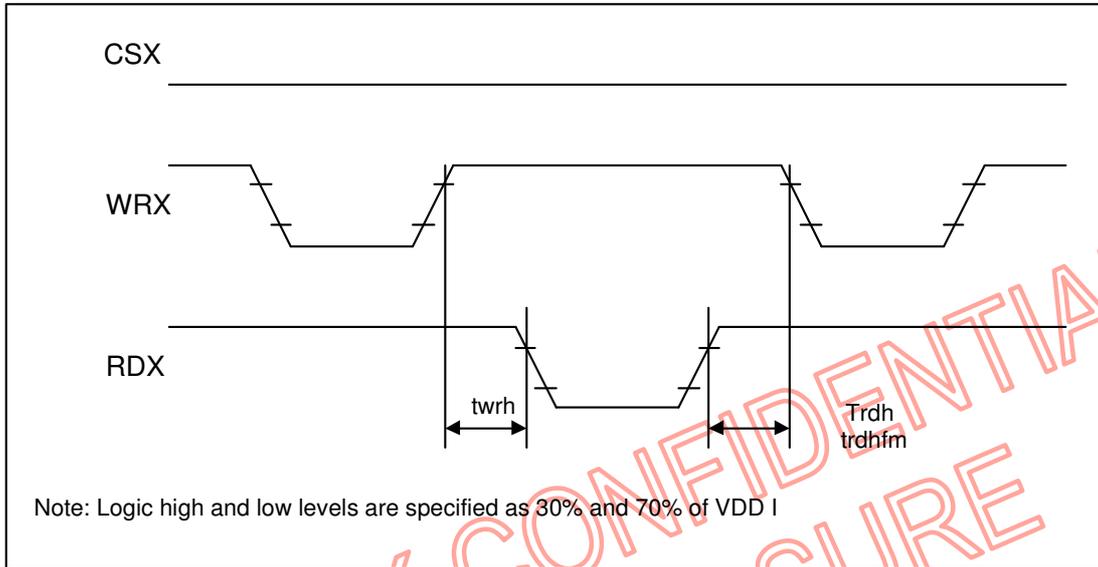
Fig. 7.7.1 Parallel interface characteristics (80-Series)

CSX timings:



Note: Logic high and low levels are specified as 30% and 70% of VDD

Write to read or read to write timings:



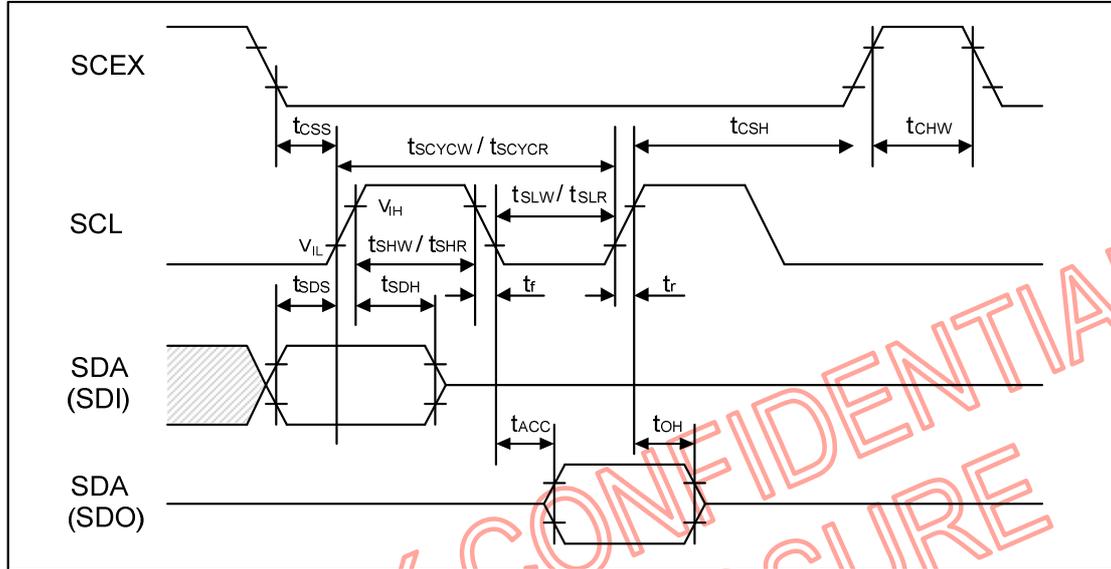
(VSS=0V, VDDI=1.65V to 4.8V, VPNL=2.3V to 4.8V, Ta = -30 to 70 °C)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DCX	tAST	Address setup time	0	-	ns	
	tAHT	Address hole time	10	-	ns	
CSX	tCHW	CSX "H" pulse width	0	-	ns	
	tCS	Chip select setup time (Write)	15	-	ns	
	trCS	Chip select setup time (Read ID)	45	-	ns	
	trCSFM	Chip select setup time (Read FM)	355	-	ns	
WRX	tCSF	Chip select wait time (Write/Read)	10	-	ns	
	tWC	Write cycle	37	-	ns	
	tWRH	Control pulse "H" duration	15	-	ns	
RDX(ID)	tWRL	Control pulse "L" duration	15	-	ns	
	trC	Read cycle (ID)	160	-	ns	
	trDH	Control pulse "H" duration (ID)	90	-	ns	When read ID data
RDX(FM)	trDL	Control pulse "L" duration (ID)	45	-	ns	
	trCFM	Read cycle (FM)	450	-	ns	
	trDHFM	Control pulse "H" duration (FM)	90	-	ns	When read from frame memory
D[17:0]	trDLFM	Control pulse "L" duration (FM)	355	-	ns	
	tDST	Data setup time	10	-	ns	
	tDHT	Data hold time	10	-	ns	
	trAT	Read access time (ID)	-	40	ns	For maximum CL=30pF
	trATFM	Read access time (FM)	-	340	ns	For minimum CL=8pF
	tODH	Output disable time	20	80	ns	

Note 1) VDDI=1.65 to 4.8V, VPNL=2.3 to 4.8V, VSS=0V, Ta=-30 to 70 °C (to +85 °C no damage)

Note 2) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.7.2 Serial Interface Characteristics (3-Pin Serial)

Fig. 7.7.2 3-pin serial interface characteristics

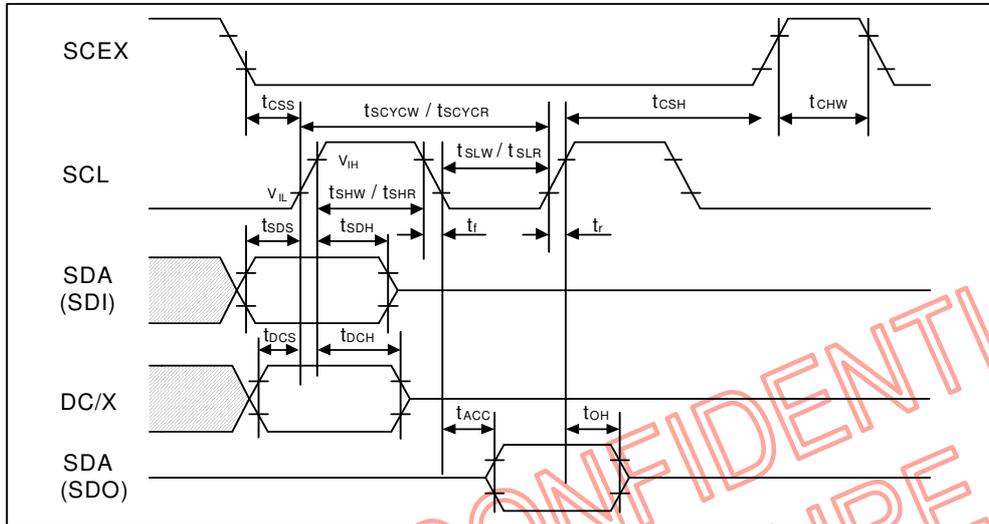
(VSS=0V, VDDI=1.65V to 4.8V, VPNL=2.3V to 4.8V, Ta = -30 to 70 °C)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
SCL	t_{SCYW}	Serial clock cycle (Write)	37	-	ns	
	t_{SHW}	SCL "H" pulse width (Write)	15	-	ns	
	t_{SLW}	SCL "L" pulse width (Write)	15	-	ns	
	t_{SCYCR}	Serial clock cycle (Read GRAM)	150	-	ns	
	t_{SHR}	SCL "H" pulse width (Read GRAM)	60	-	ns	
	t_{SLR}	SCL "L" pulse width (Read GRAM)	60	-	ns	
	t_{SCYCR}	Serial clock cycle (Read ID)	150	-	ns	
	t_{SHR}	SCL "H" pulse width (Read ID)	60	-	ns	
SDI (SDO)	t_{SDS}	Data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	t_{SDH}	Data hold time	10	-	ns	
	t_{ACC}	Access time	10	50	ns	
	t_{OH}	Output disable time	15	50	ns	
CSX	t_{CHW}	Chip select "H" pulse width	40	-	ns	
	t_{CSS}	Chip select setup time (Write)	15	-	ns	
	t_{CSH}	Chip select hold time (Write)	15	-	ns	
	t_{CSS}	Chip select setup time (Read)	60	-	ns	
	t_{CSH}	Chip select hold time (Read)	60	-	ns	

Note 1) VDDI=1.65 to 4.8V, VPNL=2.3 to 4.8V, VSS=0V, Ta=-30 to 70 °C (to +85 °C no damage)

 Note 2) The input signal rise time and fall time (t_r , t_f) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.7.3 Serial Interface Characteristics (4-Pin Serial)

Fig. 7.7.3 4-pin serial interface characteristics

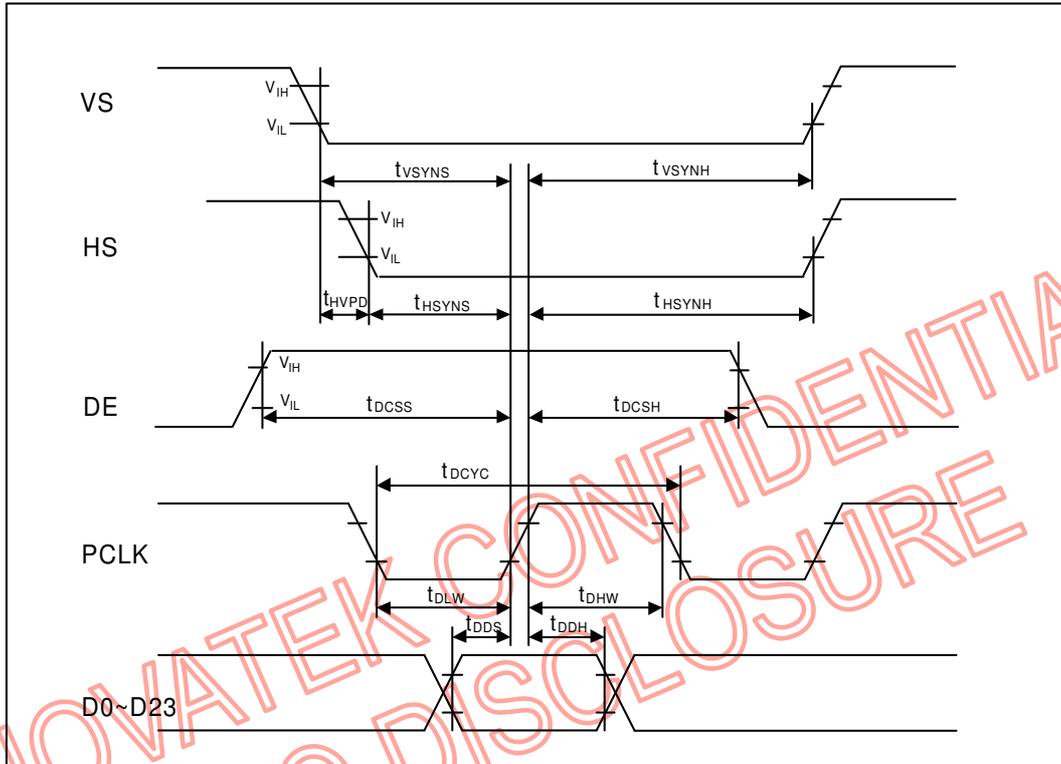
(VSS=0V, VDDI=1.65V to 4.8V, VPNL=2.3V to 4.8V, Ta = -30 to 70 °C)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
SCL	t_{SCYW}	Serial clock cycle (Write)	37	-	ns	
	t_{SHW}	SCL "H" pulse width (Write)	15	-	ns	
	t_{SLW}	SCL "L" pulse width (Write)	15	-	ns	
	t_{SCYCR}	Serial clock cycle (Read GRAM)	150	-	ns	
	t_{SHR}	SCL "H" pulse width (Read GRAM)	60	-	ns	
	t_{SLR}	SCL "L" pulse width (Read GRAM)	60	-	ns	
	t_{SCYCR}	Serial clock cycle (Read ID)	150	-	ns	
	t_{SHR}	SCL "H" pulse width (Read ID)	60	-	ns	
SDI (SDO)	t_{SDS}	Data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	t_{SDH}	Data hold time	10	-	ns	
	t_{ACC}	Access time	10	50	ns	
	t_{OH}	Output disable time	15	50	ns	
DC/X	t_{DCS}	DC/X setup time	10	-	ns	
	t_{DCH}	DC/X hold time	10	-	ns	
CSX	t_{CHW}	Chip select "H" pulse width	40	-	ns	
	t_{CSS}	Chip select setup time (Write)	15	-	ns	
	t_{CSH}	Chip select hold time (Write)	15	-	ns	
	t_{CSS}	Chip select setup time (Read)	60	-	ns	
	t_{CSH}	Chip select hold time (Read)	60	-	ns	

Note 1) VDDI=1.65 to 4.8V, VPNL=2.3 to 4.8V, VSS=0V, Ta=-30 to 70 °C (to +85 °C no damage)

 Note 2) The input signal rise time and fall time (t_r , t_f) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.7.4 RGB Interface Characteristics

Fig. 7.7.4 RGB interface characteristics

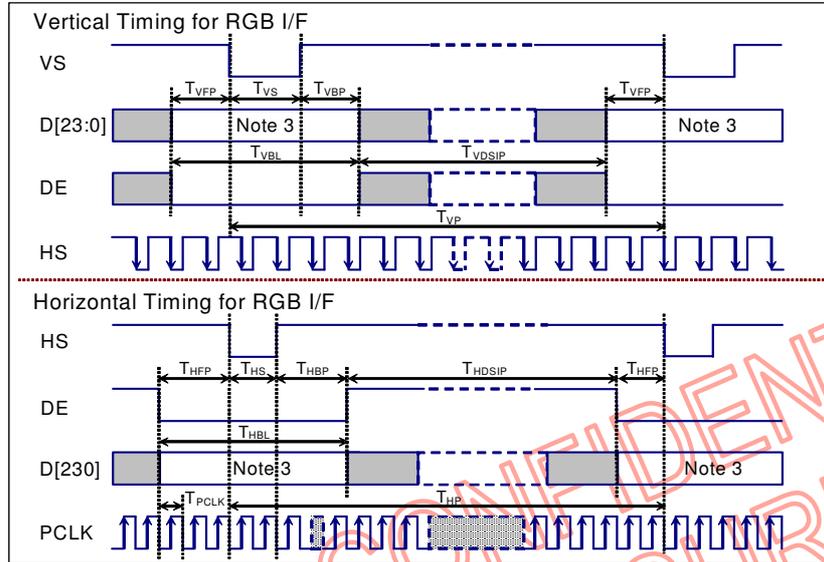
(VSS=0V, VDDI=1.65V to 4.8V, VPNL=2.3V to 4.8V, Ta = -30 to 70 °C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
VS	t _{VSYNS}	VSYNC setup time	10	-	-	ns	
	t _{VSYNH}	VSYNC hold time	10	-	-	ns	
HS	t _{HSYNS}	HSYNC setup time	10	-	-	ns	
	t _{HSYNH}	HSYNC hold time	10	-	-	ns	
	t _{HVPD}	HSYNC to VSYNC falling edge	0	-	-	ns	
PCLK	t _{DCYC}	PCLK cycle time	40	-	125	ns	
	t _{DLW}	PCLK "L" pulse width	10	-	-	ns	
	t _{DHW}	PCLK "H" pulse width	10	-	-	ns	
	f _{DFREQ}	PCLK frequency	8	-	25	MHz	
DE	t _{DCSS}	DE setup time	10	-	-	ns	
	t _{DCSH}	DE hold Time	10	-	-	ns	
D0~D23	t _{DDS}	RGB Data setup time	10	-	-	ns	
	t _{DDH}	RGB Data hold time	10	-	-	ns	

Note 1) VDDI=1.65 to 4.8V, VPNL=2.3 to 4.8V, VSS=0V, Ta=-30 to 70 °C (to +85 °C no damage)

Note 2) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.


Fig. 7.7.5 Vertical and Horizontal timing for RGB I/F

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
VS	TVP	Vertical cycle period	694	-	1023	HS	360x640
			534	-	1023	HS	360x480
			534	-	1023	HS	320x480
	TVS	Vertical "L" pulse width	2	-	-	HS	
	TVBP	Vertical back porch period	2	-	64	HS	
	TVFP	Vertical front porch period	50	-	1023	HS	
	TVBL	Vertical blanking period	54	-	-	HS	TVS + TVBP + TVFP
	TVDISP	Vertical active area	-	640	-	HS	360x640
-	480		-	HS	360x480		
-	480		-	HS	320x480		
TVRR	Vertical refresh rate	5	-	80	Hz	Frame Rate	
HS	THP	Horizontal cycle period	374	-	-	PCLK	360x640
			374	-	-	PCLK	360x480
			334	-	-	PCLK	320x480
	THS	Horizontal "L" pulse width	2	-	-	PCLK	
	THBP	Horizontal back porch period	2	-	64	PCLK	
	THFP	Horizontal front porch period	10	-	1023	PCLK	
	THBL	Horizontal blanking period	14	-	-	PCLK	THS + THBP + THFP
	THDISP	Horizontal active area	-	360	-	PCLK	360x640
-	360		-	PCLK	360x480		
-	320		-	PCLK	320x480		

PCLK	TPCLK	Pixel clock cycle time	50	-	-	ns	
			-	-	20	MHz	

(VSS=0V, VDDI=1.65V to 4.8V, VPNL=2.3V to 4.8V, Ta = -30 to 70 °C)

Note 1) Measuring of input signals are using 0.3 x VDDI for low state and 0.7 x VDDI for high state.

Note 2) Data lines can be set to "High" or "Low" during blanking time – Don't care.

Note 3) HS is multiples of eight PCLK.

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7.7.5 MIPI DSI Timing Characteristics
7.7.5.1 High Speed Mode

(VSS=0V, VDDI=1.65V to 4.8V, VPNL=2.3V to 4.8V, Ta = -30 to 70 °C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	-	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halves	2	-	12.5	ns	UI = UI_{INSTA} = UI_{INSTB}
DSI-D0+/-	t_{DS}	Data to clock setup time	$0.15xUI$	-	-	ps	
DSI-D0+/-	t_{DH}	Data to clock hold time	$0.15xUI$	-	-	ps	
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	$0.3xUI$	ps	
DSI-D0+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	$0.3xUI$	ps	
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	$0.3xUI$	ps	
DSI-D0+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	$0.3xUI$	ps	



Fig. 7.7.6 DSI clock channel timing

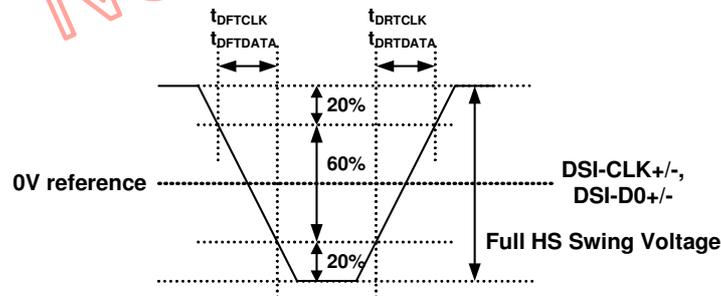
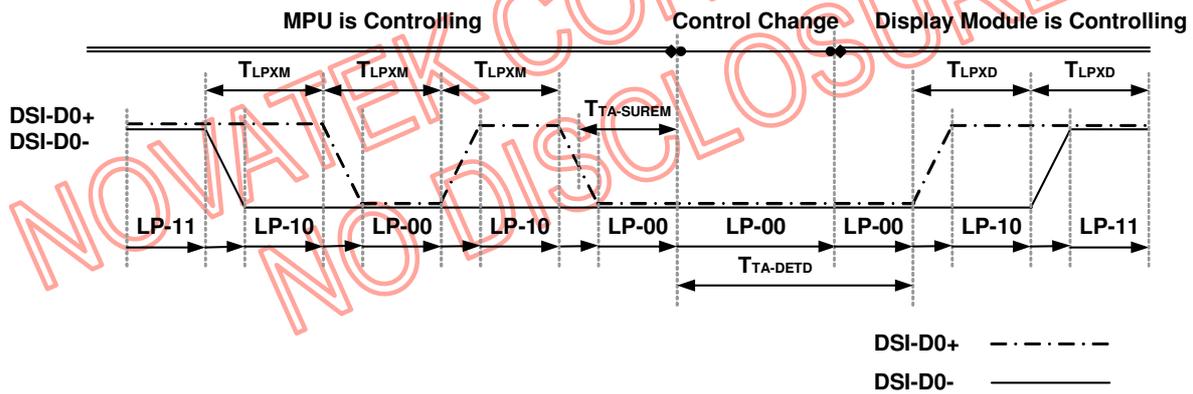
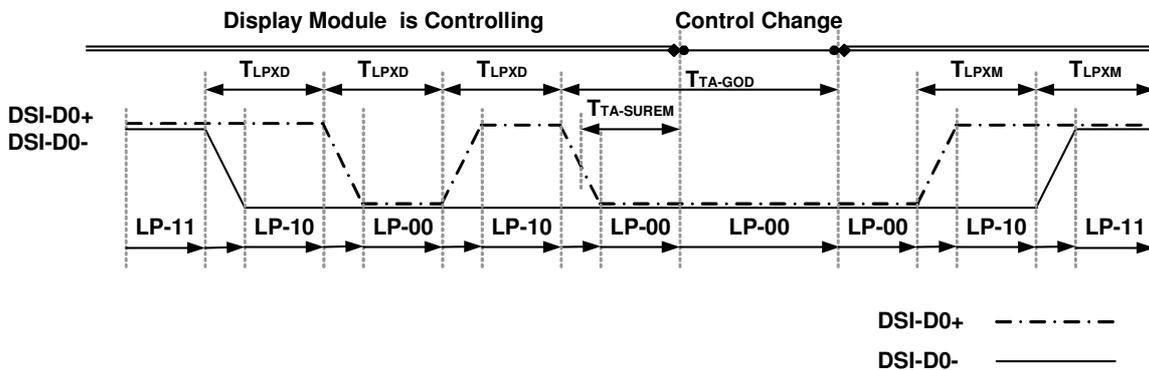


Fig. 7.7.7 Rising and fall time on clock and data channel

7.7.5.2 Low Power Mode

(VSS=0V, VDDI=1.65V to 4.8V, VPNL=2.3V to 4.8V, Ta = -30 to 70 °C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-D0+/-	T _{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module	50	-	75	ns	Input
DSI-D0+/-	T _{TA-SUREM}	Time-out before the display module start driving	T _{LPXM}	-	2xT _{LPXM}	ns	Input
DSI-D0+/-	T _{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU	50	-	75	ns	Output
DSI-D0+/-	T _{TA-SURED}	Time-out before the MPU start driving	T _{LPXM}	-	2xT _{LPXM}	ns	Output
DSI-D0+/-	T _{TA-GETD}	Time to drive LP-00 by display module	5xT _{LPXD}	-	-	ns	Input
DSI-D0+/-	T _{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	4xT _{LPXD}	-	-	ns	Output


Fig. 7.7.8 Bus Turnaround (BAT) from MPU to display module Timing

Fig. 7.7.9 Bus Turnaround (BAT) from display module to MPU Timing

7.7.5.3 DSI BURSTS

(VSS=0V, VDDI=1.65V to 4.8V, VPNL=2.3V to 4.8V, Ta = -30 to 70 °C)

Symbol	Description	MIN	TYP	MAX	Unit	Note
Low Power Mode to High Power Mode Timing (Data Lane)						
T _{LPX}	Length of any low power state period	50	-	-	ns	
T _{HS-PREPARE}	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Note 2
T _{HS-PREPARE+} T _{HS-ZERO}	T _{HS-PREPARE} + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	300	-	-	ns	
T _{D-TERM-EN}	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	-	35+4xUI	ns	
T _{HS-SETTLE}	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of T _{HS-PREPARE-} .	85 ns + 6*UI	-	145 ns + 10*UI	ns	
High Speed Mode to Low Power Mode Timing (Data Lane)						
T _{HS-SKIP}	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	
T _{HS-SKIP}	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	
T _{HS-EXIT}	Time to drive LP-11 after HS burst	100	-	-	ns	Note 2
T _{HS-TRAIL}	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max(8*UI, 60 ns+ 4*UI)	-	-	-	Note 1
High Speed Mode to/from Low Power Mode Timing (Clock Lane)						
T _{CLK-MISS}	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns	
T _{CLK-POST}	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+52xUI	-	-	-	Note 2
T _{CLK-TRAIL}	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Note 2
T _{HS-EXIT}	Time to drive LP-11 after HS burst	100	-	-	ns	
T _{CLK-PREPARE}	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Note 2
T _{CLK-TERM-EN}	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	
T _{CLK-PREPARE} + T _{CLK-ZERO}	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Note 2
T _{CLK-PRE}	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	UI	
T _{CLK-SETTLE}	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of T _{CLK-PREPARE-} .	95	-	300	ns	
T _{EOT}	Transmitted time interval from the start of T _{HS-TRAIL} or T _{CLK-TRAIL} , to the start of the LP-11 state following a HS burst.	-	-	105 ns + 12*UI	-	Note 2

Note :

1. If $a > b$ then $\max(a, b) = a$ otherwise $\max(a, b) = b$
2. Transmitter-specific parameter, the timing of transmitter shall meet this requirement.

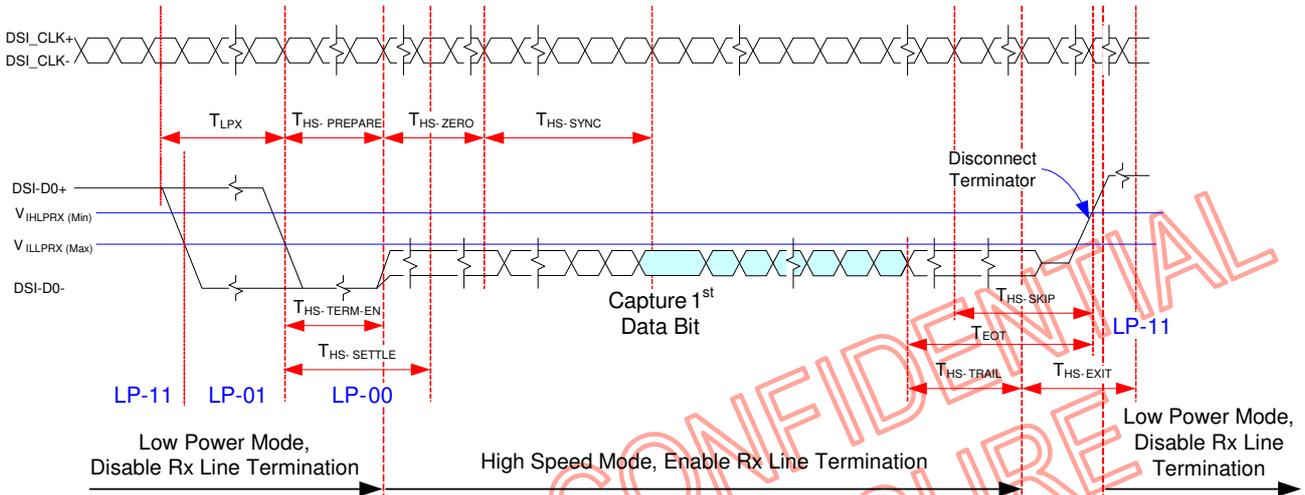


Fig. 7.7.10 Data lanes-Low Power Mode to/from High Speed Mode Timing

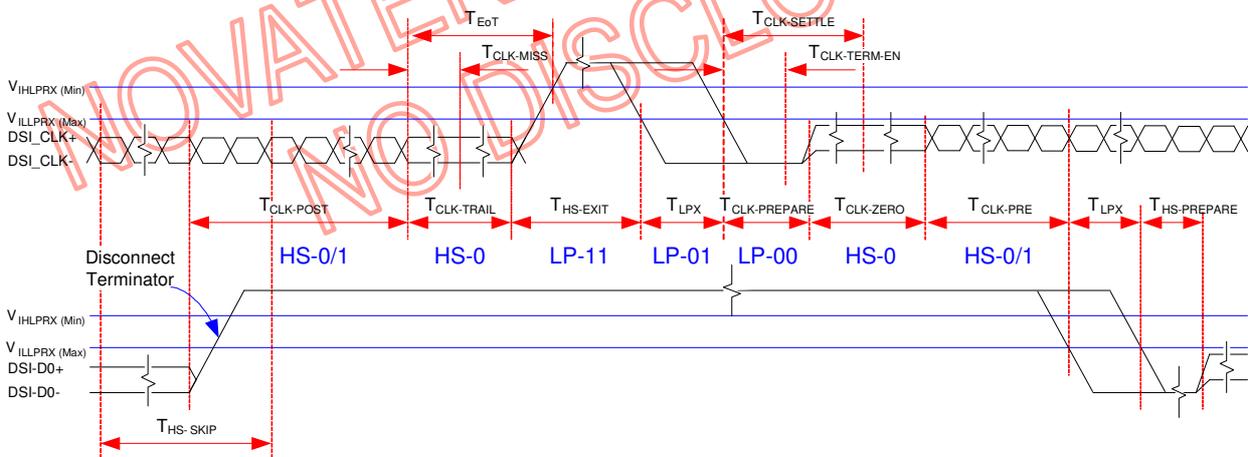
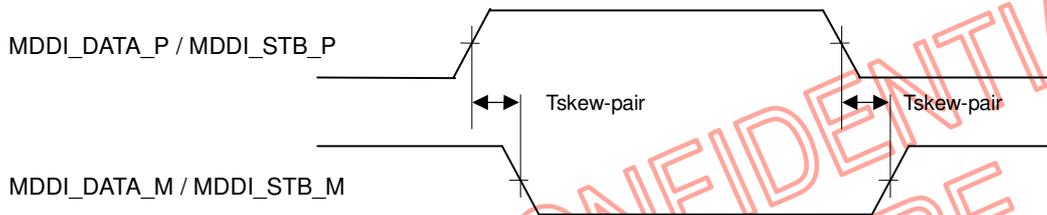
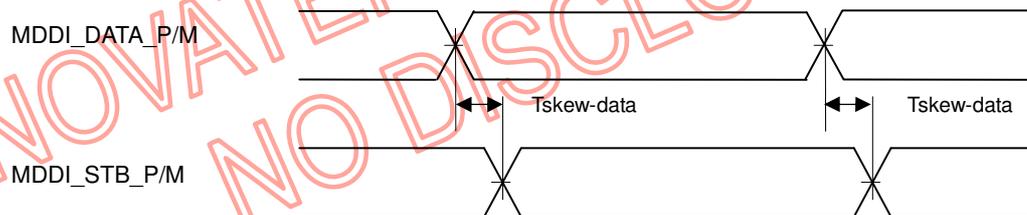


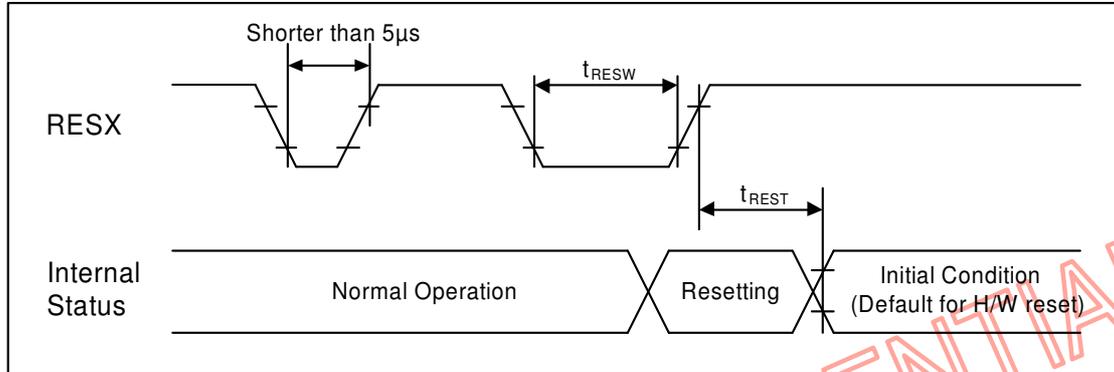
Fig. 7.7.11 Clock lanes- High Speed Mode to/from Low Power Mode Timing

7.7.6 MDDI Timing Characteristics

(VSS=0V, VDDI=1.65V to 4.8V, VPNL=2.3V to 4.8V, Ta = -30 to 70 °C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
MDDI_STB_P/M MDDI_DATA_P/M	1/Tbit	Data transfer rate	-	384	400	Mbps	
MDDI_STB_P/M MDDI_DATA_P/M	Tskew-pair	Differential transfer input skew	-	-	0.25	ns	
MDDI_STB_P/M MDDI_DATA_P/M	Tskew-data	Data/Strobe input skew	-	-	0.3	ns	


Fig. 7.7.12 Skew between MDDI positive and negative signal pair

Fig. 7.7.13 Skew between MDDI_DATA_P/M and MDDI_STB_P/M

7.7.7 Reset Input Timing

Fig. 7.7.14 Reset input timing

(VSS=0V, VDDI=1.65V to 4.8V, VPNL=2.3V to 4.8V, Ta = -30 to 70 °C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	t _{RESW}	Reset "L" pulse width (Note 1)	10	-	-	µs	
	t _{REST}	Reset complete time (Note 2)	-	-	60	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode

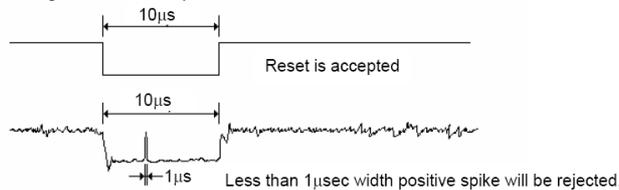
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5µs and 10µs	Reset Start

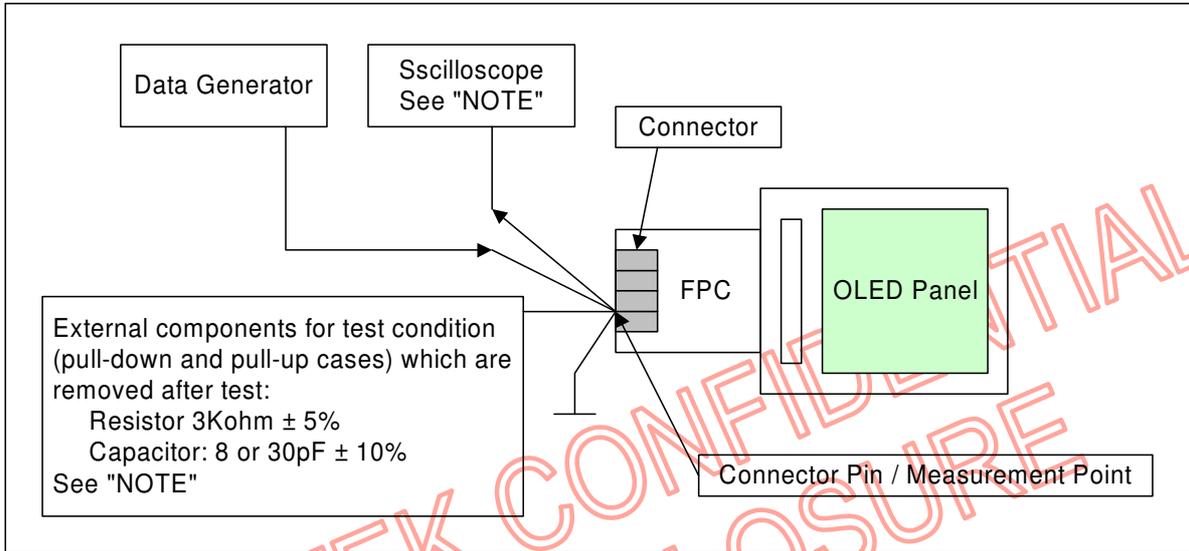
Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out-mode. The display remains the blank state in Sleep In-mode) and then return to Default condition for H/W reset.

 Note 3) During Reset Complete Time, value for Extended Instruction Code in flash memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

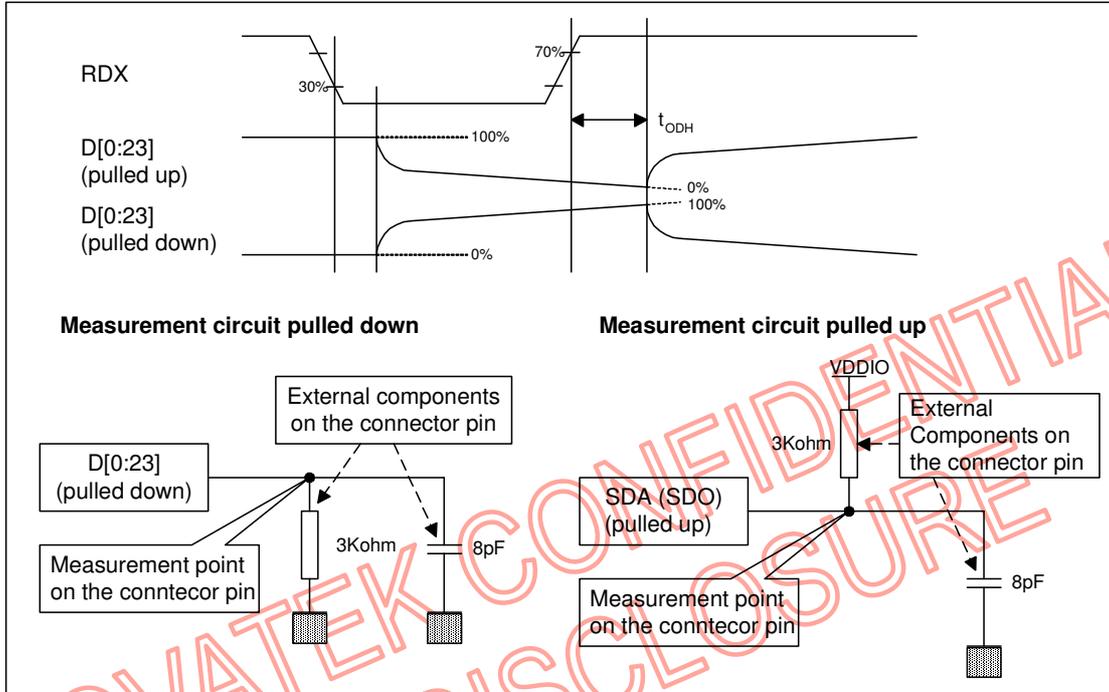
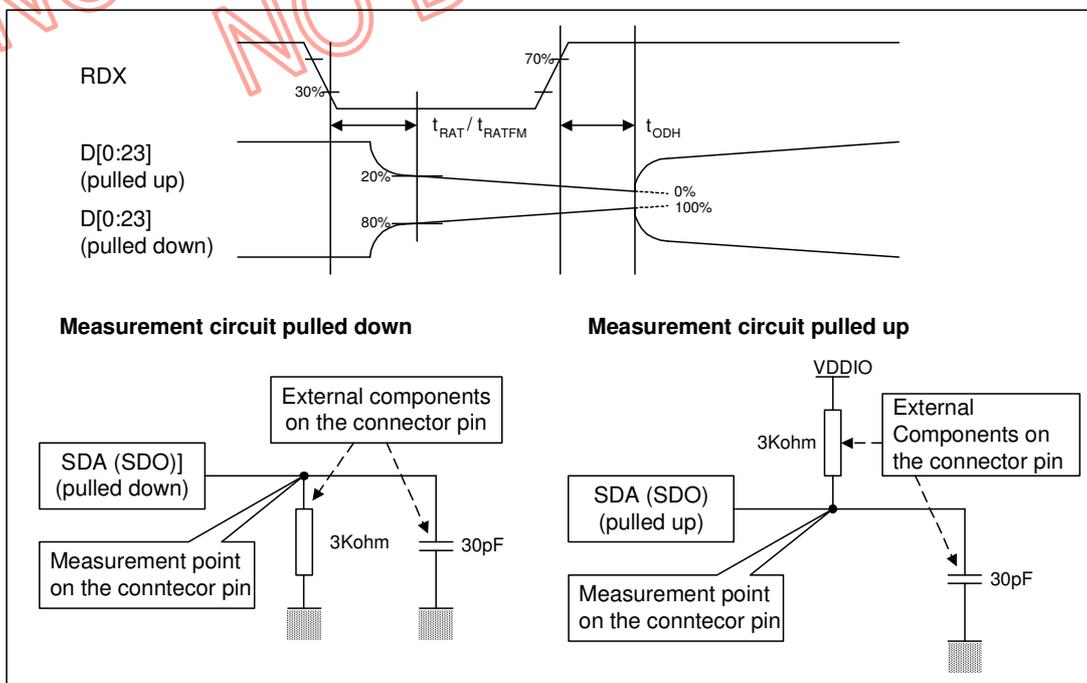
Note 4) Spike Rejection also applies during a valid reset pulse as shown below:

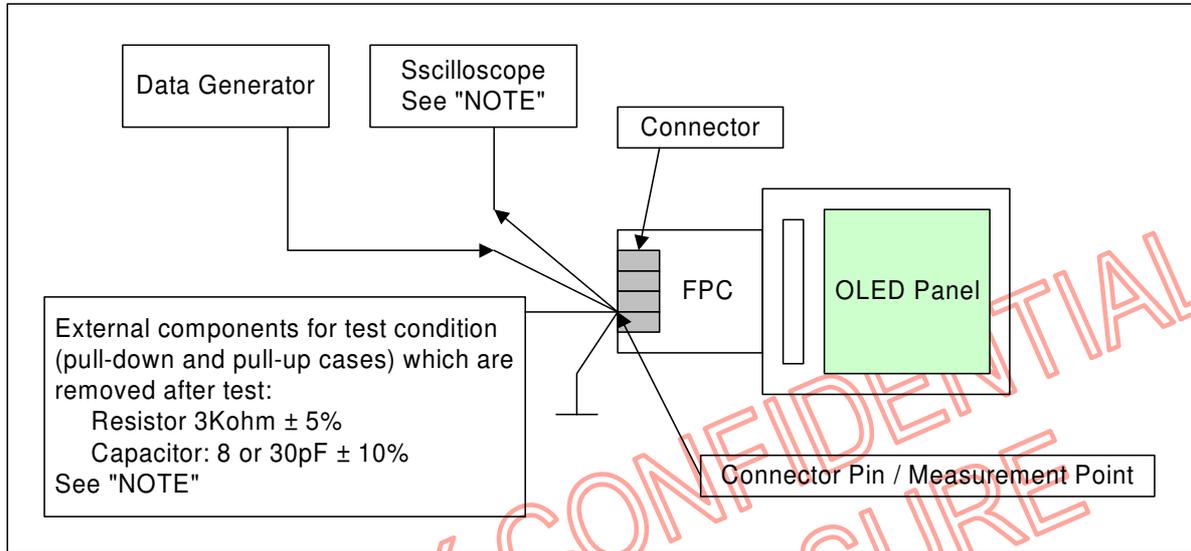


Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

7.7.8 Measurement Conditions
7.7.8.1 TRAT, TRATFM, TODH MEASUREMENT CONDITION
Measurement Condition Set-up

NOTE:

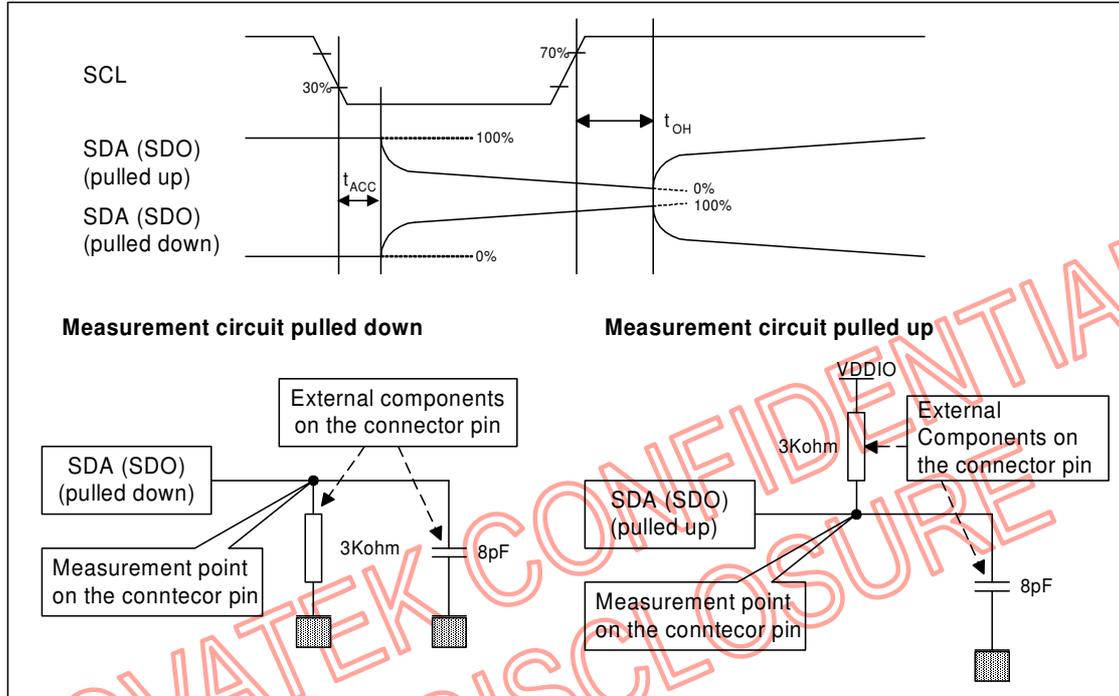
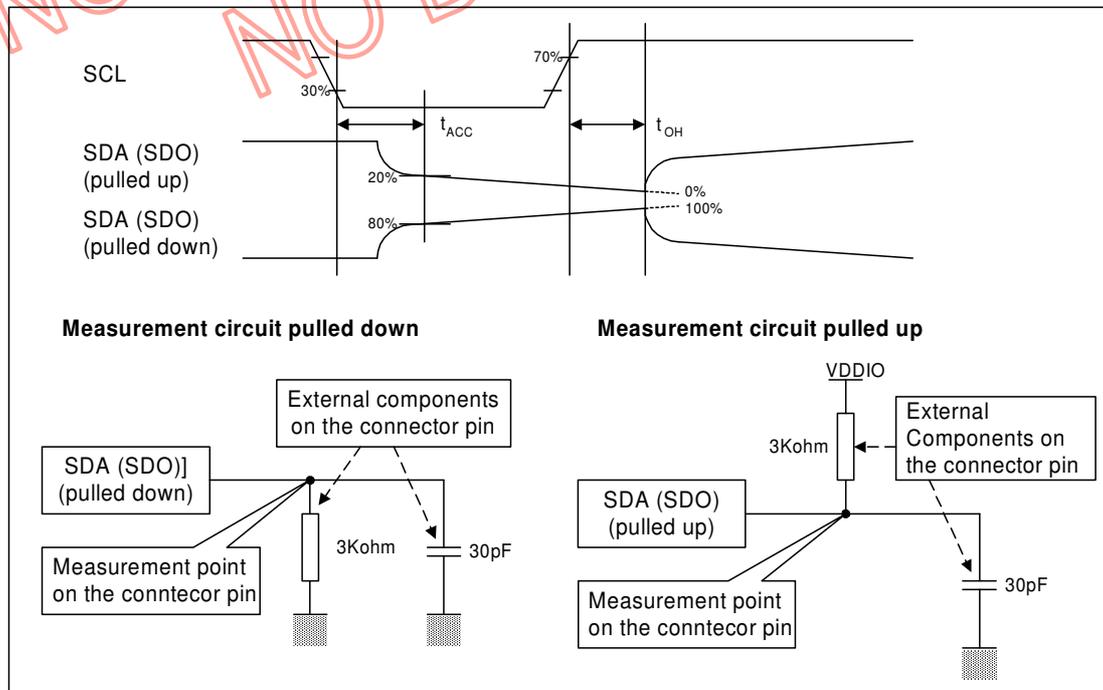
Capacitances and resistances of the oscilloscope probe must be included external components in these measurements.

Minimum Value Measurement

Maximum Value Measurement


**7.7.8.2 T_{ACC}, T_{OH} MEASUREMENT CONDITION
Measurement Condition Set-up**

NOTE:

Capacitances and resistances of the oscilloscope probe must be included external components in these measurements.

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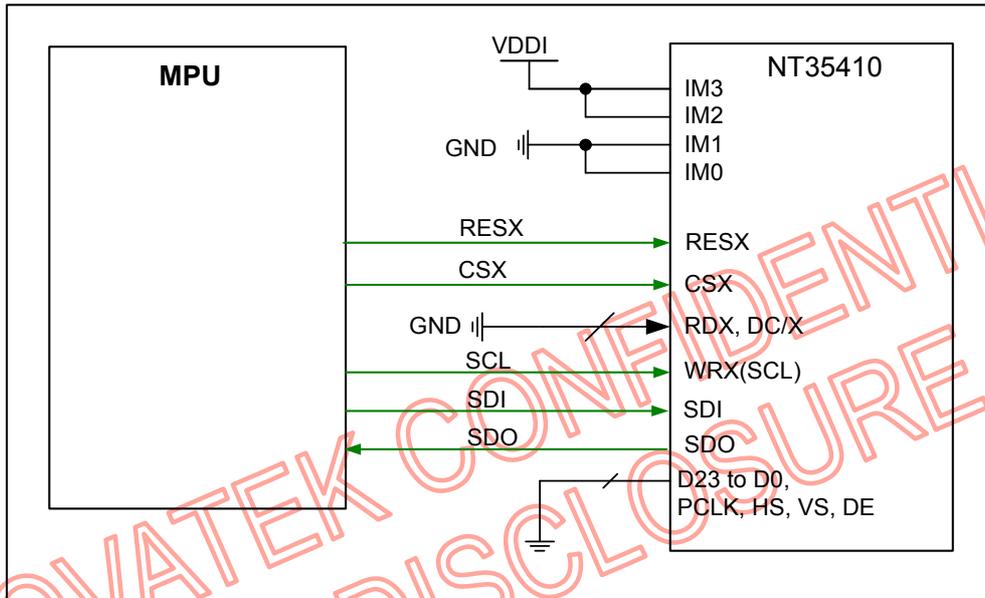
Minimum Value Measurement

Maximum Value Measurement


8 REFERENCE APPLICATIONS

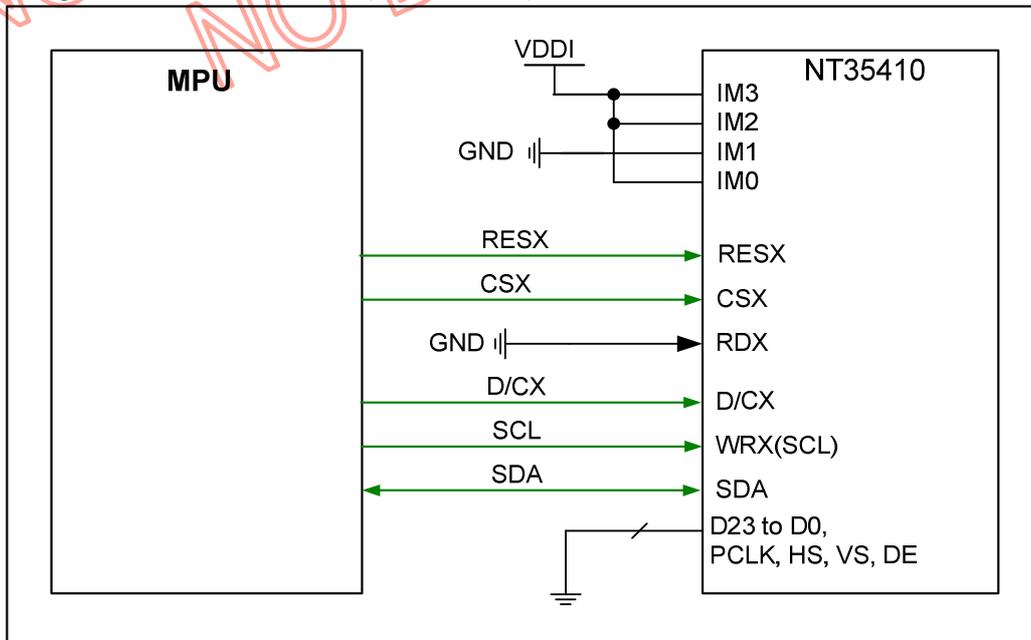
8.1 MICROPROCESSOR INTERFACE

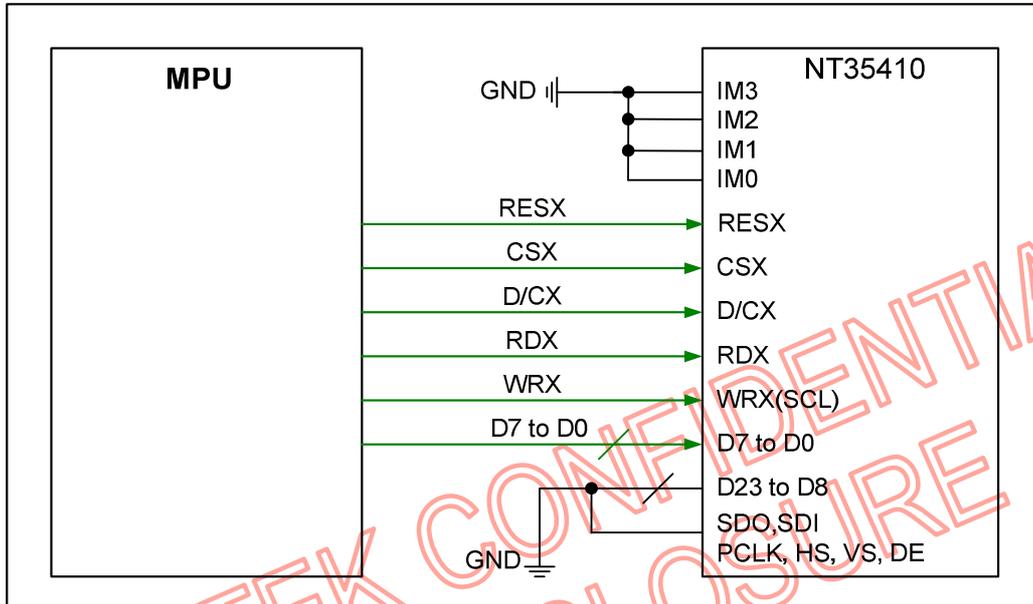
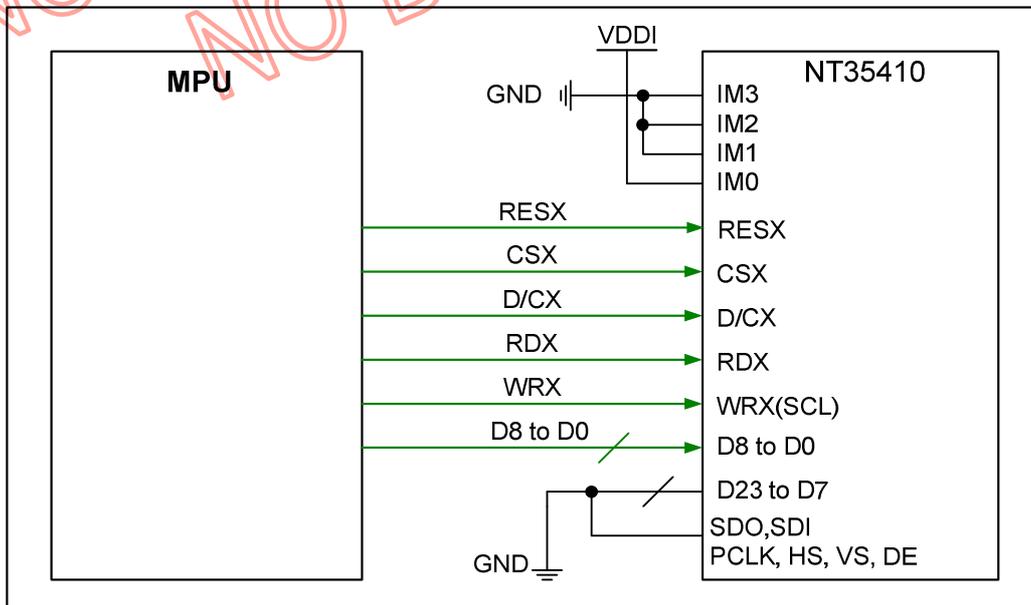
The display, which is using 80-series MPU interface, is connected to the MPU as it is illustrated below.

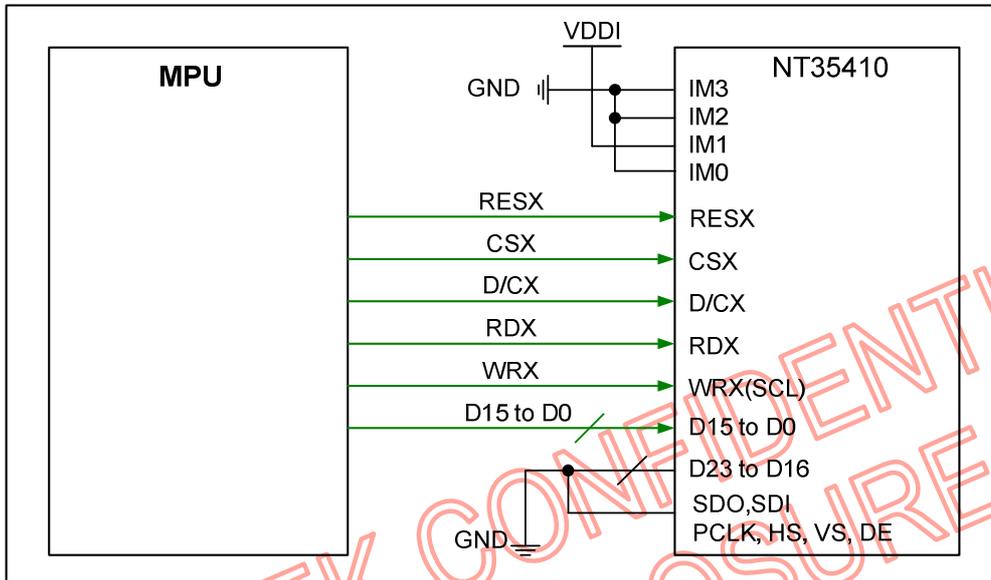
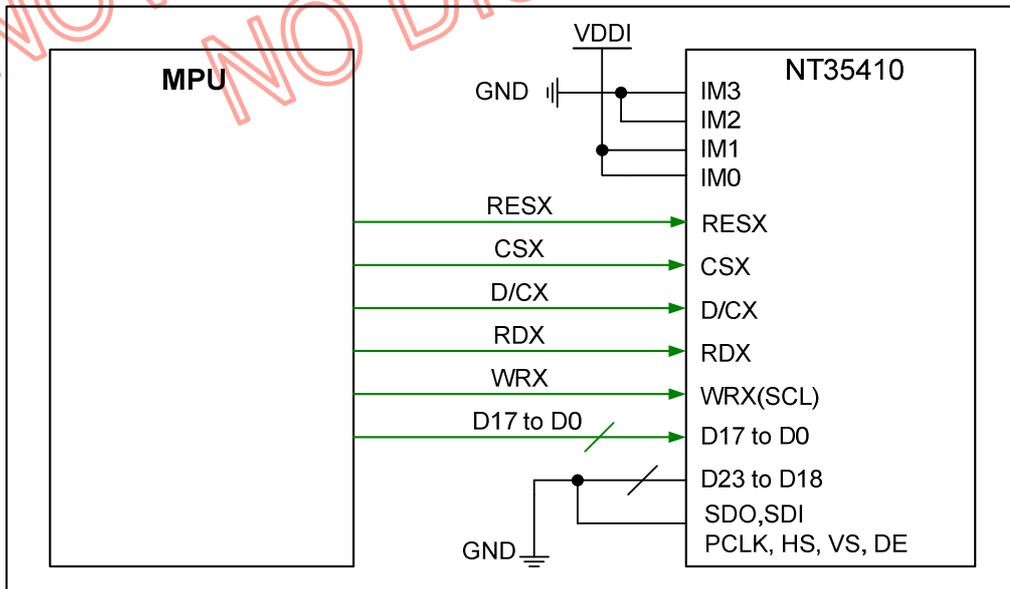
8.1.1 Interfacing with 3-Pin Serial Mode (IM3-0='1100')

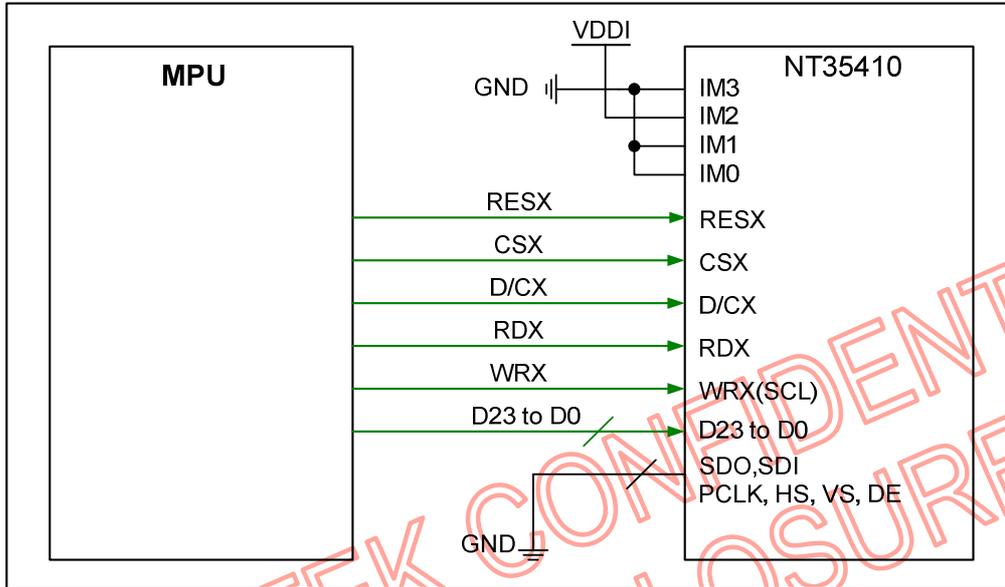


8.1.2 Interfacing with 4-Pin Serial Mode (IM3-0='1101')

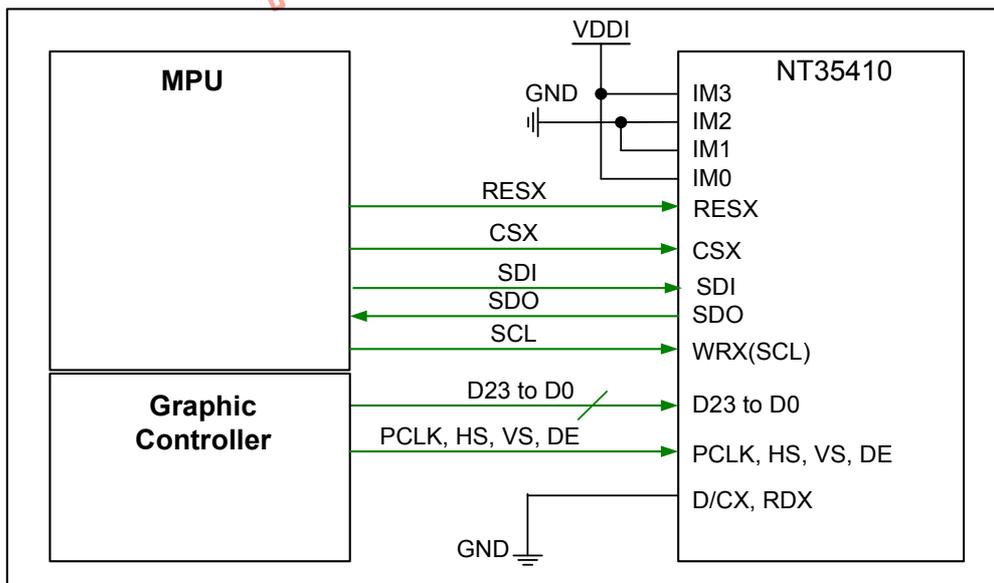


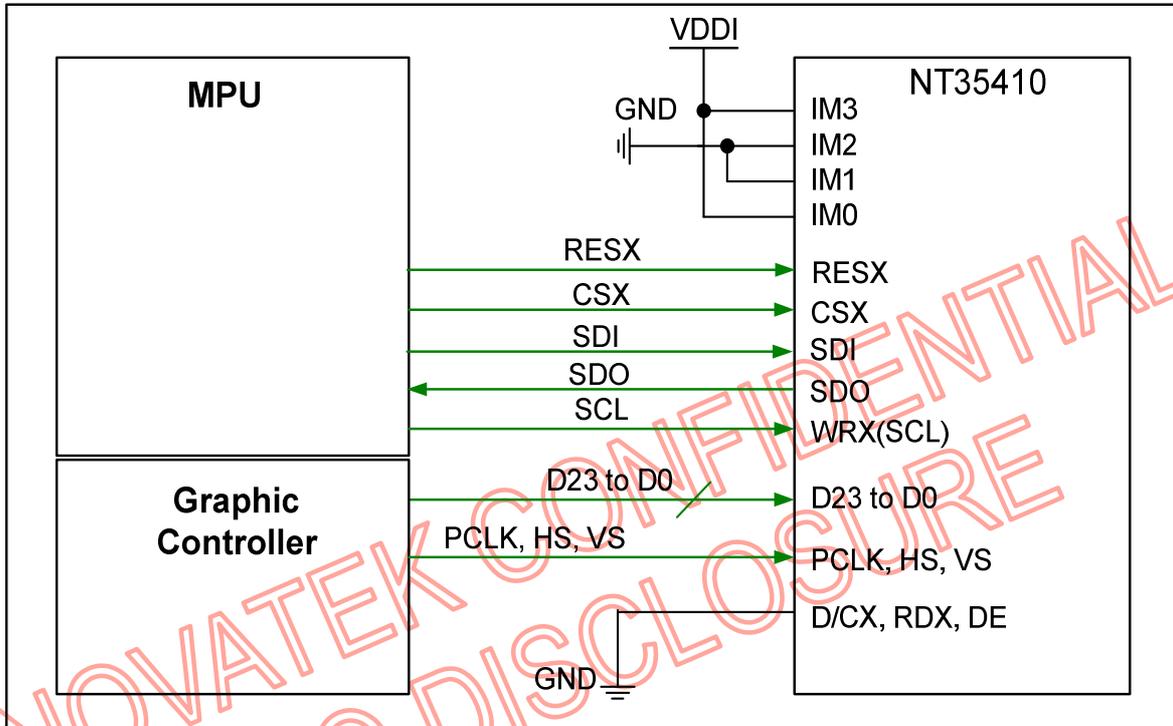
8.1.3 Interfacing with 8080- 8 bit Mode (IM3-0='0000')

8.1.4 Interfacing with 8080- 9 bit Mode (IM3-0='0001')


8.1.5 Interfacing with 8080- 16 bit Mode (IM3-0='0010')

8.1.6 Interfacing with 8080- 18 bit Mode (IM3-0='0011')


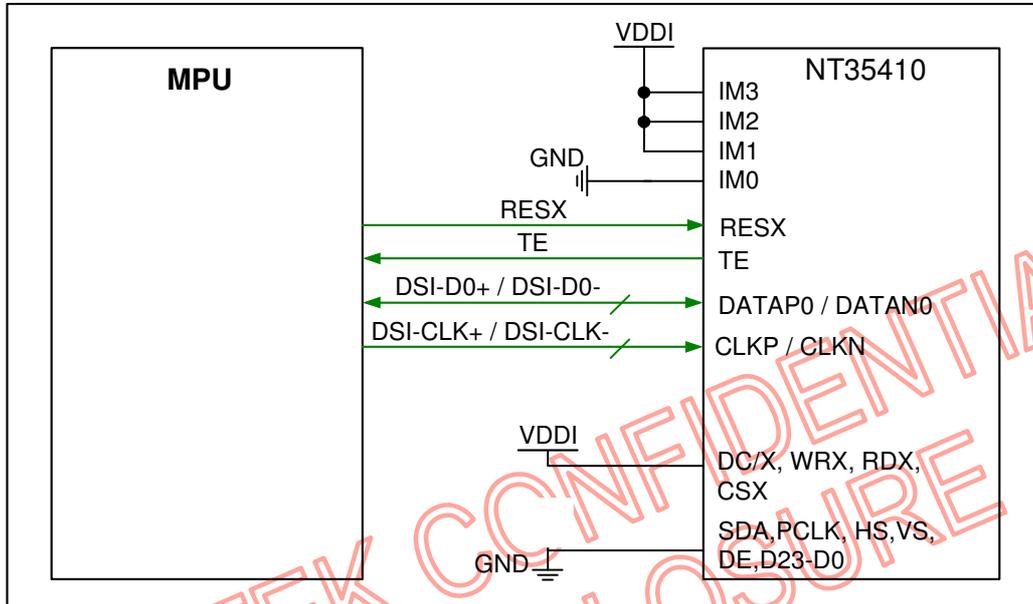
8.1.7 Interfacing with 8080- 24 bit Mode (IM3-0='0100')


Note: Connecting CLK_P/N and D0_P/D0_N to LVDSVSS and left LVDSVDD and VCCM12 open (not used) when using 80-series MPU interface.

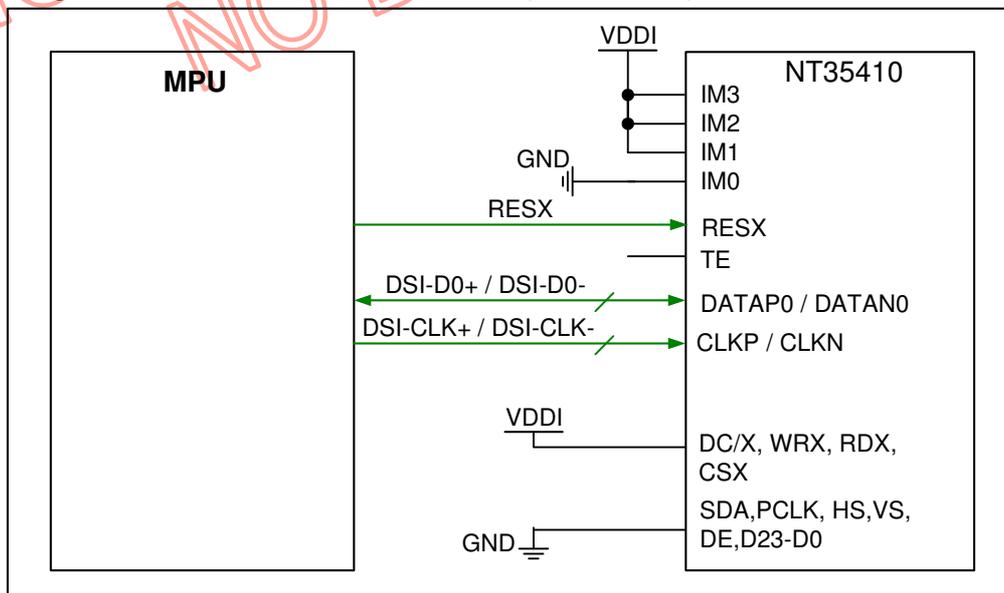
8.1.8 Interfacing with RGB Mode 1 with 3-SPI (IM3-0='1001')


8.1.9 Interfacing with RGB Mode 2 with 3-SPI (IM3-0='1001')

Notes:

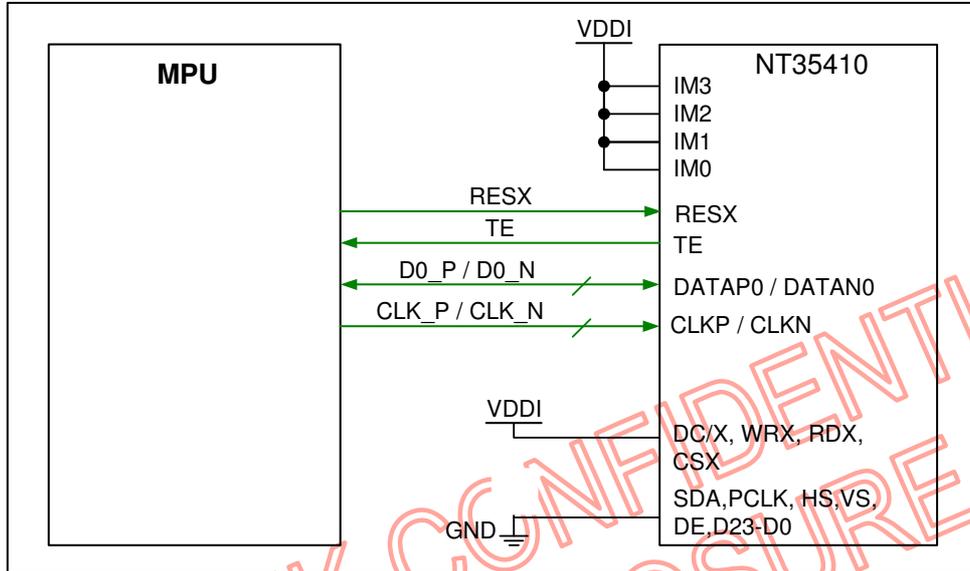
1. Connecting D23, D22, D15, D14, D7 and D6 to VSS when using 18-bit/pixel (VIPF[3:0]="0110").
Connecting D23, D22, D16, D15, D14, D7, D6 and D0 to VSS when using 16-bit/pixel (VIPF[3:0]="0101").
2. Connecting CLK_P/CLK_N and D0_P/D0_N to LVDSVSS and left MVDDI and LVDSVDD open (not used) when using RGB with SPI interface.

8.1.10 Interfacing with MIPI DSI Mode with TE Line (IM3-0='1110')


Note: Bit DSITE should be "1", the TE line is enabled, when using this application.

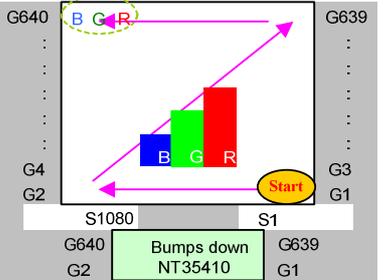
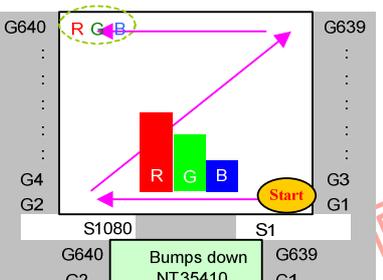
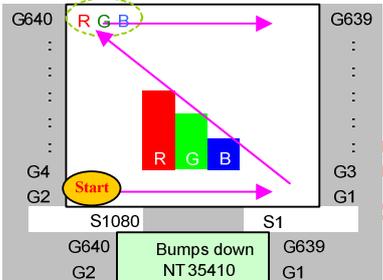
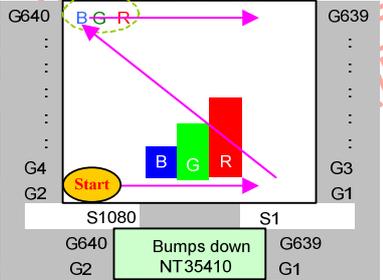
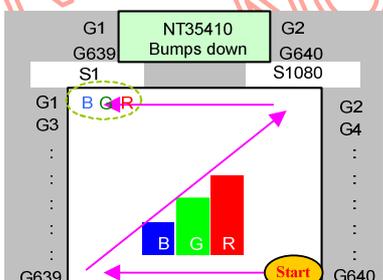
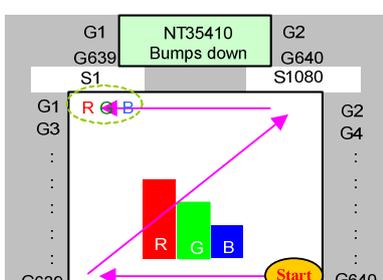
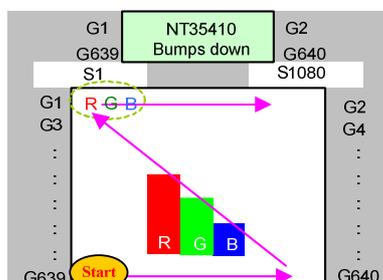
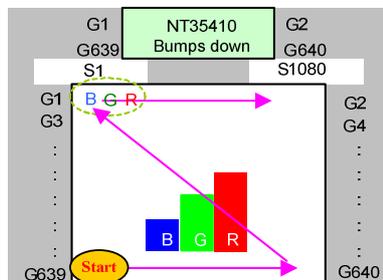
8.1.11 Interfacing with MIPI DSI Mode without TE Line (IM3-0='1110')


Note: Bit DSITE should be "0", the TE line is disabled, when using this application. The command 35h TEON cannot active the separated TE line.

8.1.12 Interfacing with MDDI Mode with TE Line (IM3-0='1111')


Note: If 3SPI is no need to use, please connect DC/X, WRX, RDX, CSX to VDDI

8.2 CONNECTIONS WITH LCD PANEL

RGB filter order=RGB(from left top of the panel)	RGB filter order=BGR(from left top of the panel)
<p>CASE1</p>  <p>SMX=0 SMY=0 SRGB=0</p> <p>S1 = Filter R S2 = Filter G S3 = Filter B</p> <p>...</p>	<p>CASE 2</p>  <p>SMX=0 SMY=0 SRGB=1</p> <p>S1 = Filter B S2 = Filter G S3 = Filter R</p> <p>...</p>
<p>CASE3</p>  <p>SMX=1 SMY=0 SRGB=0</p> <p>S1 = Filter B S2 = Filter G S3 = Filter R</p> <p>...</p>	<p>CASE4</p>  <p>SMX=1 SMY=0 SRGB=1</p> <p>S1 = Filter R S2 = Filter G S3 = Filter B</p> <p>...</p>
<p>CASE 5</p>  <p>SMX=1 SMY=1 SRGB=0</p> <p>S1 = Filter B S2 = Filter G S3 = Filter R</p> <p>...</p>	<p>CASE 6</p>  <p>SMX=1 SMY=1 SRGB=1</p> <p>S1 = Filter R S2 = Filter G S3 = Filter B</p> <p>...</p>
<p>CASE 7</p>  <p>SMX=0 SMY=1 SRGB=0</p> <p>S1 = Filter R S2 = Filter G S3 = Filter B</p> <p>...</p>	<p>CASE 8</p>  <p>SMX=0 SMY=1 SRGB=1</p> <p>S1 = Filter B S2 = Filter G S3 = Filter R</p> <p>...</p>

8.3 EXTERNAL COMPONENTS CONNECTION

Pad Name	Connection	Typical Capacitance Value
VDDI	I/O Pad Power input, Connected to capacitor (Max. 6V): VDDI ---- ---- GND	1.0uF, Optional
VPNL	Analog Power input, Connected to capacitor (Max. 6V): VPNL ---- ---- GND	1.0uF, Optional
VREF	Reference power used, Connected to capacitor (Max. 6V): Vref ---- ---- GND	1.0uF,
VCC	Internal Logical used, Connected to capacitor (Max. 6V): VCC ---- ---- GND	1.0uF, Necessary
NVDDI	Internal Logical used, Connected to capacitor (Max. 6V): NVDDI ---- ---- GND	1.0uF, Necessary
AVSS	Analog ground (Connected to GND)	
VSSR	Regulator ground (Connected to GND)	
LVDSVSS	MIPI ground (Connected to GND)	
CVSS	Booster ground (Connected to GND)	
VSS	Digital ground (Connected to GND)	
LVDSVDD	For MIPI, Connected to capacitor (Max. 6V): LVDSVDD ---- ---- GND If MIPI is not used, this capacitor is not necessary	1.0uF, For MIPI / MDDI Only
VCCM12	For MIPI, Connected to capacitor (Max. 6V): VCCM12 ---- ---- GND If MIPI is not used, this capacitor is not necessary	1.0uF, For MIPI Only
C41P, C41N	Connected to capacitor (Max. 16V): C41P ---- ---- C41N	1.0uF, Necessary
C51P, C51N	Connected to capacitor (Max. 16V): C51P ---- ---- C51N	1.0uF, Necessary
C31P, C31N	Connected to capacitor (Max. 10V): C31P ---- ---- C31N	1.0uF, Necessary
C21P, C21N	Connected to capacitor (Max. 10V): C21P ---- ---- C21N	1.0uF, Necessary
C22P, C22N	Connected to capacitor (Max. 10V): C22P ---- ---- C22N	1.0uF, Necessary
C23P, C23N	Connected to capacitor (Max. 16V): C23P ---- ---- C23N	1.0uF, Necessary
C11P, C11N	Connected to capacitor (Max. 6V): C11P ---- ---- C11N	1.0uF, Necessary
C12P, C12N	Connected to capacitor (Max. 10V): C12P ---- ---- C12N	1.0uF, Necessary
C13P, C13N	Connected to capacitor (Max. 10V): C13P ---- ---- C13N	1.0uF, Necessary
PAVDD	Connected to capacitor (Max. 10V): PAVDD ---- ---- GND	2.2uF, Necessary
NAVDD	Connected to capacitor (Max. 10V): NAVDD ---- ---- GND	2.2uF, Necessary
VGH	Connected to capacitor (Max. 25V): VGH ---- ---- GND	2.2uF, Necessary
VGL/VGLO	Connected to capacitor (Max. 25V): VGL ---- ---- GND	2.2uF, Necessary
DIOPWR	Connected to capacitor (Max. 6V): DIOPWR ---- ---- GND	1.0uF, Necessary
VCOM	Connected to capacitor (Max. 6V): VCOM ---- ---- GND	2.2uF, Necessary
VCL	Connected to capacitor (Max. 6V): VCL ---- ---- GND	2.2uF, Necessary
VGL	Connected to schottky diode: VGL ----▶ ---- GND VF<0.42V (@IF=100mA), VR≥30V	Schottky diode, Optional

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