8280-A,F,W • 8281-A,F,W

DESCRIPTION

The 8280 Decade Counter and 8281 16-State Binary Counter are four-bit subsystems providing a wide variety of counter/storage register applications with a minimum number of packages.

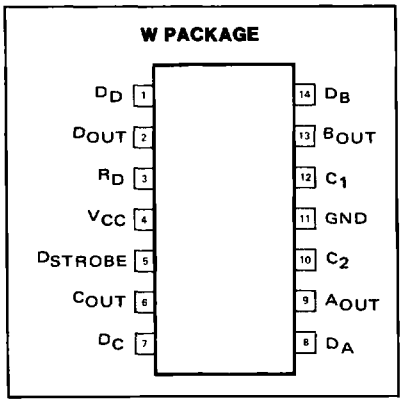
The 8280 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

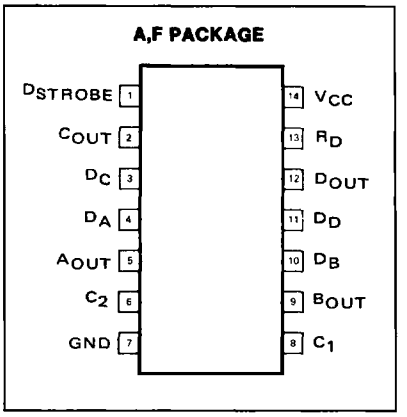
The 8281 Binary Counter may be connected as a divide-by-two, eight, or sixteen counter.

Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. For additional flexibility, both units are provided with a reset input which is common to all four bits. A "0" on the reset line produces "0" at all four outputs.

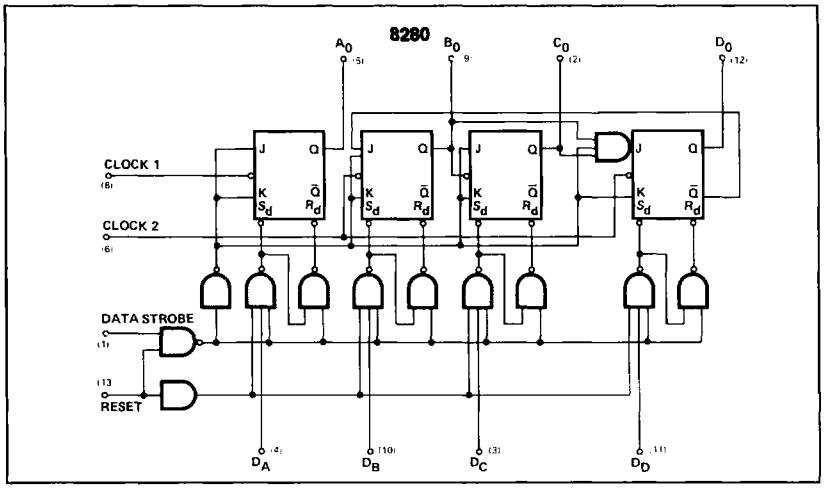
The counting operation is performed on the falling (negative-going) edge of the input clock pulse, however there is no restriction on the transition time since the individual binaries are level-sensitive.

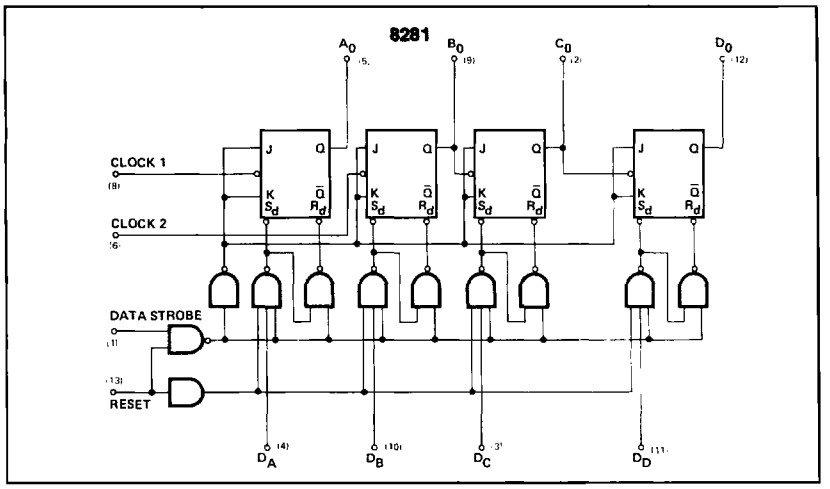
PIN CONFIGURATION





LOGIC DIAGRAMS





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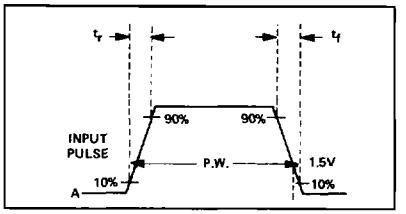
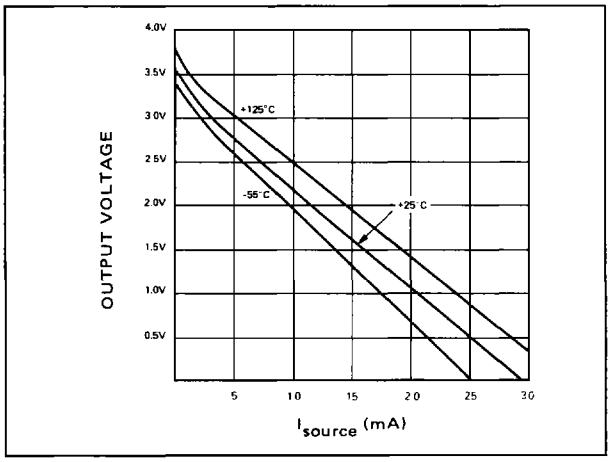
SWITCHING CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$

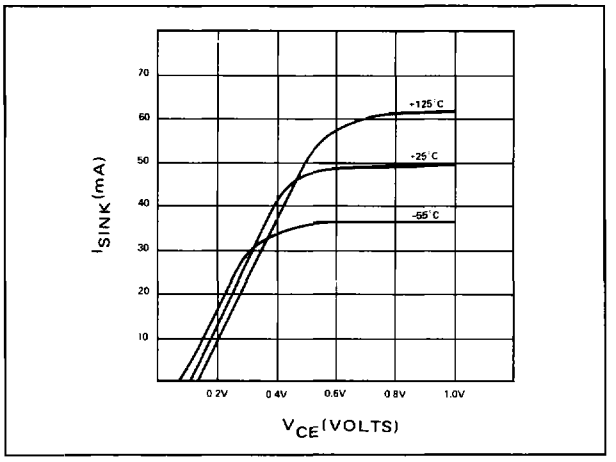
PARAMETER		TEST CONDITIONS	LIMITS 8280/8281 MIN	TYP	MAX	UNIT
t_{on}	Turn-on delay time					
	Clock mode	Bit A,B,C,D		15	25	ns
	Data/strobe			25	35	
t_{off}	Turn-off delay time					
	Clock mode	Bit A,B,C,D,		15	25	ns
	Data strobe			30	40	
Toggle rate			20	25		MHz
t_w	Width of input pulse					
	$\overline{\text{Strobe}}$			20	35	ns
	$\overline{\text{Reset}}$			20	35	
$t_{release}$	Release time					
	$\overline{\text{Strobe}}$			30	40	ns
	$\overline{\text{Reset}}$			50	75	

AC WAVEFORM



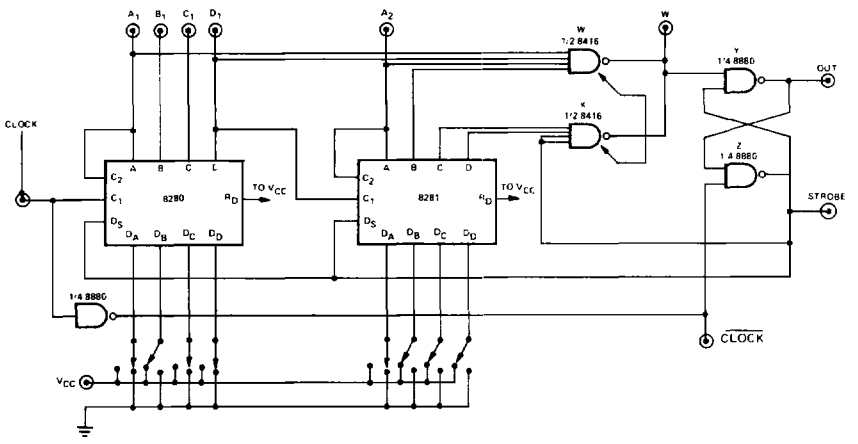
TYPICAL OUTPUT CHARACTERISTICS





TYPICAL APPLICATIONS

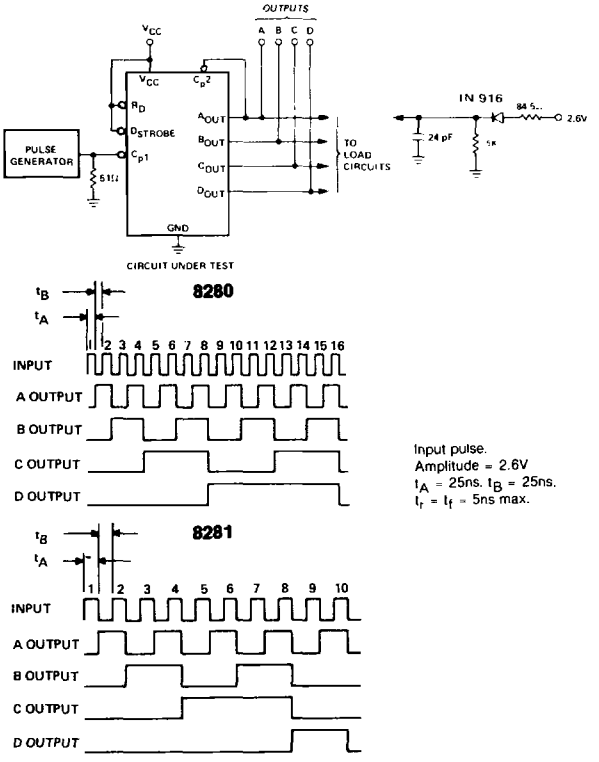
VARIABLE MODULUS COUNTER



LOGIC

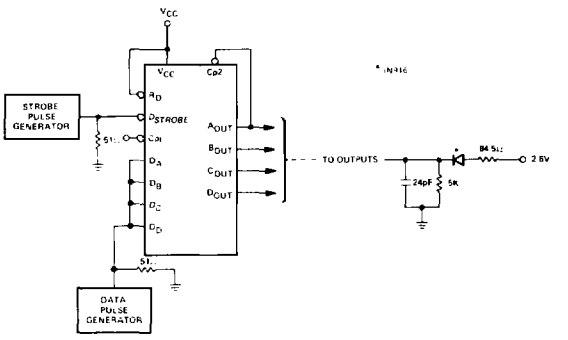
AC TEST FIGURES AND WAVEFORMS

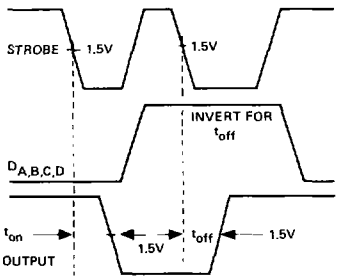
TOGGLE RATE



Input pulse.
Amplitude = 2.6V
t_A = 25ns. t_B = 25ns.
$t_r = t_f$ = 5ns max.

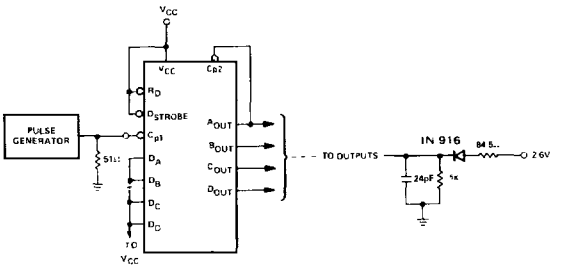
DATA/STROBE t_{on}/t_{off}

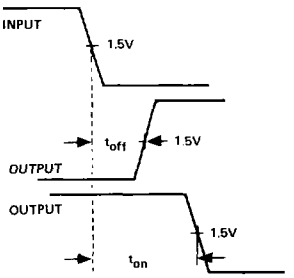




Strobe. P.A. = 2.6V
P.W. = 300ns
PRR = 1 MHz
$t_r = t_f$ = 5ns
Data. P.A. = 2.6V
P.W. = 500ns
PRR = 500 KHz
$t_r = t_f$ = 5ns.

CLOCK MODE t_{on}/t_{off} DELAY

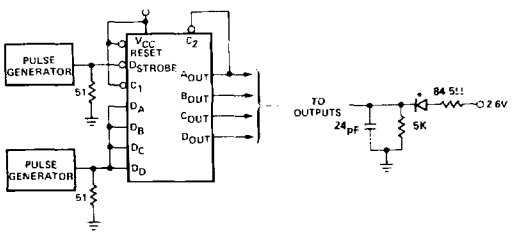


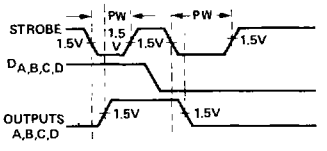


Input pulse:
Amplitude = 2.6V
P.W. = 30ns
$t_r = t_f$ = 5ns.

1. t_{on} and t_{off} are measured from the clock input of each binary to the Q output of that binary.
2. Each Q output will be loaded with a load circuit as shown

MINIMUM STROBE PULSE WIDTH

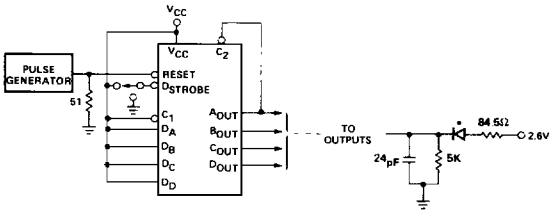


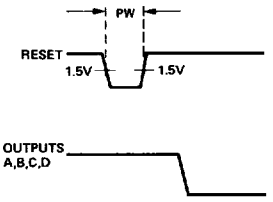


INPUT PULSE:
Amplitude = 2.6V
$t_r = t_f$ = 5ns.

AC TEST FIGURES AND WAVEFORMS

MINIMUM RESET PULSE WIDTH

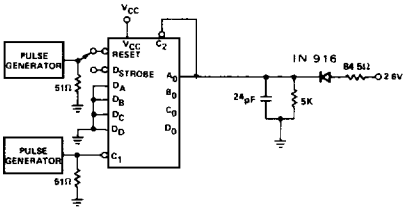


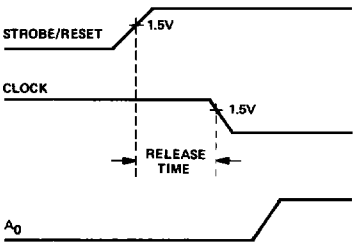


INPUT PULSE:
Amplitude = 2.6V
$t_r = t_f$ = 5ns max.

Note: Outputs must be previously brought high by placing a "0" on the D strobe input. A pulse generator may be substituted for the switch.

STROBE/RESET RELEASE TIME

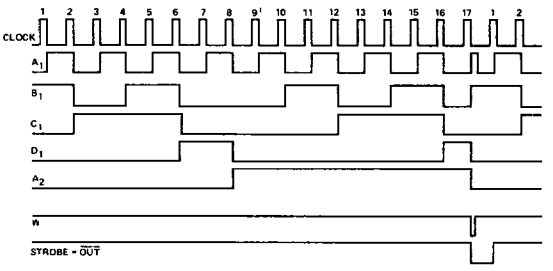




Clock, Strobe/Reset:
Ampl = 2.6V
tr = tf = 5ns max.
PRR = 1 MHz 50% Duty Cycle.

NOTES:
1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance.
3. Input pulse notations apply unless otherwise specified.

TIMING DIAGRAM



LOGIC