Siliconix

SMP25N05-45L

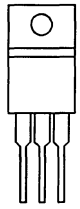
N-Channel Enhancement-Mode Transistor, Logic Level

175°C Maximum Junction Temperature

Product Summary

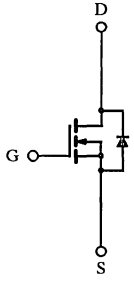
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
50	0.045 @ V_{GS} = 10 V	25
	0.060 @ V_{GS} = 4.25 V	25

TO-220AB



Drain Connected to Tab

Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Gate-Source Voltage		V_{GS}	16	V
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	25	A
	T_C = 100°C		±16	
Pulsed Drain Current		I_{DM}	100	
Avalanche Current (see Thermal Ratings, page 6-104)		I_{AR}	25	
Repetitive Avalanche Energy[a]	L = 0.05 mH	E_{AR}	31	mJ
Maximum Power Dissipation	T_C = 25°C	P_D	70	W
	T_C = 100°C		36	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient	R_{thJA}		80	°C/W
Maximum Junction-to-Case	R_{thJC}		2.08	
Case-to-Sink	R_{thCS}	1.0		

Notes:
a. Duty cycle ≤ 1%

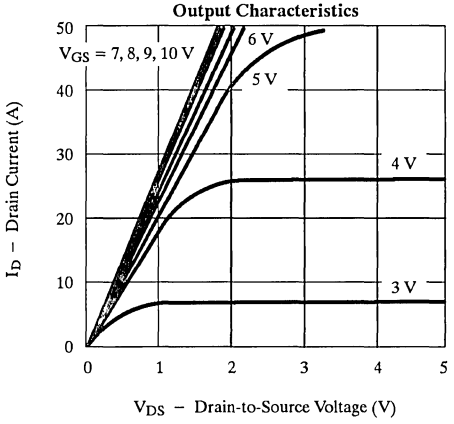
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ[a]	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	50			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.0	1.5	3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±16 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V			2	µA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 125°C			100	
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 175°C			500	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 2 V, V_{GS} = 10 V	25			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 12.5 A		0.035	0.045	Ω
		V_{GS} = 10 V, I_D = 12.5 A, T_J = 125°C		0.060	0.080	
		V_{GS} = 10 V, I_D = 12.5 A, T_J = 175°C		0.062	0.085	
		V_{GS} = 4.25 V, I_D = 12.5 A		0.045	0.060	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 12.5 A		19		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		950		pF
Output Capacitance	C_{oss}			320		
Reverse Transfer Capacitance	C_{rss}			110		
Total Gate Charge[c]	Q_g	V_{DS} = 25 V, V_{GS} = 10 V, I_D = 25 A		22		nC
Gate-Source Charge[c]	Q_{gs}			5		
Gate-Drain Charge[c]	Q_{gd}			10		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 25 V, R_L = 1 Ω I_D ≅ 25 A, V_{GEN} = 10 V, R_G = 7.5 Ω		10	20	ns
Rise Time[c]	t_r			25	40	
Turn-Off Delay Time[c]	$t_{d(off)}$			35	60	
Fall Time[c]	t_f			20	40	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				25	A
Pulsed Current	I_{SM}				100	
Diode Forward Voltage[b]	V_{SD}	I_F = 25 A, V_{GS} = 0 V		1.0	1.8	V
Reverse Recovery Time	t_{rr}	I_F = 25 A, di/dt = 100 A/µs		120		ns
Peak Reverse Recovery Current	$I_{RM(rec)}$					A
Reverse Recovery Charge	Q_{rr}			0.42		µC

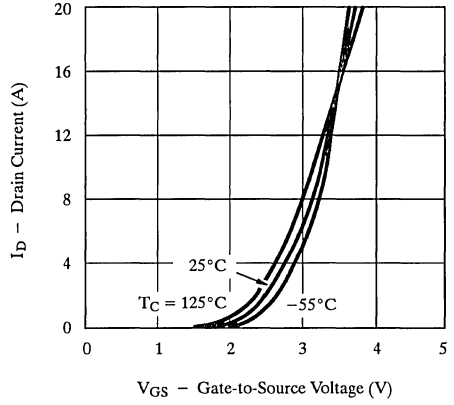
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

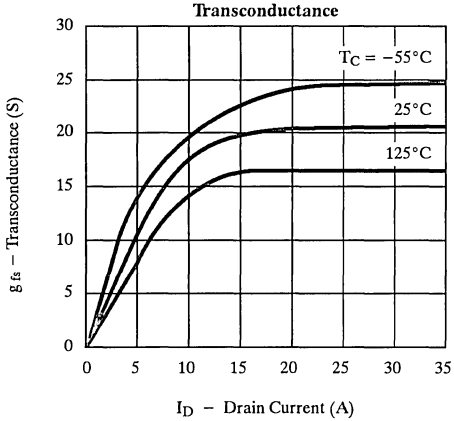
Output Characteristics



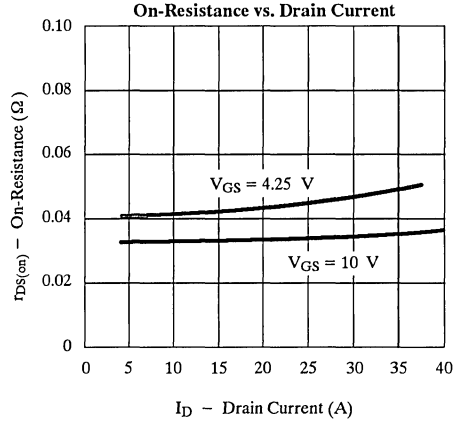
Transfer Characteristics



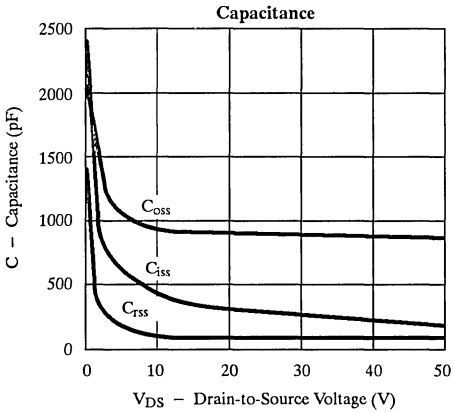
Transconductance



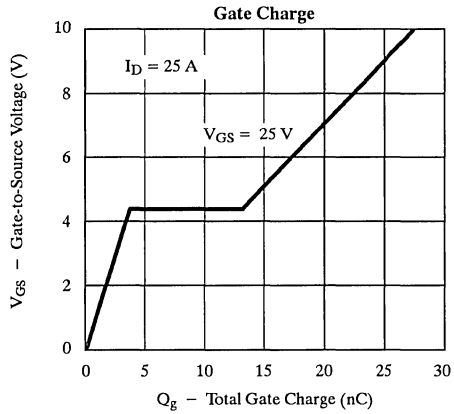
On-Resistance vs. Drain Current



Capacitance



Gate Charge



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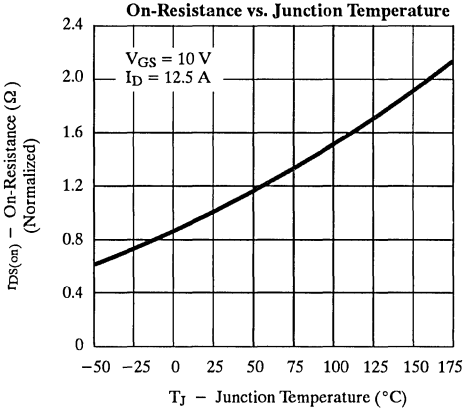

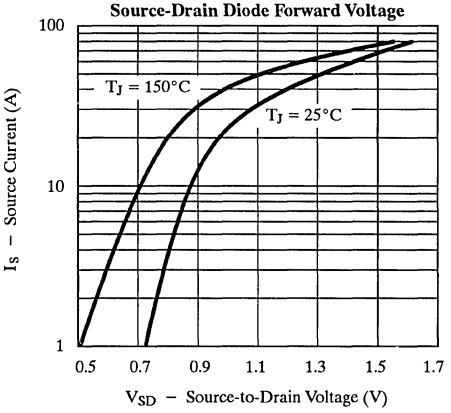

Thermal Ratings