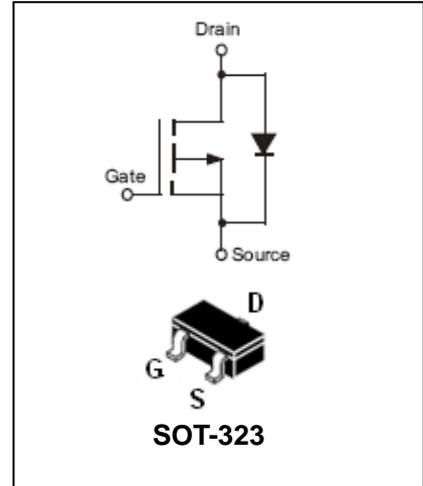


P-Channel Enhancement Mode Field Effect Transistor

FEATURES

- Low On-Resistance.
- Low Gate Threshold Voltage.
- Low Input Capacitance.
- Fast Switching Speed.
- Available in Lead Free Version.



APPLICATIONS

- P-channel enhancement mode effect transistor.

ORDERING INFORMATION

Type No.	Marking	Package Code
ÓÙÙÌ I SÜ	K84	SOT-323

MAXIMUM RATING @ Ta=25°C unless otherwise specified

Symbol	Parameter	Value	Units
V _{DSS}	Drain-Source voltage	-50	V
V _{DGR}	Drain-Gate voltage	-50	V
V _{GSS}	Gate -Source voltage	continuous ± 20	V
I _D	Drain current (Note1)	continuous -130	mA
P _D	Power Dissipation (Note1)	200	mW
R _{θJA}	Thermal resistance, Junction-to-Ambient	625	°C/W
T _J , T _{stg}	Junction and Storage Temperature	-55 to +150	°C

Note: 1. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch; pad layout as shown on GALAXY Inc. suggested pad layout document AP02001.

P-Channel Enhancement Mode Field Effect Transistor

ELECTRICAL CHARACTERISTICS @ Ta=25°C unless otherwise specified

Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-50	-75	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-1mA$	-0.8	-1.6	-2.0	
Gate-body Leakage Forward Reverse	I_{GSS}	$V_{DS}=0V, V_{GS}=20V$ $V_{DS}=0V, V_{GS}=-20V$	- -	- -	100 -100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-50V, V_{GS}=0V, T_J = 25^\circ C$	-	-	-15	μA
		$V_{DS}=-50V, V_{GS}=0V, T_J = 125^\circ C$			-60	
		$V_{DS}=-25V, V_{GS}=0V, T_J = 25^\circ C$	-	-	-100	
Forward transconductance	g_{FS}	$V_{DS}=-25V, I_D=100mA$	50	-	-	mS
Static drain-Source on-resistance	$R_{DS(ON)}$	$V_{GS}=-5.0V, I_D=100mA$	-	6	10	Ω
Input capacitance	C_{ISS}	$V_{DS}=-25V, V_{GS}=0V, f=1.0MHz$	-	-	45	μF
Output capacitance	C_{OSS}		-	-	25	
Reverse transfer capacitance	C_{RSS}		-	-	12	
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD} = -30V, I_D = -0.27A,$ $V_{GS} = -10V, R_{GEN} = 50\Omega$	-	10	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$		-	18	-	ns

P-Channel Enhancement Mode Field Effect Transistor

TYPICAL CHARACTERISTICS @ $T_a=25^\circ\text{C}$ unless otherwise specified

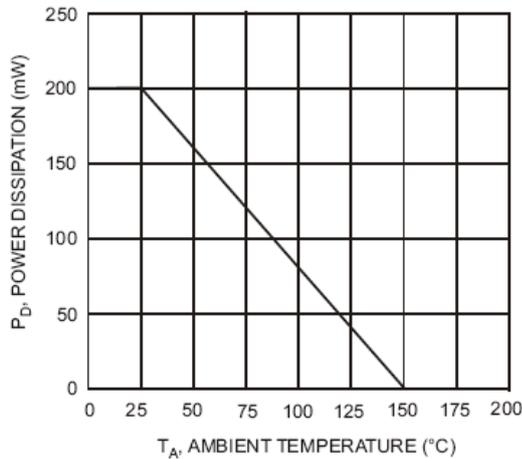


Fig. 1, Max Power Dissipation vs Ambient Temperature

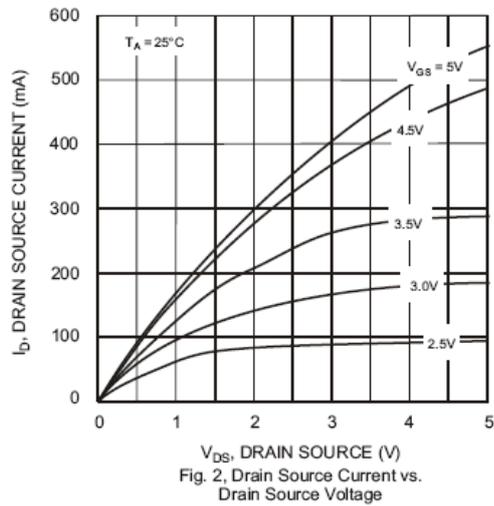


Fig. 2, Drain Source Current vs. Drain Source Voltage

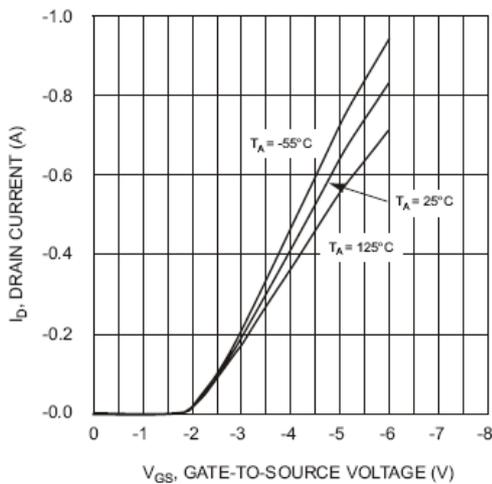


Fig. 3, Drain Current vs. Gate Source Voltage

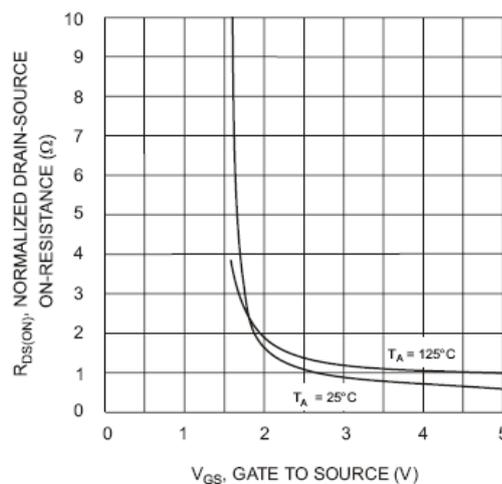


Fig. 4, On Resistance vs. Gate Source Voltage

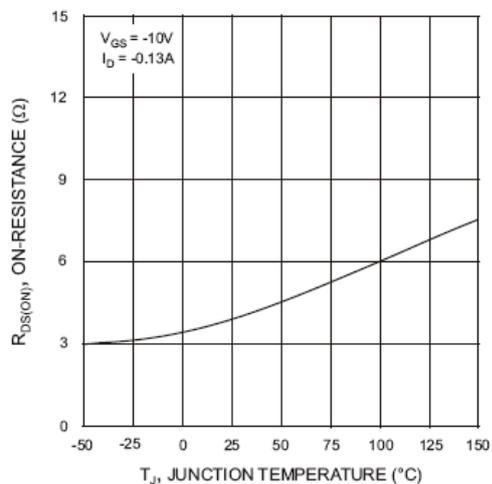


Fig. 5, On-Resistance vs. Junction Temperature

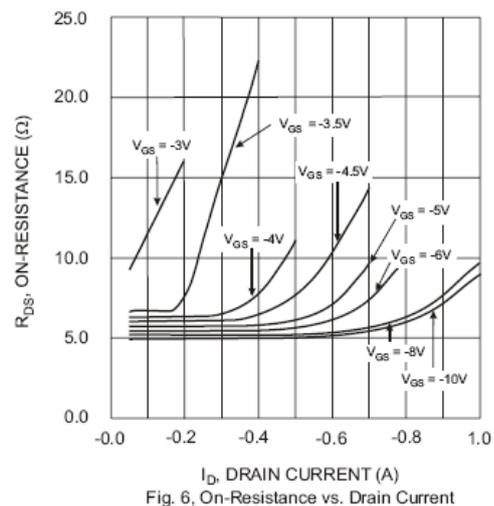


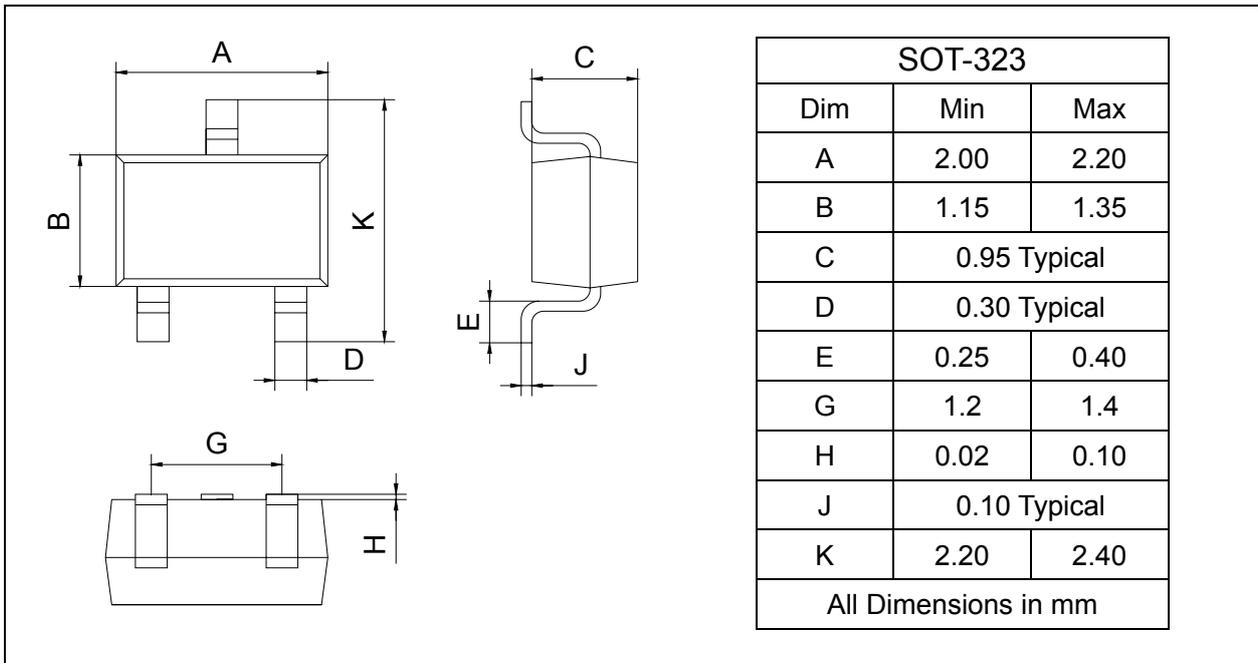
Fig. 6, On-Resistance vs. Drain Current

P-Channel Enhancement Mode Field Effect Transistor

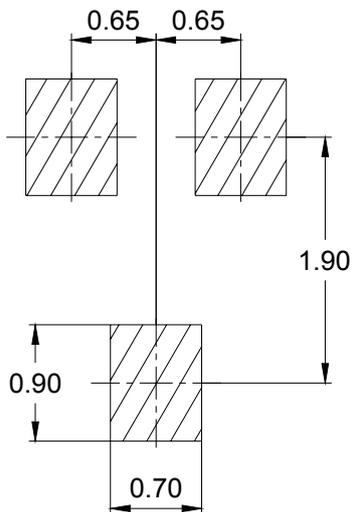
PACKAGE OUTLINE

Plastic surface mounted package

SOT-323



SOLDERING FOOTPRINT



Unit : mm

PACKAGE INFORMATION

Device	Package	Shipping
6 GG, (? F	SOT-323	3000/Tape&Reel