

The J111A Series is a low-cost, all-purpose analog switch designed to support a wide range of applications. In addition to low on-resistance and capacitance, this series guarantees higher breakdown voltage and significantly lower leakage than its counterpart, the J111 Series. Finally, its TO-92 package allows a variety of lead-forms or tape and reel combinations. (See Section 8.)

For further design information please consult the typical performance curves NCB which are located in Section 7.

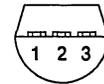
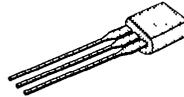
PART NUMBER	V <sub>GS(OFF)</sub> MAX (V)	r <sub>ds(ON)</sub> MAX (Ω)	I <sub>D(OFF)</sub> MAX (pA)	t <sub>ON</sub> TYP (ns)
J111A	-10	30	200	4
J112A	-7	50	200	4
J113A	-5	80	200	4

## SIMILAR PRODUCTS

- SOT-23, See SST111 Series
- TO-18, See 2N4391 Series
- Duals, See 2N5564 Series
- Chips, Order J11XACHP

TO-92

BOTTOM VIEW



- 1 DRAIN
- 2 SOURCE
- 3 GATE

## ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V <sub>GD</sub>	-40	V
Gate-Source Voltage	V <sub>GS</sub>	-40	
Gate Current	I <sub>G</sub>	50	mA
Power Dissipation	P <sub>D</sub>	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T <sub>J</sub>	-55 to 135	°C
Storage Temperature	T <sub>stg</sub>	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T <sub>L</sub>	300	

ELECTRICAL CHARACTERISTICS <sup>1</sup>				LIMITS						
PARAMETER	SYMBOL	TEST CONDITIONS	TYP <sup>2</sup>	J111A		J112A		J113A		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
<b>STATIC</b>										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = -1 \mu A, V_{DS} = 0 V$	-55	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	$V_{DS} = 5 V, I_D = 1 \mu A$		-5	-10	-2	-7	-1	-5	V
Saturation Drain Current <sup>3</sup>	$I_{DSS}$	$V_{DS} = 15 V, V_{GS} = 0 V$		30		15		8		mA
Gate Reverse Current	$I_{GSS}$	$V_{GS} = -15 V$ $V_{DS} = 0 V$ $T_A = 125^\circ C$	-5		-200		-200		-200	pA
			-3							nA
Gate Operating Current	$I_G$	$V_{DG} = 15 V, I_D = 10 mA$	-5							pA
Drain Cutoff Current	$I_{D(OFF)}$	$V_{DS} = 5 V, V_{GS} = -10 V$ $T_A = 125^\circ C$	5		200		200		200	pA
			3							nA
Drain-Source On-Resistance	$r_{DS(ON)}$	$V_{GS} = 0 V, V_{DS} = 0.1 V$			30		50		80	$\Omega$
Gate-Source Forward Voltage	$V_{GS(F)}$	$I_G = 1 mA, V_{DS} = 0 V$	0.7							V
<b>DYNAMIC</b>										
Common-Source Forward Transconductance	$g_{fs}$	$V_{DG} = 20 V, I_D = 1 mA$ $f = 1 kHz$	6							mS
	$g_{os}$		25							$\mu S$
Drain-Source On-Resistance	$r_{ds(ON)}$	$V_{GS} = 0 V, I_D = 0 V$ $f = 1 kHz$			30		50		80	$\Omega$
Common-Source Input Capacitance	$C_{iss}$	$V_{DS} = 0 V, V_{GS} = -10 V$ $f = 1 MHz$	7		12		12		12	pF
Common-Source Reverse Transfer Capacitance	$C_{rss}$		3		5		5		5	
Equivalent Input Noise Voltage	$\bar{e}_n$	$V_{DG} = 10 V, I_D = 1 mA$ $f = 1 kHz$	4							$nV/\sqrt{Hz}$
<b>SWITCHING</b>										
Turn-on Time	$t_{d(ON)}$	$V_{DD} = 10 V, V_{GS(ON)} = 0 V$ P/N $I_{D(ON)} V_{GS(OFF)} R_L$	2							ns
	$t_r$		2							
Turn-off Time	$t_{d(OFF)}$	J111A 12 mA -12 V 800 $\Omega$	6							ns
	$t_f$	J112A 6 mA -7 V 1600 $\Omega$ J113A 3 mA -5 V 3200 $\Omega$	15							

- NOTES: 1.  $T_A = 25^\circ C$  unless otherwise noted.  
 2. For design aid only, not subject to production testing.  
 3. Pulse test; PW = 300  $\mu S$ , duty cycle  $\leq 3\%$ .