SST5114 SERIES

Siliconix incorporated

P-Channel JFETs

The SST5114 Series is a p-channel JFET analog switch designed to complement our n-channel SST4391 Series. They feature low on-resistance and good off-isolation as well as the fast switching associated with JFETs. They are housed in SOT-23 packages and are available tape and reeled to support automated assembly. (See Section 8.)

For additional design information please see performance curves PSCIA, which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (pA)	t_{ON} MAX (ns)
SST5114	10	75	-500	16
SST5115	6	100	-500	30
SST5116	4	150	-500	60

SOT-23 **TOP VIEW**

1 GATE
2 DRAIN
3 SOURCE

SIMILAR PRODUCTS

- TO-18, See 2N5114 Series
- TO-92, See J174 Series
- Chips, Order 2N511XCHP

PRODUCT MARKING	
SST5114	S14
SST5115	S15
SST5116	S16

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	30	V
Gate-Source Voltage	V_{GS}	30	
Gate Current	I_G	50	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]				LIMITS							
					SST5114		SST5115		SST5116		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V		45	30		30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = -15 V, I_D = -1 nA			5	10	3	6	1	4	V
Saturation Drain Current[3]	I_{DSS}	V_{GS} = 0 V	V_{DS} = -18 V		-30	-90					mA
			V_{DS} = -15 V				-15	-60	-5	-25	mA
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V		5		500		500		500	pA
			T_A = 150°C	0.01							µA
Gate Operating Current	I_G	V_{DG} = -15 V, I_D = -1 mA		5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = -15 V	V_{GS} = 12 V	-10		-500					pA
			V_{GS} = 7 V	-10				-500			pA
			V_{GS} = 5 V	-10						-500	pA
		V_{DS} = -15 V, T_A = 150°C	V_{GS} = 12 V	-0.02							nA
			V_{GS} = 7 V	-0.02							nA
			V_{GS} = 5 V	-0.02							nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = -1 mA				75		100		150	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = -1 mA, V_{DS} = 0 V		-0.7		-1		-1		-1	V
DYNAMIC											
Common-Source Forward Transconductance	g_{fs}	V_{DG} = -15 V, I_D = -1 mA, f = 1 kHz		4.5							mS
Common-Source Output Conductance	g_{os}	V_{DG} = -15 V, I_D = -1 mA, f = 1 kHz		20							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0, f = 1 kHz				75		100		150	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz		20							pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, f = 1 MHz	V_{GS} = 12 V	5							pF
			V_{GS} = 7 V	6							pF
			V_{GS} = 5 V	6							pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = -10 V, I_D = -1 mA, f = 1 kHz		20							$nV/\sqrt{Hz}$
SWITCHING											
Turn-on Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V				6		10		25	ns
	t_r	P/N: SST5114	V_{DD} -10 V, $I_{D(ON)}$ -15 mA, $V_{GS(OFF)}$ 20 V, R_L 130 Ω			10		20		35	ns
Turn-off Time	$t_{d(OFF)}$	SST5115	-6 V, -7 mA, 12 V, 900 Ω			6		8		20	ns
	t_f	SST5116	-6 V, -3 mA, 8 V, 2000 Ω			15		30		60	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

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