

# SST5114 SERIES



## P-Channel JFETs

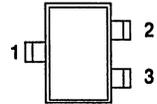
The SST5114 Series is a p-channel JFET analog switch designed to complement our n-channel SST4391 Series. They feature low on-resistance and good off-isolation as well as the fast switching associated with JFETs. They are housed in SOT-23 packages and are available tape and reeled to support automated assembly. (See Section 8.)

PART NUMBER	V <sub>GS(OFF)</sub> MAX (V)	r <sub>ds(ON)</sub> MAX (Ω)	I <sub>D(OFF)</sub> MAX (pA)	t <sub>ON</sub> MAX (ns)
SST5114	10	75	-500	16
SST5115	6	100	-500	30
SST5116	4	150	-500	60

For additional design information please see performance curves PSCIA, which are located in Section 7.

SOT-23

TOP VIEW



1 GATE  
2 DRAIN  
3 SOURCE

## SIMILAR PRODUCTS

- TO-18, See 2N5114 Series
- TO-92, See J174 Series
- Chips, Order 2N511XCHP

PRODUCT MARKING

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SST5114	S14
SST5115	S15
SST5116	S16

## ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V <sub>GD</sub>	30	V
Gate-Source Voltage	V <sub>GS</sub>	30	
Gate Current	I <sub>G</sub>	50	mA
Power Dissipation	P <sub>D</sub>	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature	T <sub>J</sub>	-55 to 150	°C
Storage Temperature	T <sub>stg</sub>	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T <sub>L</sub>	300	

ELECTRICAL CHARACTERISTICS <sup>1</sup>					LIMITS					
PARAMETER	SYMBOL	TEST CONDITIONS	TYP <sup>2</sup>	SST5114		SST5115		SST5116		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
<b>STATIC</b>										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = 1 \mu A, V_{DS} = 0 V$	45	30		30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	$V_{DS} = -15 V, I_D = -1 nA$		5	10	3	6	1	4	
Saturation Drain Current <sup>3</sup>	$I_{DSS}$	$V_{GS} = 0 V$	$V_{DS} = -18 V$	-30	-90					mA
			$V_{DS} = -15 V$			-15	-60	-5	-25	
Gate Reverse Current	$I_{GSS}$	$V_{GS} = 20 V$ $V_{DS} = 0 V$	$T_A = 150^\circ C$	5	500	500	500	500		pA
				0.01						
Gate Operating Current	$I_G$	$V_{DG} = -15 V, I_D = -1 mA$	5							
Drain Cutoff Current	$I_{D(OFF)}$	$V_{DS} = -15 V$	$V_{GS} = 12 V$	-10	-500					pA
			$V_{GS} = 7 V$	-10		-500				
			$V_{GS} = 5 V$	-10				-500		
		$V_{DS} = -15 V$ $T_A = 150^\circ C$	$V_{GS} = 12 V$	-0.02						nA
			$V_{GS} = 7 V$	-0.02						
			$V_{GS} = 5 V$	-0.02						
Drain-Source On-Resistance	$r_{DS(ON)}$	$V_{GS} = 0 V, I_D = -1 mA$			75	100	150		$\Omega$	
Gate-Source Forward Voltage	$V_{GS(F)}$	$I_G = -1 mA, V_{DS} = 0 V$	-0.7	-1	-1	-1	-1		V	
<b>DYNAMIC</b>										
Common-Source Forward Transconductance	$g_{fs}$	$V_{DG} = -15 V, I_D = -1 mA$ $f = 1 kHz$	4.5							mS
Common-Source Output Conductance	$g_{os}$		20							$\mu S$
Drain-Source On-Resistance	$r_{ds(ON)}$	$V_{GS} = 0 V, I_D = 0$ $f = 1 kHz$			75	100	150			$\Omega$
Common-Source Input Capacitance	$C_{iss}$	$V_{DS} = -15 V, V_{GS} = 0 V$ $f = 1 MHz$	20							
Common-Source Reverse Transfer Capacitance	$C_{rss}$	$V_{DS} = 0 V$ $f = 1 MHz$	$V_{GS} = 12 V$	5						pF
			$V_{GS} = 7 V$	6						
			$V_{GS} = 5 V$	6						
Equivalent Input Noise Voltage	$\bar{e}_n$	$V_{DG} = -10 V, I_D = -1 mA$ $f = 1 kHz$	20							$nV/\sqrt{Hz}$
<b>SWITCHING</b>										
Turn-on Time	$t_{d(ON)}$	$V_{GS(ON)} = 0 V$			6	10	25			ns
	$t_r$		P/N	$V_{DD}$	$I_{D(ON)}$	$V_{GS(OFF)}$	$R_L$	10	20	
Turn-off Time	$t_{d(OFF)}$	SST5114	-10 V	-15 mA	20 V	130 $\Omega$	6	8	20	
		SST5115	-6 V	-7 mA	12 V	900 $\Omega$				
		SST5116	-6 V	-3 mA	8 V	2000 $\Omega$	15	30	60	

- NOTES: 1.  $T_A = 25^\circ C$  unless otherwise noted.  
 2. For design aid only, not subject to production testing.  
 3. Pulse test;  $PW = 300 \mu s$ , duty cycle  $\leq 2\%$ .