U443 SERIES

Siliconix incorporated

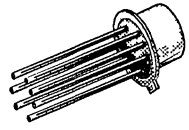
N-Channel JFET Pairs

The U443 Series are matched pairs of JFETs mounted in a single TO-78 package. This two chip design reduces parasitic performance at high frequency while ensuring extremely tight matching. The U443 features high speed amplification (slew rate), high gain (typically > 6 mS), and low gate leakage (typically < 1 pA). This performance makes these devices perfect for use as wideband differential amplifiers in demanding test and measurement applications. Finally, its TO-78 hermetically sealed package is available with military screening per MIL-S-19500. (See Section 1.)

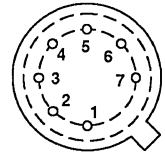
For additional design information please see performance curves NZF, which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS_1} - V_{GS_2} \rvert$ MAX (mV)
U443	-25	4.5	-500	10
U444	-25	4.5	-500	20

TO-78



BOTTOM VIEW



1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 CASE
5 SOURCE 2
6 DRAIN 2
7 GATE 2

SIMILAR PRODUCTS

- TO-71, See U440 Series
- SO-8, See SST440 Series
- Low Noise, See U401 Series
- Low Leakage, See U421 Series
- Chips, Order U44XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	-25	V
Gate-Source Voltage		V_{GS}	-25	
Gate-Gate Voltage		V_{GG}	± 50	
Forward Gate Current		I_G	50	mA
Power Dissipation	Per Side	P_D	367	mW
	Total		500	
Power Derating	Per Side		3	mW/°C
	Total		4	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 150	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				U443		U444		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	-3.5	-1	-6	-1	-6	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	15	6	30	6	30	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-1		-500		-500	pA
		T_A = 150°C	-2					nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 5 mA	-1		-500		-500	pA
		T_A = 125°C	-0.3					nA
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	6	4.5	9	4.5	9	mS
Common-Source Output Conductance	g_{os}		70		200		200	µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 10 V, I_D = 5 mA, f = 1 MHz	3					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1					pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 5 mA, f = 10 kHz	4					$nV/\sqrt{Hz}$
MATCHING								
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2} \rvert$	V_{DG} = 10 V, I_D = 5 mA	6		10		20	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1}-V_{GS2} \rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 5 mA, T = -55 to 25°C	20					µV/°C
		T = 25 to 125°C	20					µV/°C
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.97					
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	0.97					
Common Mode Rejection Ratio	CMRR	V_{DD} = 5 to 10 V, I_D = 5 mA	85					dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

4