SD/SST2100 SERIES

Siliconix incorporated

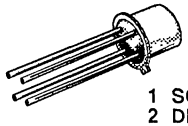
N-Channel Depletion-Mode Lateral DMOS FETs

The SD/SST2100 Series is a depletion-mode MOSFET which utilizes our lateral DMOS process to provide low capacitance, fast switching, and high operating frequency. This DMOS process effectively bridges the operating frequency gap between JFETs and costly gallium-arsenide devices. Additionally, this series is available in both a TO-72 hermetically sealed can as well as the SOT-143 package for commercial applications.

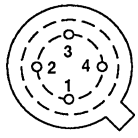
For additional design information please see performance curves DMCD, which are located in Section 7. Application hints can be found in LPD-12 (See Section 9).

PART NUMBER	$V_{(BR)DS}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	C_{rss} MAX (pF)	t_{ON} TYP (ns)
SD2100	15	50	2	1.1
SST2100	15	50	2	1.1

TO-72



BOTTOM VIEW

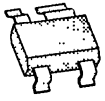


1 SOURCE
2 DRAIN
3 GATE
4 SUBSTRATE

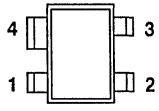
SIMILAR PRODUCTS

- Chips, Order SD2100CHP

SOT-143



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE
4 SUBSTRATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT		UNITS
		SD2100	SST2100	
Gate-Source Voltage	V_{GS}	± 25	± 25	V
Drain-Source Voltage	V_{DS}	25	25	
Drain Current	I_D	50	50	mA
Power Dissipation (T_A = 25°C)	P_D	350	350	mW
Power Derating		2.8	2.8	mW/°C
Operating Junction Temperature	T_J	-55 to 150		°C
Storage Temperature	T_{stg}	-55 to 150		
Lead Temperature (1/16" from case for 10 seconds)	T_L	300		

ELECTRICAL CHARACTERISTICS [1]				LIMITS			
					SD/SST2100		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP [2]	MIN	MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = -5$ V, $I_D = 1$ µA		25	15		V
Gate Reverse Current	I_{GSS}	$V_{GS} = \pm 25$ V, $V_{DS} = V_{BS} = 0$ V		± 0.05		± 1	nA
Saturation Drain Current	I_{DSS}	$V_{DS} = 10$ V, $V_{GS} = V_{BS} = 0$ V		7	0.5	10	mA
Gate-Source Cutoff	$V_{GS(OFF)}$	$V_{DS} = 10$ V, $I_D = 1$µA $V_{BS} = 0$ V		-1.5		-2	V
Gate-Source Voltage	V_{GS}	$V_{DG} = 10$ V $V_{BS} = 0$ V	$I_D = 5$ mA	-0.3	-1	1	V
			$I_D = 10$ mA	0.4	0	1.5	
Drain-Source On-Resistance	$r_{DS(ON)}$	$I_D = 100$ µA $V_{BS} = 0$ V	$V_{GS} = 0$ V	120		200	Ω
			$V_{GS} = 5$ V	40		50	
DYNAMIC							
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{GS} = V_{BS} = 0$ V $f = 1$ kHz		8000	1000		µS
Output Conductance	g_{os}			250		500	
Forward Transconductance	g_{fs}	$V_{DG} = 10$ V, $V_{BS} = 0$ V $I_D = 10$ mA, $f = 1$ kHz		10000	7000		
Output Conductance	g_{os}			350		500	
Common-Source Input Capacitance	C_{iss}	$V_{DS} = 10$ V, $f = 1$ MHz $V_{GS} = V_{BS} = -5$ V		5		6	pF
Reverse Transfer Capacitance	C_{rss}			1		2	
SWITCHING							
Turn-ON Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680$ Ω $V_{IN} = -4$ V to -2 V		0.7			ns
	t_r			0.4			
Turn-OFF Time	t_{OFF}			5			

NOTES: 1. $T_A = 25$ °C unless otherwise noted.
2. For design aid only, not subject to production testing.

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