P-Channel Enhancement Mode MOSFET

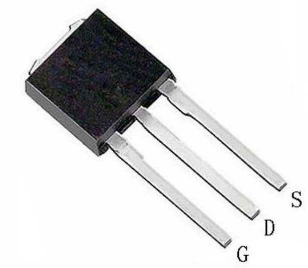
- **Features**

VDS	VGS	RDSon TYP	ID
-30V	±20V	15mR@-10V	-11A
		20mR@-4V5	

- **Applications**
  - Load Switch
  - DCDC conversion
  - NB battery

- **Pin configuration**

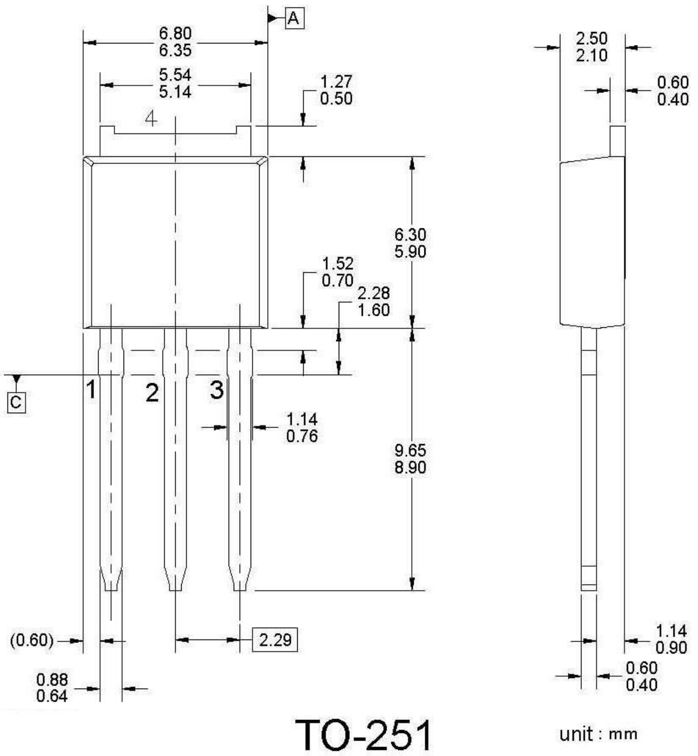
Top View



- **General Description**

This device is produced with high cell density, DMOS trench technology, which is especially used to minimize on-state resistance. This device is particularly suited for low voltage power management requiring a wild range of given voltage ratings(4.5V~25V) such as load switch and battery protection.

- **Package Information**



- **Absolute Maximum Ratings** @T_A = 25℃ unless otherwise noted

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DSS}	30	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current	Continuous	I_D	11	A
	Pulsed		28	
Power Dissipation[1]		P_D	2.5	W
Operating and Storage Junction Temperature Range		T_J, T_{STG}	-55 to +150	°C

- **Electrical Characteristics** @TA = 25℃ unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain–Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -250uA	-30	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30 V, V_{GS} = 0 V	--	--	-1	uA
Gate–Body Leakage Current	I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0 V	--	±1.5	±100	nA
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D =-250uA	-1	-1.3	-3	V
Drain–Source On–State Resistance	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -10A	--	15	20	mR
		V_{GS} = -4.5V, I_D = -7A	--	20	35	
Forward Transconductance	G_{FS}	V_{DS} = -5 V, I_D = -10 A	--	18	--	S
Input Capacitance	C_{ISS}	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz	--	2000	--	pF
Output Capacitance	C_{OSS}		--	550	--	
Reverse Transfer Capacitance	C_{RSS}		--	800	--	
Turn–On Delay Time	$T_{D(ON)}$	VGS=-10V，VDS=-15V, RL=1.5R, RGEN=3R	--	8.6	--	nS
Turn–Off Delay Tim	$T_{D(OFF)}$		--	39	--	
Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = -2 A	--	-0.75	-1.2	V

Notes :

1. Surface Mounted on FR4 Board, t < 10 sec.

   Pulse Test: Pulse Width < 300μs, Duty Cycle < 2%

- **Typical Performance Characteristics**

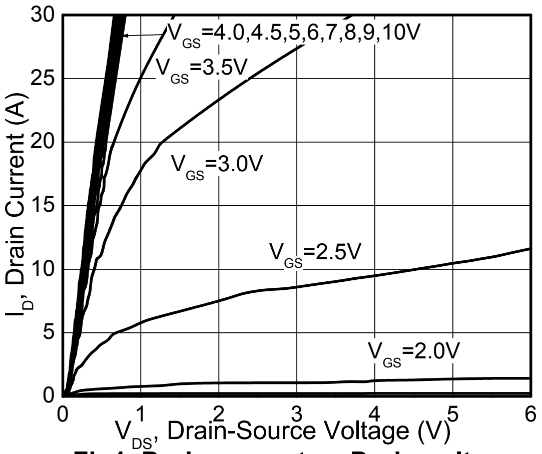


Fig1. Drain current vs Drain voltage

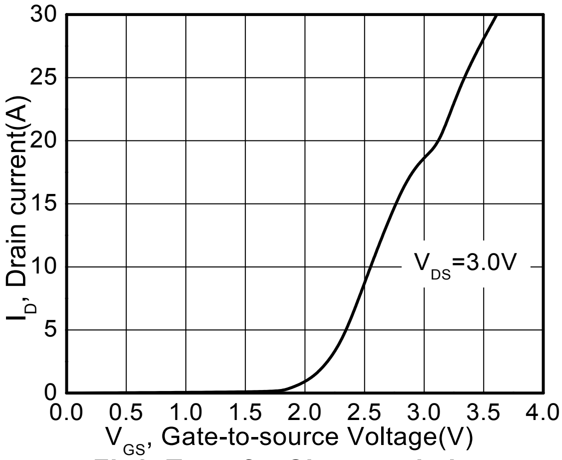


Fig2. Transfer Characteristics

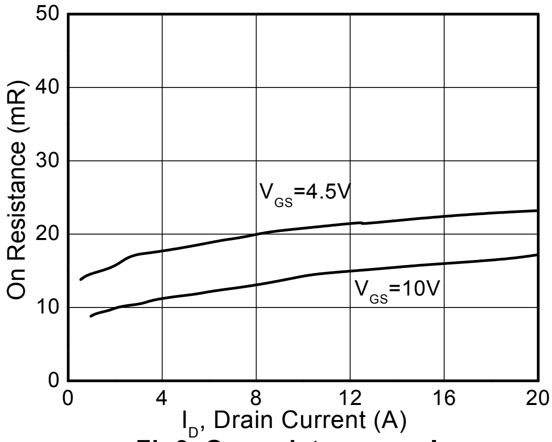


Fig3. On-resistance vs. I_D

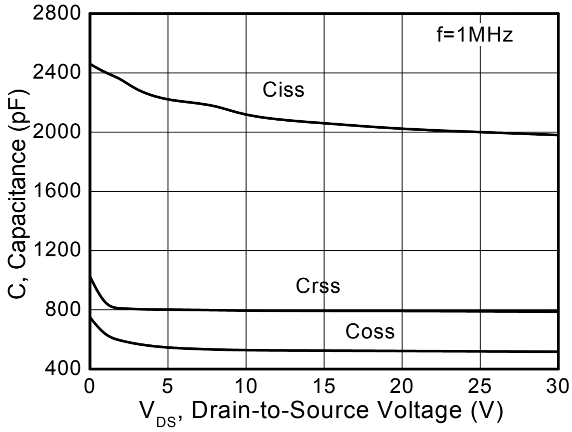


Fig4. Capacitance vs. V_{DS}

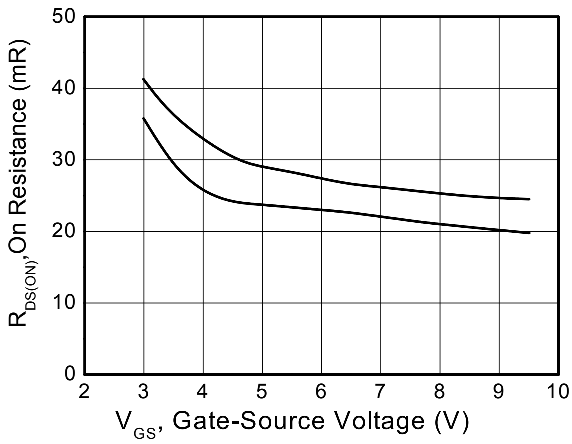


Fig5. On-resistance vs. Gate-Source Voltage

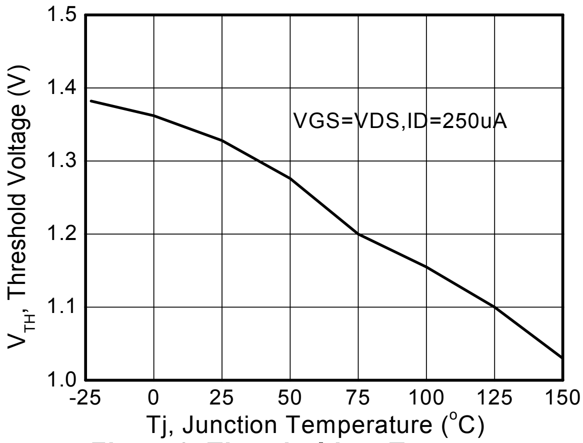


Figure6. Threshold vs Temperature

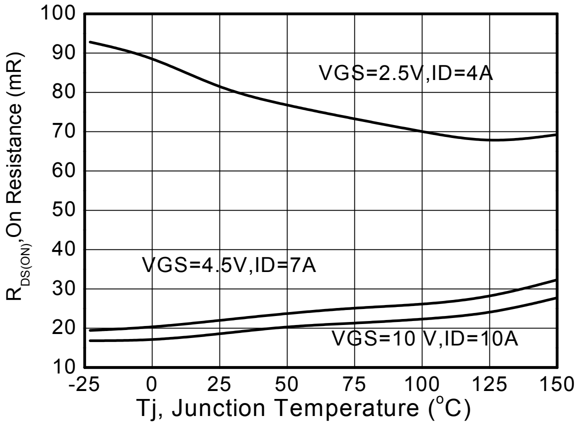


Fig7. On-resistance vs. Temperature

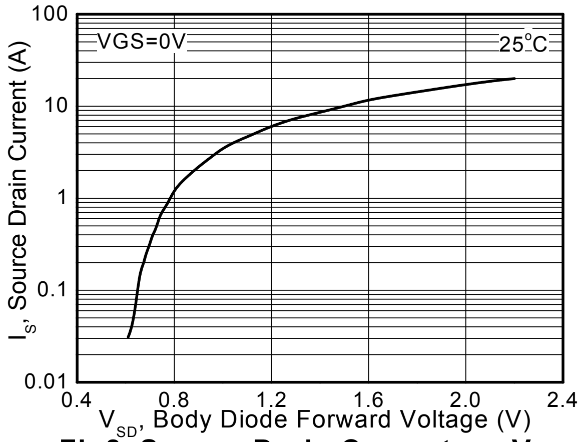


Fig8. Source Drain Current vs. V_{SD}

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