SSC8336GS1

Dual N-Channel Enhancement Mode MOSFET

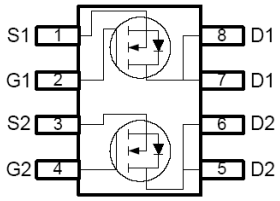
- **Features**

VDS	VGS	RDSon TYP	ID
30V	±20V	16mR@10V	9A
		20mR@4V5	

- **Applications**
  - Inverter;

- **Pin configuration**

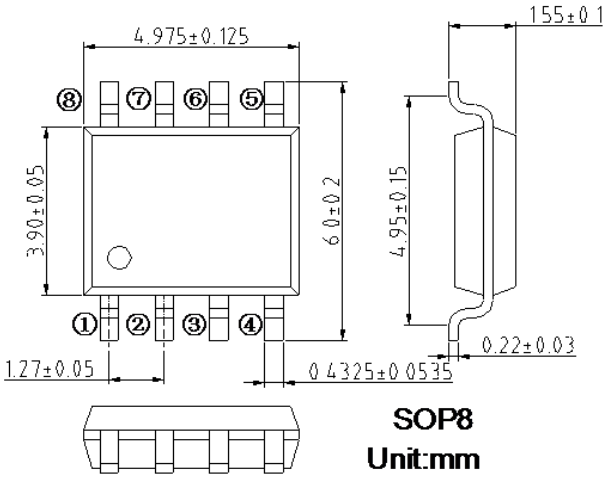
Top View



- **General Description**

This N-Channel enhancement mode power FETs are produced with high cell density, DMOS trench technology, which is especially used to minimize on-state resistance. This device is suitable for use as a load switch，power management in PWM controlled DC/DC Converter and push-pull DC/AC Inverter Systems.

- **Package Information**



- **Ordering Information**

Device	Marking	Package	Qty per Reel	Reel Size
SSC8336GS1	SSC 8336GS1	SOP8	2500	13 Inch

- **Thermal resistance ratings**

Single Operation					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Junction-to-Ambient Thermal Resistance [a]	t ≤ 10 s	$R_{\theta JA}$	56	65	°C/W
	Steady State		87	105	
Junction-to-Ambient Thermal Resistance [b]	t ≤ 10 s	$R_{\theta JA}$	64	76	
	Steady State		96	115	
Junction-to-Case Thermal Resistance	Steady State	$R_{\theta JC}$	32	40	
Dual Operation					
Junction-to-Ambient Thermal Resistance [a]	t ≤ 10 s	$R_{\theta JA}$	61	70	°C/W
	Steady State		92	112	
Junction-to-Ambient Thermal Resistance [b]	t ≤ 10 s	$R_{\theta JA}$	69	82	
	Steady State		102	120	
Junction-to-Case Thermal Resistance	Steady State	$R_{\theta JC}$	36	45	

a Surface mounted on FR4 Board using 1 square inch pad size, 1oz copper

b Surface mounted on FR4 board using minimum pad size, 1oz copper

c Repetitive rating, pulse width limited by junction temperature, t_p=10μs, Duty Cycle=1%

d Repetitive rating, pulse width limited by junction temperature T_J=150°C.

- **Absolute Maximum Ratings** @ T_A = 25°C unless otherwise noted

Parameter	Symbol	N-channel	Unit
Drain-Source Voltage	V_{DSS}	30	V
Gate-Source Voltage	V_{GSS}	±20	V
Continuous Drain Current@T_A=25°	I_D	9	A
Plused Drain Current (Note 1)	I_{DM}	36	A
Total Power Dissipation (Note 2)	P_D	2	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C

Notes：

1:Ratings are based on low frequency and duty cycles to keep initialT_J=25°.

2:The power dissipationg P_D is based on $T_{J(MAX)}$=150°,using≤10s junction-to-ambient thermal resistance.

- **N-channel Electrical Characteristics** @ T_A = 25°C unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain–Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 uA	30	--	--	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D =250 uA	1.3	1.5	2.1	V
Gate–Body Leakage Current	I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0 V	--	--	±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V	--	--	1	uA
Drain–Source On–State Resistance	$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 6.9A	--	16	18	mR
		V_{GS} = 4.5 V, I_D = 5.8A	--	20	23	
Forward Transconductance	G_{FS}	V_{DS} = 5 V, I_D = 5 A	--	7.3	--	S
Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 1.7 A	--	0.79	1	V
Input Capacitance	C_{ISS}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz	--	570	750	pF
Output Capacitance	C_{OSS}		--	113	--	
Reverse Transfer Capacitance	C_{RSS}		--	57	--	
Turn–On Delay Time	$T_{D(ON)}$	V_{Ds} = 15 V, R_L = 2.3R, V_{GS} = 10V, R_{GEN}=3R	--	5.5	8	nS
Turn–Off Delay Tim	$T_{D(OFF)}$		--	21	25	

- **N-channel Typical Performance Characteristics**

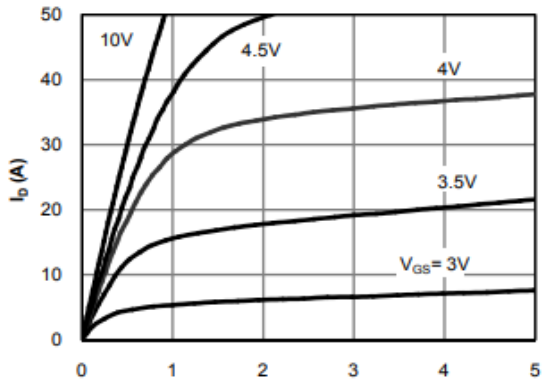


Figure 1: On-Region Characteristics

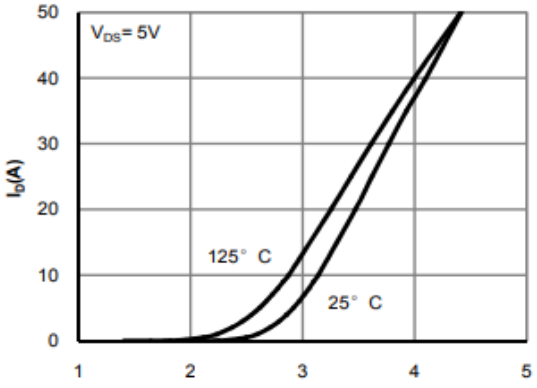


Figure 2: Transfer Characteristics

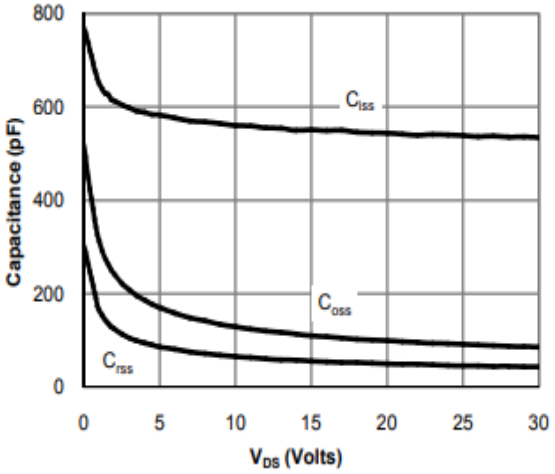


Figure3:Capacitance Characteristics

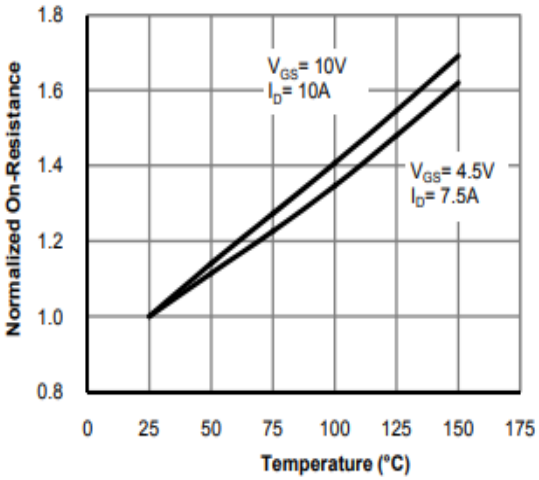


Figure4:On-Resistance vs.Junction Temperature

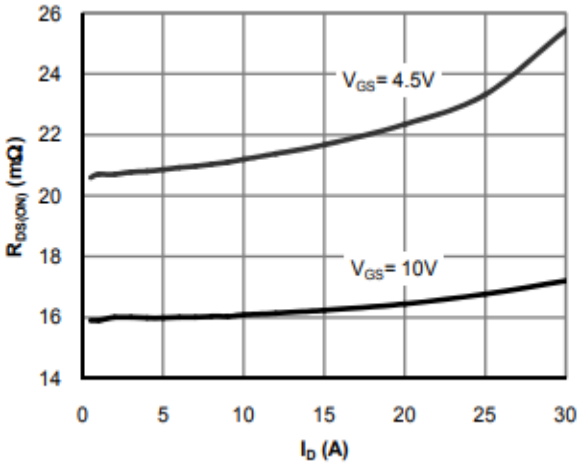


Figure5:On-Resistance vs.Drain Current and Gate Voltage

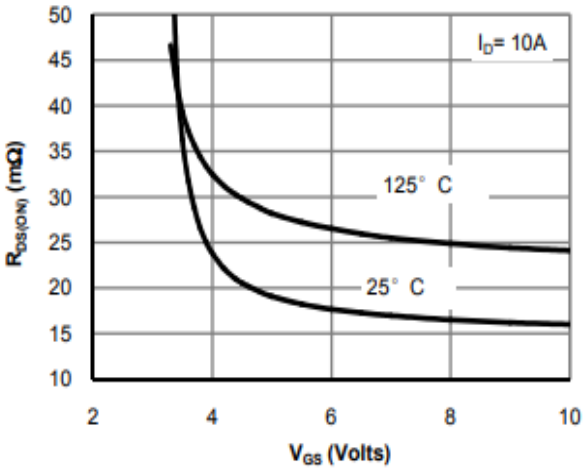


Figure6:On-Resistance vs. Gate-Source Voltage

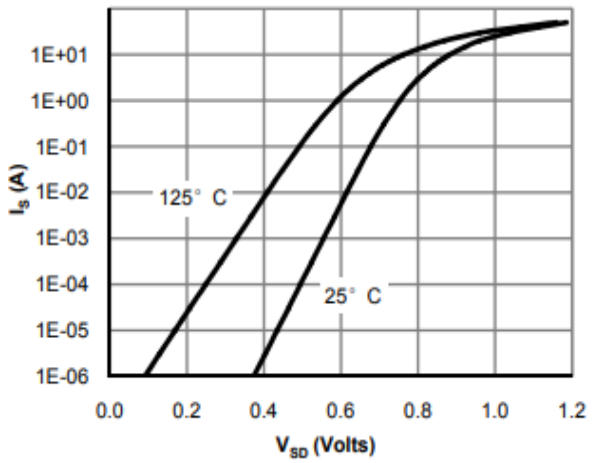


Figure7:Body-Diode Characteristic

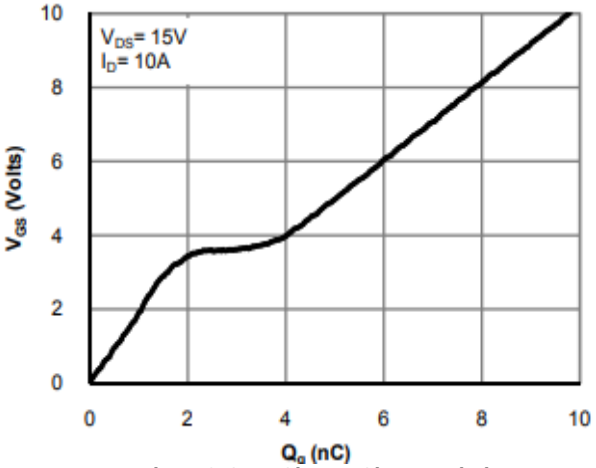


Figure8:Gate-Charge Characteristic

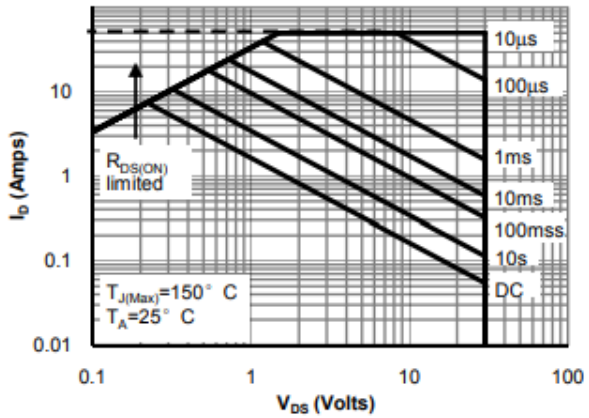


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

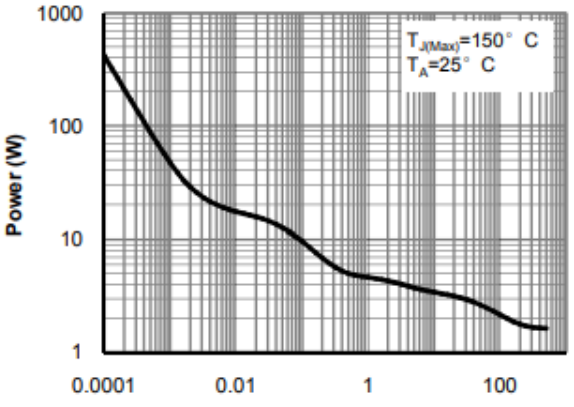


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

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