SSC8330GQ4

Dual Asymmetric N-Channel Enhancement Mode MOSFET

- **Features**

	V_{DS}	V_{GS}	R_{DSon} TYP	I_D
Q1	30V	±20V	9.5 mR@10V	15A
			12.5mR@4V5	
Q2	30V	±20V	8 mR@10V	18A
			10mR@4V5	

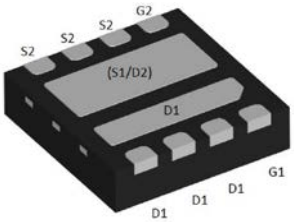
- **General Description**

This device uses advanced trench technology to provide excellent RDS(ON) and low gate charge. This device is suitable for use as a load switch or in PWM applications.

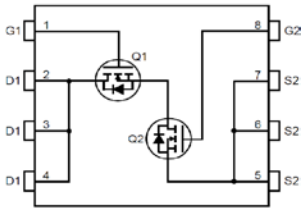
- **Applications**
  - Load Switch
  - Isolated DC/DC Converters
  - DCDC conversion in Computing

- **Pin configuration**

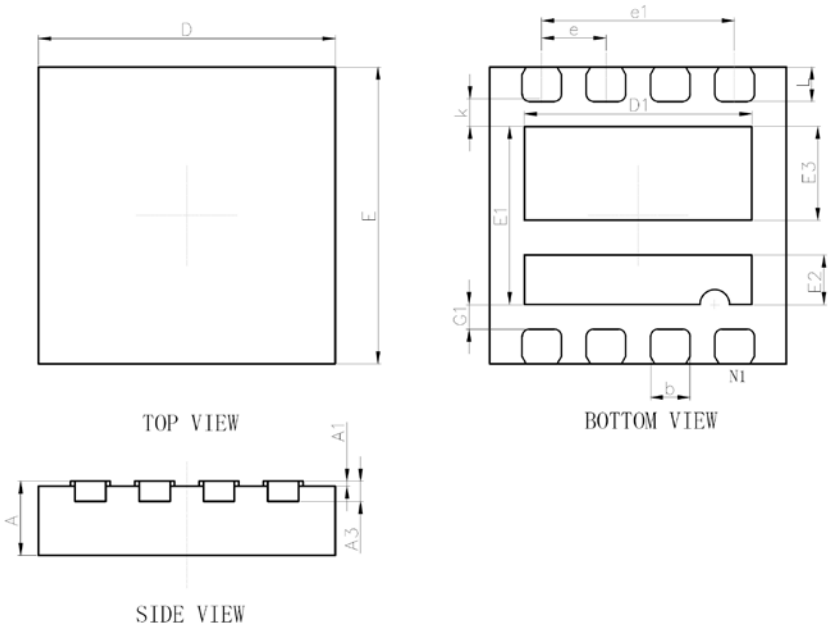
Bottom View



Top View



- **Package Information**



Package: DFN3X3-8L

Symbol	Dimensions In Millimeters	
	Min.	Max.
A	0.700/0.800	0.800/0.900
A1	0.000	0.050
A3	0.203REF.	
D	2.950	3.050
E	2.950	3.050
D1	2.250	2.350
E1	1.700	1.900
E2	0.450	0.550
E3	0.900	1.000
k	0.200	0.300
G1	0.200	0.300
b	0.350	0.450
e	0.650BSC	
e1	1.95BSC	
L	0.300	0.400

- **Absolute Maximum Ratings** @ T_A = 25°C unless otherwise specified

Parameter	Symbol	Maximum		Unit
		Q1	Q2	
Drain-Source Voltage	V_{DSS}	30	30	V
Gate-Source Voltage	V_{GSS}	±20	±20	V
Continuous Drain Current [1] V_{GS}@10V T_C = 25°C	I_D	15	18	A
Continuous Drain Current [1] V_{GS}@10V T_C = 100°C		12	13	A
Continuous Drain Current [2] V_{GS}@10V T_A = 25°C	I_{DSM}	12.5	15	A
Continuous Drain Current [2] V_{GS}@10V T_A = 70°C		7	8	A
Plused Drain Current [3]	I_{DM}	60	70	A
Repetitive avalanche energy L=0.1mH [3]	E_{AS}	9	16	mJ
Power Dissipation [1] T_C = 25°C	P_D	22	24.5	W
Power Dissipation [1] T_C = 100°C		8	10	W
Power Dissipation [2] T_A = 25°C	P_{DSM}	3	3	W
Power Dissipation [2] T_A = 70°C		1	1	W
Storage and Junction Temperature Range	T_J, T_{STG}	-55 to +150		°C

- **Thermal Characteristics**

Parameter		Symbol	Typ Q1	Max Q1	Typ Q2	Max Q2	Units
Maximum Junction-to-Ambient[2]	t≤10S	$R_{\theta JA}$	42	55	41	55	°C/W
Maximum Junction-to-Ambient [2] [4]	Steady-State		73	95	72	95	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	4.8	5.6	4.6	5.4	°C/W

- **Q1 Electrical Characteristics** @ T_A = 25°C unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain–Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA	30	--	--	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D =250 μA	1	1.65	2.1	V
Gate–Body Leakage Current	I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0 V	--	--	±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V	--	--	1	uA
Drain–Source On–State Resistance	$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 15 A	--	9.5	13	mR
		V_{GS} = 4.5 V, I_D = 12 A	--	12.5	16	
Forward Transconductance	G_{FS}	V_{DS} = 15 V, I_D = 12 A	8	16	--	S
Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 0.5A	--	0.8	1.3	V
Input Capacitance	C_{ISS}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz	--	800	--	pF
Output Capacitance	C_{OSS}		--	255	--	
Reverse Transfer Capacitance	C_{RSS}		--	75	--	
Turn–On Delay Time	$T_{D(ON)}$	V_{DS} = 15 V, R_L = 2.3Ω, V_{GS} = 10V, R_{GEN}=3Ω	--	--	15	ns
Turn–Off Delay Tim	$T_{D(OFF)}$		--	--	55	

Note :

1. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t ≤ 10s value and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.
4. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

Q1 Typical Performance Characteristics

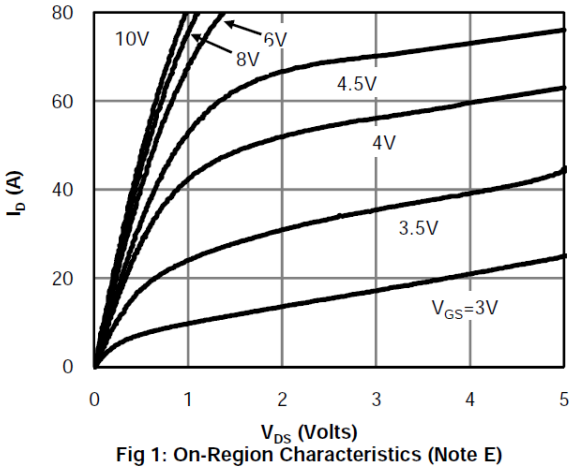


Fig 1: On-Region Characteristics (Note E)

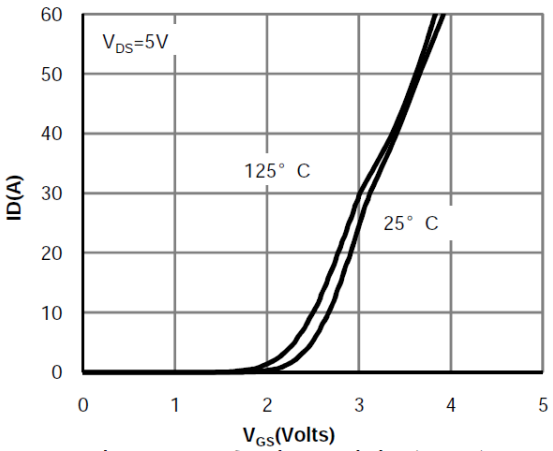


Figure 2: Transfer Characteristics (Note E)

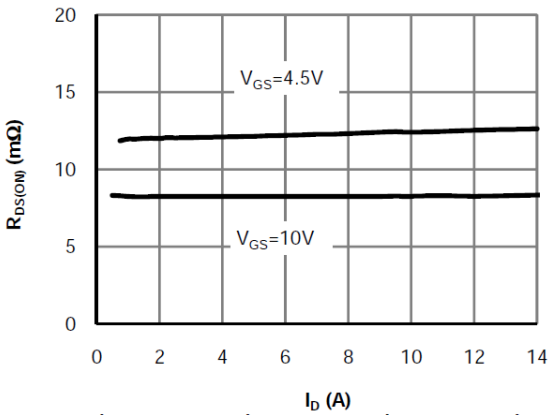


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

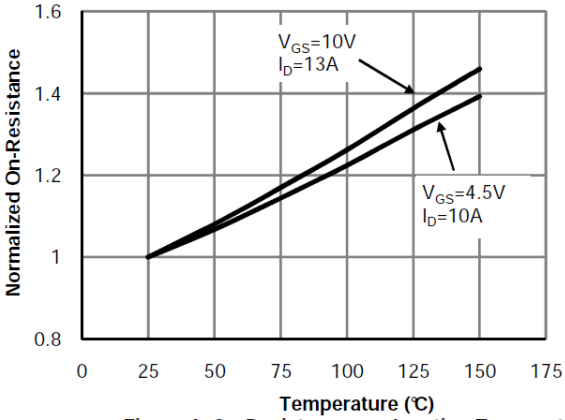


Figure 4: On-Resistance vs. Junction Temperature (Note E)

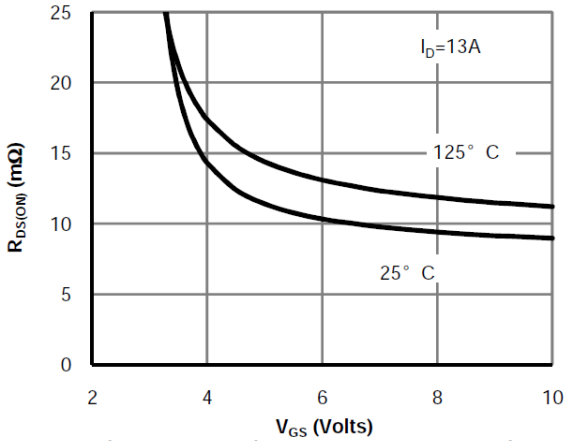


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

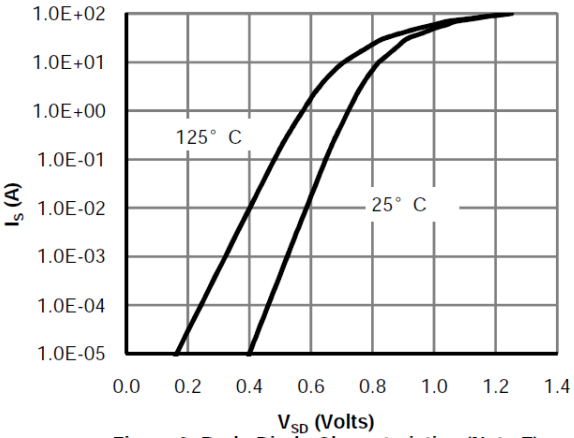


Figure 6: Body-Diode Characteristics (Note E)

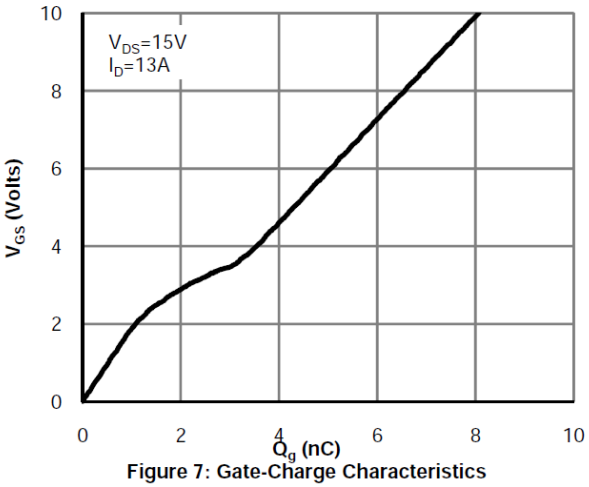


Figure 7: Gate-Charge Characteristics

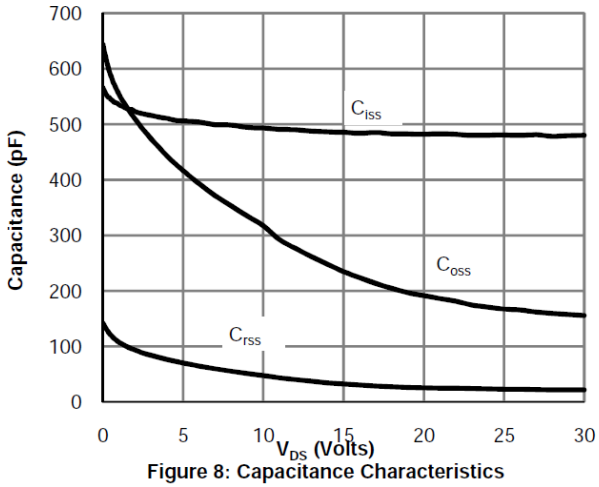


Figure 8: Capacitance Characteristics

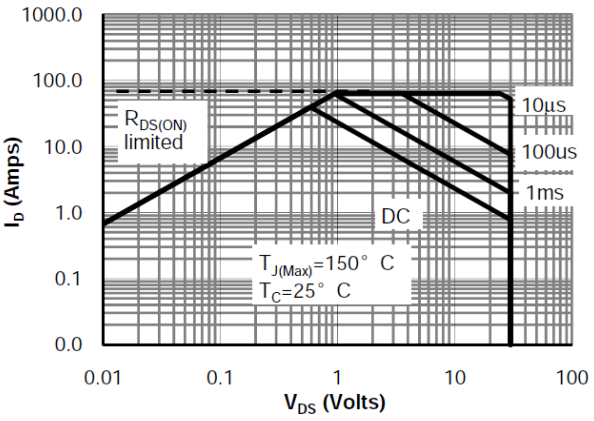


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

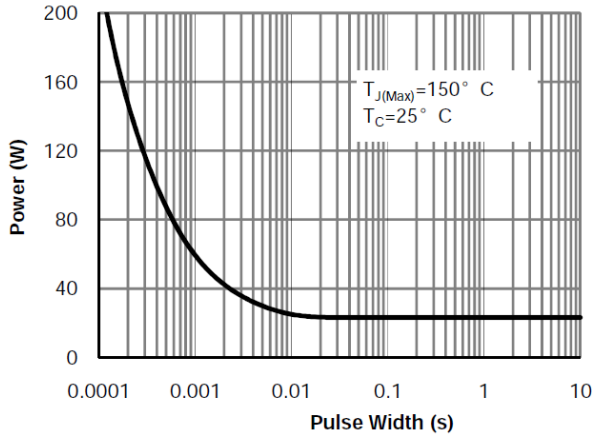


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

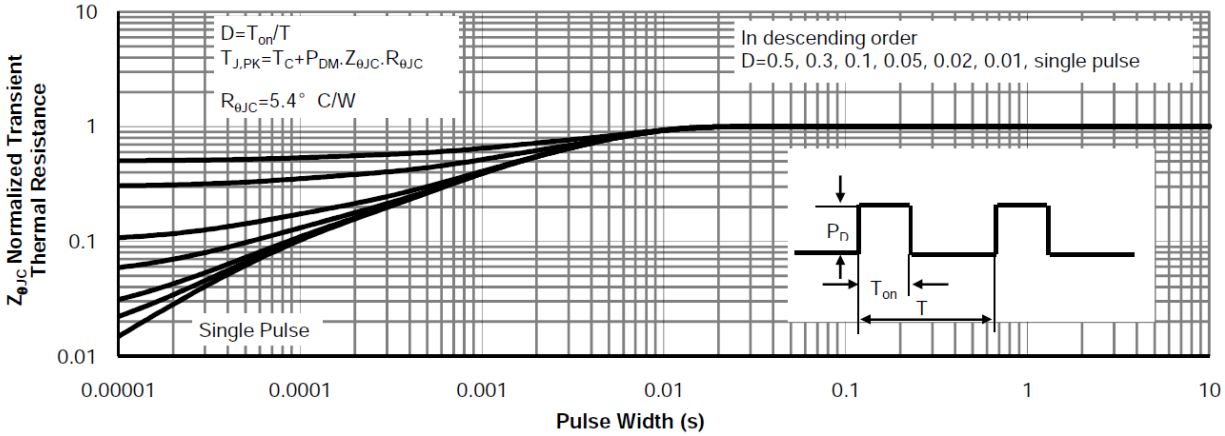


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

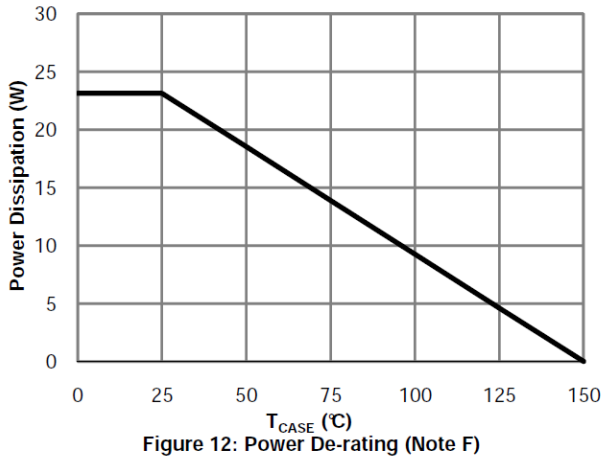


Figure 12: Power De-rating (Note F)

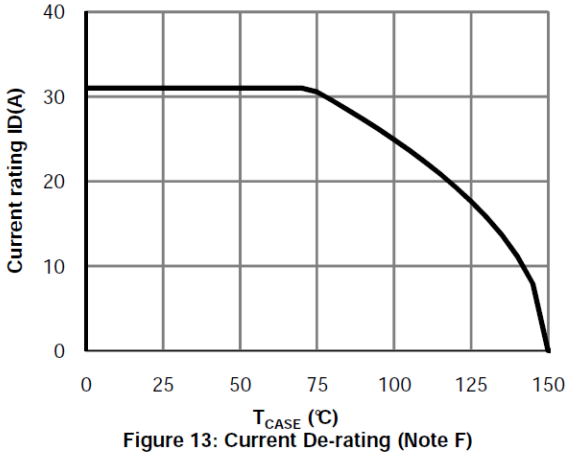


Figure 13: Current De-rating (Note F)

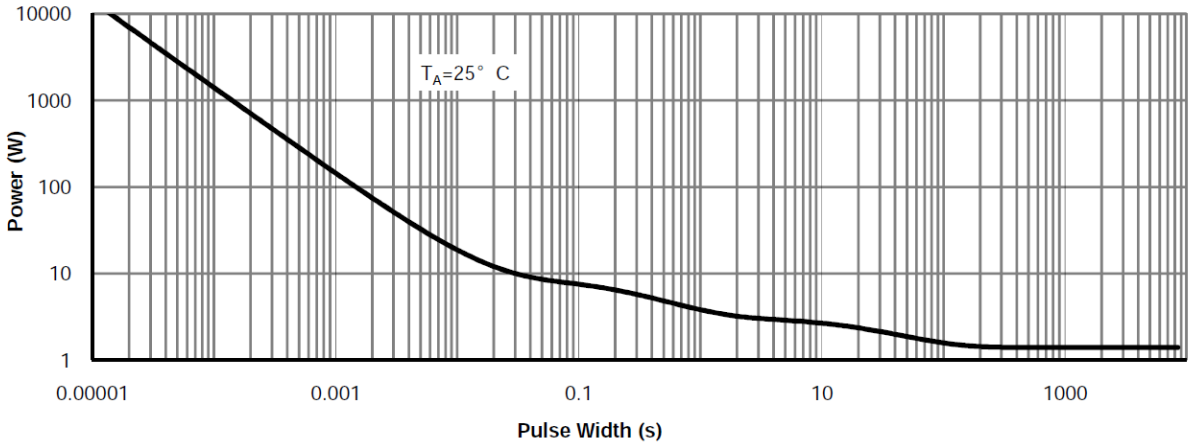


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

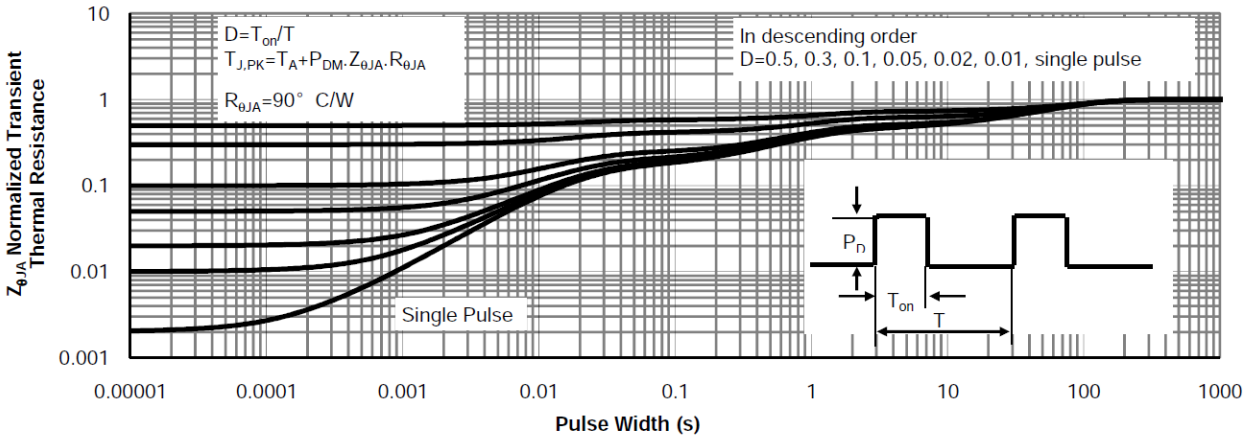


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

- **Q2 Electrical Characteristics** @ T_A = 25°C unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain–Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA	30	--	--	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D =250 μA	1	1.55	3	V
Gate–Body Leakage Current	I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0 V	--	--	±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V	--	--	1	uA
Drain–Source On–State Resistance	$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 15 A	--	8	11	mR
		V_{GS} = 4.5 V, I_D = 12 A	--	10	14	
Forward Transconductance	G_{FS}	V_{DS} = 15 V, I_D = 12 A	8	16	--	S
Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 1A	--	0.8	1.5	V
Input Capacitance	C_{ISS}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz	--	1000	--	pF
Output Capacitance	C_{OSS}		--	269	--	
Reverse Transfer Capacitance	C_{RSS}		--	105	--	
Turn–On Delay Time	$T_{D(ON)}$	V_{DS} = 15 V, R_L = 2.3Ω, V_{GS} = 10V, R_{GEN}=3Ω	--	--	18	ns
Turn–Off Delay Tim	$T_{D(OFF)}$		--	--	70	

Note :

1. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t ≤ 10s value and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.
4. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

Q2 Typical Performance Characteristics

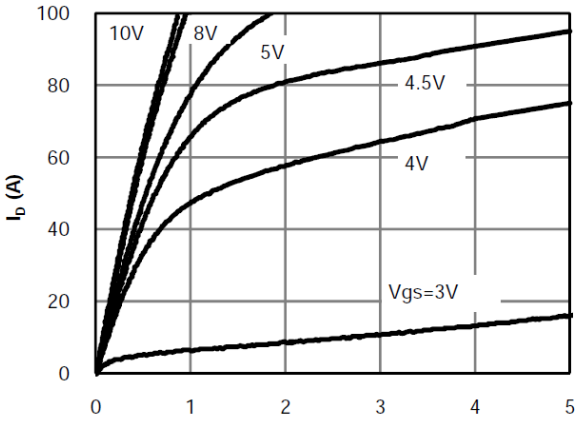


Fig 1: On-Region Characteristics (Note E)

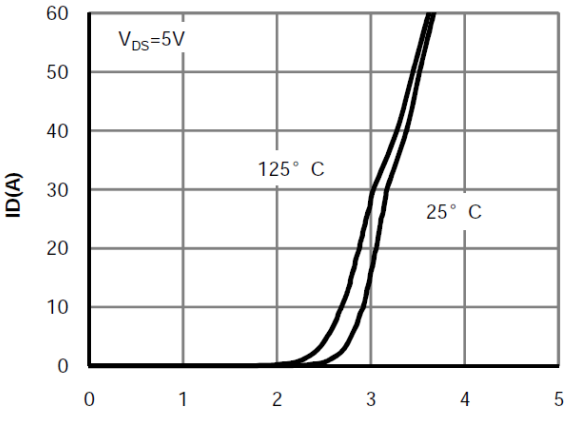


Figure 2: Transfer Characteristics (Note E)

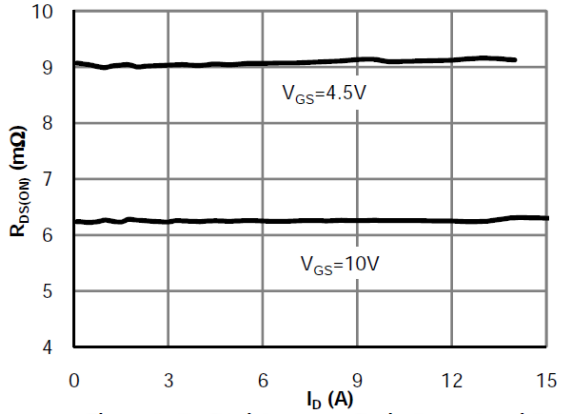


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

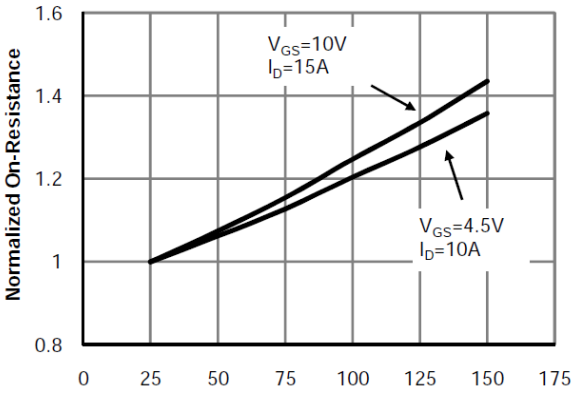


Figure 4: On-Resistance vs. Junction Temperature (Note E)

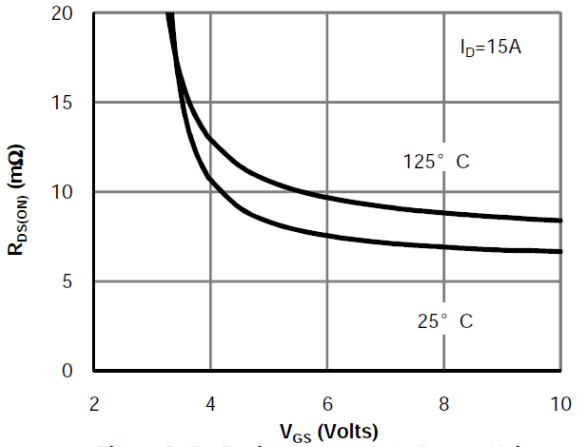


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

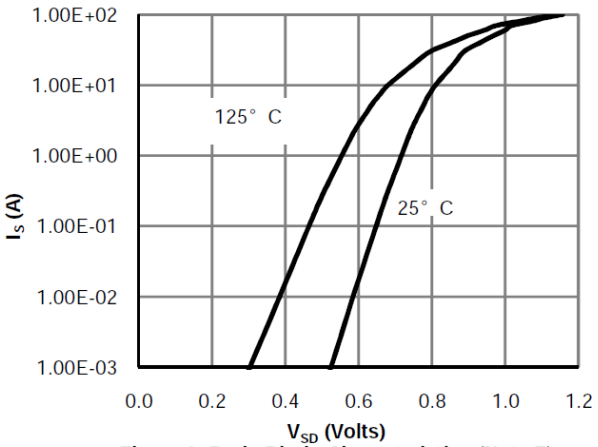


Figure 6: Body-Diode Characteristics (Note E)

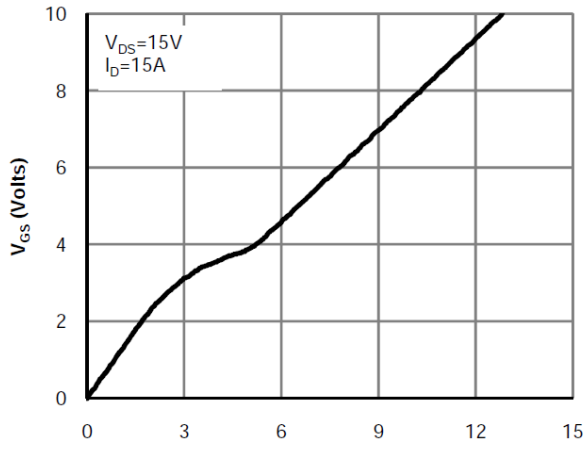


Figure 7: Gate-Charge Characteristics

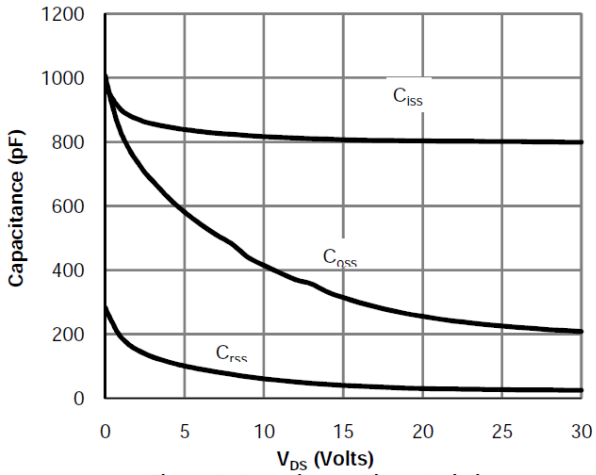


Figure 8: Capacitance Characteristics

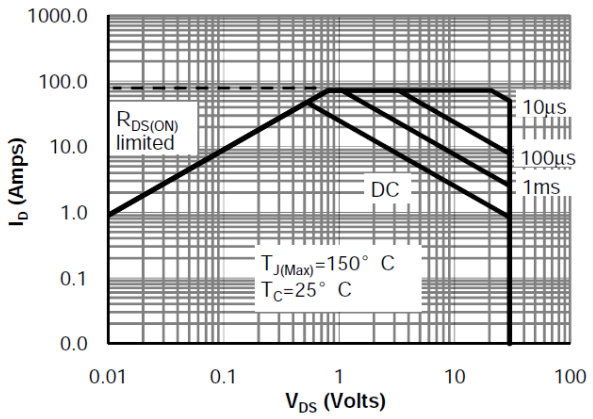


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

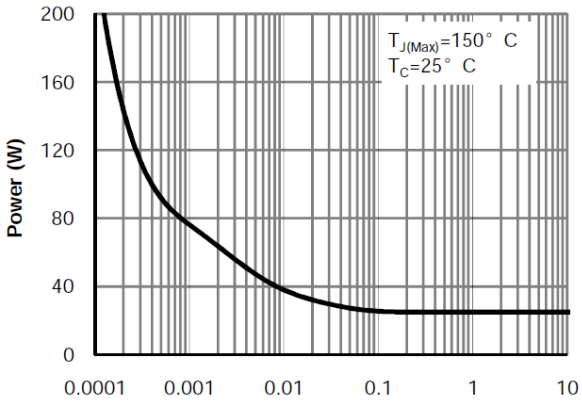


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

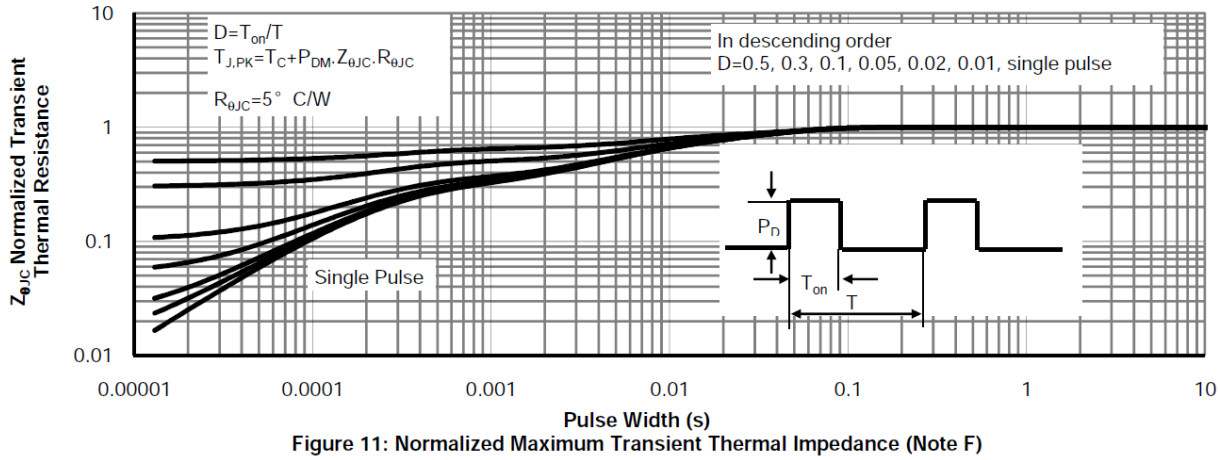


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

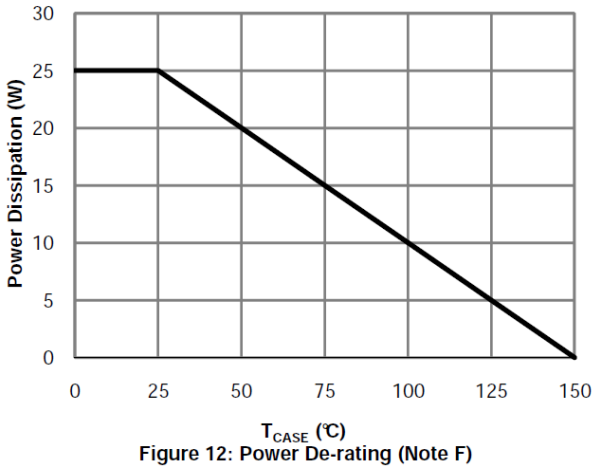


Figure 12: Power De-rating (Note F)

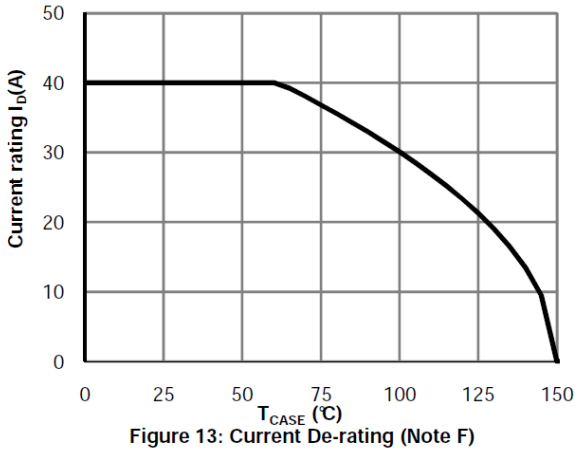


Figure 13: Current De-rating (Note F)

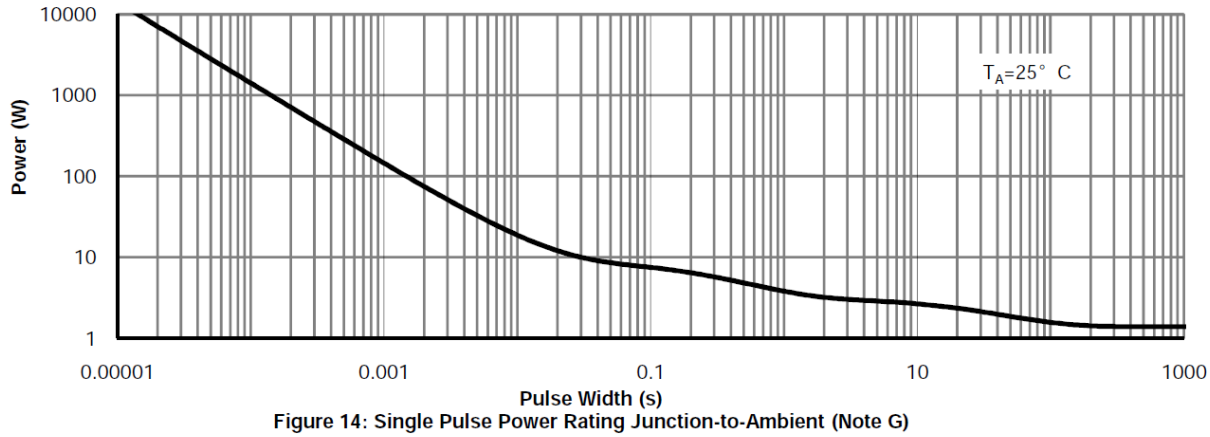


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

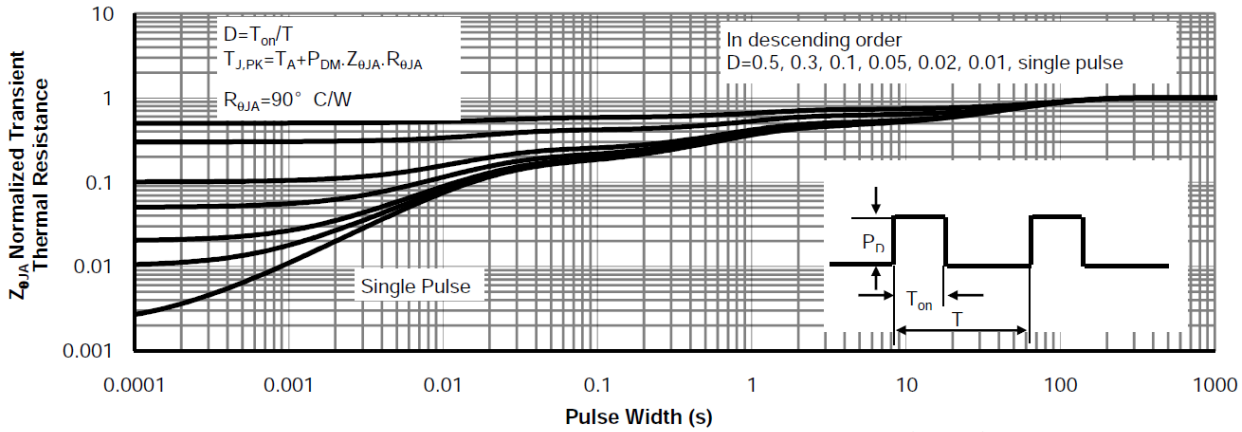


Figure 15: Normalized Maximum Transient Thermal Impedance (Note G)

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