



# STV300NH02L

## N-channel 24 V, 0.8 mΩ typ., 200 A STripFET™ III Power MOSFET in a PowerSO-10 package

Datasheet — production data

### Features

Order code	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STV300NH02L	24 V	0.001 Ω	200 A <sup>(1)</sup>

1. This value is limited by package

- R<sub>DS(on)</sub>\*Q<sub>g</sub> industry's benchmark
- Conduction losses reduced
- Low profile, very low parasitic inductance
- Switching losses reduced

### Applications

- Switching applications
  - OR-ing
- Specially designed and optimized for high efficiency DC/DC converters.

### Description

This N-channel enhancement mode Power MOSFET benefits from the latest refinement of STMicroelectronics' unique "single feature size" strip-based process, which decreases the critical alignment steps to offer exceptional manufacturing reproducibility. The result is a transistor with extremely high packing density for low on-resistance, rugged avalanche characteristics and low gate charge.

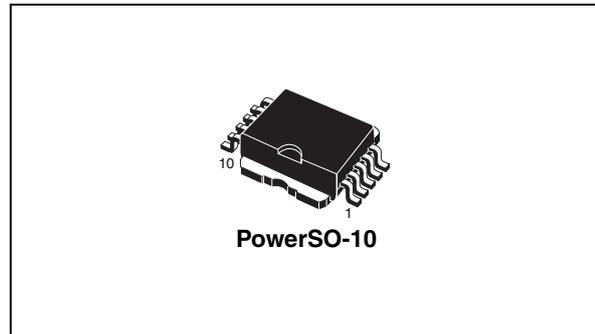


Figure 1. Internal schematic diagram

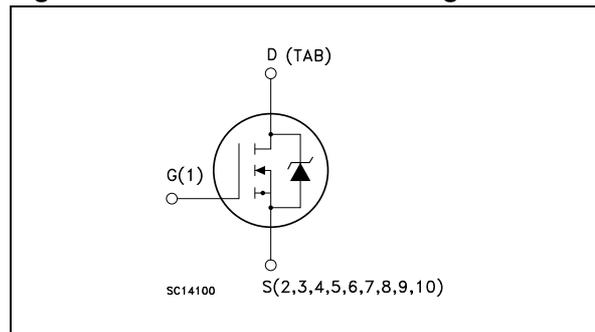


Figure 2. Connection diagram (top view)

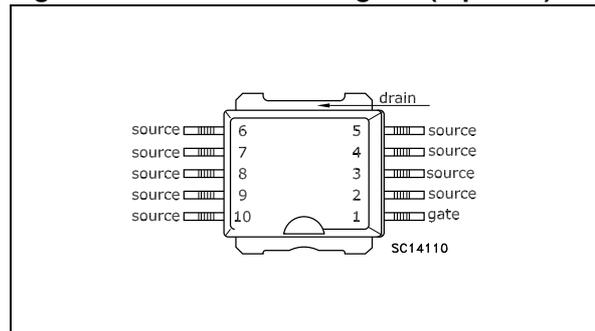


Table 1. Device summary

Order code	Marking	Package	Packaging
STV300NH02L	300NH02L	PowerSO-10	Tape and reel

# Content

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	24	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	200	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	200	A
$I_{DM}^{(2)}$	Drain current (pulsed)	800	A
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	300	W
	Derating factor	2	W/°C
$E_{AS}^{(4)}$	Single pulse avalanche energy	1.6	J
$T_{stg}$	Storage temperature	-55 to 175	°C
$T_j$	Operating junction temperature		

1. This value is limited by package
2. Pulse with limited by safe operating area
3. This value is rated according to  $R_{thj-c}$
4. Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = 60\text{ A}$ ,  $V_{DD} = 20\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.5	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	35	°C/W

1. When mounted on 1 inch<sup>2</sup> FR-4, 2 oz Cu

## 2 Electrical characteristics

(T<sub>case</sub> = 25°C unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage (V <sub>GS</sub> = 0)	I <sub>D</sub> = 1 mA	24			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = 24 V V <sub>DS</sub> = 24 V, T <sub>c</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>DS</sub> = ± 20 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1	1.5	2.5	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 5 V, I <sub>D</sub> = 40 A V <sub>GS</sub> = 10 V, I <sub>D</sub> = 80 A		1.15 0.8	1.5 1	mΩ

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 15V, f = 1 MHz, V <sub>GS</sub> = 0	-	7055	-	pF
C <sub>oss</sub>	Output capacitance			3251		
C <sub>rss</sub>	Reverse transfer capacitance			307		
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 12V, I <sub>D</sub> = 120A,	-	109	-	nC
Q <sub>gs</sub>	Gate-source charge	V <sub>GS</sub> = 10V		30		
Q <sub>gd</sub>	Gate-drain charge	(see Figure 15)		26		
R <sub>G</sub>	Gate input resistance	V <sub>DS</sub> = 0V, f = 1 MHz, V <sub>GS</sub> = 0	-	4.4	-	Ω

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 12V, I <sub>D</sub> = 60A R <sub>G</sub> = 4.7Ω, V <sub>GS</sub> = 10V, (see Figure 14)	-	18	-	ns
t <sub>r</sub>	Rise time			275		
t <sub>d(off)</sub>	Turn-off delay time	V <sub>DD</sub> = 12V, I <sub>D</sub> = 60A R <sub>G</sub> = 4.7Ω, V <sub>GS</sub> = 10V, (see Figure 14)	-	138	-	ns
t <sub>f</sub>	Fall time			94.4		

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		200	A
$I_{SDM}$	Source-drain current (pulsed)				800	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 120A, V_{GS} = 0$	-		1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 120A, di/dt = 100A/\mu s$		63		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 20V, T_j = 25^\circ C$	-	85		nC
$I_{RRM}$	Reverse recovery current	(see Figure 19)		2.7		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 120A, di/dt = 100A/\mu s$		63		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 20V, T_j = 150^\circ C$	-	88		nC
$I_{RRM}$	Reverse recovery current	(see Figure 19)		2.8		A

1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 3. Safe operating area

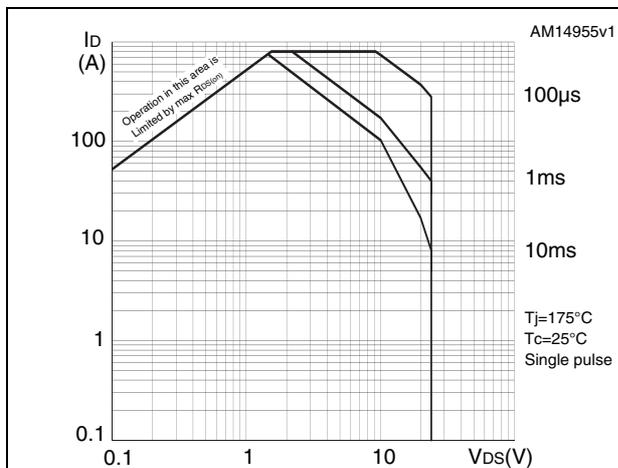


Figure 4. Thermal impedance

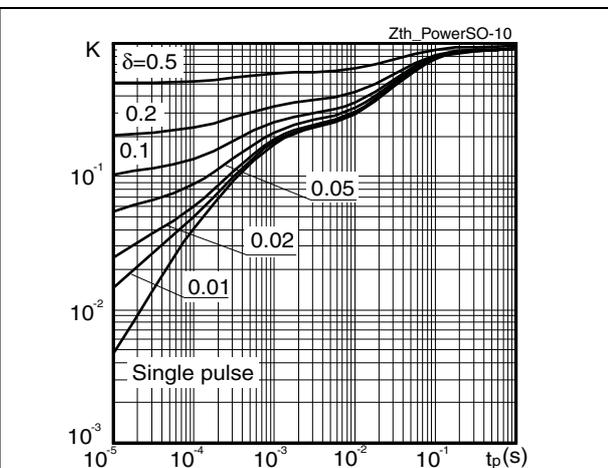


Figure 5. Output characteristics

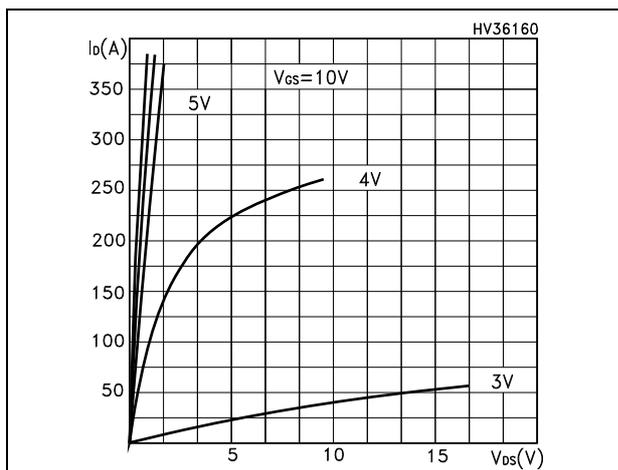


Figure 6. Transfer characteristics

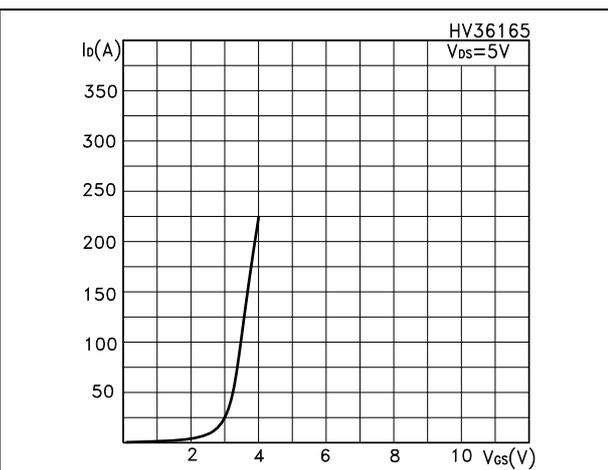


Figure 7. Static drain-source on-resistance

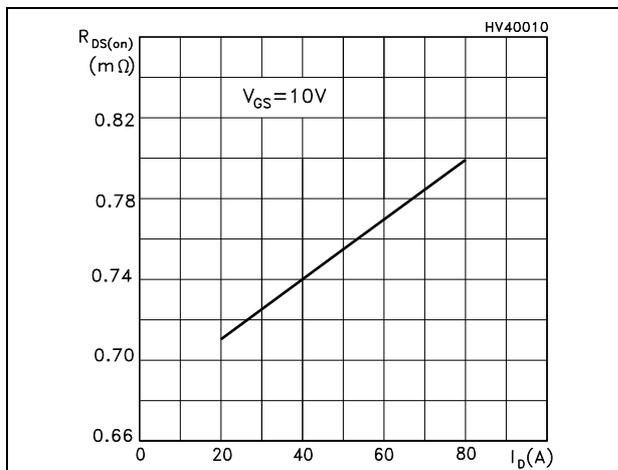


Figure 8. Normalized  $BV_{DSS}$  vs temperature

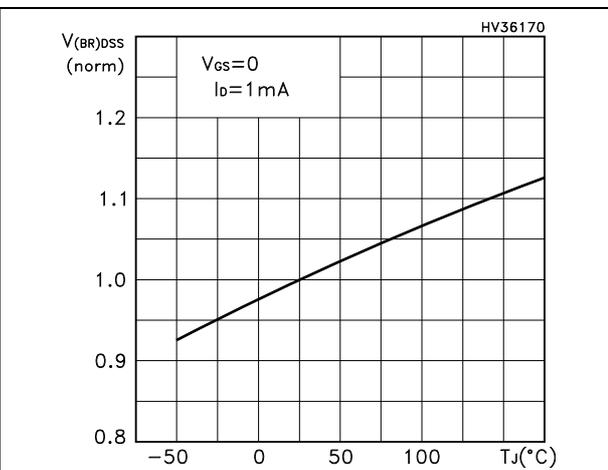


Figure 9. Gate charge vs gate-source voltage Figure 10. Capacitance variations

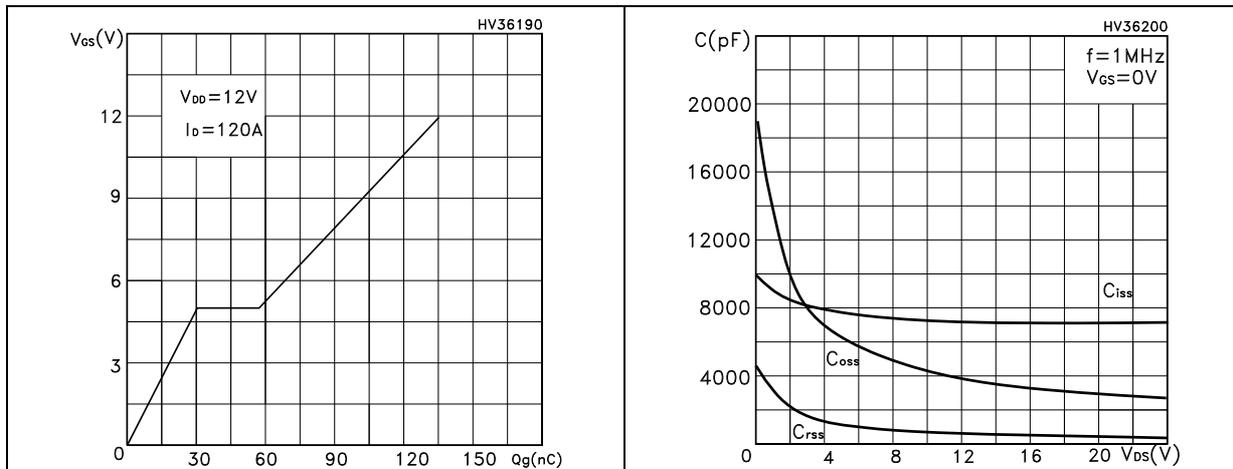


Figure 11. Normalized gate threshold voltage vs temperature Figure 12. Normalized on-resistance vs temperature

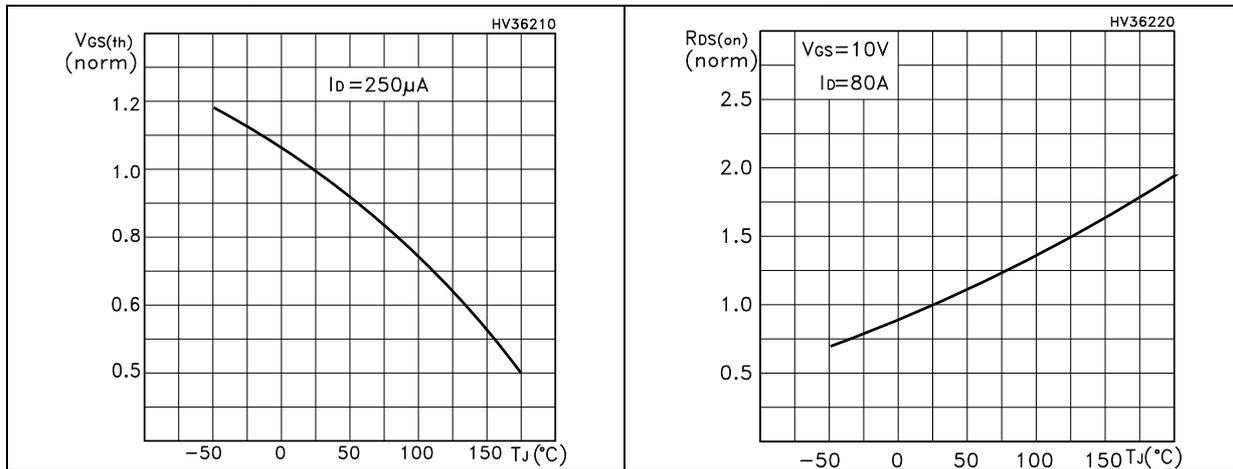
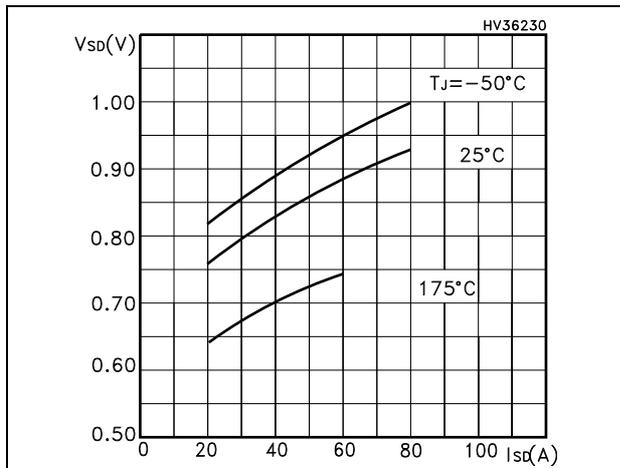
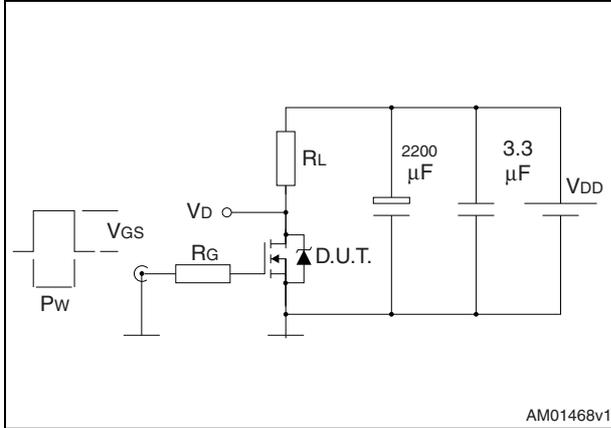


Figure 13. Source-drain diode forward characteristics



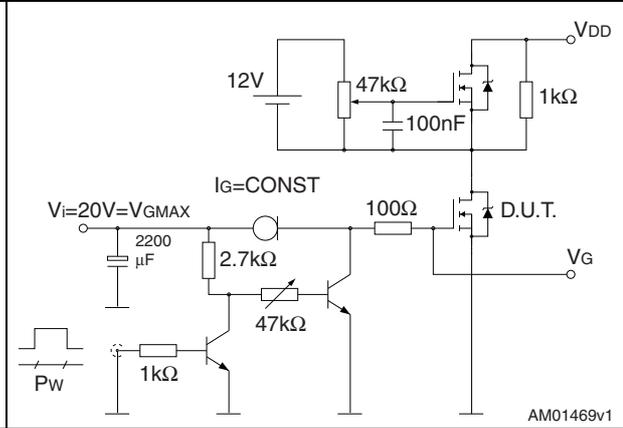
### 3 Test circuits

**Figure 14. Switching times test circuit for resistive load**



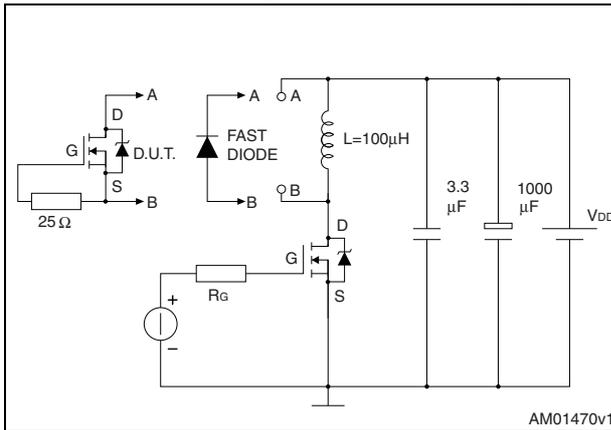
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**Figure 15. Gate charge test circuit**



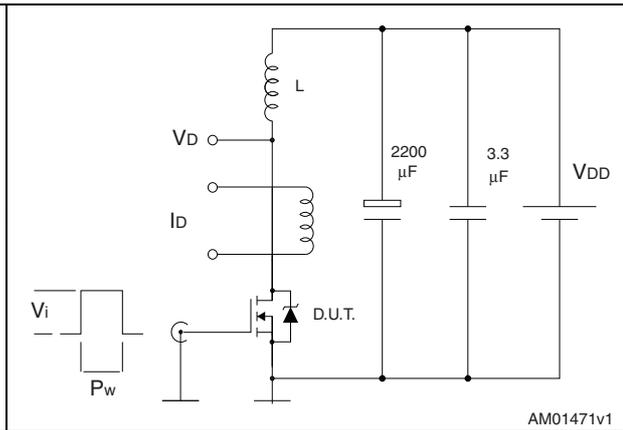
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**Figure 16. Test circuit for inductive load switching and diode recovery times**



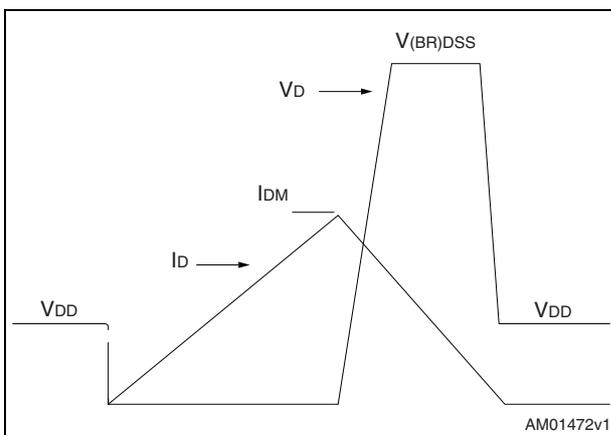
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**Figure 17. Unclamped inductive load test circuit**



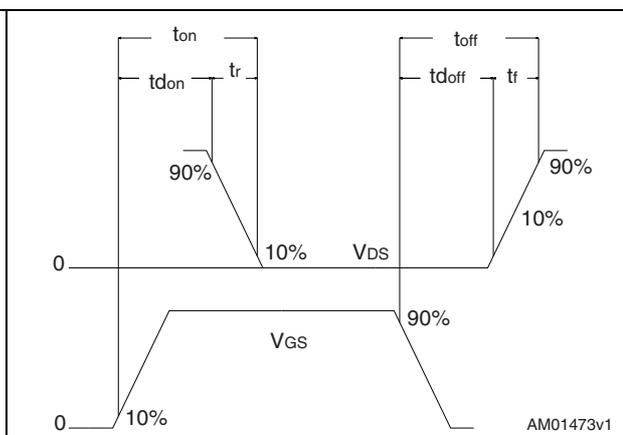
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**Figure 18. Unclamped inductive waveform**



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**Figure 19. Switching time waveform**



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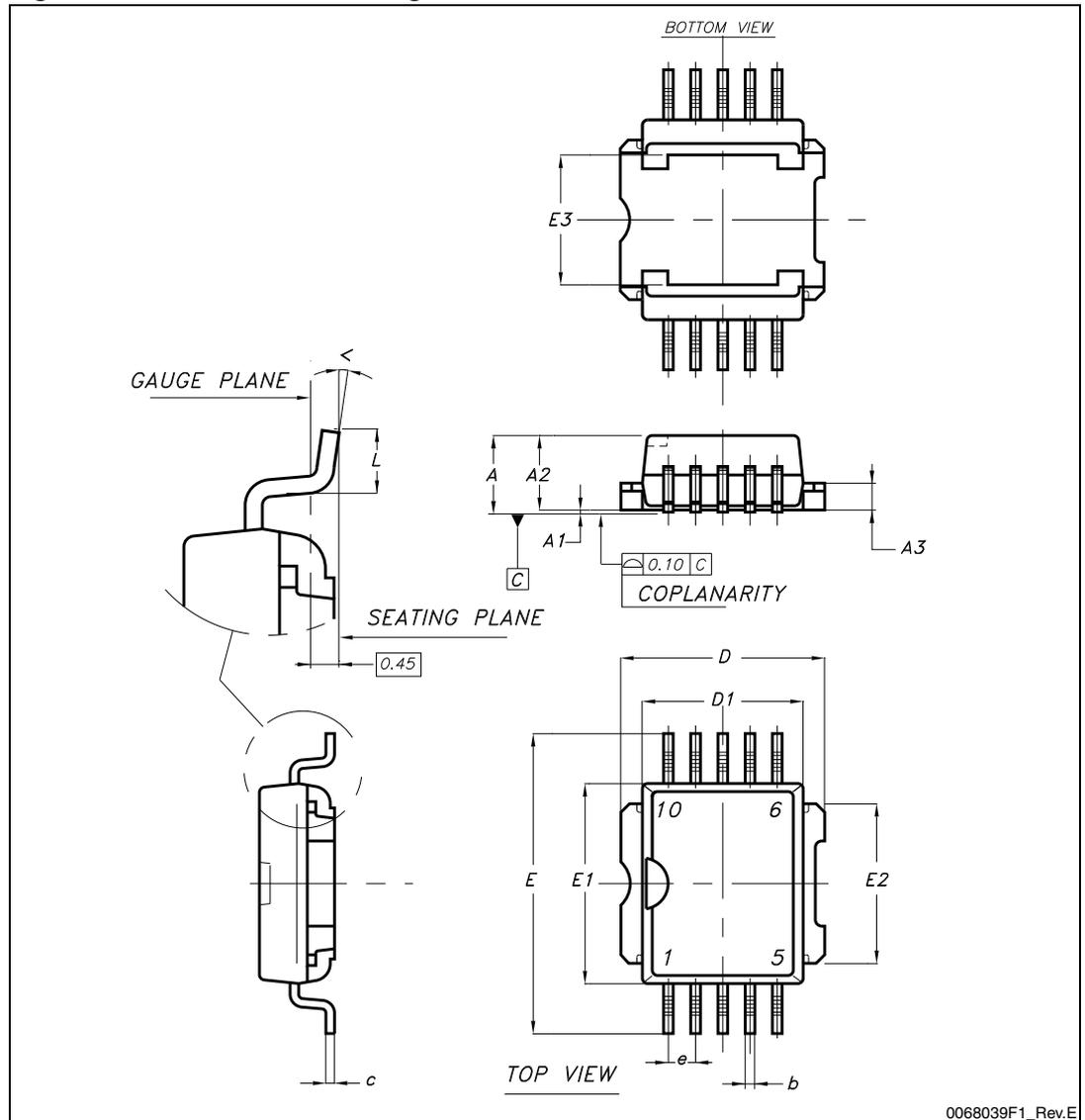
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**Table 8. PowerSO-10 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			3.70
A1	0.00		0.10
A2	3.40		3.60
A3	1.25		1.35
b	0.40		0.53
c	0.35		0.55
D	9.40		9.60
D1	7.40		7.60
E	13.80		14.40
E1	9.30		9.50
E2	7.20		7.60
E3	5.90		6.10
e		1.27	
L	0.95		1.65
<	0°		8°

Figure 20. PowerSO-10 drawing



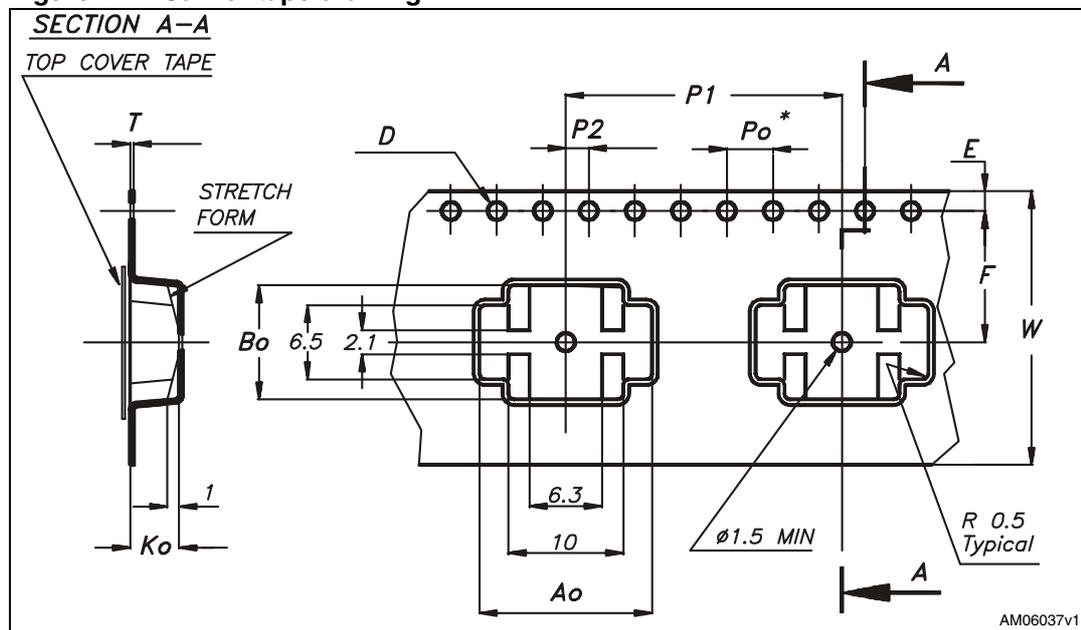
## 5 Packaging mechanical data

Table 9. Carrier tape dimensions

Ref.	mm		
	Min.	Typ.	Max.
A0	14.9	15.0	15.1
B0	9.9	10.0	10.1
K0	4.15	4.25	4.35
F	11.4	11.5	11.6
E	1.65	1.75	1.85
W	23.7	24.0	24.3
P2	1.9	2.0	2.1
P0	3.9	4.0	4.1
P1	23.9	24.0	24.1
T	0.025	0.30	0.35
D(Ø)	1.50	1.55	1.60

Note: 10 sprocket hole pitch cumulative tolerance  $\pm 0.2$  mm.

Figure 21. Carrier tape drawing (a)



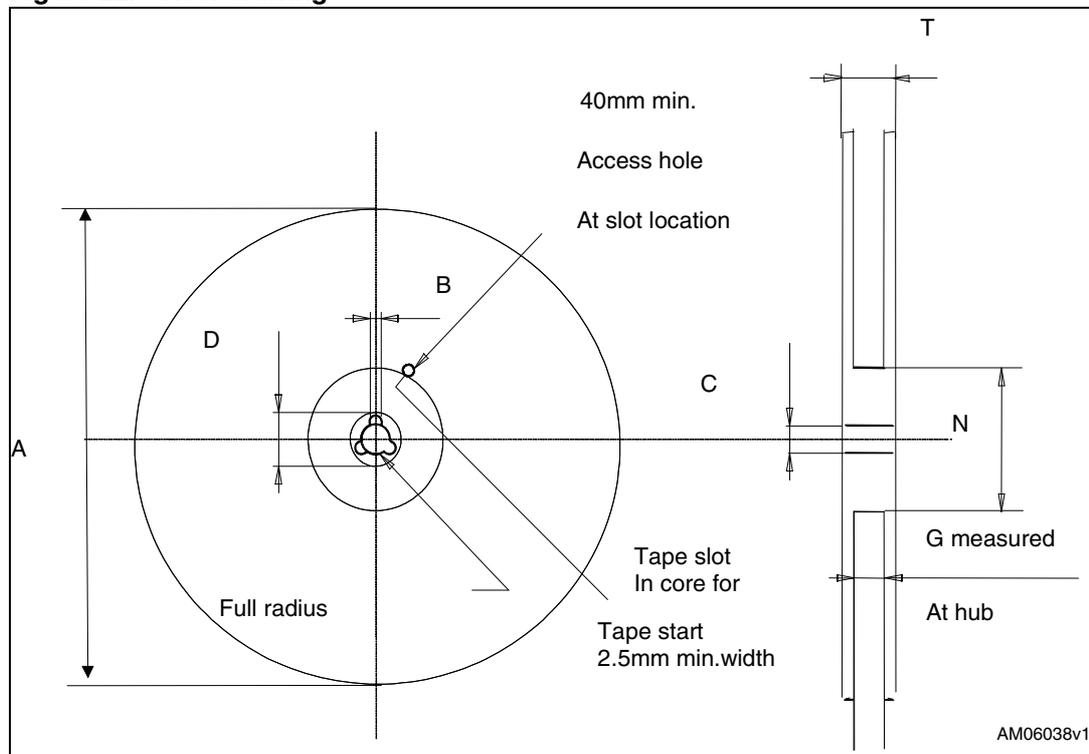
a. Drawing is not to scale.

**Table 10. Reel dimensions**

Ref.	mm		
	Min.	Typ.	Max.
A			330
B	1.5		
C	12.8	13	13.2
D	20.2		
N	60		
G		24.4	
T			30.4

Note: 10 sprocket hole pitch cumulative tolerance  $\pm 0.2$  mm.

**Figure 22. Reel drawing (b)**



**Table 11. Base/bulk quantities**

Base qty.	Bulk qty.
	600

b. Drawing is not to scale.

## 6 Revision history

Table 12. Revision history

Date	Revision	Changes
08-Feb-2007	1	First release
13-Sep-2007	2	New section has been added: <a href="#">2.1: Electrical characteristics (curves)</a> .
10-Oct-2012	3	Updated <a href="#">Table 4: On /off states</a> and <a href="#">Section 4: Package mechanical data</a> . Inserted <a href="#">Section 5: Packaging mechanical data</a> . Minor text changes.

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