

## N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

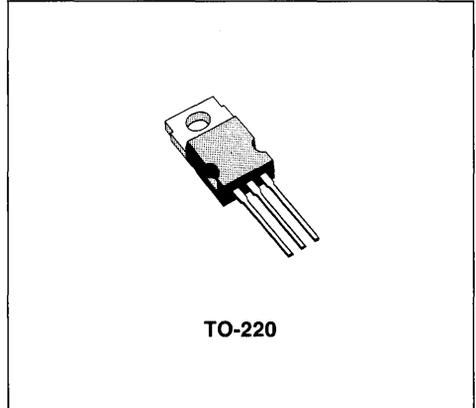
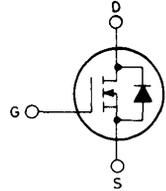
TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
SGSP358	50 V	0.3 Ω	7 A

- HIGH SPEED SWITCHING APPLICATIONS
- GENERAL PURPOSE
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

**INDUSTRIAL APPLICATIONS:**

- D.C. SWITCH
- UNINTERRUPTIBLE POWER SUPPLIES

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include DC switching, uninterruptible power supplies and drive circuits for power bipolar transistor.


**INTERNAL SCHEMATIC  
DIAGRAM**

**ABSOLUTE MAXIMUM RATINGS**

V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	50	V
V <sub>DGR</sub>	Drain-gate voltage (R <sub>GS</sub> = 20 KΩ)	50	V
V <sub>GS</sub>	Gate-source voltage	±20	V
I <sub>D</sub>	Drain current (cont.) at T <sub>c</sub> = 25°C	7	A
I <sub>D</sub>	Drain current (cont.) at T <sub>c</sub> = 100°C	4.4	A
I <sub>DM</sub> (*)	Drain current (pulsed)	28	A
I <sub>DLM</sub> (*)	Drain inductive current, clamped	28	A
P <sub>tot</sub>	Total dissipation at T <sub>c</sub> < 25°C	50	W
	Derating factor	0.4	W/°C
T <sub>stg</sub>	Storage temperature	-65 to 150	°C
T <sub>j</sub>	Max. operating junction temperature	150	°C

(\*) Pulse width limited by safe operating area

**THERMAL DATA**

$R_{thj - case}$	Thermal resistance junction-case	max	2.5	°C/W
$T_L$	Maximum lead temperature for soldering purpose		275	°C

**ELECTRICAL CHARACTERISTICS** ( $T_{case} = 25^{\circ}C$  unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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**OFF**

$V_{(BR) DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A$	$V_{GS} = 0$	50		V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$				250 $\mu A$ 1000 $\mu A$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 V$				$\pm 100$ nA

**ON (\*)**

$V_{GS (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$	$I_D = 250 \mu A$	2		4	V
$R_{DS (on)}$	Static drain-source on resistance	$V_{GS} = 10 V$ $I_D = 3.5 A$ $V_{GS} = 10 V$ $I_D = 3.5 A$ $T_c = 100^{\circ}C$				0.3 0.6	$\Omega$ $\Omega$

**DYNAMIC**

$g_{fs}$	Forward transconductance	$V_{DS} = 25 V$	$I_D = 3.5 A$	1.5			mho	
$C_{iss}$	Input capacitance	$V_{DS} = 25 V$ $f = 1 \text{ MHz}$ $V_{GS} = 0$			210	270	pF	
$C_{oss}$	Output capacitance					150		pF
$C_{rss}$	Reverse transfer capacitance						70	

**SWITCHING**

$t_{d (on)}$	Turn-on time	$V_{DD} = 25 V$	$I_D = 3.5 A$		10	15	ns
$t_r$	Rise time	$V_i = 10 V$	$R_i = 4.7 \Omega$		35	45	ns
$t_{d (off)}$	Turn-off delay time	(see test circuit)			20	30	ns
$t_f$	Fall time				15	20	ns

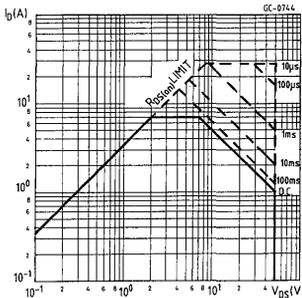
ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ Source-drain current $I_{SDM}$ (*) Source-drain current (pulsed)				7 28	A A
$V_{SD}$ Forward on voltage	$I_{SD} = 7\text{ A}$ $V_{GS} = 0$			1.4	V
$t_{rr}$ Reverse recovery time	$I_{SD} = 7\text{ A}$ $V_{GS} = 0$ $di/dt = 25\text{ A}/\mu\text{s}$		65		ns

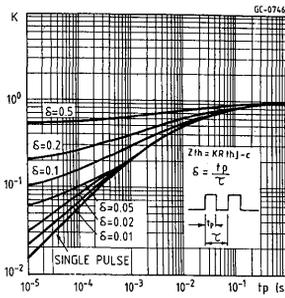
(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

(\*) Pulse width limited by safe operating area

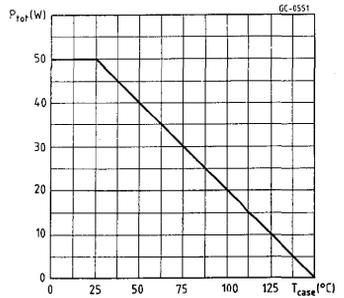
Safe operating areas



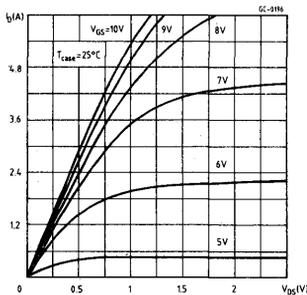
Thermal impedance



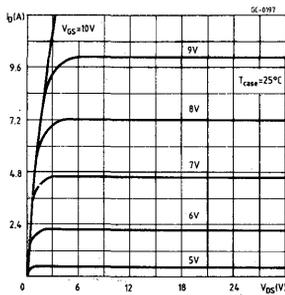
Derating curve



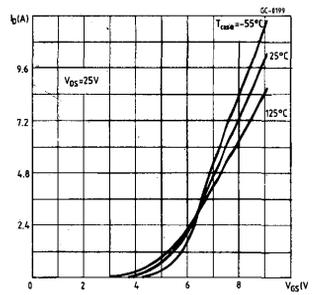
Output characteristics



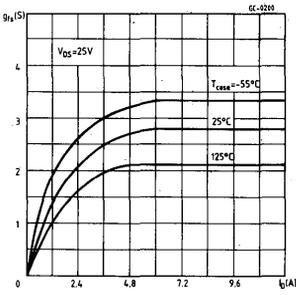
Output characteristics



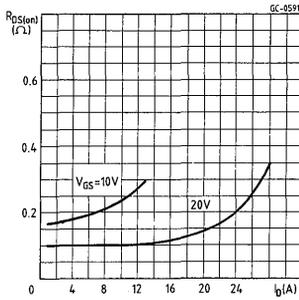
Transfer characteristics



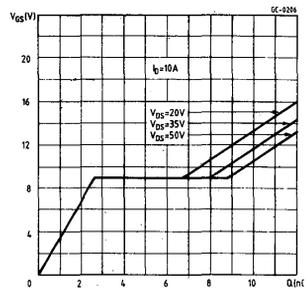
Transconductance



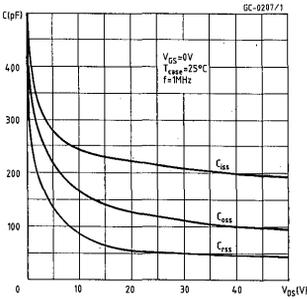
Static drain-source on resistance



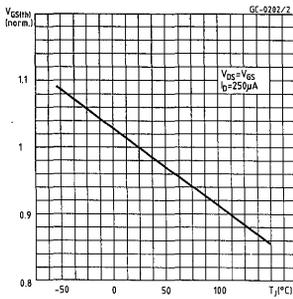
Gate charge vs gate-source voltage



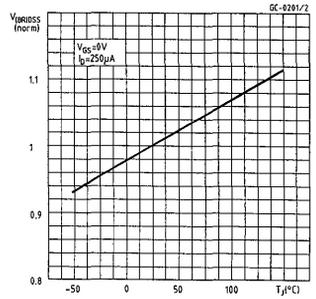
Capacitance variation



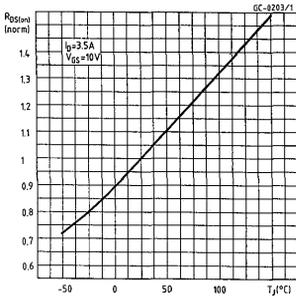
Normalized gate threshold voltage vs temperature



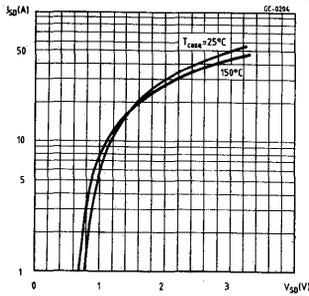
Normalized breakdown voltage vs temperature



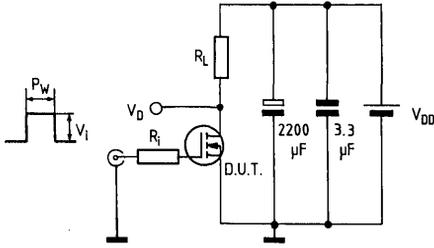
Normalized on resistance vs temperature



Source-drain diode forward characteristics



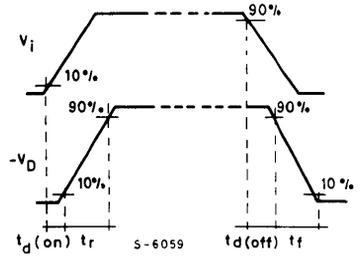
Switching times test circuit for resistive load



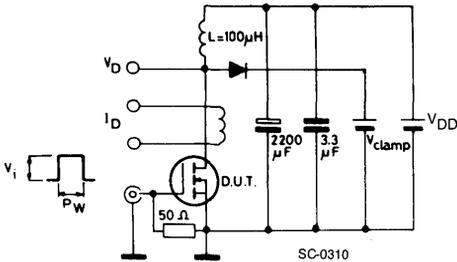
Pulse width  $\leq 100 \mu s$   
Duty cycle  $\leq 2\%$

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Switching time waveforms for resistive load



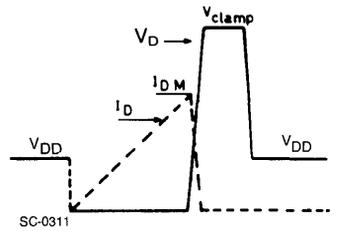
Clamped inductive load test circuit



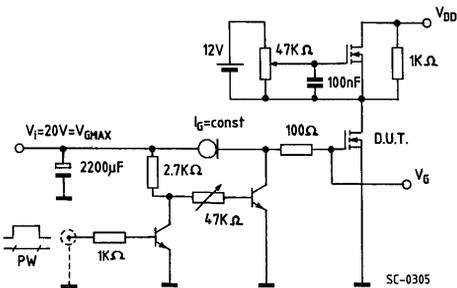
$V_i = 12 V$  - Pulse width: adjusted to obtain specified  $I_{DM}$ ,  $V_{clamp} = 0.75 V_{(BR) DSS}$

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Clamped inductive waveforms



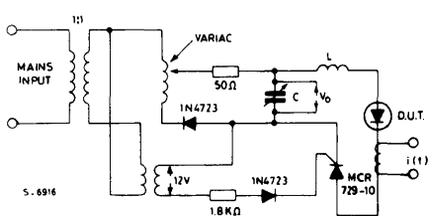
Gate charge test circuit



PW adjusted to obtain required  $V_G$

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Body-drain diode  $t_{rr}$  measurement Jedec test circuit



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